The Effect of Fluorine on Low Temperature Boron Activation in Ultra Shallow Junctions

Jeremy J. Kempisty,
Microelectronic Engineering
Rochester Institute of Technology
Rochester, NY 14623

Abstract-- As CMOS device dimensions continue to shrink below 200nm, one of the major limiting factors in scaling size will become the drain and source junction depth. Using fluorine to create shallower p-type junctions during ion implant is one way to decrease the junction depth. The effect of fluorine on the implant and subsequent anneal processes was studied. A low temperature annealing process was developed to decrease junction depths although sufficient dopant activation is being studied.

1. INTRODUCTION

Critical dimensions of CMOS transistors continue to shrink well below 200nm, with current processes producing gates as low as 130nm. While microlithography has been a major limiting factor in the scaling of transistors, another has been the drain/source junction depth. The junction depths must be scaled accordingly with the channel width to avoid undesirable short channel effects such as threshold voltage roll off and punchthrough. Current processing requires a drain junction depth (Xj) of 450-900Å with a sheet resistance of 200-700 Ω/sq.[1] These requirements pose very serious problems to the processes, which have begun to rely heavily on rapid thermal processing such as spike annealing to replace the slower diffusion processes which result in deeper junctions. Newer forms of doping are also being studied, including plasma doping and high-energy recoil implants. These two solutions may provide long-term revolutionary answers to doping issues, but using diffusion in a different fashion may provide a short-term solution.

Low energy ion implantation is presently the method of choice for the formation of source/drain junctions. On the other hand, ion implantation creates defects, giving rise to unwanted effects such as dopant clustering and transient enhanced diffusion (TED). The problem for making shallow boron doped p+ junctions is more severe because of higher boron ion implantation projected range and higher TED effects. Boron is usually introduced by implanting BF2 that causes amorphous layer damage that allows recrystallization through solid phase epitaxy (SPE). The temperature-time product of post implantation anneal is desired to be kept low. Reducing anneal times is possible with rapid thermal processing (RTP) by ramping temperature to the target temperature and cooling down faster, approaching a spike shaped anneal temperature-time profile. The damage produced by an implant causes a large enhancement in the diffusion coefficient of dopants, until such time as the damage is completely repaired. Experimental findings have shown that the point defects responsible for TED are interstitial type extended defects in the form of {311} clusters. The balance between cluster growth and evaporation determines the enhancement in diffusivity observed during TED. It has been suggested that at lower temperatures, the supersaturation in point defect levels is high, and excess defects remain longer due to the lower interstitial diffusion coefficient, leading to greater motion of dopants. The role of fluorine on the TED of boron is not fully understood

Experimentation was done on wafers implanted at Texas Instruments on an Applied Materials XRLeap Implanter, which is capable of low-energy implants without the use of a deceleration mode. Five sets of wafers were implanted, each with a different variation on a boron or BF2 implant. These wafers were then sent to RIT for continued processing. The wafers sent to RIT were as follows:

Wafer	Implant	Energy
2	5E14 BF2	10KeV
6	1E15F/5E14B	3.9KeV/2.2KeV
10	5E14F/5E14B	3.9KeV/2.2KeV
13	5E14B	2.2KeV
16	5E14B/1E15F	2.2KeV/3.9KeV

Table 1: Wafer Process Description

Results for the experiment come from various sources, including a standard four-point probe system at RIT and Texas Instruments. Also used were Secondary Ion Mass Spectroscopy (SIMS) and Spreading Resistance Profiling (SRP). SIMS results show the distribution of dopant atoms (Both B11 and B10) through the use of an oxygen beam that cuts into the wafer. This test is an accurate way to measure the number of atoms present in

the wafer, but does not show the amount of dopant atoms that have been activated through annealing. SRP analysis is a two-probe measurement tool stepped across a beveled edge of the wafer, used to calculate the active dopant concentration and consequently the sheet resistance of the junction.

Use of the SRP system in ultra-shallow junctions (USJ) is difficult due to several phenomena. Using a standard SRP system for USJ processes often results in abnormally high sheet resistance calculations. The high sheet resistance is commonly attributed [2] to surface damage introduced by the beveling process. Wolf et al. have developed a low-weight SRP system using a single probe called nano-SRP which also uses an Atomic Force Microscope to produce quality SRP measurements on USJ wafers. In a standard SRP system, the probes in contact with the wafer actually produce a series of small micro-contacts. However, when SRP was developed, it was intended for use over structures tens or hundreds of microns thick, and the micro-contact effect could be easily neglected with no effect on the readings. However, as Clarysse and Vandervorst show [3], with shrinking junctions, this effect can no longer be ignored. Clarysse et al [4] also show an effective surface and equipment preparation strategy for electrically characterizing USJ profiles.

2. EXPERIMENTAL SETUP

The wafers sent to RIT, outlined above, were cleaved into 12 pieces to be annealed using a low temperature process taking advantage of solid phase epitaxy to activate the dopant without the added diffusion that is associated with high temperature activation. The resulting profile should be a shallow junction with as little depth added post-anneal as possible. One segment of each wafer was loaded into RIT's Bruce Diffusion furnace for each of 12 different anneals. The anneal recipes used diffusion times of 4,6,8, and 10 hours at temperatures of 400, 600, and 800°C. All anneals were done in an inert nitrogen ambient. The processes were set up so that the furnace would ramp up to temperature and stabilize before the wafers were pushed in. This process allowed the wafers to be in the furnce at a constant temperature at all times. It also allowed the recipes to be set up without needing to account for differences in ramp times. The temperatures used were low enough so the wafers were pulled out of the furnace at temperature without causing warpage.

The segments were measured using four-point probe analysis following the anneal process. The Alesi Industries four point probe uses a probe spacing of .0625" and all measurements were based on a current of 1mA, which was decided on through previous experimentation.

3. Results and Discussion

The results of the four-point probe measurements are as follows:

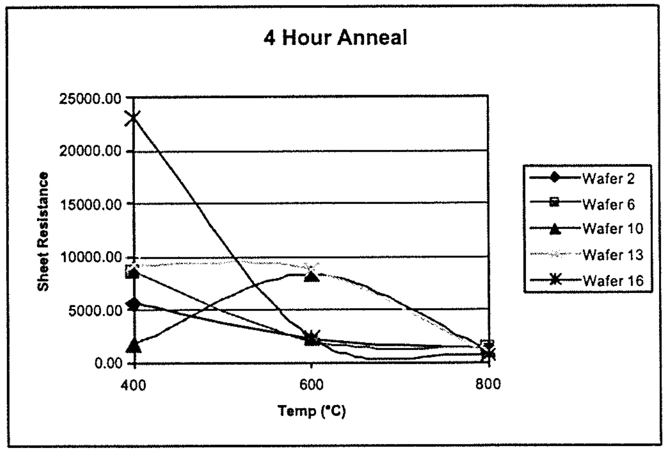

Figure 1: Sheet Resistance an a function of annealing temperature

This chart is the representation of the 4-hour anneal processes, since the data showed that the time (4-10 hours) was not a significant factor in sheet resistance measurement. The 400°C anneal provided very poor results, indicating that the dopats were not activated at this low temperature. Still, the values show some insight into the process. The highest value is that of the 5E14 Boron implant followed by a 1E15 fluorine implant, meaning that at the time of boron implantation, there was no fluorine or preamorphization present in the wafer. The lowest value is the 5E14F/5E14F implant in which half of the Fluorine was present in the wafer at the time of implant as the three intermediate lines.

At 600°C, the anneals become divided into two distinct segments, one between 5000 and 10,000ohms/sq, and one near 2000 ohms/sq. These two segments are divided solely on fluorine concentration in the wafer. The higher segment shown is of the 5E14 Fluorine implant (half the amount of the standard BF2 implants) and that of the exclusively boron implant. The three lines in the lower segment all contain a 5E14 dose of Boron, and a 1E15 dose of fluorine. The order of the implant becomes irrelevant at this process.

At the 800°C anneal, all of the processes result in very similar sheet resistance values, regardless of boron and fluorine concentration. However, the difference in the 600°C anneal is clearly shown by the data.

REFERENCES

[1] "International Technology Roadmap for Semiconductors" 2000 Update.

[2]. Wolf, P. De; Clarysse, T.; Vandervorst, W.; Hellemans, L.; "Low Weight Spreading Resistance Profiling of Ultrashallow Dopant Profiles." Journal of Vacuum Science Technology B. 16(1) Jan/Feb 1998.

[3]. Clarysse, T.; Vandervorst, W.; "Need to Incorporate the Real Micro-Contact Distribution in Spreading Resistance Correction Schemes." Journal of Vacuum Science Technology B. 18(1) Jan/Feb 2000.

[4]. Clarysse, T.; Vandervorst, W.; Collart, E.J.H.; Murrell, A.J.; "Electrical Characterization of Ultrashallow Dopant Profiles." Journal of the Electrochemical Society 147(9) 2000.

[5] P.A. Packan and J.D. Plummer, "Transient Enhanced Diffusion of Low Concentration B in Si due to Si Implantation Damage, Applied Physics Lett., Vol 56, No. 18, p. 1787,1990