

Polysilicon-Germanium Films Fabricated by Ge Sputtering

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Abstract— Poly-Si_xGe_{1-x} films were fabricated on 500 Å of oxide by a novel process. Values for X range from 0.86 to 0.45. This novel process consists of two steps as opposed to the single step polysilicon-germanium deposition methods currently used in industry. Ge was deposited by PVD and polysilicon was deposited on top of the germanium by LPCVD in a silane ambient. The films were doped P⁺ with boron dopant and annealed at 1,000°C for 50 minutes in a nitrogen ambient. Films with 65 and 55% Ge suffered from voids and hillocks and film discontinuity. Films with 20 and 14% Ge were relative smooth compared to the films with a high percentage of Ge. Standard polysilicon films yield a sheet resistance of 59.01 ohm/square while films with 20 and 14% Ge yield values of 44.71 and 41.41 ohm/square respectively.

I. INTRODUCTION

As the semiconductor industry approaches deep sub-micron device regime more challenges are being encountered in the fabrication of such small devices. To make symmetric n- and p- channel devices, dual gate approach becomes necessary i.e. n+ polygate for NMOS and p+ polygate for PMOS devices. As the devices are shrinking in lateral dimensions so are the vertical dimensions. Gate oxide has already reached ~ 2 nm in thickness. Boron penetration into the thin gate oxide from the p+ polygate has become a serious problem[2]. This is illustrated in Figure 1. If boron is kept away from the oxide-poly interface, it gives rise to gate depletion effect (GDE)[2]. The gate region close to the interface goes into depletion causing extra capacitance and effective reduction of gate voltage and drive current. This is illustrated in Figure 2. Polysilicon-germanium films have been proposed as potential replacement for conventional polysilicon gates. Various film compositions of polySi_xGe_{1-x} have been suggested, all with promising results[1][2][3][4]. This material requires lower temperature for dopant activation, which reduces boron penetration yielding better gate oxide reliability, decreases thermal budget and processing time. PolySi_xGe_{1-x} is usually deposited by Low Pressure Chemical Vapor Deposition (LPCVD) with the use of Silane, SiH₄, and Germanium, GeH₄ gases.

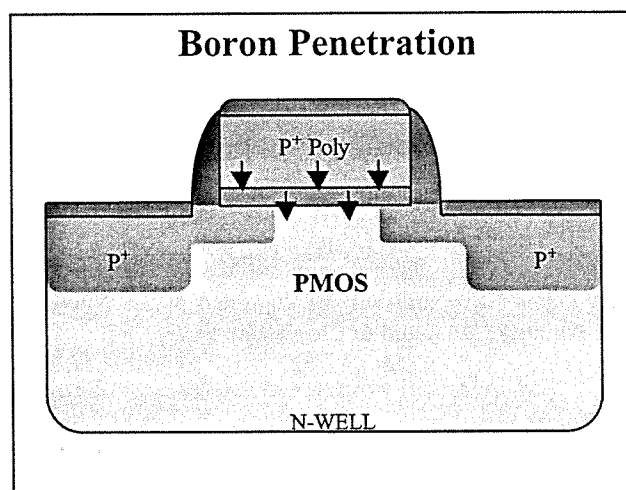


Figure 1

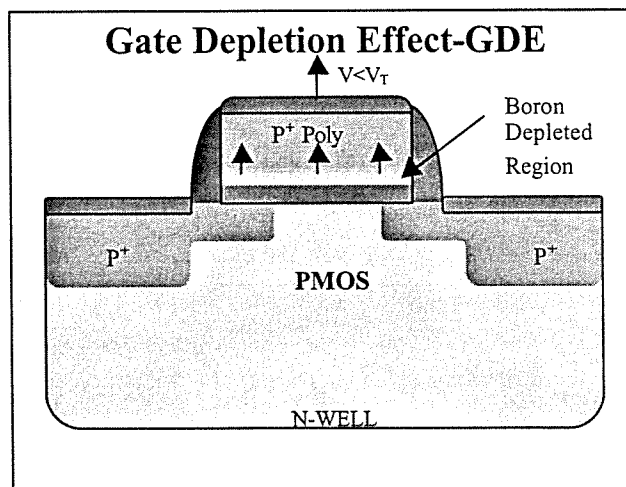


Figure 2

In this investigation, polysilicon-germanium films have been fabricated by depositing LPCVD polysilicon on PVD germanium films. Germanium films were deposited from a four-inch target in a sputtering system and polysilicon was deposited using silane gas in a LPCVD furnace. During the polysilicon deposition and the subsequent anneal after the doping of the film, the two

films are expected to react to form $\text{polySi}_x\text{Ge}_{1-x}$. The films were doped with boron and annealed at 1,000°C. Polysilicon-germanium composition and resistivity will be studied and compared to standard polysilicon films.

II. EXPERIMENT

The first step in the two-step process of fabricating polysilicon-germanium films by Ge sputtering is to deposit Ge. A process to deposit Ge by PVD was generated and optimized using a CVC601 sputtering tool and a 4" germanium target. To obtain a desired Ge thickness of 1,500 Å, the deposition time was set to 20 minutes, the power was set to 200 Watts and the argon flow was set to 56.5 sccm yielding a sputtering pressure of 5 mTorr. The second step in this two-step novel process is to deposit polysilicon using a LPCVD tube with a silane ambient. A 6,000 Å polysilicon film was deposited on top of the 1,500 Å of Ge using RITs standard polysilicon recipe for their PW-3 CMOS process. A $\text{polySi}_{0.80}\text{Ge}_{0.20}$ film was achieved with this process. A $\text{polySi}_{0.86}\text{Ge}_{0.14}$ film was fabricated by depositing a 2,700 Å LPCVD polysilicon film before this novel process was started. The deposition time in the sputtering tool was increased to fabricate the films with a high percentage of Ge. All samples were doped P^+ with boron dopant and annealed at 1,000°C for 50 minutes in a nitrogen ambient. Film microstructures were examined in a 501 Phillips SEM at 320X and 10,000X magnifications. Sheet resistance of the films was measured at the five standard points of interest used at RIT during routine inspections.

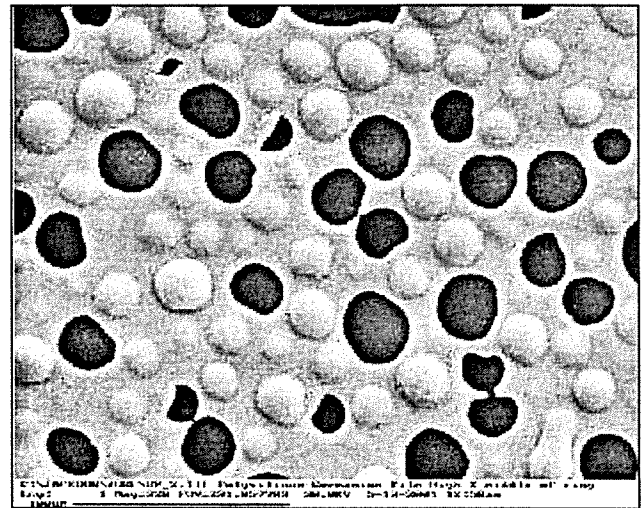
III. RESULTS AND DISCUSSION

Usual percentages of germanium in Polysilicon for industry do not exceed 35%. In this experimentation the fabrication of films with a relatively high Ge concentration, 65 and 55%, produce reasons as to why the germanium concentration in a polysilicon film must be low. Films with 65 and 55% Ge suffered from voids and hillocks and film discontinuity. This is illustrated in Micrograph 1 and 2. The discontinuity of polysilicon-germanium films with high Ge concentrations due to voids and hillocks makes this film unusable in the semiconductor industry. Films with 20 and 14% Ge were relative smooth compared to the films with a high percentage of Ge. This is illustrated in Micrograph 3 and 4. These films are ideal for IC manufacturing since a continuous signal can be sent through wires made with this material. Another reason for the ideality of these films smoothness would be the decrease in resistance achieved as a result of reduced film discontinuity. Standard polysilicon films yield a sheet resistance of 59.01 ohm/square while films with 20 and 14% Ge yield values of 44.71 and 41.41 ohm/square respectively. From these results the decrease of sheet

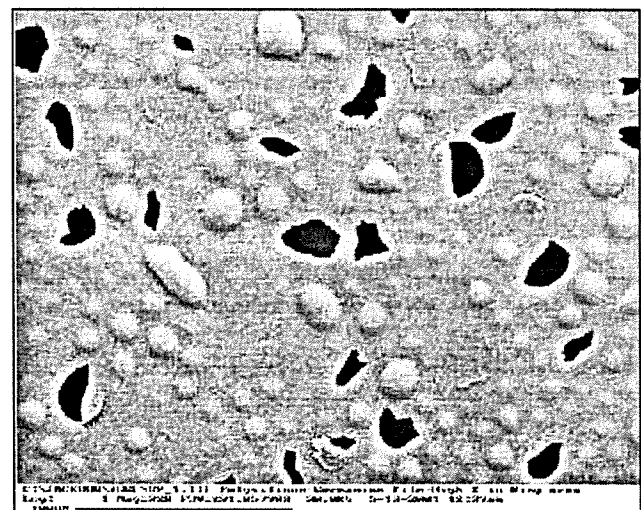
resistance as a result of the introduction of germanium into these films is proven. Table 1 summarizes the film thickness, Ge percentage and sheet resistance values obtained throughout this investigation.

Film Composition and Sheet Resistance			
Film	Thickness (Å)	Ge (%)	Rs (ohm/square)
Polysilicon	6000	0	59.01
Poly/Ge	6000/1500	20	44.72
Poly/Ge/Poly	6000/1500/2700	14	41.41

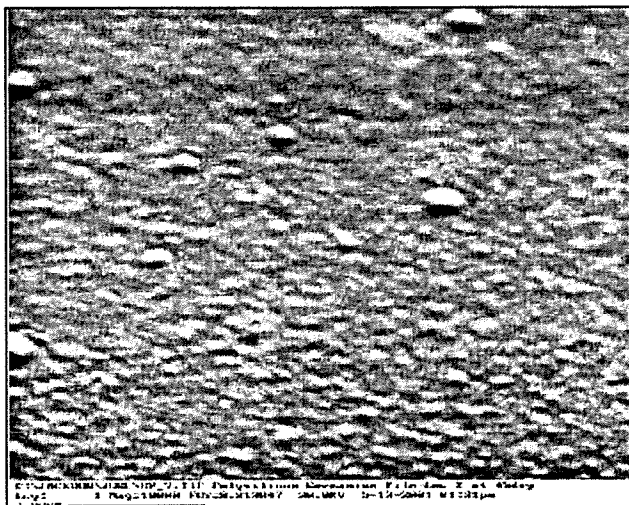
Table 1: Summarized results.



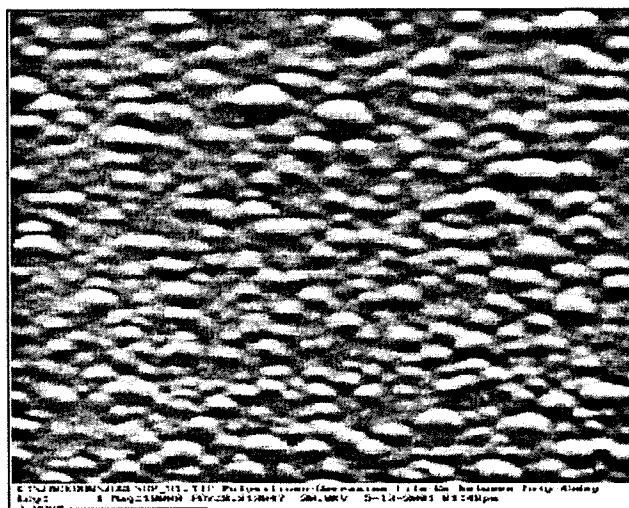
Micrograph 1: Polysilicon-Germanium film after anneal with a Ge concentration of 65% taken at a magnitude of 320X.



Micrograph 2: Polysilicon-Germanium film after anneal with a Ge concentration of 55% taken at a magnitude of 320X.



Micrograph 3: Polysilicon-Germanium film after anneal with a Ge concentration of 20% taken at a magnitude of 10,000X.



Micrograph 4: Polysilicon-Germanium film after anneal with a Ge concentration of 14% taken at a magnitude of 10,000X.

IV. CONCLUSION

Polysilicon-germanium films have been successfully fabricated at RITs Microelectronic Engineering Laboratory by Ge sputtering. Films with low percentages of Ge demonstrated desirable film microstructures with potential for use in microelectronic devices. Lower sheet resistance was obtained when adding Ge to standard polysilicon films. A reduction of 25% in sheet resistance for films with 20% Ge was achieved. For films with 14% Ge, a reduction in sheet resistance of 35% was achieved. Another possible reason for the improvement in sheet resistance for the films with 14% Ge would be that Ge was in between polysilicon films possibly creating a better distribution of Ge in polysilicon. Future work to be done as a

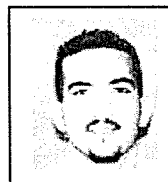
continuation of this investigation is to study the Ge profile in polysilicon after LPCVD poly deposition, to study the boron profile in polysilicon-germanium after anneal, to study effects on boron activation of time and temperature during anneal and to incorporate an optimized process to fabricate these films into PMOS devices to study its electrical properties when testing a device.

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Jose L. Medina, originally from San Juan, PR, received B.S. in Microelectronic Engineering from Rochester Institute of Technology in 2001. He attained co-op work experience at Fairchild Semiconductor in South Portland, ME and RIT in Rochester, NY. He is joining Microchip Technology as a process engineer in the yield group starting June 2001.