

CMP Process Development for Shallow Trench Isolation (STI)

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Abstract—Tool characterization and optimization was performed on a Westech Model 372 Polisher. A Rhodes ESM-U pad with a #5 groove with PSA and two slurries: a Rodel Klebosol 1501-50 silica based slurry and a proprietary cerium oxide slurry were utilized. Initial polishing of blanket thermal oxide wafers on the Westech produced %WIWNU greater than 80% using the Klebosol slurry. Following tool calibrations and modifications to machine configurations, %WIWNU dropped to approximately 5%. Characterization studies were performed for Removal Rate vs. Platen RPM and for Removal Rate vs. Down Force. An increase in removal rate was determined with an increase in platen RPM while a linear relationship between removal rate and down force existed. Blanket nitride and low temperature oxide (LTO) wafers were polished using both silica and ceria slurries to determine removal rates. Oxide to Nitride Selectivity for the Klebosol slurry was 4:1 while the ceria slurry was 100 times more selective. STI structures were manufactured and polished. Trench dishing was studied using Alphastep measurements. Severe dishing was observed with the silica based slurry. The ceria slurry produced no dishing effects.

1. BACKGROUND

As design rules shrink and microprocessor speeds increase, the ability to isolate devices becomes more and more important. A transition from LOCOS (Local Oxidation of Silicon) to Shallow Trench Isolation (STI) is needed for scaling beyond 0.25 μm . STI dramatically shrinks the area needed to isolate transistors while offering more functionality, more speed per unit area, superior latch-up immunity, and better planarity. However, the more complex STI process creates challenges in providing void-free CVD films, sloped etch profiles, and uniform planarization by CMP.

STI structures represent CMP's newest and most important application for device-level processing. The mainstream implementation of STI throughout the semiconductor has taken place throughout industry. Currently, STI processing is unavailable at the Rochester

Institute of Technology. The purpose of this project was to develop and optimize a CMP process for future STI applications at RIT. This was achieved by identifying appropriate CMP consumables for current STI processes. Both silica and ceria based slurries were investigated. Removal rates, oxide-to-nitride selectivity, and uniformities were determined to be a function of process parameters and materials. SEM pictures and Alphastep measurements were utilized to determine the effects of trench dishing.

2. EXPERIMENTAL

Initial tool training was given on the Westech Model 372 Polisher by Bruce Tolleson. Two issues with the CMP tool were discovered during this session. The first issue was the inability to flow DI water to the primary platen. The other problem was the slurry flow was not calibrated. A setting of 100mL/min corresponded to an actual flow of 149mL/min.

The pad that would be used on the Westech Model 372 Polisher was a Rhodes ESM-U. Rhodes is a division of Universal Photonics. The pad had a thickness of 0.1" and a groove depth of 0.050". The groove pattern was an x-y pattern with 5mm islands and the groove width was 1mm. This pad is very similar to the IC1000/SubaIV with a k-groove manufactured by Rodel. Two slurries were utilized during the experimental section of this project. The first slurry was a Klebosol 1501-50, silica based slurry manufactured by Rodel. The second slurry was proprietary cerium oxide slurry.

Lot #1 consisted of twenty-five 4" monitor wafers and were scribed Drew1 EMCR690 to Drew25 EMCR690. These wafers will be used for STI structures. The structures that were constructed on these wafers resembled STI-structures, however, the silicon trench etch were not performed on these wafers. The silicon trench for Shallow Trench Isolation was being development and optimized by another student, Patrick Reese. Thus, the structures created to characterize and optimize a CMP process for STI were referred to as STI-like structures.

The processing steps for the STI-like structures are as follows:

1. RCA Clean
2. Pad Oxide Growth (500Å)
3. Nitride Deposition (1600Å)
4. Pattern Nitride with CMP Test Mask
5. Nitride etch (DryTech Quad)
6. LTO Deposition (5500Å)
7. LTO Densification

The RCA clean used was the standard recipe used at RIT. The pad oxide growth took place in the Bruce Furnace using Recipe #250. Thickness measurements were verified using the Nanospec. The nitride growth was performed in lower tube of the 6" LPCVD furnace. The nitride film deposited was a 1:1 ratio of ammonia to dichlorosilane. The deposition time for a thickness of 1600Å was 29 minutes. Nitride thickness measurements were performed on bare Si test wafers using the Nanospec. The nitride film was then patterned using CMP Test Mask. Standard coat and develop recipes were used on the 4" Wafertrac. Exposure was performed on the GCA stepper using recipe Ricky. The nitride film was then etched using the DryTech Quad. The settings for this etch are as follows: 30sccm of SF₆ (gas flow), 300mTorr (pressure), 267W (Power), and a etch time of 2 minutes. The resist was ashed using the ozone asher for 45 minutes. The LTO deposition was performed in the upper tube of 6" LPCVD furnace. The recipe used was the standard 425°C LTO for a deposition time of 60 minutes. LTO densification was performed in Tube 14 of the mechanical furnace. The wafers were exposed to an O₂ ambient for 2 hours.

Twenty-five 4" monitor wafers were used for initial polishing and tool characterization. These wafers underwent a RCA clean prior to a one-micron thermal oxide growth in tube 4 of the Bruce Furnace. This group of wafers was Lot #2 and were scribed Drew26 EMCR690 to Drew50 EMCR690.

Another lot of twenty-five 4" monitor wafers were used for blanket nitride and low temperature oxide (LTO) wafers. Nitride and LTO films were deposited by use of the 6" LPCVD and recipe specifications were the same as those previously mentioned for STI-like structures. A pad oxide of 500Å was grown on the nitride wafers before nitride deposition. These wafers were Lot #3 and were scribed Drew51 EMCR690 through Drew75 EMCR690. Wafers Drew51 EMCR690 through Drew63 EMCR690 were used for blanket nitride wafers and the remaining wafers were utilized for blanket LTO films.

Additional tool repairs and operator training were performed before the initial polishing on the Westech CMP tool began. Wafer Drew26 was first wafer polished on the Westech Model 372 Polisher. Additional blanket thermal oxide wafers were polished on the tool to study uniformity issues. Tool calibrations and modifications to

machine configurations were performed. A %WIWNU study was performed using blanket thermal oxide wafers to determine optimum tool settings. Additional tool characterization was performed by a Removal Rate vs. Platen RPM and Removal Rate vs. Down Force studies.

Blanket nitride and LTO wafers were polished using both silica and ceria slurries. Removal rates and selectivities were determined. STI-like structures were also polished using both silica and ceria slurries. Optical images were used to compare structures before and after CMP. Trench dishing measurements were performed using the Alphastep. SEM images were also taken on wafers polished using the silica slurry. Wafers polished using the ceria slurry were unable to be SEM'ed due to inadequate slurry removal procedures.

3. RESULTS AND DISCUSSION

The first wafer polished on the Westech Model 372 Polisher was very non-uniform. There were many hot spots on the wafer where all the oxide was completely removed. The non-uniform polish can be attributed to problems with the tool sensing pressure. The pressure readout on the tool varied from 1PSI to as high as 10.5PSI. Figure 1 and Figure 2 show a 1µm thermal oxide wafer before and after CMP. The wafer was polished for one minute using a down force of 4PSI, a slurry flow of 30mL/min, a Platen RPM of 32RPM, a Carrier RPM of 28 RPM, and Rodel Klebosol silica based slurry.

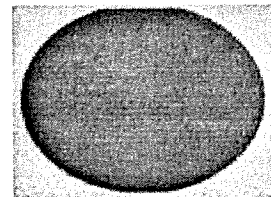


Figure 1: 1µm thermal oxide wafer before CMP



Figure 2: 1µm thermal oxide wafer after CMP

Down force calibrations were performed to make sure the applied down force was equal to the pressure readout on the Westech Polisher. Troubleshooting was performed on the tool and constant pressure readings were finally achieved. Modifications to the machine configuration were also performed. Figure 3 shows a thermal oxide

wafer polished after tool calibrations using the same settings as the wafer polished in Figure 2.

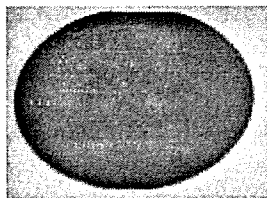


Figure 3: 1μm thermal oxide wafer after CMP and tool calibrations

Tool characterizations studies were performed to determine the optimum tool settings that yield the lowest %WIWNU. The ideal settings were a Platen RPM of 40RPM and a down force of 4PSI. Slurry flow and platen RPM were kept constant at 30mL/min and 28RPM, respectively. Figure 4 is a plot of uniformity across the wafer for various RPMs: Wafer #31-50RPM, Wafer #32 – 40RPM, and Wafer #33 – 30RPM. Wafer #30 is a 1μm thermal oxide wafer before CMP.

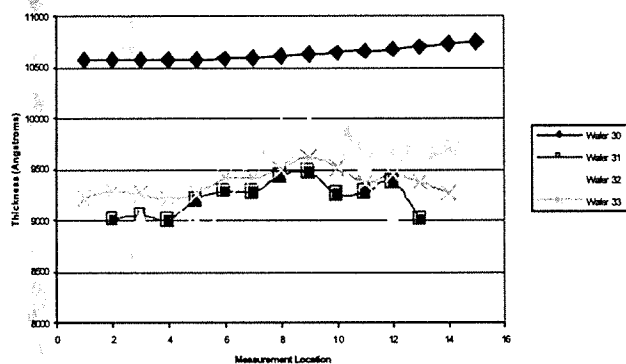


Figure 4: Thickness across the wafer (Across the diameter of the wafer, minor flat to major flat)

Removal rate versus Platen RPM was also studied. It was determined that the removal rate increased with an increase in Platen RPM. This corresponds to Preston's Equation, which is listed below:

$$\text{Polish Rate} = K_p P (\Delta s / \Delta t)$$

Thus, the equation states as the linear velocity increases relative to the workpiece, the polish rate will also increase. Figure 5 is a graph of Removal Rate versus Platen RPM.

Removal Rate vs. Platen RPM

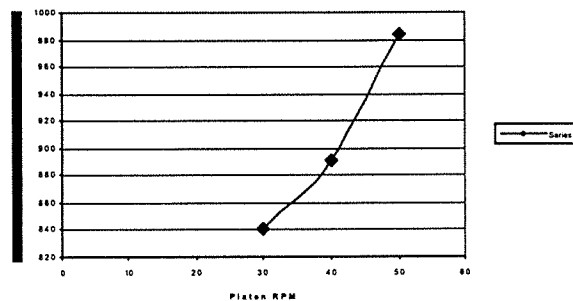


Figure 5: Removal Rate vs. Platen RPM

Removal rate versus down force was studied to test that an increase in down force corresponds to an increase in removal rate. A linear relationship between removal rate and down force existed and can be seen in Figure 6.

Removal Rate vs Down Force

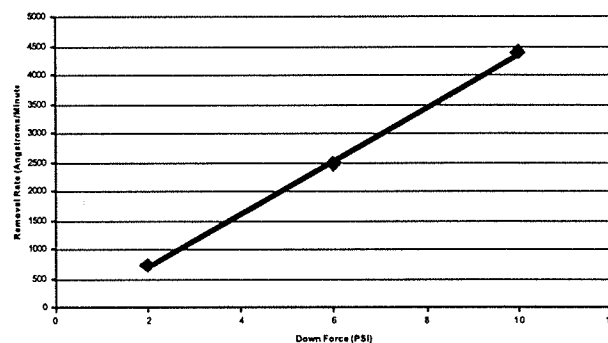


Figure 6: Removal Rate vs. Down Force

Blanket nitride and LTO wafers were polished using the Rodel Klebosol slurry and the proprietary ceria slurry to determine removal rates. These wafers were polished using the following parameters:

- Down Force: 4PSI
- Slurry Flow: 30mL/min
- Platen RPM: 50 RPM
- Carrier RPM: 28 RPM
- Polish Time: 1.5 minutes

Results for nitride and LTO polishing are listed in Table 1.

Table 1: Removal Rates and Selectivity for LTO and Nitride blanket wafers using Silica and Ceria Slurries

	Silica Slurry	Ceria Slurry
LTO Removal Rate	1990Å/minute	595Å/minute
Nitride Removal Rate	485Å/minute	1.5Å/minute
Selectivity (Oxide: Nitride)	4:1	400:1

The ceria slurry was 100 times more selective than the silica slurry.

STI-like structures were polished using both silica and ceria slurries using the following parameters:

- Down Force: 4PSI
- Slurry Flow: 30mL/min
- Platen RPM: 40 RPM
- Carrier RPM: 28 RPM
- Polish Time: Dependent on Removal Rate

Trench dishing was evaluated by the use of Alphastep measurements. The silica based slurry produced very severe dishing while the ceria slurry exhibited no dishing effects. The dishing effect was affected greatly by the selectivity of the slurry used and by the type of feature polished. The effects of trench dishing are illustrated in Figures 7, 8, and 9. Figure 7 illustrates 5µm lines and 45µm spaces before CMP. Figures 8 and 9 show the effects of trench dishing on 5µm lines and 45µm spaces after CMP using a silica and ceria slurry, respectively.

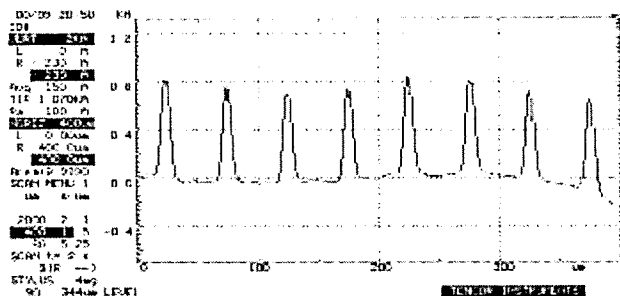


Figure 7: 5µm lines and 45µm spaces; Before CMP

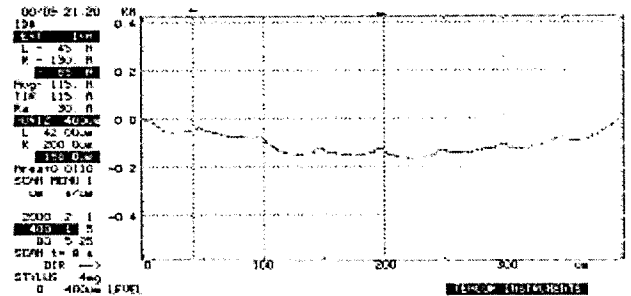


Figure 8: 5µm lines and 45µm spaces; After CMP w/ Silica Slurry

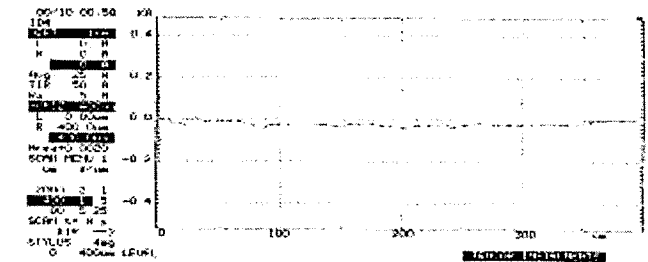


Figure 9: 5µm lines and 45µm spaces; After CMP w/ Ceria Slurry

4. CONCLUSIONS

The development of CMP process for Shallow Trench Isolation was a success. The base CMP process can be applied to future STI applications at the Rochester Institute of Technology. The ceria based slurry produced oxide to nitride selectivities of 400:1 and produced no dishing effects while using a Rhodes ESM-U pad. Future work using the Westech Model 372 Polisher can be performed in the areas of endpoint detection, slurry and pad characterization, and down force pressure optimization.

REFERENCES

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