Dry Etch of Shadow Trench Isolation

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Abstract-- Shallow trench isolation (STI) planarized with chemical mechanical polishing (CMP) has replaced local oxidation of silicon (LOCOS) as the conventional isolation technique for sub-micron devices. STI increases transistor-packing density, allowing for more functionality and speed per unit area. STI offer superior latch-up immunity, smaller channel-width encroachment and better planarity. The implementation and feasibility of STI has been examined for device fabrication at RIT previously. The process utilized was etching of shallow trenches using SF_6-O_2 dry chemistry and trench fill by TEOS (tetraethylorthosilicate) oxide deposition. The etch chemistry used did not yield anisotropic etching and appreciable undercutting was observed.

In the present study, STI process used includes 60 nm of thermal pad oxide and 160 nm of LPCVD nitride as the hard mask. To create the shallow trenches, Si is etched using SF_6-CHF_3 chemistry for dry etching. The objective is to etch the trenches of depth ~ 0.5 μm - 0.8 μm deep without undercutting and with high selectivity on resist. A series of experiments have been done to study the Si trench etching using SF_6-CHF_3 chemistry in the DryTek Quad tool by varying process parameters. The results will be presented at the conference.

1. INTRODUCTION

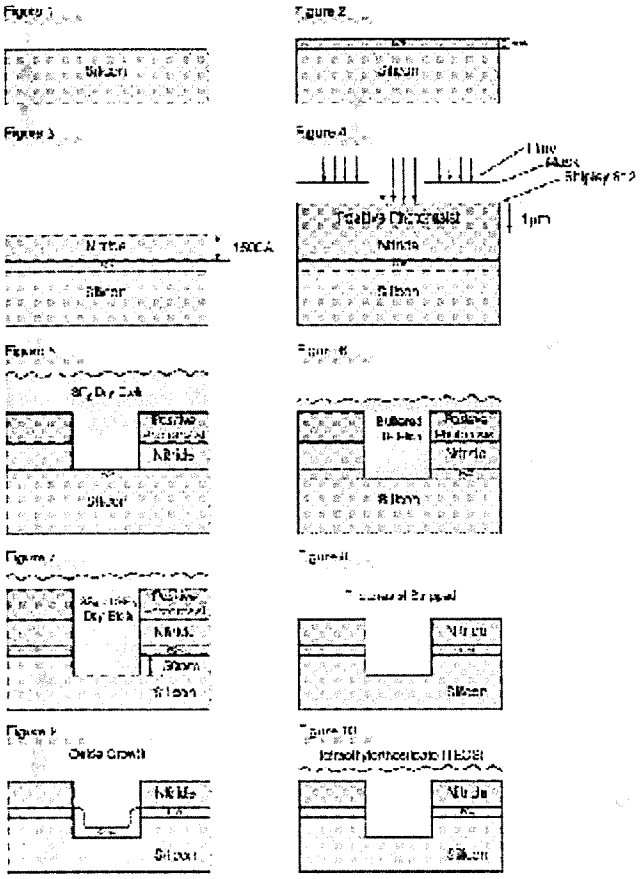
The LOCOS (LOCal Oxide of Silicon) is used as a conventional isolation technology for CMOS and BiCMOS. LOCOS geometries reach submicron size, therefore it reach the limits of effectiveness because of "bird's beak". The encroachment of the field oxide becomes significantly unacceptable large when the size of LOCOS is shrunk down to the smallest geometry devices as possible in submicron technology. Because the bird's beak extends the large encroachment into the device active regions. And another problem is that thickness of the field oxide in submicron regions. Since the thickness of the field oxide becomes significantly thinner than that grown in wider spacing of the field oxide, which create the significant problem with respect to field threshold voltage and field-edge leakage. The shadow trench isolation (STI) is another isolation method in CMOS for latch up protection. Since STI is compatible to the CMOS or BiCMOS technologies, LOCOS is simply and easily replaced with STI for devices within the same tub in CMOS or BiCMOS. STI is now widely used in any semiconductor industrial to manufacture the submicron devices with STI.

After the 1500 Å nitride and 500 Å oxide layers are etched into the trench by sulfur hexafluoride (SF_6) a dry etch, and buffered hydro fluoride (HF) wet etch, the trench in the silicon substrate is anisotropically etched between .5 μm and .8 μm depth by DryTek Quad with sulfur hexafluoride (SF_6) and trifluoridemethane (CHF_3) dry etch gas species. The sidewalls in those trenches should be smooth with an angle of 87 degree. Also the undercutting of the nitride mask should be avoided. The bottom of trench should be smooth with nice rounded corners as "U" shaped. The polymer deposition is built up by CHF_3 gas. Therefore the deposited polymeric and positive photoresist films should be removed prior to annealing and refilling of the trench by ashing with dry oxygen for 45 minutes. Annealing with dry oxide at 1000oC for 45 minutes in the Bruce furnace should repair the damaged sidewalls. The thickness of dry oxide on the sidewalls and bottom of trench is about 50 nm. The refilling chemical in the trench is a tetraethylorthosilicate (TEOS) deposition process. The TEOS deposition process is done in which TEOS layer can be deposited in the trench with void-free gap fill and on the surface of nitride at lower temperature at between 350°C and 800°C. This TEOS deposition ensures a good isolation between the devices

2. EXPERIMENTATION

In first fabrication step, at least 500 Å thickness of pad oxide layer is grown on the top of bare silicon wafer. The recipe of dry oxide growth is uploaded into Bruce furnace system with the temperature at about 1000°C for 45 minutes from ramp up to ramp down. The dry oxygen is feeding into the furnace tube to grow the oxide layer

slowly on the surface of bare silicon wafer.



And then at least 1500 Å thickness of nitride layer is done in the low-pressure chemical vapor deposition (LPCVD) tool with a standard Nitride 1:1 recipe. The recipe is uploaded into the LPCVD system with 800°C for 27 minutes. The rate of nitride 1:1 growth is approximately 58 Å/min. The ratio of Nitride and pad oxide is 3 to 1. The nitride layer is characterized as a hard mask to resist the dry etching and as CMP stopper.

The positive photoresist (Shipley 812), as shown in Figure 4, is coated on the top of nitride layer by the GCA WaferTrac. The thickness of positive photoresist is approximately 1 um thick. This positive photoresist thickness allows resisting the sulfur hexafluoride (SF_6) and trifluoridemethane (CHF_3) dry etch gas species in the Dry Etch Quad system. The developer of Shipley CD-26 removes the exposed area of the photoresist coat. The patterned area is an open area where allow the dry etch to etch into the trench. The rate of 30 sccm SF_6 for Shipley 812 photoresist is approximately 861 Å/sec with the pressure of 300 mTorr and RF Forward power of 276 w. The etch rate of both 30 sccm SF_6 and 30 sccm CHF_3 for the same photoresist is about 1175.17 Å/min.

The trench of nitride is etched with 30 sccm SF_6 dry etch in DryTec Quad system for about 44 seconds with low pressure of 300 mTorr and RF Forward power of 276 watt as shown in Figure 5. The etch rate is approximately 2480 Å/min.

The layer of oxide would slow the dry chemical etching down and is being etched isotropically by the dry etching, therefore there is a different kind of solution to etch the oxide layer faster. The layer of oxide is removed by Buffered HF, a wet etch solution, for approximately minutes as shown Figure 6. The characterization of wet etch solution is a true isotropic etch.

Etching the .5 μm-.8 μm silicon trench is done with a gas mixture of 30 sccm SF_6, and 30 sccm CHF_3 gas species, which is produces very large concentrations of free fluoride, F, as shown in Figure 8. In the low pressure environment at 65 mTorr, the ion bombardment of fluoride with 267 w RF Forward is a characterization to etch the silicon, because silicon is quite attracted to fluoride, and the methane, CH, is a polymerization that the film is created to passivate the sidewalls, preventing lateral etching.

After the dry etching in silicon trench is done, asher removes the polymeric films such as positive resist and CH for 45 minutes. Acetone is used to remove those polymeric residual in the trench and surface.

After 45 minutes annealing process with 1000° C of dry oxide is required for repairing the damaged surface of sidewalls and bottom of trench, the Tetraethylorthosilicate (TEOS) is injected to deposit SiO_2 into the shadow trench isolation at approximately 400°C for couple minutes as shown in Figure 10. Thickness of TEOS is required to be about at least 1500 Å for the planarization.

3. EXPERIMENTAL RESULTS

Nitride etch: The etch rate for the nitride is about 2465.4 Å/minute. The nitride layer is entirely etched into trench for about 40 seconds in DryTek Quad Chamber. The RF Forward is approximately 276 watt. The pressure in the chamber #2 is 300 mTorr. The gas flow dispensing in the chamber is about 30 sccm SF_6. The green color of nitride is disappeared after dry etching is performed. The photoresist layer is remained the same, but the thickness is reduced from 1 um to about .94 um. The SF_6 etch rate for positive photoresist is approximately 14.35 Å/second.

Oxide etch: The layer of 600 Å dry oxide is removed entirely. The tan color for oxide is disappeared in the trench regions by buffered hydro fluoride. After the wet etching, the measurement of oxide thickness is less than 20 Å as it is revealed by Nanospec instrument.

Silicon etch: the etch time increment is about 10 seconds for each run. The etching time for the first run is 140 seconds. The etching time for the last run is about 180 seconds. The pressure in the chamber #2 is 65 mTorr, the pressure setting is remained the same for every run. The RF Forward is 276 watt for every wafer. The gas flow for this mixture gas contains 30 sccm SF_6 and 30 sccm CHF_3 gases. The etch rate of gas mixture for silicon trench is about 55.38 Å/second. The etch rate for silicon trench ranges from 42.5 Å/second to 71.81 Å/second. The etch rate for the photoresist ranges from 32.39 Å/second to 65.35 Å/second. The etch ratio of photoresist ranges from 1:1.27 to 1:1.50. The most photoresist thickness is remained on the surface of nitride.

Trench sidewalls: The images from SEM show that those sidewalls are some curve and straight as steep. "Over-annealing" with very high temperature and very long time caused to create some curve walls. The length of temperature and time of annealing should be about 1000^0 C and 45 minutes in dry oxide furnace. The device #14 looks very good comparing with other devices. The device #14 is about .5 um depth of silicon trench as shown in Picture 1.

Trench bottom: The trench bottom corners are very rounded corners as shaped "U". They look very excellent shape of trench bottom as shown Picture 1, 2, 3, and 4.

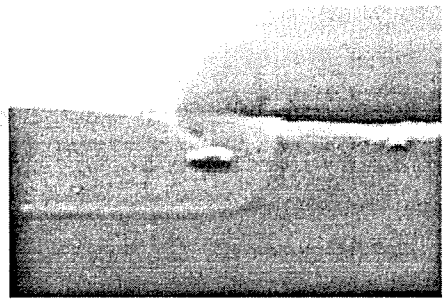
Chemical Filling: The TEOS chemical filling is substituted to LTO filling due to the contaminated LPCVD tube #15. The LTO or TEOS experiment is not intended to use for dry etch studying. Chemical filling is merely used for observation in x-section results. The TEOS filling is a standard for STI technology in semiconductor industrials. The LTO chemical depositing rate in the trench and on the surface is about 100 Å/minutes. LTO depositing time for STI in LPCVD for approximately 2.5 hours at 425° C. The measurement of LTO thickness on the monitor wafer is about 15000 Å. It was measured by ellipsometric instrument.

4. CONCLUSION

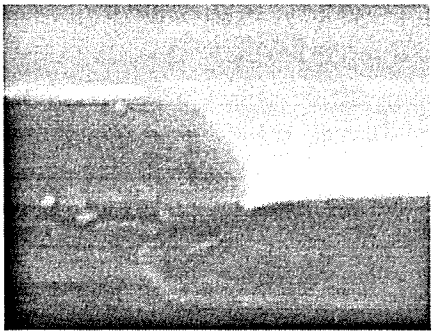
The trench sidewalls is possibly an evidence of the etch profile of silicon trench, that may suppresses the polymeric formation with high concentrations of SF_6 and CHF_3 gas species, and the characterization of etch profile is isotropic with substantial "undercut" of the mask as shown in Picture 2, 3, and 4. The result of device 14 of .5 μm silicon trenches, as shown in Picture 1, looks better than the rest of other STI results.

The aggressive gas mixture of SF6 and CHF3 species quickly and wholly devoured the nitride layer in a minute in range from 100 mTorr to 300 mTorr. The nitride layer does not do well in masking against dry etching. The photoresist of 1 μm thickness is placed to stay on the top of nitride layer for this gas mixture etching. The nitride is for the CMP stopper. It is designed to stop the polishing from destroying the surface of device and isolation.

Picture 1 .51 um Silicon Trench



Picture 2 .93 um Silicon Trench



Picture 3 .87 um Silicon Trench

Picture 4 .72 um Silicon Trench

4. FUTURE WORK

The gas mixture of SF_6 and CHF_3 may need adjusted in various size of gas concentration in the order to be achieved in a pure anisotropic dry etching without suppressing the polymeric formation or the annealing setting may be adjusted in temperature and time to improve the sidewall and reduce the "curve" wall. . Predicting etch rate is enhanced by controls some certain parameters such as temperature, concentration, pressure, and RF forward power. The RF power supply will have to be replaced since it behaves crazy and it does not keep those DC Bias, RF Forward, and other parameters stabilized. The DryTec Quad apparently does not have the temperature controlling such as coolant system to keep the temperature in constant.

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ACKNOWLEDGMENTS

The author acknowledges Dr. Santosh Kurinec, Dr. Lynn Fuller, Dr. Jackson, and Dr. Rack for their guidance in this dry etch of shadow trench isolation project and Mr. Bruce Tolleson, Mr. David Yackoff, and Scott Blondell for their equipment support.

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