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Morphological and Electrical Variance in Polysilicon Thin Film Transistors Crystallized by Flash Lamp Annealing

by

Glenn Packard

A dissertation submitted in partial fulfillment of the requirements
for the degree of Doctorate of Philosophy in Microsystems Engineering

Microsystems Engineering Program
Kate Gleason College of Engineering

Rochester Institute of Technology
Rochester, NY

July 26, 2023

Morphological and Electrical Variance in Polysilicon Thin Film Transistors Crystallized by Flash Lamp Annealing

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We, the undersigned committee members, certify that we have advised and/or supervised the candidate on the work described in this dissertation. We further certify that we have reviewed the dissertation manuscript and approve it in partial fulfilment of the requirements of the degree of Doctor of Philosophy in Microsystems Engineering.

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ABSTRACT

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Degree: Doctor of Philosophy **Program**: Microsystems Engineering

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Dissertation Title: Morphological and Electrical Variance in Polysilicon Thin Film Transistors Crystallized by Flash Lamp Annealing

This work is a wide-reaching study of the factors that impact the in-situ crystallization of thin films of amorphous silicon into low-temperature polycrystalline silicon (LTPS) by flash lamp annealing (FLA) on glass substrates, which is used to develop thin film transistors (TFTs) with an eye towards display applications. The body of research surrounding FLA LTPS is thus advanced by identifying several challenges towards industrial integration and exploring solutions involving device configuration, novel methods of dopant introduction and activation, and novel TFT material systems. It is unlikely that FLA will ever produce LTPS superior to the laser-annealing techniques currently dominating the market, but its significant improvements in throughput and roll-to-roll compatibility make it an attractive complementary technology.

In this work, existing FLA LTPS TFT research is expanded into complementary metal-oxide-semiconductor (CMOS) logic to take advantage of the n- and p- channel compatibility of LTPS over competing amorphous oxide technology. A processing alternative is developed for scaling these devices down to current dimensions of liquid crystal display (LCD) transistor backplanes

and then further improved by exploring a silicon ion self-implant to preamorphize the polycrystalline lattice structure, allowing enhanced dopant activation at temperatures compatible with thermally-fragile substrates. This method is also shown to be compatible with a self-aligned device configuration for ease of processing and reduced parasitic capacitance. Additionally, a new strategy for producing bottom-gate LTPS devices (a consistent challenge for laser-annealed LTPS) is presented by incorporating a transparent conductive oxide as a gate structure. The increased thermal mass provided by the bottom gate is harnessed to improve the impact of channel crystallization at lower pulse intensity, producing devices with extremely high channel mobility at low drain voltage.

Monolayer Doping (MLD) is demonstrated to be compatible with FLA LTPS, utilizing a simultaneous anneal to both crystallize amorphous silicon and activate selectively self-assembled MLD-adhered dopants. MLD phosphorus n-channel TFTs are presented with activation on par with that of ultra-shallow MLD junctions on bulk silicon. Further, Gallium MLD is demonstrated for the first time, successfully producing p-channel TFTs with FLA.

The material system of FLA-crystallized silicon on chromium, already well established in the micrometer-thick film range for PV applications, is given an in-depth investigation in the nanometer thin film range for TFT applications. A unique set of crystallization patterns and texture on the nanometer scale is revealed and characterized to determine the extent, cause, and impact of chromium redistribution in this material, which is also explored as a predictable and edge-directed morphology of FLA LTPS for a wide variety of device configurations.

Finally, the individual advancements in this work are explored in many combinations in a wide multi-process study to determine their efficacy as techniques for producing FLA LTPS TFTs.

Using this broad information, the field of flash-lamp crystallized TFTs is advanced and several challenges are more specifically identified as a foundation for future research.

ACKNOWLEDGMENTS

During my journey through the RIT Microsystems Engineering Ph.D. program, I've been fortunate enough to have received support, motivation, and assistance from many wonderful people. The friends and mentors who have helped sculpt this work are too numerous to exhaustively list here, but I am deeply thankful for them all.

Foremost, I must offer my most sincere gratitude to my thesis advisor, Prof. Karl D. Hirschman. Beyond his expertise and direction, he taught me to consider every challenge and setback as a puzzle to be solved with invention and creativity. I could not have come this far without his support, pushback, and sometimes just enough bizarre thinking to crack a particularly difficult conundrum.

The contributions of Dr. Robert G. Manley have also been invaluable during this study. In addition to his practical experience and technical knowledge, Rob has always been willing to offer pointed insights that I would never have considered on my own. Further, his support and that of the other researchers at Corning Inc., especially Dr. Bin Zhu, during this research has underpinned and enabled every aspect of its work from funding to sample preparation to characterization.

I would like to thank my professorial committee members for their valuable expertise and individual assistance during this work. Prof. Denis Cormier, along with the staff of the AMPrint Center at RIT, first introduced me to the FLA system located there; his patience and constructive criticism was instrumental in navigating the PulseForge through the various ups and downs of its operation. Prof. Parsian Mohseni has greatly contributed to my understanding of nanomaterial characterization, which has turned out to be a cornerstone of this research. Prof. Santosh Kurinec's

creativity and enthusiasm for collaborative research projects brought the FLA MLD project from an idea to a reality. Thank you all for your insights and support.

I'm grateful to have worked and learned alongside numerous other researchers in Prof. Hirschman's Thin Film Electronics Research Group. Thank you to the FLA research team over the years: Karthik Bhadrachalam, Paul Bischoff, Viraj Garg, Adam Rosenfeld, Matt Hum, and Ankur Korad, who all helped to bring this research to its current state. Additionally, I'm deeply grateful to Patricia Meller for her patience and teaching instruction early on as I learned the ropes of the SMFL toolset.

Thanks also to: the staff of the RIT NanoFab/SMFL, whose eternal expertise keeps fabrication equipment operational; Prof. Scott Williams and the College of Science MLD group, for taking care of all the tricky chemical synthesis; and Lisa Zimmerman, for keeping me on track.

Finally, I am grateful to my parents, who have loved and believed in me even when I haven't. Their support has made this possible.

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LIST OF ABBREVIATIONS

Abbreviation	Meaning
AFM	Atomic force microscope
AOS	Amorphous oxide semiconductor
AR	Antireflective
a-Si	Amorphous silicon
a-Si:H	Amorphous hydrogenated silicon
BOE	Buffered oxide etch
CG, WG, FM	Cross-Grain, With-Grain, or Full-Mesa
CMOS	Complementary metal-oxide-semiconductor
CrLG	Chromium-enhanced large grain
c-Si	Crystalline silicon
CVD	Chemical vapor deposition
DVP	Diethyl vinylphosphonate
EDS	Energy-dispersive x-ray spectroscopy
ELA	Excimer laser annealing
FLA	Flash lamp annealing
FPD	Flat panel display
GIDL	Gate-induced drain leakage
HAADF	High-angle annular dark field
IC	Integrated circuit
IGZO	Indium gallium zinc oxide
ITO	Indium tin oxide
LCD	Liquid crystal display
LPCVD	Low pressure chemical vapor deposition
l-Si	Liquid silicon
LTPS	Low-temperature polycrystalline silicon
MIC	Metal induced crystallization
MLD	Monolayer doping
NFET	Negative field effect transistor
NMOS	Negative metal-oxide-semiconductor
OLED	Organic light emitting diode
PECVD	Plasma-enhanced chemical vapor deposition
PFET	Positive field effect transistor
PMOS	Positive metal-oxide-semiconductor
p-Si	Polycrystalline silicon
RIE	Reactive ion etch
RTA (or RTP)	Rapid thermal annealing / processing
SA	Self-aligned
SEM	Scanning electron microscope

Abbreviation	Meaning
SOI	Silicon-on-insulator
SPC	Solid-phase crystallization
SPER	Solid-phase epitaxial regrowth
SRP	Spreading resistance profiling
TAT	Trap-assisted tunneling
TCO	Transparent conducting oxide
TED	Transient-enhanced diffusion
TEM	Transmission electron microscope
TEOS	Tetraethyl orthosilicate
TFT	Thin film transistor
ULSIC, VLISC	Ultra / Very large-scale integrated circuit

LIST OF VARIABLES

A	Total absorbed energy per area
C_{ox}	Capacitance of oxide dielectric
C_p	Specific heat capacity
D_T	Thermal diffusivity
g_m	Transconductance: change in I_{DS} due to a corresponding change in V_D
I_{DS}	Current measured from source to drain of a transistor
I_{min}	Minimum drain current
I_{Tot}	Total emitted energy per area
I_{VT+10}	Drain current at a gate voltage of $10+\|V_T\|$
k	Coefficient of extinction (imaginary component of refraction)
L	Transistor channel length
n	Coefficient of refraction.
R	Total reflectance
R_p	Reflectance of *p*-polarized light
R_s	Reflectance of *s*-polarized light
SS	Subthreshold swing
t	Silicon thickness
T	Temperature
t	Time
V_D	Drain voltage
V_G	Gate voltage
V_T	Threshold voltage
W	Transistor channel width
x	Thickness of material, in absorbance calculations
x_T	Thermal diffusion length
z	Chromium agglomeration invasion distance
$\alpha(\lambda)$	Absorption coefficient at a particular wavelength
θ_i	Angle of incident light
θ_t	Angle of transmitted light
K	Thermal conductivity
λ	Wavelength
μ	Charge carrier mobility
μ_{chan}	Charge carrier mobility in the transistor channel
ρ	Material density

Chapter 1. INTRODUCTION

Flat panel displays (FPDs) have been a burgeoning industry for several years now, ever since first coming to the personal television market in 1997. Since then, the market share for alternative display configurations, such as projection or cathode ray, has been steadily subsumed by FPD until the present, when they have vanished from all but extremely niche sectors. And yet, the estimated market size for FPDs continues to increase. This expansion is driven now by novel display applications in our increasingly electronic world, as briefly illustrated in Figure 1.1. Smart appliances regularly bear flat panel readouts and personal vehicles are more and more heavily populated with touchscreens. It is clear that not only will the market for displays continue to increase for the foreseeable future, but that much of this growth will come from applications that may require novel technology to meet these demands.

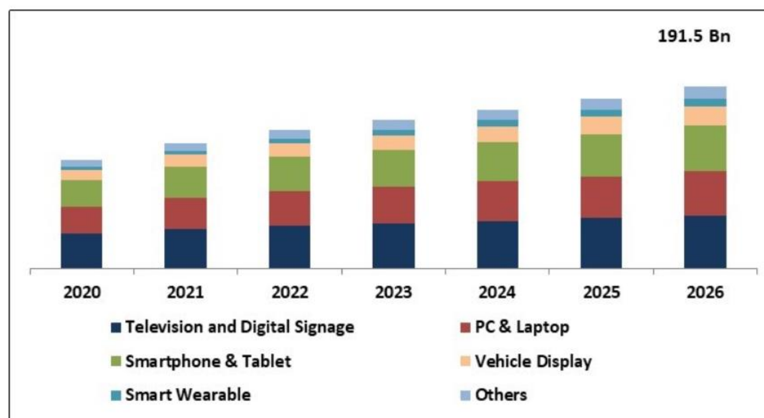

Figure 1.1: Rough projected market growth of FPDs by sector. From [1]

1.1 FLAT PANEL DISPLAY DESIGN

The construction of a flat panel display requires the creation of a matrix of dense and independently addressable elements which control outputs of light, either by regulating transmission of a separate light generation element or by toggling emission of light directly. These picture elements, or pixels, all exist on an array that can include up 8,294,400 pixels for a modern 4K display.

1.2 TRANSMISSIVE VS. EMISSIVE STRATEGIES

At heart, the pixel is a method of regulating the presence or absence of light in a specific area. This can be done through transmission regulation, in which a light source on a separate circuit is alternatingly blocked and transmitted, or through emission regulation, in which a single circuit controls the operation and cessation of small localized light sources directly. Both of these methods require the existence of a robust and independently addressable logic backplane. Figure 1.2 shows a comparison of these two methods of pixel mechanics.

Liquid Crystal Displays (LCDs) are the primary example of transmission regulation FPDs. In this structure, light emitted from a separate illumination backplane is passed through a polarization filter to leave uniformly polarized light. At the opposite end of the layer stack is another polarization filter of the opposite orientation, which normally blocks all light from transmitting. Between these filters, however, is a layer of liquid crystal material that responds to an applied voltage by twisting or untwisting, thus modifying the polarization of the light and allowing it to pass through a localized region [2]. The transistor logic layer of an LCD must therefore be designed to apply particular voltages across specified areas, while also having high overall transmission.

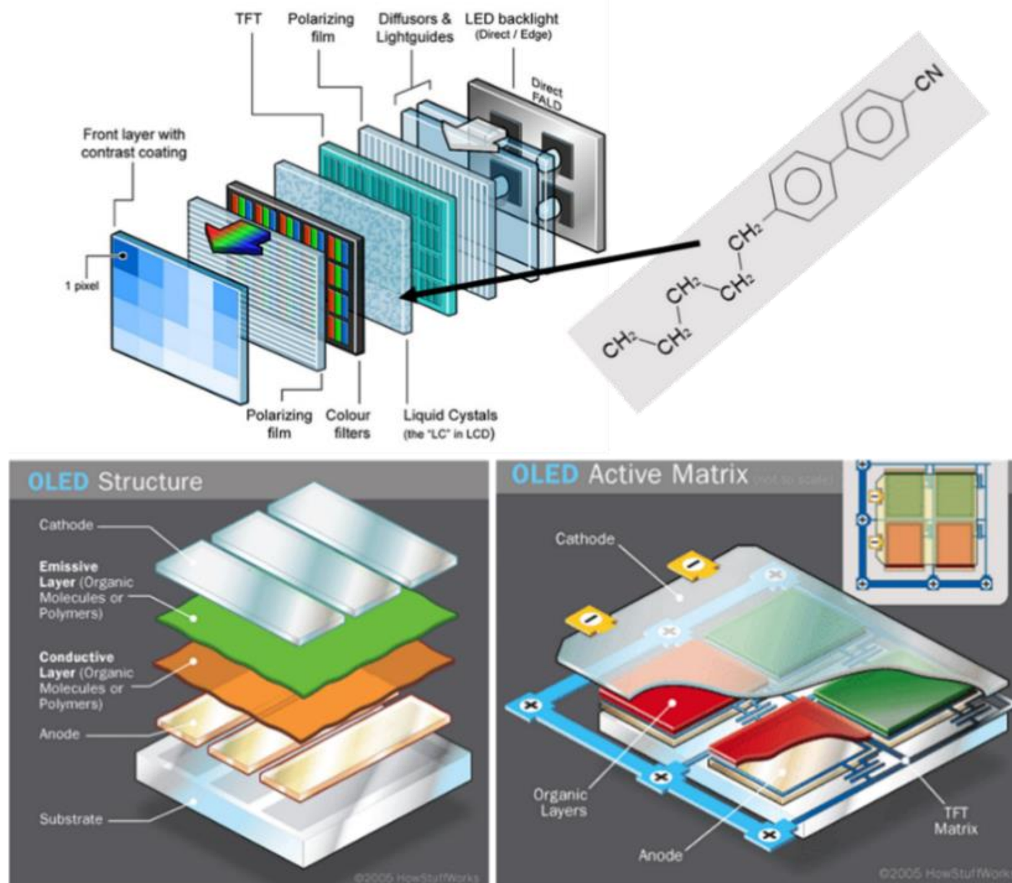

Figure 1.2: Diagram comparisons of LCD (top) and LED (bottom) display technology. Adapted from [3]

Emission regulation FPDs, in the current market, are primarily Organic Light Emitting Diode (OLED) displays. The structure of these is relatively simple, requiring only a transistor logic layer in the backplane to which an array of LEDs is affixed. These LEDs are built of an organic emissive layer that can be easily solution-deposited on a back electrode linked to the addressing logic backplane. Transistors directly control the functioning of their associated OLED, such that all current that passes into a diode to generate light must pass through a regulating transistor first [4]. This structure is thus a current-controlled system, and its transistors must be able to transmit a well-regulated current flow.

1.2.1 Display Transistor Semiconductor Material

An exploration of the technologies available in FPD design reveals that Thin Film Transistors (TFTs) play a pivotal role in their construction and have several specific requirements. The logic plane of a display must be thin and not obstruct light transmission, especially in LCDs. It must be fabricated directly on substrates used for displays, such as glass, which have a lower degree of thermal tolerance than silicon-based integrated circuit (IC) processing. Each transistor must have uniform electrical responses with those in other pixels to ensure all areas of the display operate identically. Finally, the resolution and refresh rates of displays are limited by the amount of current that can be passed through the transistor backplane.

For much of the history of displays in commercial electronics, the TFT logic plane was built from hydrogenated amorphous silicon (a-Si:H). This material was first considered for its ease of fabrication and compatibility with existing silicon processing techniques in IC fabrication facilities. A thin layer of disordered silicon can be conformally deposited at low temperatures using common chemical vapor deposition (CVD) techniques. Hydrogenation in a plasma or forming gas overpressure allows dangling silicon bonds to be passivated by hydrogen, reducing the number of electron traps within the material. The result was an extremely uniform material from a simple and glass-compatible process. Electron channel mobilities of a-Si:H tended to hover around 1 $cm^2/(Vs)$, which was sufficient for early displays [5].

As demands for higher resolution and quicker refresh rate increased, the FPD industry searched for alternative semiconductor materials and processing techniques that could offer superior performance to a-Si:H without compromising cost and manufacturability. Two main contenders emerged: Amorphous Oxide Semiconductors (AOS) such as Indium-Gallium-Zinc Oxide (IGZO)

and Low Temperature Polycrystalline Silicon (LTPS). The comparative strengths and weaknesses of these materials are shown in Table 1.

Table 1: Comparison of commercially mature TFT semiconductor materials for FPDs

	a-Si:H	**AOS (IGZO)**	**LTPS (ELA)**
Uniformity	High	High	Challenging
Process Complexity	Simple	Simple	High
Leakage Current	Low	Very low	Moderate
Channel Mobility	~1 cm^2/Vs	~10-15 cm^2/Vs	> 100 cm^2/Vs
Device Type	NMOS	NMOS	CMOS

Since being first demonstrated in 2004 by Nomura *et al*. [6], IGZO has quickly become the dominant oxide semiconductor in research and industry. IGZO can be deposited in an amorphous structure by a simple DC sputter [7], providing a uniform coating to any substrate size. Due to its *s*-orbital conduction mechanism, IGZO can conduct electrons in an amorphous state without causing scattering effects as in silicon and thus retains a fairly high mobility. However, IGZO can only produce NMOS devices and p-type AOS such as tin oxide are not yet technologically mature [8]. IGZO is suitable for large-area displays in which CMOS logic is not needed and an electron mobility of 10 cm^2/(Vs) is sufficient. For very high-performance displays, another material is needed.

1.3 Low Temperature Polycrystalline Silicon

LTPS is the preferred replacement material for a-Si:H in display applications where high carrier mobility is necessary. With proper preparation, the theoretical limit of LTPS electronic properties is that of bulk crystalline silicon [9], far surpassing both IGZO and a-Si:H. TFTs built on LTPS can be either n- or p-type depending on doping, making integrated CMOS logic possible. However, there are many challenges to effective LTPS fabrication.

The term “LTPS” is a blanket designation incorporating any method of in-situ crystallizing amorphous silicon after it has been deposited. As FPD substrates are typically glass, the thermal limit of this process is much lower than that of traditional integrated circuit silicon processing. Hence, low-temperature strategies are necessary and can be performed in two broad strategies. In a bulk heating method, both the a-Si layer and the substrate are heated to glass-compatible temperatures in a thermodynamic equilibrium. Depending on the properties of the glass used, this limits allowable sustained temperatures below 400 to 600 °C. In a surface heating method, a brief and targeted energy impingement process heats only the surface of the sample, allowing a-Si to potentially reach temperatures well in excess of that experienced by the substrate. Figure 1.3 demonstrates the design space of common bulk and surface heating strategies.

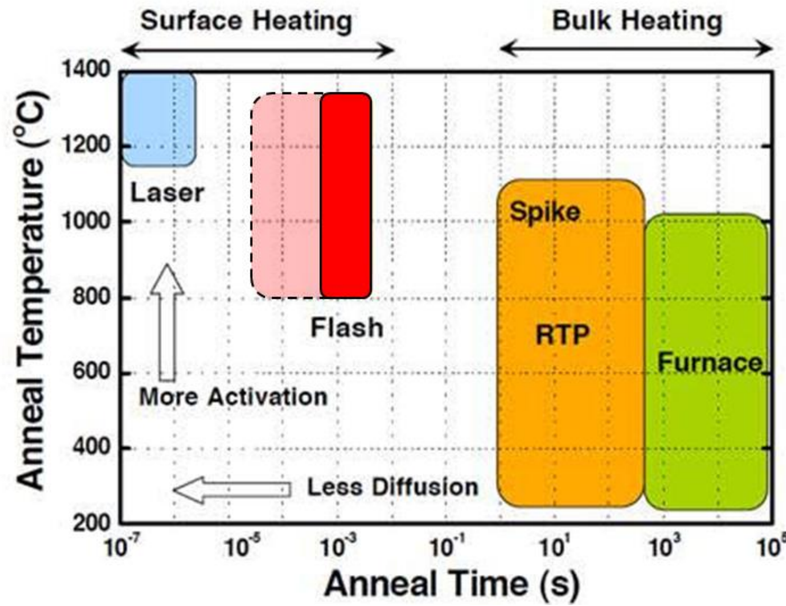

Figure 1.3 Demonstration of various short timeframe annealing techniques. Adapted from [10]

1.3.1 Bulk Annealing Methods

Bulk heating processes in LTPS consist of any method whereby the entire substrate is heated to the same temperature. As glass easily warps, melts, or cracks at common silicon processing temperatures, low-temperature strategies are necessary. If amorphous silicon is annealed in a furnace at 500 to 600 °C for long periods of time, it will crystallize through solid-phase nucleation to produce a uniform layer of very small grain polycrystalline silicon, which can still have reasonable electrical functionality [11]. However, a furnace anneal of 12 to 24 hours is rarely practical for an industrial practice.

LTPS can also be formed through bulk heating through Metal Induced Crystallization (MIC). In this method, a metallic phase, often aluminum, is added in contact with the a-Si layer and the sample is furnace annealed at a low temperature for a more reasonable amount of time. This allows the silicon to crystallize at a lower temperature, but also results in metallic contaminants thoroughly penetrating the LTPS layer [12]. More involved strategies, such as metal induced

lateral crystallization and metal induced layer exchange [13], have been developed to mitigate this effect, but contamination remains an obstacle that impedes technological adoption.

1.3.2 Surface Annealing Methods

LTPS in modern industrial applications is fabricated with Excimer Laser Annealing (ELA). This process irradiates an a-Si layer with a UV laser, such as XeCl which has a wavelength of 308 nm. The laser is usually designed as a line beam, with a long length and narrow width, such that it must scan along the entire area of a substrate, often in multiple passes depending on laser and substrate dimensions. Figure 1.4 demonstrates this scanning process and a typical current-technology system for performing ELA. This process can reliably crystallize an a-Si layer with a high degree of precision and neither damages the substrate nor introduces contaminants.

Figure 1.4: Diagram of ELA scanning process and photograph of a modern ELA system capable of crystallizing Gen 6 glass in a single scan. Adapted from [14]

However, ELA is an extremely expensive and time-consuming process. By definition, excimers do not exist in a ground state and must be continuously charged and discharged for each laser pulse. Though each pulse cycle is very rapid, each area of a-Si must be pulsed between 10 and 20 times for optimal crystallization [15]. For this reason, ELA systems are designed with line beam lasers to minimize the number of scan passes needed to sweep across a substrate. As typical

glass substrates increase in size, beam design becomes more challenging and requires multiple emitters to be coupled together. ELA is thus very expensive in both hardware and operational costs and presents obstacles for substrate scalability and throughput. Despite these shortcomings, it is the preferred method for producing high mobility TFT semiconductor material for displays due to its high mobility output.

1.4 FLASH LAMP ANNEALING

Flash Lamp Annealing (FLA) is an alternative surface annealing process that represents an intermediate point between extreme-surface ELA and bulk heating methods. The history of this technology is many decades old: Arc lamps were first introduced by Harold Edgerton in 1930 as a technique for high-speed photography [16]. These early systems used a mercury vapor through which streams of stored electricity could be discharged in the span of 1-5 seconds, the first reliable way of producing short, intense bursts of light without resorting to explosions.

Flash lamps were mainly limited to rapid lighting applications until the introduction of lasers for surface heating, when they were incorporated as a method for charging lasing cavities. It was not until a (possibly apocryphal) accident in which a sample intended for laser irradiation fell into the laser's flashbulb charging array that researchers made the lateral realization that the flash lamps used to charge up their lasers for surface annealing could be used for annealing themselves, thus cutting out an expensive middle step and increasing efficiency [17].

The modern FLA system can be seen as an evolution of Rapid Thermal Annealing (RTA), which in its introduction was also considered a "flash" process. Both systems incorporate a substrate-scale chamber in which samples to be annealed are inserted and heated to a background temperature, either by direct conduction or convection from halogen lamps. Once the sample has

stabilized to the proper temperature, it is exposed to an energetic discharge from one or more xenon flashbulbs in the span of 10 to 1000 microseconds. Multiple discharges may be performed in rapid succession to extend the annealing period. In a crucial difference between FLA and RTA, rapid emittance of energy via flashbulbs means the surface and base of a sample may not experience the same degree of heating. Figure 1.5 illustrates the structure of an FLA chamber.

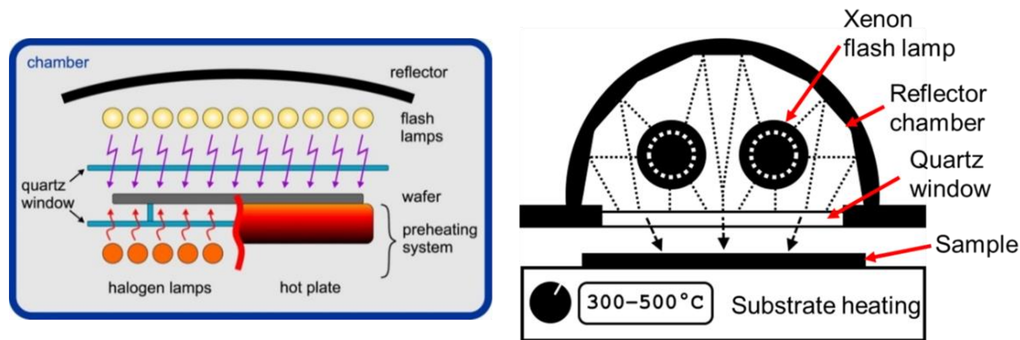

Figure 1.5: Left, diagram of possible FLA chamber structures, adapted from[18]. Right, diagram a simple, single-wafer scale FLA system representing the system used elsewhere in this document.

Xenon flash lamps are naturally a broad-spectrum emitter, making them less controlled as an energy source in comparison with XeCl excimer lasers. However, elemental xenon emits a large percentage of its energy in the near-UV, which is readily absorbed by amorphous silicon and not by glass. Figure 1.6 demonstrates this overlap; thinner a-Si will obviously absorb less. FLA is able to crystallize a large area of amorphous silicon as a sub-second or sub-millisecond process and the emission area is theoretically scalable to any size substrate simply by adding more flashbulbs; conversely, expanding the exposure area of an ELA system requires focusing a laser to a larger and longer spot homogeneous size, which is much more complicated.

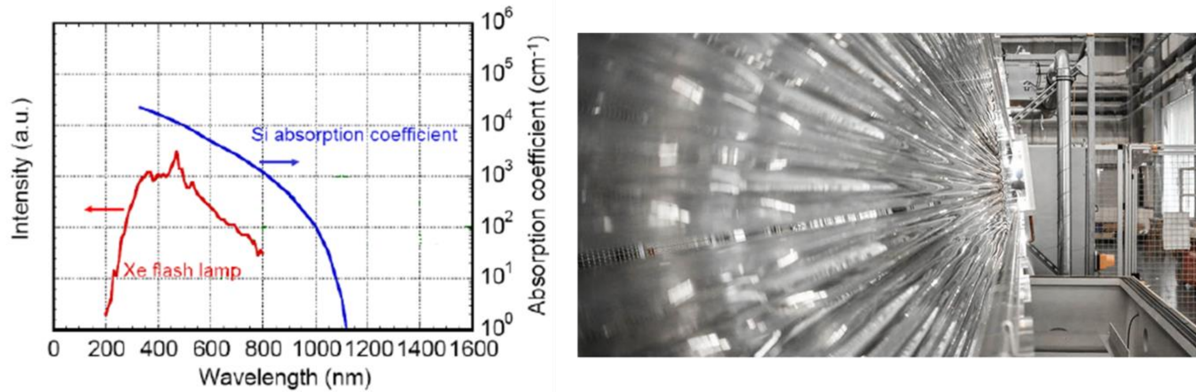

Figure 1.6: Left, emission spectrum of xenon and absorption spectrum of silicon, adapted from [19].. Right, 3.8 m flash lamp array for architectural coatings, from [20].

1.5 Extant Applications of FLA

Flash Lamp Annealing is a mature and well-studied technology in electronics processing which is incorporated into numerous applications requiring a broad-area surface heating. Its sub-second time scale makes it attractive not only for processes requiring thermodynamic non-equilibrium between surface and substrate, but also as a faster and more automation-friendly alternative to conventional furnace anneals.

1.5.1 FLA for Dopant Activation

The first published work involving thermal processes with flash lamps in silicon processing is likely Cohen et al. from July 1978 "Thermally assisted flash annealing of silicon and germanium" [21]. In this paper, FLA was used to heal damage to a crystalline silicon lattice caused by ion implantation with comparable results to that of long furnace annealing. Crystalline <100> silicon samples were implanted with a high dose of arsenic and exposed to successive FLA pulses.

Rutherford backscattering was used to show that each pulse reduced the thickness of the surface amorphized region while also incorporating the arsenic into lattice sites, as seen in Figure 1.7.

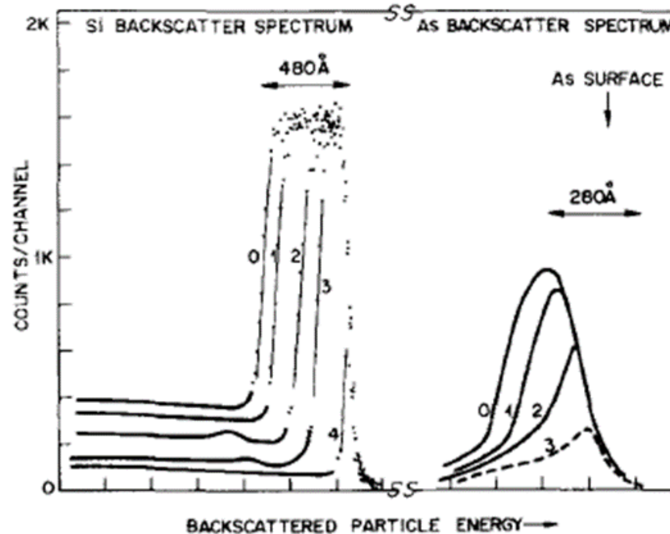

Figure 1.7: Backscatter signal of arsenic-implanted silicon after successive FLA treatments, indicating implant damage and possible arsenic uptake. From [21]. Figure quality reflects original publication.

Later in 1978, a paper from Bomke *et al*. titled "Annealing of ion-implanted silicon by an incoherent light pulse" [22] first explored the concept of using flash lamps as a method of activating implanted dopants in a bulk silicon sample. This research was inspired by recent interest in laser-induced dopant activation. The authors of this study assumed that the intensity of flash exposure would need to be sufficient to melt silicon and calculated (but could not directly measure) an attainable surface temperature of > 1600 °C; FLA energy density values were not recorded. By exposing silicon samples implanted with 10^{15} /cm^2 boron ions, the group was able to attain a spreading resistance reduction from 5500 Ω to 125 Ω. These two enabling sources demonstrated the value of FLA in microelectronics processing. Following these resources, FLA was used to

activate and measure implanted phosphorus [23], boron difluoride [24], and arsenic [25] ions with promising results.

At this point, FLA is a mature technology with respect to dopant activation in silicon. The work of Prucnal, Rebohle, and Skorupa has extended this field in numerous directions and enabled FLA dopant activation to become industrially viable. An excellent review paper from 2017 by those authors entitled "Doping by flash lamp annealing" goes into thorough detail about the many dopant activation and introduction applications for which FLA is used, in silicon and beyond [18]. The main advantages of FLA over other activation methods are its rapidity and efficiency in thin film processes [26], [27], its shallow junction capabilities in bulk processes [28]–[30], and its micrometer penetration in nanostructure arrays [31], [32], which can be important for targeting buried layers in complex structures.

1.5.2 FLA for Non-Silicon Processes

The increasing interest in FLA applications is not limited to traditional silicon semiconductors. This annealing method has found use in a wide array of electronics processing. A common use of FLA is to enhance the cracking of precursor gases in deposition processes to facilitate single-layer depositions. This process was first demonstrated in 1991 by Sakuraba *et al*. [33] as an extension to a similar excimer laser cracking strategy. In this work, Sakuraba successfully deposited atomic layers of germanium on silicon substrates from a GeH_4 source by using FLA as a heat source to interrupt surface adsorption reactions, generating a single Ge atomic layer per flash strategy. Figure 1.8 shows a schematic of FLA integration into this deposition process and the average thickness of each flash-deposition. After this success, the same technology was applied to the cracking of SiH_4 [34] and NH_3 [35]. This strategy is being refined to develop a technique of flash-

enhanced atomic layer deposition [36], offering a method of selectively adjusting the surface temperature of some stages in a multi-stage ALD process.

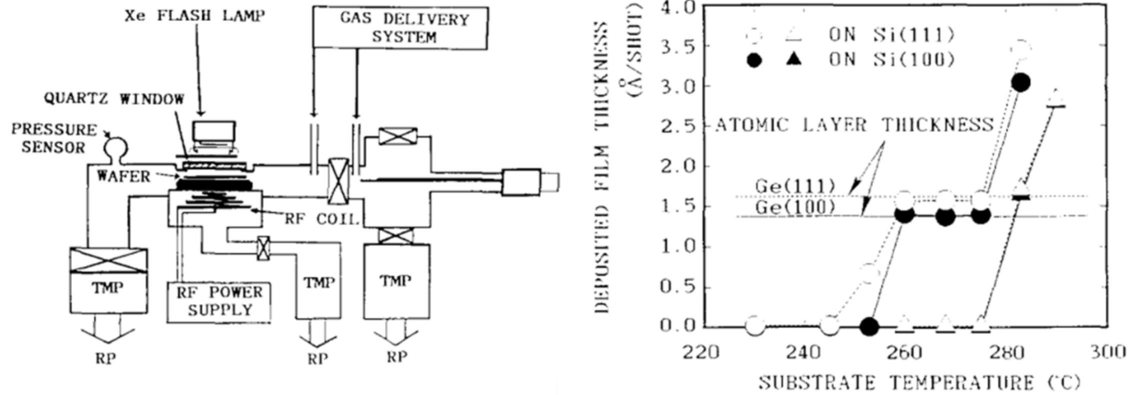

Figure 1.8: Left: Diagram of an FLA system integrated into a deposition process for the purpose of cracking an atomic layer of adhered molecules. Right: Average film thickness of 150 FLA-deposited Ge layers in a variety of substrate temperatures. The band of 260-275 °C very closely matches the empirical atomic layer thickness of Ge. Adapted from [33].

Departing from semiconductors entirely, FLA is often used in the electronics industry as an annealing method for the Transparent Conducting Oxide (TCO) Indium Tin Oxide (ITO). ITO has a wide arrange of applications as a material that is transparent in much of the visible light spectrum while still boasting a very high conductivity. As such, it is the most common top contact for any application through which light must travel without significant interaction, including many photovoltaic and display anodes. ITO can be deposited in a low temperature sputter and is thus compatible with most substrates; however, it must be annealed to improve its transparency and conductivity. Extended FLA treatments in the millisecond range have been shown to provide nearly all the benefits of a bulk furnace anneal [37], [38] in a much faster process that is compatible with thermally-fragile substrates, such as polyimide [39].

1.6 FLA FOR AMORPHOUS SILICON CRYSTALLIZATION

FLA was first used as a method for crystallizing amorphous silicon on glass by Loisel et al. in the 1984 paper "Flash lamp crystallization of amorphous silicon films on glass substrates" [40]. The authors used 300-500 nm a-Si films heated to 500 °C and exposed to a 200 μs pulse, though they did not record the irradiance intensity. Using this method, they determined that FLA could crystallize silicon in either "furnace-like crystallization" or "explosive crystallization". The former material had little texture and resembled that of nano-scale polycrystalline material obtainable through moderate-temperature furnace annealing, while the latter demonstrated optically visible elongated grain structure. Transmission electron microscope (TEM) analysis, shown in Figure 1.9, revealed these grains to be at most 15 μm in length.

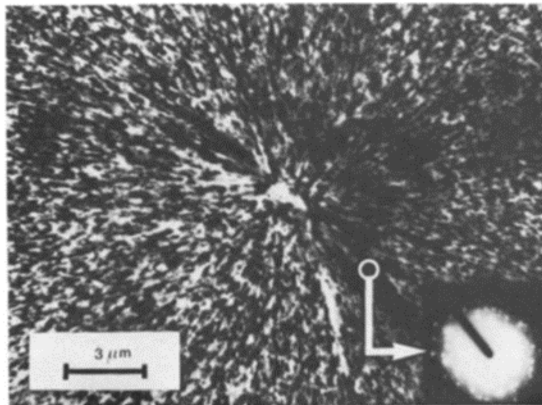

Figure 1.9: TEM of explosive crystallization after FLA, showing 15 μm grains. From [40]

It was not until 2004 that FLA was established as a means of in-situ crystallizing amorphous silicon on glass with controlled and well-described settings, with the paper "Crystallization of amorphous-Si films by flash lamp annealing" by Pécz et al [41]. This group deposited a-Si in 50-250 nm layers on glass substrates with a SiO_2 intermediary protective layer and irradiated these

samples for 20 ms with FLA exposures between 49 and 87 J/cm^2. Using this method, a variety of polycrystalline silicon structures were obtained and quantified. The authors noted a large dependence on substrate heating temperature and film thickness. Using a 50 nm a-Si film heated to 450 °C, they were able to produce maximum polycrystalline grain sizes of 60 to 100 nm in diameter with no mass transport identified, suggesting a solid-phase crystallization regime. When a 250 nm a-Si film heated to 600 °C was exposed to similar irradiance, the resulting mean grain size was 5 μm and produced texture characteristic of liquid silicon melting and recrystallization. These two morphologies are shown in Figure 1.10.

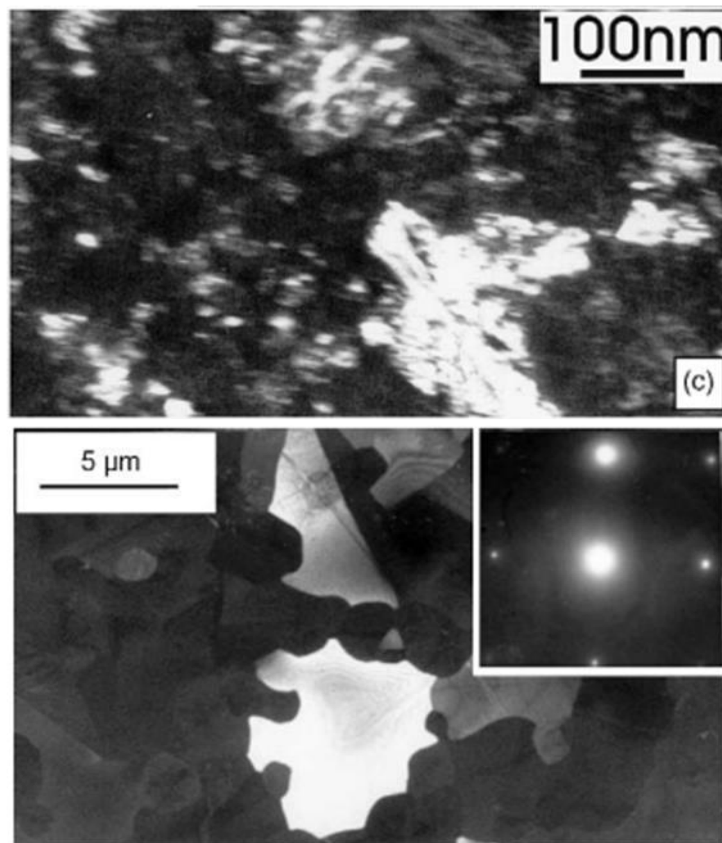

Figure 1.10: Top: Dark field micrograph of 50 nm a-Si at 450 °C substrate heating FLA crystallized with two pulses of 34 and 59 J/cm2, demonstrating average grain sizes of 100 nm with no significant surface texture. Bottom, DF micrograph of 250 nm a-Si at 600 °C substrate heating FLA crystallized with one pulse of 66 J\cm2, demonstrating average grain sizes of 5 μm and preferential [001] orientation. Adapted from [41]

1.6.1 FLA for Polycrystalline Silicon Photovoltaics

Based on the foundational work in crystallizing amorphous silicon via FLA, the group of Ohdaira *et al*. explored the use of FLA for LTPS formation in photovoltaic applications. Absorption of photons is a statistical process which increases in probability with the thickness of the absorbing medium, therefore PV requires at least several micrometers of semiconductor to properly function. In the 2007 paper "Formation of highly uniform micrometer-order-thick polycrystalline silicon films by flash lamp annealing of amorphous silicon on glass substrates" [42], the authors used high-intensity FLA to crystallize 3-4.5 µm of a-Si on glass. A chromium underlayer was incorporated initially for an electrical contact and back reflector. Figure 1.11 demonstrates some of their results.

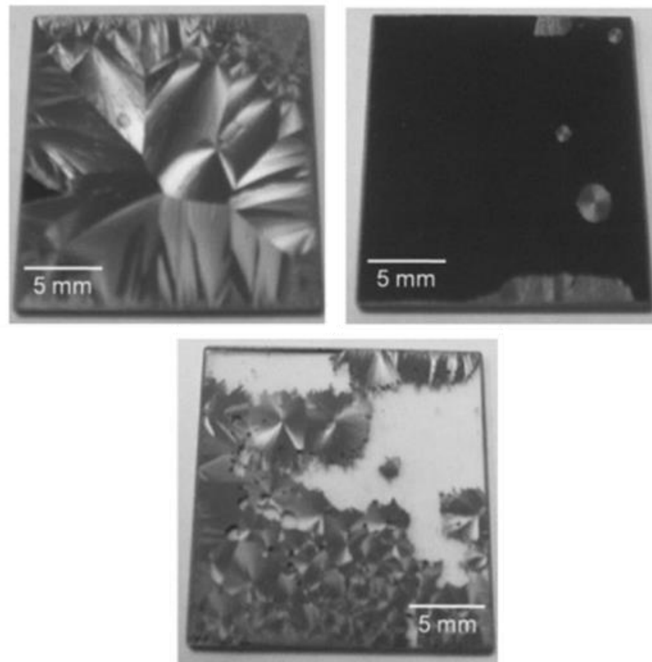

Figure 1.11 Top: FLA crystallization of 4.5 µm on Cr at "optimal" (left) and "low" (right) intensities. Bottom: FLA crystallization of 4.5 µm without Cr insert, demonstrating silicon flaking. From [42]

Ohdaira *et al.* discovered two important features of FLA polycrystalline silicon. First, the presence of very large directionally crystallized regions could be obtained and enhanced by increasing the thickness of the original a-Si layer. Tailoring the FLA intensity could produce either partial, solid phase crystallization or a liquid-phase explosive crystallization morphology. Second, the use of chromium as an underlayer strongly promoted adhesion of the LTPS layer in addition to its intended effects. Samples that did not include a Cr insertion were very likely to ablate and flake off in large areas. The research group of Ohdaira et al. further explored the crystallization and application of thick-film FLA LTPS in electrical [43], formation [44]–[46], and failure-state analysis [47]–[49].

1.6.2 FLA for LTPS TFTs

The first instance of a thin film transistor fabricated with FLA-crystallized polysilicon was presented by Saxena and Jang et al. in their 2010 paper "Polycrystalline silicon thin-film transistor using Xe flash-lamp annealing" [50]. The authors exposed a 50 nm a-Si layer on an SiO_2-coated glass substrate to a single high-energy 100 µs FLA pulse. With these conditions, they achieved elongated polycrystalline grains similar to Ohdaira's work on thick-film silicon on Cr. Figure 1.12 shows the material utilized in this process.

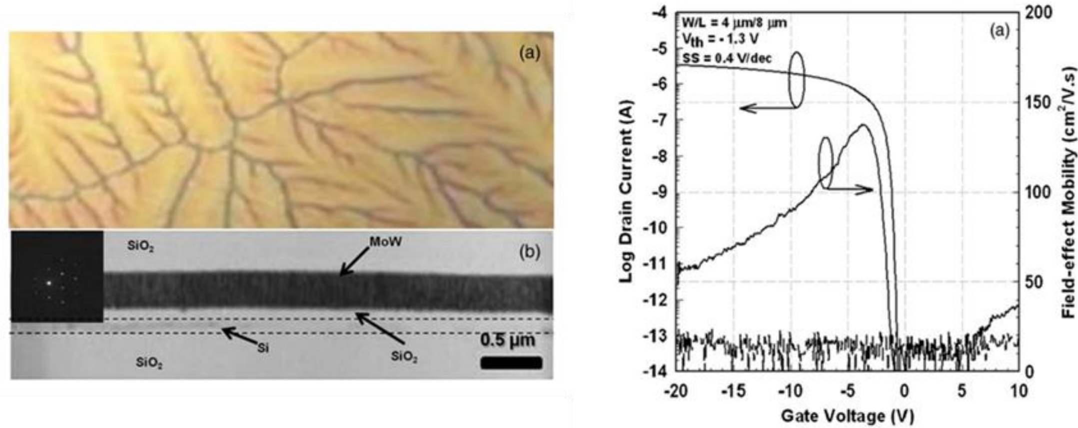

Figure 1.12 Left, Optical micrograph of obtained polysilicon morphology and TEM image of device channel showing no grain boundaries. Right, Current-Voltage switching characteristics of a L/W 4 µm / 8 µm FLA polysilicon TFT at V_D = -0.1. From [50]

From this material, a p-type polysilicon TFT was formed with boron ion-shower doping and low-temperature furnace activation. A device with channel dimensions of L/W 4 µm/8 µm was demonstrated, with electrical characteristics also shown in Figure 1.12. TEM analysis determined that no visible grain boundaries were present in the channel, making this a device built on a single silicon crystal. Excellent transistor operation was documented, with a steep subthreshold swing of 400 mV/dec, a threshold voltage of -1.3 V, and extracted field-effect mobility of 138 cm^2/(Vs). Only low drain bias characteristics were presented, thus there is no way to determine the stability of this device or the degree of off-state leakage at high drain potential.

This work was followed by Saxena and Jang in 2011 with "Protrusions of super grains formed by ultrashort Xe flash-lamp annealing of amorphous silicon and its effects on the performances of thin-film transistors" [51]. In this work, the authors further demonstrated the morphology of their FLA polysilicon material, explicitly highlighting what they termed super grains and their growth structure. Figure 1.13 shows some adapted figures from this work. Using electron backscatter

diffraction and other techniques, they posited that very large grains of polycrystalline silicon were forming in seeds and growing radially outwards, also protruding away from the substrate.

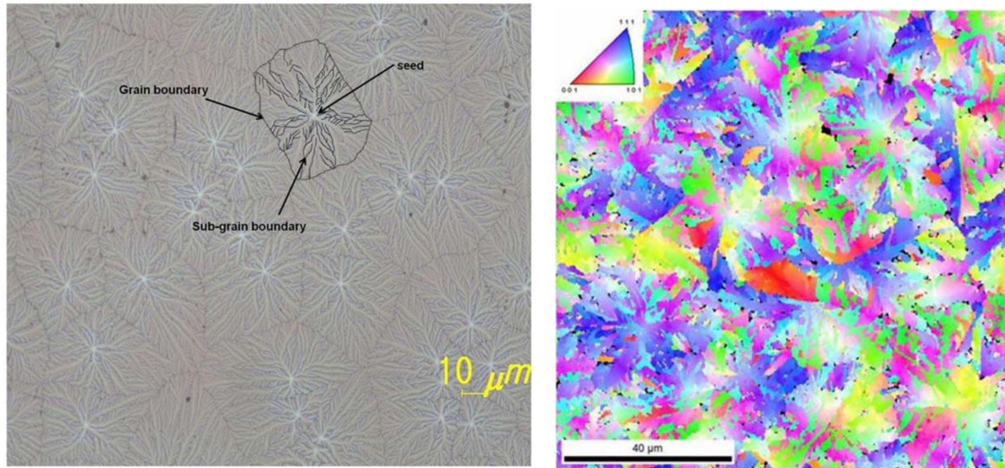

Figure 1.13: Micrograph and electron backscatter diffraction images of super grains. From [51]

Several TFTs were presented in this work and compared by the number of grain boundaries visible within the channel. The authors presented an inverse relationship between number of grain boundaries and maximum field-effect mobility, which corresponds well with the understanding of grain boundaries in polycrystalline silicon as areas of charge scattering [52]. Thus, the feasibility of FLA polycrystalline silicon for the production of p-type TFTs at low drain bias was well established.

After Jang's work in 2010-11, research in this field pivoted away from FLA and towards other methods of producing LTPS for TFTs. Refinements in ELA [15], [53] and continuous-wave annealing methods [54], [55] including blue-light diode annealing [56]–[58] appeared more promising; though expensive, these techniques appeared to offer greater control and precision at a cost of throughput. However, as FPD markets expand into more and more novel applications, a need arises for additional competing methods of LTPS fabrication, in which extremely high degrees of control are less important than high yield and processing simplicity.

1.7 Goals of this Study

The goals of this study can be classified as an exploration of different mechanisms for implementing FLA in the crystallization and processing of thin film polycrystalline silicon, with a focus towards its industrial implementation as a complementary technology to ELA-LTPS, by using a variety of techniques: analysis of physical properties and crystallization patterns, exploration of TFT device configuration, development of novel doping techniques, and analysis of novel combined material systems. The following listing summarizes key accomplishments achieved in each component of the investigation.

- Relation of FLA exposure parameters and silicon sample parameters to extent and pattern of crystallization: Development and characterization of a strategy of a-Si mesa pre-patterning prior to FLA. Identifying proximity-impeded crystallization. Wide-scale comparisons of intensity, substrate heating, silicon thickness, and film stack composition.
- Expansion of FLA LTPS TFT development: Replication of existing state-of-the-art work and extension into CMOS-compatible structures. Development of a scalable alternative process with self-aligned devices realized down to existing LCD display TFT backplane scales. Establishing a truly low-temperature "FLA-Only" crystallization and activation process compatible with thermally fragile substrates. Establishing and characterizing the first bottom-gate FLA LTPS TFTs using a novel TCO gate.
- Development of doping techniques unexplored in LTPS TFTs: Improvement of dopant activation at low, glass-compatible temperatures with Si-ion preamorphization.

Development of a monolayer doping – FLA activation process for TFTs, including the first demonstration of MLD on amorphous surfaces and gallium MLD for p-type devices.

- Investigation into novel thin-silicon-on-chromium system for LTPS electronics: Identification and characterization of material at the micro- and nano-scale. Analysis of chromium distribution during and after crystallization, and its impact on electrical behavior of TFTs. Electrical analysis of numerous configurations of TFTs constructed on this material.

1.8 DOCUMENT OUTLINE

The first chapter of this document briefly explains the motivation of an investigation into FLA LTPS for display application TFTs, as well as providing a historical background of the technology in relation with other technologies in the same field. The remainder of the document is organized as follows:

Chapter 2 outlines the physical systems associated with FLA LTPS crystallization. It positions FLA as an intermediary between isothermal bulk heating and fully nonequilibrium laser annealing and explores the optical, thermal, and phase change factors that are relevant to understanding the process. Lastly, various mechanisms of crystallization are briefly considered.

Chapter 3 details several experiments into FLA-crystallized LTPS from a material analysis standpoint. The individual layers of a crystallization sample film stack and their respective functions are explained. Following this, some obstacles associated with FLA LTPS are identified

and demonstrated, including silicon dewetting and proximity-dependent behavior. Variations on pulse intensity, silicon sample thickness, and underlayer material are presented.

Chapter 4 details several experiments on TFTs made using FLA LTPS as a semiconductor. The timing and methodology of dopant introduction is identified as a key factor in device functionality, and experiments are presented using a pre-amorphization ion implant and self-aligned device configurations. Additionally, comparisons of dopant activations are made between various furnace anneals and a multi-stage full-FLA process. Lastly, bottom gate devices made using a transparent conductive oxide are demonstrated.

Chapter 5 explores monolayer doping, a recent advancement in dopant introduction, to the FLA LTPS system. Phosphorus MLD is used to demonstrate the compatibility of these techniques by producing functional n-type TFTs. Gallium MLD is then demonstrated for the first time, producing functional p-type TFTs.

Chapter 6 introduces an FLA LTPS morphology incorporating a thin chromium adhesion layer to produce edge-directed crystallization with very little dewetting and much larger crystal grains. TFTs fabricated on this material demonstrate promising behavior, though issues associated with chromium contamination are identified. The chromium-enhanced LTPS is then investigated in detail with various microscopy techniques to identify the behavior and distribution of Cr during and following crystallization, revealing and explaining the material's unique texture at the nanometer scale. Using this, a hypothesis of the electrical impact of this contamination is justified using a comparative study of different thicknesses of TFTs.

Chapter 7 is a broad integration of MLD, dopant timing, full-FLA processing, and chromium-enhanced crystallization in a comparative study of FLA LTPS processing techniques using

phosphorus-doped NMOS TFTs. Certain combinations of techniques are identified as incompatible, while others produce promising electrical behavior.

To conclude this thesis, Chapter 8 lists a summary of key findings and contributions, including suggestions for additional research into this field.

Chapter 2. Relevant Physical Systems of FLA LTPS Crystallization

Flash lamp annealing (FLA) is a complex thermal process that takes place outside of thermodynamic equilibrium, but not so far outside that impacts to surrounding material can be entirely ignored. Elements of optical absorbance, heat transfer, liquid phase transition from a metastable amorphous state, and recrystallization pathways must all be considered. The mechanism of crystallization is directly related to polycrystalline grain size and thus quality of semiconductor material; this factor is dependent on the degree of liquid-phase undercooling and the extent and location of simultaneous melt.

2.1 Comparison of System Physics

The physics of crystallization by flash lamp annealing are complicated and incorporate many factors that act on different time scales. This annealing method is most easily considered in a contrast to two similar methods which also use light to anneal and crystallize thin films: Rapid Thermal Annealing (RTA) (or sometimes Rapid Thermal Processing (RTP)), and laser annealing, especially pulsed Excimer Laser Annealing (ELA). In many ways, FLA occupies a middle ground between these methods and exhibits some of the benefits and drawbacks of both.

RTA is a method in which a sample is loaded into a chamber and heated to a pyrometer-monitored setpoint with a bank of halogen lamps in a controlled environment for a set duration. Well-designed RTA systems can ramp up chamber temperature at a rate of > 500 °C/s, allowing

for the programming of temperature "spikes" to rapidly encourage the regrowth of damaged crystal lattice and the uptake of interstitial dopants, which can then be rapidly cooled down with attached cooling systems [59]. This annealing technique was originally used in semiconductor processing as a method of quickly forming silicides to better contact metals such as titanium to silicon [60], but quickly found a niche as an alternative method of thermally activating dopants introduced by ion implantation as the existing method of heating samples for a long duration in a conventional furnace resulted in significant dopant diffusion and undesirably large junction depths. As devices began to be scaled down below the micrometer level, ultra-shallow junctions went from being desirable to necessary.

Like the furnace annealing it was designed to complement, RTA is a bulk heating, or isothermal, process: the entire thickness of the sample experiences the same overall temperature characteristics for the duration of the anneal. As the process is in thermal equilibrium, it is simple to measure the temperature at any point in the sample; it is assumed to be uniform throughout for all appreciable timescales [61]. Thus, RTA on thermally vulnerable substrates like glass must be carefully engineered to prevent substrate damage, usually by limiting temperature spikes to < 550 °C. In summary, RTA is a controllable and scalable process that takes place on a timescale of seconds to minutes and results in the uniform heating of an entire sample simultaneously, laterally and by depth.

In contrast, excimer laser annealing (ELA) is a heat treatment in which a rapidly-pulsed exciplex laser with a targeted emission wavelength is scanned across the surface of a sample. The lasing material, such as XeCl, can only be formed in an excited state and rapidly dissociates after emission, necessitating a cycle of charging and discharging with each pulse window lasting a few tens of nanoseconds. Though the pulse repetition rate of excimer lasers can reach the kilohertz

range, the extreme brief heating and cooling cycles of ELA effectively make each pulse closer to a self-contained event than a continuous scan. ELA operates in full thermodynamic disequilibrium, with all sample heating being limited to the < 100 nm irradiated surface: the backside of the sample is virtually untouched and remains at its initial temperature. This makes laser annealing a very attractive technique for applications with thermally fragile substrates [62].

Since ELA operates so far away from equilibrium, the precise absorption properties of the sample become important to understand. This includes the individual extinction coefficients, thicknesses, and intermediary interference effects of every material within the laser penetration depth. Fortunately, the single-wavelength emission and direct, collimated beam make the amount of energy absorbed fairly easy to model, and the ultra-short penetration prevents a significant amount of lateral heat propagation. This is fortunate, as direct temperature measurement during the nanosecond timescale is very challenging to measure.

FLA occupies a midpoint between these two techniques. The typical duration of a flash lamp discharge is on the order of tens of microseconds to hundreds of milliseconds. This irradiance is not long enough of a duration to fully heat the sample to a steady state, but it is still significantly more than the ultra-shallow surface-only impact of ELA. The duration of the FLA pulse can even be adjusted to penetrate more deeply or shallowly into the sample. Therefore, FLA is in a less isolated version of thermodynamic disequilibrium. A typical depth of impact is on the order of < 10 μm, based on the material properties of the sample.

The light emitted by a flash lamp is less computationally simple than that of an excimer laser. Flash lamps are typically filled with a single inert gas, such as xenon, and are therefore broad-spectrum emission sources. Unlike the halogen lamps in RTA, the exact, wavelength dependent absorption at each depth of the sample factors into the sample's transient thermal behavior. Thin

films are typically not blackbody absorbers, meaning some energy will be transmitted at every point and much of the pulse may pass through the sample altogether. This analysis only becomes more complex if the sample is not laterally uniform, as the exposure window of an FLA pulse is large enough to have a significant lateral component. Additionally, the short timescales and material dependence of FLA make in-situ temperature measurements difficult.

The primary advantage of FLA is in scalability and ease of industrial integration. The exposure area of a single FLA pulse can be theoretically expanded to any size by linking an array of flash lamps with the appropriate overlap and capacitance banks [20]. Similarly, a scanning multishot strategy has been demonstrated [63]. Either of these methods are compatible with roll to roll and highly-automated processing, representing a heat treatment that takes less than a second from start to finish.

In comparison, ELA is a scanning process that requires a laser line spot to be carefully traced over the full surface of the material to be annealed. Shaping an excimer laser to the full width of a modern substrate remains difficult, though there have been advancements in coupling multiple laser emitters into a single spot line. This is a significant bottleneck in LTPS display fabrication. RTA, meanwhile, is theoretically scalable to any substrate size, but strictly limited to temperatures that will not damage those substrates. Additionally, doing so requires the construction of a sealed furnace chamber designed exactly for the substrate and process. This becomes unwieldly at current and future glass substrate sizes.

2.2 RELEVANT PHYSICAL FACTORS

The combination of relatively large interaction volume and non-equilibrium time scales makes FLA more complicated to model than its counterpart heat treatments. The crystallization of thin silicon films by flash lamp annealing relies on a series of interplaying factors.

2.2.1 Optical Factors

The lamps used in FLA are frequently xenon flash lamps, though krypton and argon lamps exist. Each has a characteristic output spectrum, which is most strongly dependent on gas species and any sort of filtration or absorbance imparted by the flashtube jacket. Though these emission spectra can be interpreted as a series of discrete emission lines [64], they are experienced at the sample as a continuous and uneven distribution of frequencies due to reabsorption and secondary emission within the plasma.

A very simplistic analysis of light absorption in a single thin film, ignoring reflectance losses, follows the Beer-Lambert law, which for a distinct set of wavelengths λ can be written as:

$$A = I_{\mathrm{Tot}} \sum_{\lambda_{\mathrm{min}}}^{\lambda_{\mathrm{max}}} \varepsilon_{\lambda}\left(1 - e^{-\alpha(\lambda)x}\right)$$

(Eq. 1)

where A represents the total per-area energy absorbed, I_{Tot} is the total energy emitted over that area, ε_{λ} is the fraction of energy emitted at a specific wavelength, $\alpha(\lambda)$ is the absorption coefficient of the material in that wavelength, and x is the thickness of the absorbing material. The absorption coefficient is more frequently given as a set of extinction coefficients k, such that:

$$\alpha(\lambda) = 2\lambda k_{\lambda}$$

(Eq. 2)

Here, energy not absorbed is assumed to be transmitted further through the sample [65].

Figure 2.1 provides an overview of the refraction and extinction coefficients of amorphous silicon deposited at temperatures between 275 and 775 °C via electron beam evaporation [66]. Several important factors are clear from these graphs. First, the great majority of the absorption spectrum of a-Si is in the near-UV region and drops sharply as photon energy decreases below 3 eV, or 424 nm. Second, despite this diminishing response, amorphous silicon still has a much higher absorption than crystalline silicon over most of the visible spectrum. Third, different deposition methods will produce amorphous silicon that has wildly different absorption characteristics, with a greater degree of absorption corresponding with less energetic deposition conditions.

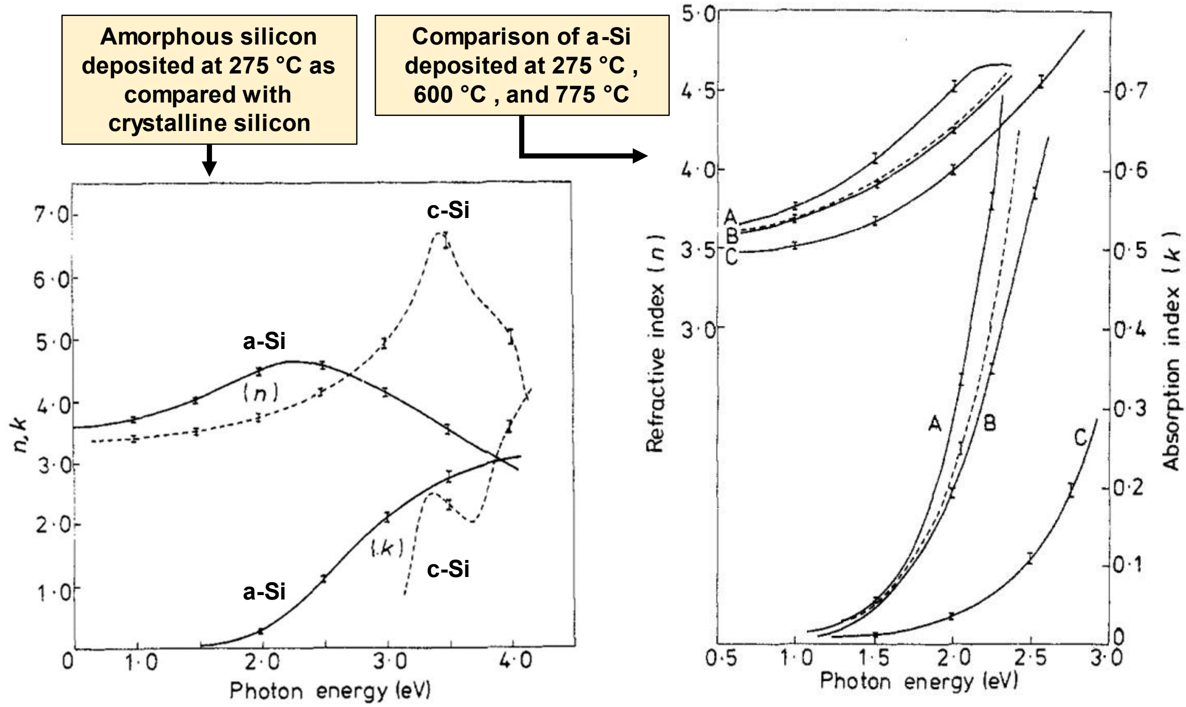

Figure 2.1: Left: Extinction and refraction coefficients of amorphous silicon (solid curve) as compared with crystalline silicon (dashed curve). Right: Extinction and refraction coefficients of amorphous silicon deposited by e-beam evaporation at 275 °C (A), 600 °C (B), and 775 °C (C). Adapted from [66]

This analysis assumes negligible reflectance loss, which is not strictly accurate. To estimate external reflectance losses, the Fresnel equations can be applied:

$$R = \frac{R_S + R_p}{2} = \frac{1}{2}\left[\left(\frac{n_1 \cos\theta_i - n_2 \cos\theta_t}{n_1 \cos\theta_i + n_2 \cos\theta_t}\right)^2 + \left(\frac{n_1 \cos\theta_t - n_2 \cos\theta_i}{n_1 \cos\theta_t + n_2 \cos\theta_i}\right)^2\right]$$

(Eq. 3)

Where n_1 and n_2 are the wavelength-dependent refractive indices of the initial medium (air or another FLA ambient) and the outermost sample layer respectively, θ_i and θ_t are the angle of incident and transmitted light respectively, and R_S and R_P represent the components of *s*- and *p*-polarized light. This average assumption is valid because the incoming light from flash lamps is

mostly nonpolarized. To further simplify this equation, it can be assumed that the average incident angle of light is normal to the sample, allowing the substitution:

$$R = \left(\frac{n_1 - n_2}{n_1 + n_2}\right)^2$$

(Eq. 4)

In order to minimize initial reflectance losses in FLA silicon crystallization, SiO_2 is often deposited as an antireflective (AR) capping layer. The refractive index of SiO_2 is much closer to that of air: about 1.5 at a wavelength of 600 nm as opposed to about 4.0 for a-Si, thus reducing reflectance constant at the outer surface from 0.36 to 0.035. The added interface between the SiO_2 and the a-Si adds an additional reflectance loss of 0.22, but this is still an improvement of 30% over no capping layer. Figure 2.2 demonstrates the ideal reflectance loss caused by three variations on an AR SiO_2 capping layer. Different portions of the emission spectrum will be lost to the sample based on AR thickness, which can be tailored to prioritize certain segments of wavelength. A capping layer of 100 nm of SiO_2 was used for most of the research in this document.

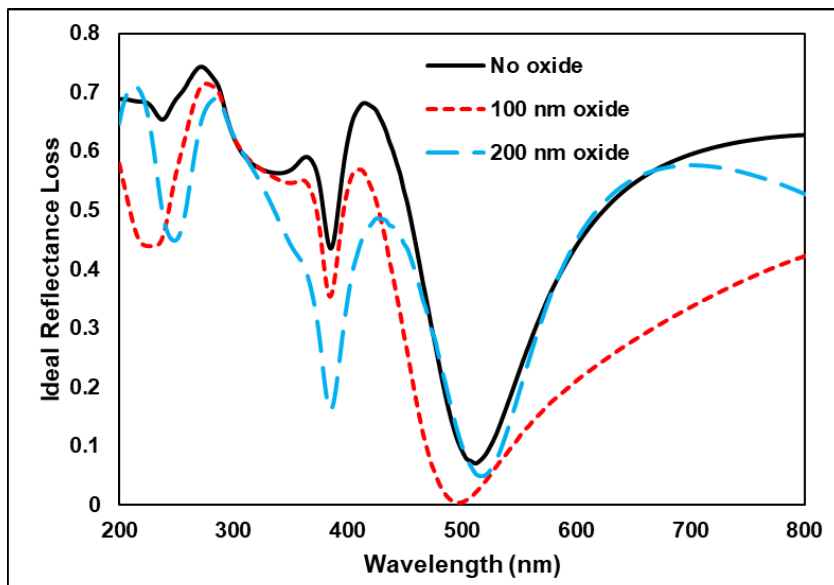

Figure 2.2: Reflectance losses in an FLA film stack of 60 nm Si on glass with no antireflective SiO_2 (black), 100 nm SiO_2 (red), and 200 nm SiO_2 (blue).

In a sample with multiple thin films, internal reflections at film interfaces can also be a significant factor. The fraction of transmitted light that reaches each interface can also be thought of as reflecting in the same normal-incident manner. For interfaces below the layer to be crystallized, this back-reflectance can result in an increase in optical path. In addition, the assumption of an effective normal angle of light incidence breaks down when considering the variation in n based on the wavelength of emitted light, implying that some wavelengths will be reflected and refracted much more strongly than others and will be less likely to reach the sample, or to enter the sample from extreme angles that encourage external reflection. FLA, unlike ELA, is absolutely not a one-dimensional system, and this presents one of many additional challenges associated with properly modeling its behavior.

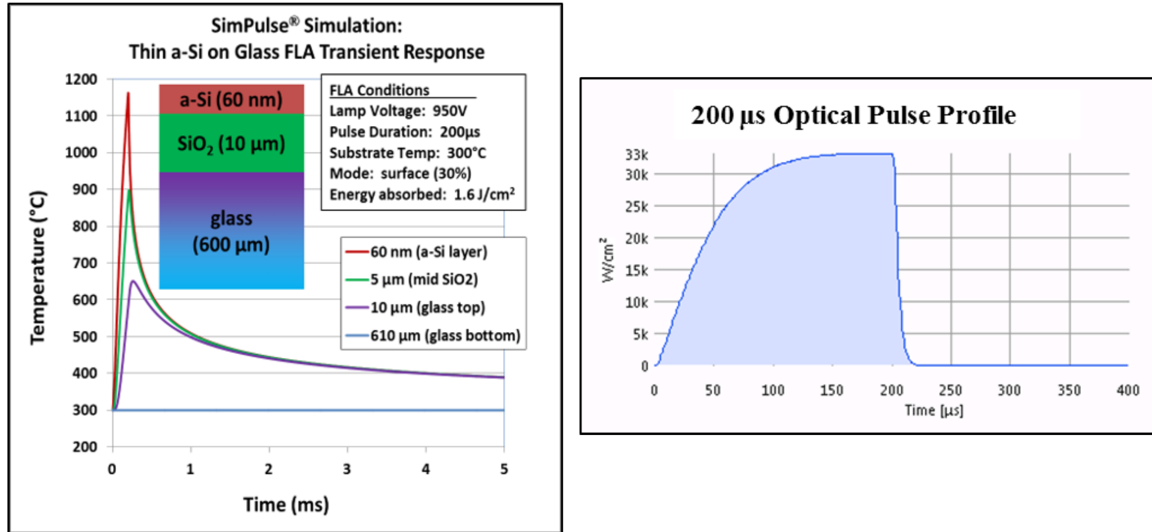

Figure 2.3: Left: one-dimensional simulation of temperature attained in a sample exposed to FLA with 300 °C substrate heating and an estimated 30% pulse absorption to account for reflectance losses. Right: example pulse profile for an FLA system.

Figure 2.3 demonstrates a simple, one-dimensional simulation of sample temperature over time for a thin layer of a-Si on a quartz/glass substrate, modeled in NovaCentrix's bundled SimPulse® pulse visualization software [67]. When an energy absorbance of 30% is estimated, temperatures exceeding the a-Si melting point are rapidly attained in a pulse window of 200 µs, with the full effective thermal cycle taking place in less than a millisecond. More thorough optical analyses of FLA might incorporate the change in refractive index and extinction coefficient of a material as a function of temperature, rather than treating all absorption as occurring to a sample at a steady initial temperature. The rate at which the sample actually heats up is commensurate with the timescale of a FLA pulse, as opposed to the nanosecond-scale pulses of ELA. This implies that some percentage of irradiance will impact the sample at a much hotter temperature than the initial burst of energy. Further factors that may complicate optical analysis include interference and lensing effects of a patterned sample and non-normal fringing light from the reflector chamber inside the FLA system.

2.2.2 Heat Transfer

The absorption of light from a flash lamp system raises the energetic level of a sample, which is mostly experienced as an increase in internal heat. This creates a temperature gradient within the sample, which is distributed from hotter to colder areas in a time frame that extends beyond the duration of the FLA pulse. The degree of transfer and temperature over time of the sample is determined not only by the duration and intensity of the pulse but also the by the sample's material properties. The most important factor to determine heat transfer in FLA is a sample's thermal diffusion length:

$$x_T = \sqrt{D_T t}$$

(Eq. 5)

where the thermal diffusivity D_T is a material property represented as:

$$D_T = \frac{\kappa}{\rho C_p}$$

(Eq. 6)

Here, κ is thermal conductivity, ρ is material density, and C_p is specific heat capacity, while t is the time over which heat is transferred. These factors, κ, ρ, and C_p, are each functions of temperature.

2.2.3 Crystallization

Amorphous silicon represents a phase with a higher free energy than that of crystalline silicon due to its disordered state, which comes about as a consequence of its low-temperature deposition or formation. It is effectively in a metastable state and can transition to a more stable regime, approximating crystalline structure, in several ways. The simplest is through a "relaxation"

process, in which heat or energy below the level necessary for melting is applied to the system. This produces a slightly more stable and “less amorphous” material based on the temperature and time to which it is applied. Relaxation temperatures are vaguely defined and significant impacts have been demonstrated with temperatures as low as 400 °C. In an extreme case, this results in solid-phase crystallization (SPC), which produces a polycrystalline phase with very small average crystal sizes; on the order of a few nanometers in diameter.

Another method of a-Si crystallization involves melting and recrystallization. In this method, the amorphous layer is raised to a temperature above its point of fusion, causing a liquid-phase transition. Since a-Si exists in a higher state of free energy than c-Si, it requires less energy to promote to a liquid state and thus has a lower melting temperature [68], [69]. This effect has been experimentally demonstrated through much research, though it has been a somewhat contentious finding [70]. Figure 2.4 demonstrates the free energy of various phases of silicon and the corresponding, empirically determined melting temperature.

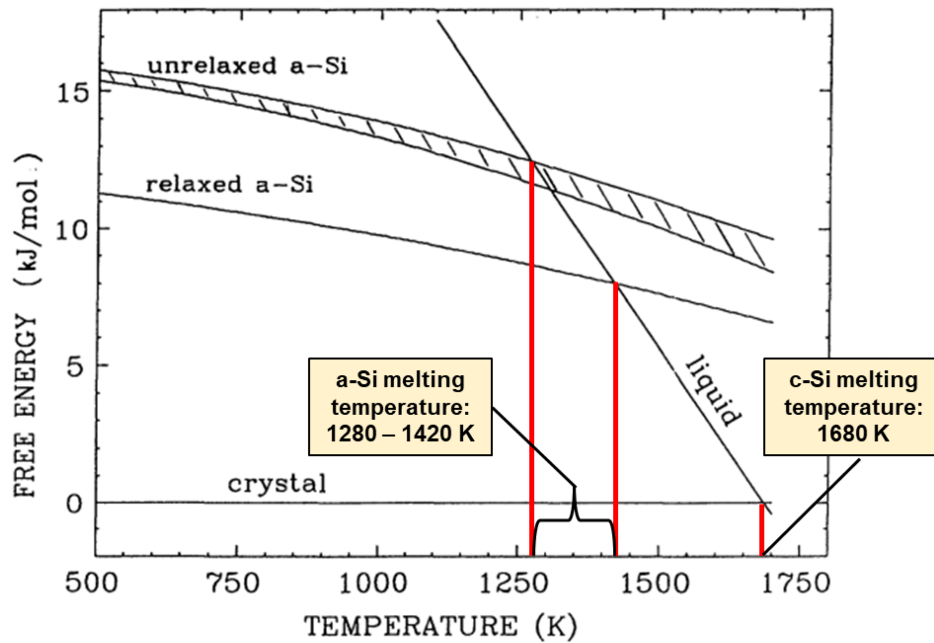

Figure 2.4: Free energy diagram of amorphous silicon as deposited and after a 450 °C relaxation heat treatment, normalized to crystalline silicon. Adapted from [69]

Once an area of amorphous silicon melts at around 1410 K, it enters a supercooled liquid phase. From there, fusing into a crystalline structure is thermodynamically favored, which may propagate through nucleation or by expansions of surviving crystalline phases. Nucleation is a kinetic process with a strong dependence on both the absolute temperature of a process and the difference in the free energy of phase formation [71], and stable nuclei are much more favorable at interfaces than in a homogeneous bulk of liquid silicon. Growth by existing crystalline phase expansion is also much more likely at an interface, as the lower deposition interface of a-Si on a substrate will have more non-amorphous content. Growth of a c-Si phase can also occur through solid phase crystallization, but this becomes increasingly unlikely as the temperature of the system increases.

A one-dimensional system of FLA crystallization of amorphous silicon on glass was modeled and experimentally validated in 2005 by Smith *et al.* [72]. In their system, a 100-250 nm a-Si layer deposited on glass by low pressure chemical vapor deposition (LPCVD) at 600 °C was exposed to a single, high energy FLA pulse. Smith found that only about 40% of emitted flash lamp energy was absorbed into the silicon, with 50% lost due to reflectance. By varying the FLA intensity, crystalline regimes with different average grain sizes from 10 nm to 6 µm could be predicted by the model and verified through experiment. Figure 2.5 demonstrates the enthalpy-based state diagram used in this model, in which silicon could be either in amorphous, crystalline, undercooled liquid, or non-undercooled liquid state, with isoenergetic phase transitions in the form of SPC and liquid-phase nucleation.

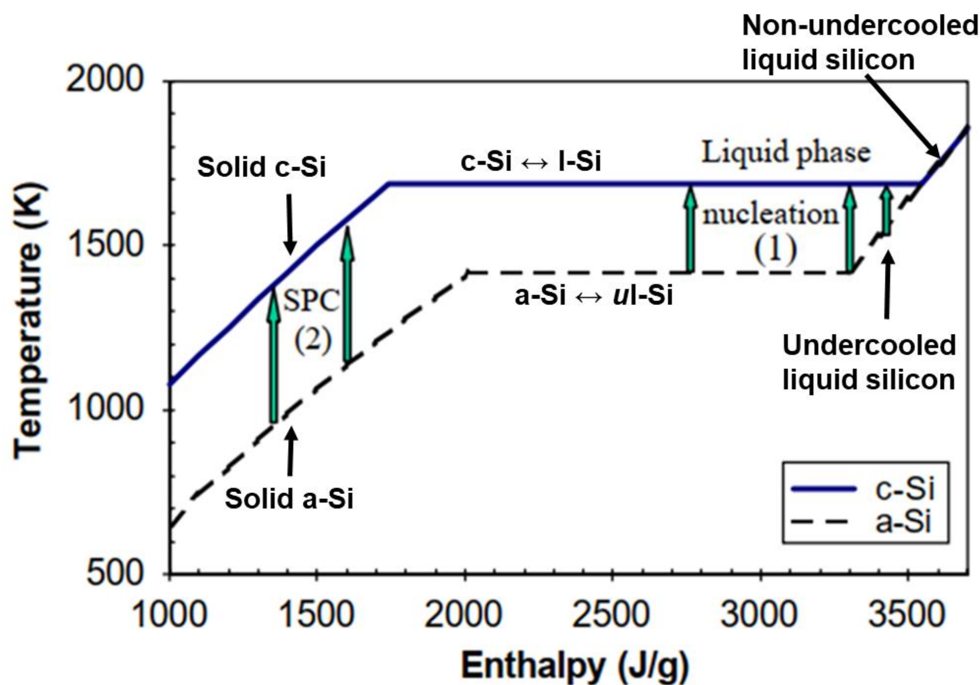

Figure 2.5: Energetic states of the Smith 1D model of FLA crystallization. Adapted from [72]

The undercooling of a liquid phase, or the amount of temperature that a liquid phase is below its crystalline melting temperature, is the chief factor in determining both the nucleation rate of a c-Si phase and the rate at which that crystalline phase grows. In this model, the lower bound of the temperature of the undercooled liquid silicon was strictly limited to the melting temperature of the amorphous silicon phase, thus the maximum degree of undercooling was set by operational parameters at 269 K. It was found, as shown in Figure 2.6, that the rate of homogeneous nucleation in liquid silicon bulk was fully negligible at this level of undercooling, while heterogeneous nucleation at the SiO_2 interfaces was much higher but still uncommon. Instead, small crystalline phases were assumed to be plentiful throughout the silicon, allowing the undercooled liquid phase to solidify at the interface of these surviving seeds. At this undercooling level, a c-Si phase growth velocity of 16 m/s was calculated.

The assumption of numerous crystalline phases present in the undercooled liquid silicon melt is likely to be correct for silicon deposited at 600 °C by LPCVD. However, it may not hold true for an a-Si layer deposited via low-energy PECVD with a higher initial amorphous fraction. As the concentration of initial crystalline seeds decreases in a FLA system, the relevance of heterogeneous nucleation increases. Additionally, two-dimensional effects of crystallization are not considered here. The work of Smith *et al.*, though important and comprehensive, leaves many questions yet to be answered.

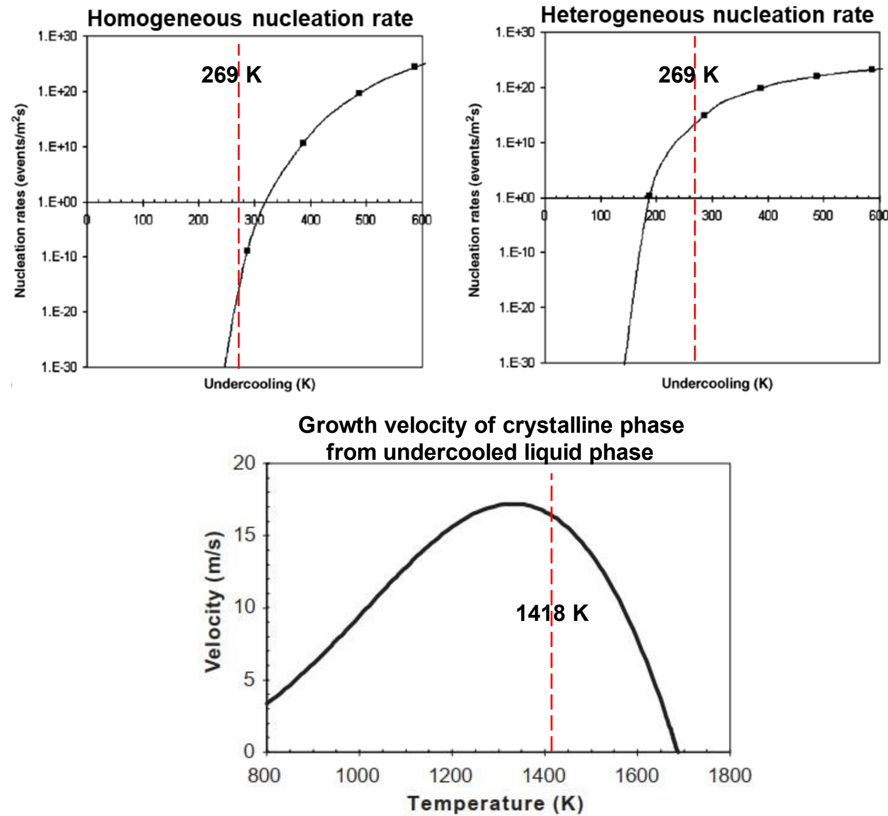

Figure 2.6: Top: Homogeneous and heterogeneous nucleation rates of liquid silicon in the Smith model, assumed to be negligible at an undercooling level of 269 K. Bottom: calculated growth velocity of existing crystalline phases in undercooled liquid silicon. Adapted from [72]

In an isothermal process, melting amorphous silicon on a glass substrate would not be possible. FLA and ELA are nonequilibrium heating methods in which these temperatures are only locally reached and the backside temperature of the substrate remains unchanged, reducing damage to fragile materials. However, a significant degree of heat may be transferred to the upper regions of a substrate during FLA depending on absorbance, relative thermal diffusion length, and duration of flash pulse.

When areas of liquid silicon solidify into c-Si, they release their excess free energy in the form of latent heat of fusion, which can result in excess heat propagating to the surrounding material.

This permits a solidification behavior called explosive crystallization, an auto-catalytic and self-propagating process in which a crystallization wave travels laterally across a metastable phase during heating. If a small region of silicon melts and recrystallizes to a solid phase with a lower free energy, the latent heat of fusion released can be sufficient to melt an adjacent region. That region then also transitions from liquid to more stable solid, releasing more heat and propagating the behavior across a medium.

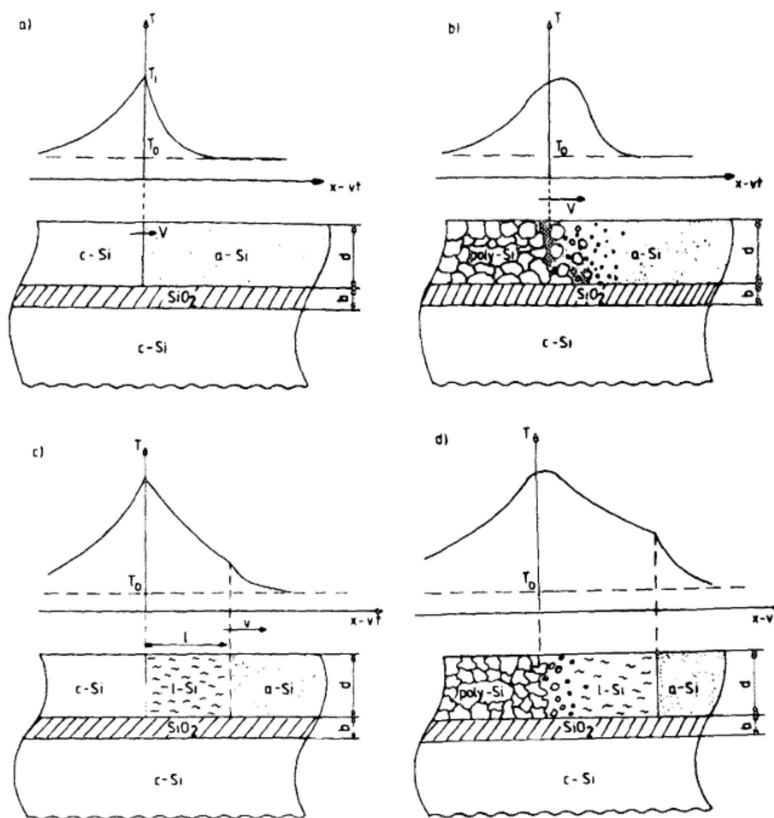

Figure 2.7: Depiction of four thermodynamic pathways that result in explosive crystallization in amorphous silicon. From [73]

Figure 2.7 demonstrates four possible thermodynamic pathways that can lead to explosive crystallization in an amorphous silicon thin film. As a-Si absorbs energy, it can transition directly to a crystalline or polycrystalline phase, or it can melt into liquid silicon and resolidify as c- or p-Si [73]. The pathway taken depends on whether nucleation or epitaxy dominates, which is itself dependent on the amount of energy absorbed, how quickly it is delivered, and how quickly that energy can be released. Thus, explosive crystallization can produce a variety of different morphologies. This process is now well established both in theory and practice in excimer laser annealing [74]–[76]. A similar mechanism is possible in FLA as long as pulse intensity is sufficient to melt the very weakest and least stable regions of a-Si, such as those at a boundary edge or near a random imperfection in the film stack.

2.3 Summary of Physical Systems

An awareness of the optical, thermal, and enthalpic factors involved in FLA amorphous silicon crystallization is necessary to predict and understand the results of an anneal. As a thermal non-equilibrium process, FLA produces phase changes with complicated kinetic relationships to temperature, time, and undercooling rate, which are also dependent on the dimensions of the film stack and the quality of the a-Si being used. Merely depositing silicon at a higher temperature can result in a vastly different crystallization product. Excellent work has already been done on analyzing this system in a one-dimensional model, with results that are physically replicable. Further work on modeling laser annealing systems can be adapted to this crystallization system. However, several two-dimensional factors such as explosive crystallization and optical lensing reveal that a full model of the FLA process is highly complicated and challenging. Understanding of the relevant factors is a good first step from which further experimentation can proceed.

Chapter 3. FLA Material and Process Parameters

The crystallization of amorphous silicon by flash lamp annealing is a complex process that incorporates many realms of physics which other annealing methods can safely ignore. However, the actual procedure by which this crystallization is carried out is relatively simple. The effect of FLA on a sample can be modified into a variety of different morphologies by adjusting either the structure of the initial film stack or the simple parameters by which a flash pulse is emitted.

3.1 FLA LTPS Crystallization

When considering the crystallization of amorphous silicon by flash lamp annealing, the structure of the initial material is the most important element. Generally, the structure of a sample to be in-situ crystallized into LTPS can be broken down into a substrate, an optional barrier layer, a layer of amorphous silicon, and an optional capping layer. Figure 3.1 shows a schematic breakdown of the various strata of these divisions.

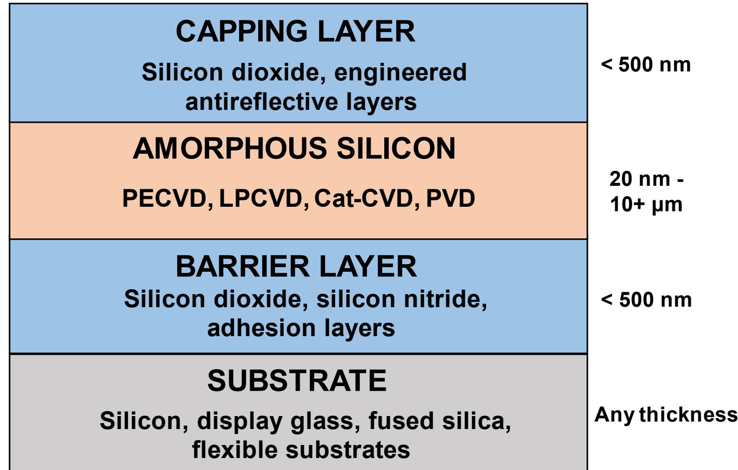

Figure 3.1: Schematic of the relevant layers in a film stack prior to crystallization via FLA

Amorphous silicon is generally deposited via chemical vapor deposition (CVD), usually as plasma-enhanced CVD (PECVD) but sometimes as low-pressure CVD (LPCVD). These reactions almost exclusively use silane (SiH_4) as a precursor gas, which must be cracked with an energy source to release free silicon atoms [77]. Conditions favoring the maximum percentage of amorphous content require low free energy at the depositing surface to ensure a rapid adhesion of silicon to the surface without formation of nanocrystalline regimes; these may be desirable in a-Si:H electronics, but they impede crystallization at low temperatures.

Because of the high hydrogen content of the precursor material, PECVD a-Si is a self-passivating deposition. Any dangling bonds that are not filled by silicon are likely to be saturated by hydrogen, preventing electron traps if used as a semiconductor [78]. However, a large hydrogen content has been reported to interfere with post-deposition crystallization by bubbling violently out of the silicon [79], [80], so FLA crystallization encourages a dehydrogenation anneal of 400-450 °C after deposition. Other methods of silicon deposition with low inherent hydrogen content

are possible: catalytic CVD has shown some promise in depositing a-Si on temperature-sensitive substrates by using a distant heat source, though thickness uniformity remains a challenge [81].

LTPS is generally used with substrates that have a lower thermal limit than traditional very/ultra large-scale integrated circuit (VLSIC/ULSIC) processing, as a substrate able to withstand the temperatures needed to melt and recrystallize silicon in bulk would have no need of the specialized low-temperature considerations. In flat panel display applications, specially formulated silica glasses such as Corning Eagle XG or AGC AN100 are most frequently used. These materials are designed to be thermally stable at moderate temperatures (> 450 °C) with minimal warping or contracting [82]. FLA LTPS can also be produced on silicon substrates, though the value of doing so is questionable and the high absorption and thermal ballast of silicon can be a significant obstacle.

Barrier layers between the a-Si and substrate can serve a variety of purposes. Many formulations of display glass contain high concentrations of aluminum, boron, and phosphorus, as well as numerous other ion contaminants, which are all elements that can activate in silicon as dopants. These elements may diffuse into silicon during crystallization and act as sources of charge in unplanned regions, causing devices to fail or behave sub optimally. By coating the substrate with a thin impermeable layer of silicon dioxide, dopant uptake is prevented without substantially changing the thermal or optical properties of the film stack. Barrier layers can also be engineered to improve uniform silicon deposition, adhesion, or stress mitigation. However, the design of materials for a barrier layer or underlayer must consider how that intervening layer will interact with the crystallizing pulse of light. In FLA, emitted energy is broad-spectrum and cannot be tailored so as to be fully absorbed by the amorphous silicon layer; some or even most of the energy will transmit through the silicon and reach the layers below. Therefore, thick films of optically or

thermally absorbent material are likely to have a significant impact on the LTPS crystallization beyond their intended effects.

A capping layer is often deposited on top of the amorphous silicon to reduce reflectance losses. As detailed in Section 2.2.1, the percentage of incoming light that is reflected off the sample can be significant, resulting in wasted power and unnecessary strain on flash lamps. Internal reflectance is a much more complicated factor which may either increase the effective light path length through the a-Si layer or prevent light from reaching it altogether. Capping layers may also be used to reduce ablation or outgassing of materials during FLA and prevent interaction of a non-controlled ambient with the a-Si layer [18], [83]. These layers are often sacrificial and removed after crystallization. SiO_2 is thus an effective capping layer due to its well-established compatibility and etch selectivity with silicon.

The experiments presented in this document use differing starting film stacks, which will be discussed in terms of variations on a “standard” sample. This standard uses a substrate of 150 mm-diameter, 500 µm-thick wafers of Corning Lotus NXT display glass, a formulation of glass substrate designed to be thermally stable at high temperatures, [84]. Onto this substrate is deposited a barrier layer of 200 nm PECVD SiO_2 from a silane precursor, 60 nm of PECVD a-Si from a silane precursor, and a capping layer of 100 nm PECVD SiO_2 from a tetraethyl orthosilicate (TEOS) precursor. The barrier and a-Si layers are deposited sequentially in the same chamber without a break in vacuum. After deposition, samples are furnace annealed in nitrogen at 400 °C for thirty minutes to dehydrogenate the amorphous silicon layer. For improved crystallization response, the amorphous silicon is then patterned into isolated mesas with an SF_6 reactive ion etch (RIE) step, rather than being crystallized as a uniform film; this will be discussed further in Section 3.2.

Similarly, a standardized set of annealing parameters is used when FLA crystallizing this standard sample. Unless otherwise noted, crystallization takes place with substrates heated to 400-500 °C through a conduction hotplate with an intermediary silicon wafer acting as a carrier to limit thermal strain during transfer. A single flash pulse is used with a targeted pulse width of 250 μs. The total energy output during this pulse is determined prior to crystallization by adjusting the voltage stored in the lamp capacitor banks until a targeted energy density is recorded by a blackbody absorbing bolometer. The true energy absorbed by a thin amorphous silicon layer is complicated to measure (as discussed in Section 2.2.3) but will be significantly lower than the stated energy density based on the limited absorbance of a-Si and the thin absorbing body.

The tool utilized in this method and elsewhere in this document was a NovaCentrix PulseForge 3300 photonic curing oven. This tool was designed for the purpose of sintering conductive inks and curing thin surface coatings in an industrial setting [67]. Two flash lamp sources, each powered by five capacitor bank drives, uniformly illuminate an exposure area of 7.5 cm by 15 cm. The bulbs are protected by a quartz window to prevent damage by outgassing or material backsplash. Substrate heating is performed by means of an external hotplate.

Numerous flash lamp annealing and curing systems exist that are more specialized towards the needs of semiconductor crystallization and processing. Several improvements can and have been made with these systems, including an integrated substrate heating source with vacuum-enhanced conduction or backside halogen lamps, an automated intensity monitoring system, isolated and controlled ambient environment for crystallization in vacuum or inert gas, automated handling and loading, and wider areas of uniform exposure through larger arrays of bulbs. The experiments demonstrated here can be considered a “base case” of what is possible: any dedicated

microfabrication FLA system with sufficient power should be able to obtain similar or better results.

3.2 Challenges towards FLA LTPS Crystallization

The unique benefits of FLA over other LTPS annealing methods are its sub-millisecond crystallization of large areas simultaneously in a thermal nonequilibrium process. This allows the use of substrates with a lower thermal limit than those used in high-temperature furnace or rapid thermal annealing while also maintaining large substrate scalability and a much faster throughput than laser-based annealing, with its spot size on the order of millimeters. However, these two concepts necessarily mean that an FLA anneal tailored to melt amorphous silicon will cause very large areas of silicon to melt simultaneously. Though the whole process of irradiance, melting, and cooling takes place in under a millisecond, the wide area of incidence can result in loss of adhesion between liquid silicon and an underlying oxide. Dewetting is thus a significant problem facing FLA LTPS procedures.

FLA is more effective at crystallizing thin a-Si if it has been previously reduced from an unbroken “blanket” film down to isolated mesas through lithographic patterning and etching. The isolated silicon regions have a reduced thermal mass and additional pathways for rapid cooling, allowing a lower flashbulb energy to melt and recrystallize. Without pre-patterning, FLA LTPS is difficult to distinguish from low-temperature solid-phase crystallized (SPC) LTPS, at least within the range of energy densities attainable by the tool used in this research. SPC, as an LTPS morphology for display applications, displays some benefits over amorphous hydrogenated silicon, but is still orders of magnitude below laser annealed LTPS [85]. These “initial

crystallization mesas" can have dimensions on the order of hundreds of micrometers and are produced with lithographic patterning and a SF_6 reactive ion etch after a-Si deposition.

Figure 3.2 demonstrates the issue of dewetting on the standard FLA film stack when crystallized with a pulse of 5.2 J/cm^2. The mesa, an alignment feature for lithography, appears as a uniform square with notched sides and a small cross in the center on the lithography mask, which is faithfully recreated after lithography and etching into an amorphous silicon layer. After FLA crystallization, however, the texture and morphology of the mesa is altered. Numerous voids with diameters of 1–5 μm populate the majority of the area, connected by narrow bridges of remaining silicon. Nomarski imaging confirms that these voids represent areas where silicon has fully pulled away from the underlying SiO_2, rather than a simple change in surface texture.

Interspersed with the voids in this material are areas of silvery, "bubble-like" appearance. This pattern is caused by optical refraction through a film of varying thickness, suggesting that silicon has transferred here from the dewetted areas to form small hillocks. The presence of localized voids therefore does not mean that the mesas experience a net loss of silicon mass; it is simply redistributed in liquid phase.

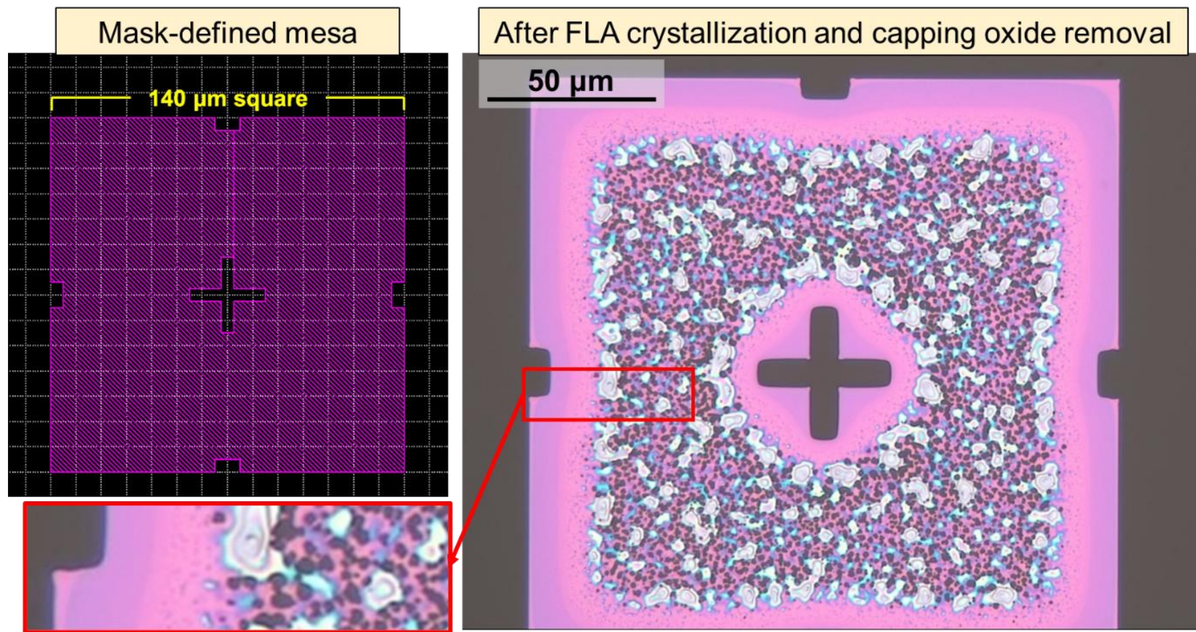

Figure 3.2: Upper left: Layout diagram of a particular initial crystallization mesa that acts as an alignment mark. Right: Micrograph of this 60 nm Si mesa after a FLA crystallization pulse at 5.0 J/cm^2 and capping oxide removal. Lower Left: higher magnification highlighting the presence of numerous few-micron voids.

Along the edges of this alignment mesa, two bands of a visibly different morphology are present within the silicon. The outermost eight micrometers are a uniform and unbroken texture of a darker magenta color than the remaining silicon in the center. Further inward is a band of lighter pink which matches the silicon in the center, but with very little texture and no large voids or puddles. Both of these bands surround interior as well as exterior edges, demonstrated clearly by the cross-shaped alignment features in the center of this mesa. The precrystallization patterning of the amorphous silicon mesa is thus necessary for limiting nonuniformities associated with multi-phase LTPS within a single device mesa. Though the lighter of these two border regions is more consistent than the central material while still being visibly impacted by the anneal, extending this material over a large enough area to reliably build a set of device channels would be a challenging feat of geometry and design.

These visible patterns of crystallization are impacted not just by the shape of the precrystallization mesas, but also by their size and proximity to other large mesa bodies. Figure 3.3 shows a wider-area micrograph of a sample crystallized by FLA to demonstrate this proximity effect. To the left of this image, mesas are small and relatively isolated, demonstrating a uniform degree of crystallization similar to that of Figure 3.2 above. The rightmost section of this array contains much larger mesas (used for measuring alignment in this experimental design) with a gradient of crystallization that spreads outward from an apparent center. This effect means that FLA crystallization is inherently a two-dimensional process, rather than simply based on 1-D depth

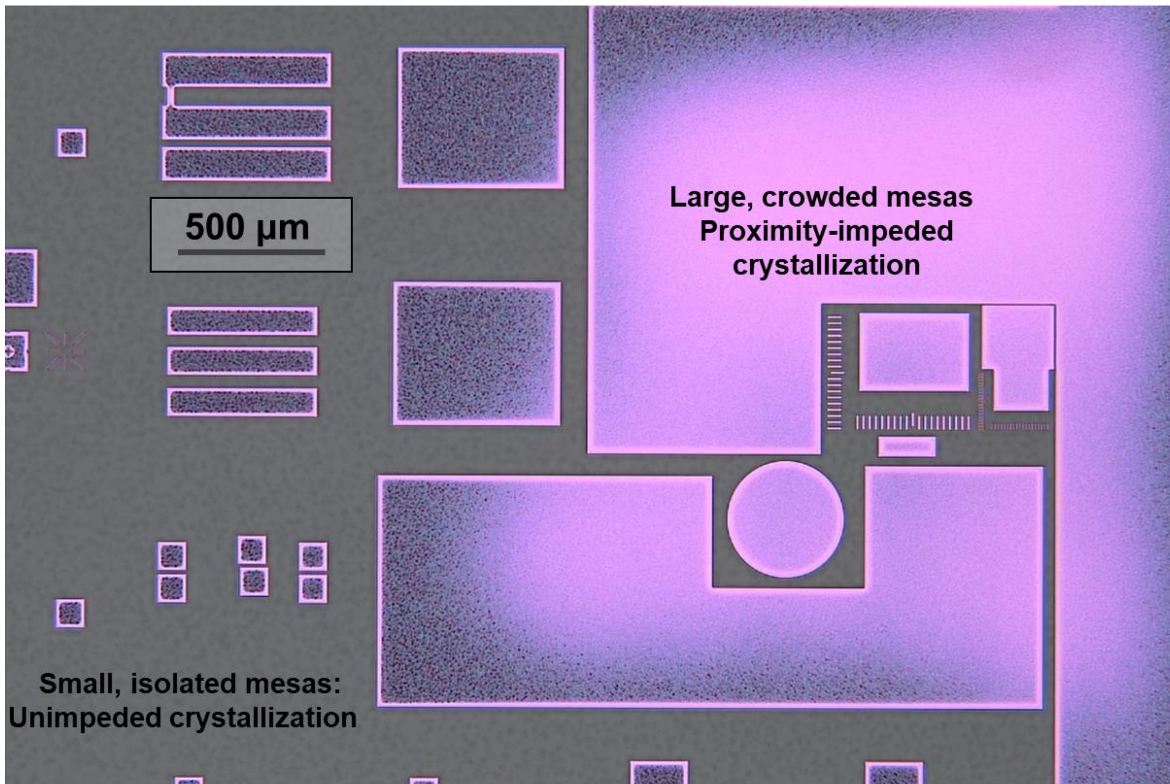

Figure 3.3: Micrograph of an array of varyingly sized initial mesas of 60 nm a-Si after FLA crystallization at 5.0 J/cm^2 demonstrating the proximity impedance effect.

The two-dimensional proximity effect, fully not considered in one-dimensional models by Smith *et al.* and elsewhere, is a complex issue that limits the density of consistent and usable LTPS in a lithographic die. It is clear that small mesas bunched closely together show a similar behavior to that of a single large mesa of a comparable size, transferring energy to surrounding bodies. This effect may be thermodynamic: as a mesa region is surrounded by more areas of unbroken silicon, its crystallization is more heavily impeded by their thermal mass and offers numerous added pathways by which heat can be dissipated. It may also be due to a more complicated optical property by allowing light to bleed off to nearby areas and lens away from the silicon body in a waveguide-like mechanism. Either way, there is a deleterious and FLA intensity-dependent limitation on the close-packing of amorphous silicon mesas during FLA crystallization in this research.

Figure 3.4 demonstrates the difficulties that can arise when a material with a randomized texture is used to produce dimensionally-scaled devices such as TFTs. Available electric current is a mass property that varies depending on the distance traveled and the cross-sectional area of the conduction path. When two transistor channels, identical in mask-defined dimensions, have differing areas of charge transport, they will act as different effective channel dimensions and produce different current output at the same voltage. As mask-defined dimensions are reduced, the variance of void fraction between devices increases. In cases of extreme scaling on a material with large voids, the difference in operation will extend to outright device failure as no intact conductive pathways remain in the silicon.

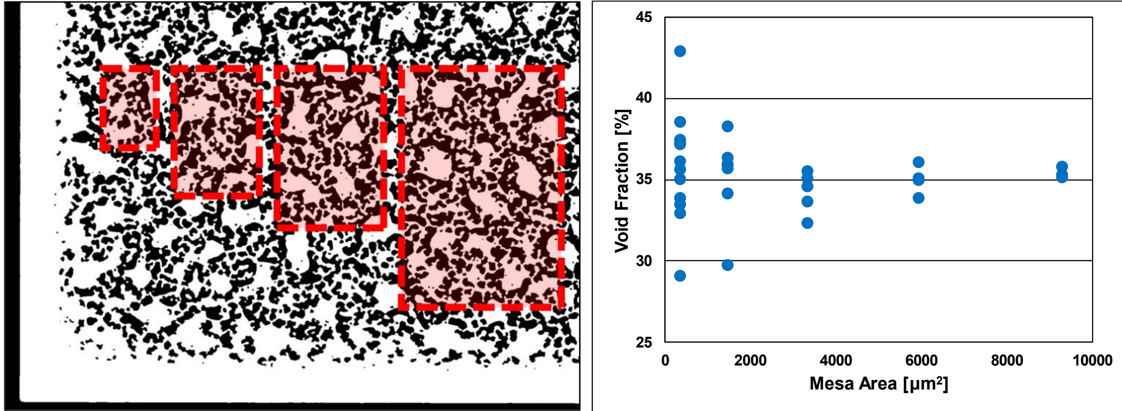

Figure 3.4: Left: a maximized contrast image of a silicon mesa after FLA crystallization in which voids are keyed to black and all other material is white with several sample mesa areas as overlay. Right: Histogram of the void fraction of several mesa areas drawn on this mesa. As area is reduced, the variance in void fraction increases.

3.3 FACTORS INFLUENCING FLA CRYSTALLIZATION STRUCTURE

Void-associated morphology has a significant impact on uniformity of device operation, while border exclusion and proximity-impeded crystallization affect the usable area of FLA-crystallized LTPS. As such, these three effects must be understood and controlled from a device layout and circuit design perspective if FLA LTPS is to be successfully implemented in any real-world application. Several adjustments can be made to the initial a-Si sample or to the FLA process to obtain a desired morphology.

Each of these three effects—randomized central voids, border exclusion, and proximity-limited crystallization—are themselves impacted by the energy density output of the flash bulbs during annealing; the "intensity" of FLA crystallization. Figure 3.5 demonstrates these relations with a set of standard FLA crystallized samples exposed to increasing flash lamp intensities. The upper three images show a tight array of 200 × 100 μm rectangular mesas with 10 μm gaps. As FLA intensity increases from 4.6 to 5.0 J/cm^2, the visible proliferation of voids extends further

into the mesa grid, stopping first at the 3-2 position, then 4-3, then 5-4/5-5. The proximity-effect impedance of crystallization is gradually overwhelmed by an increase in available energy.

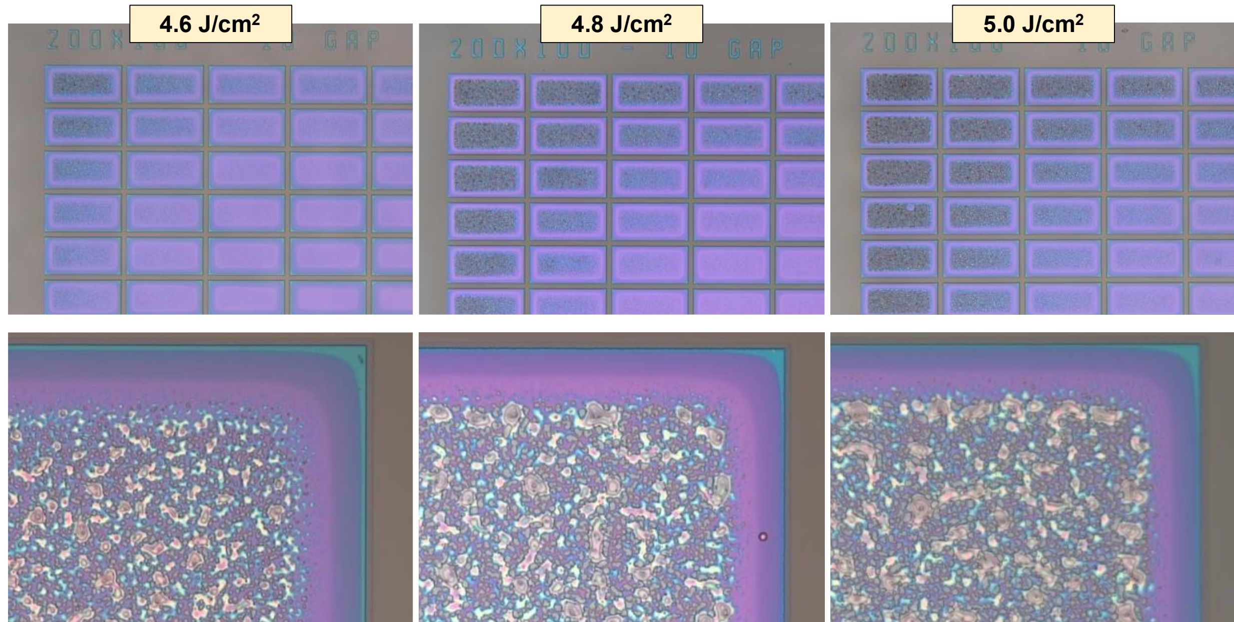

Figure 3.5: FLA-crystallized 60 nm silicon mesa grids (upper, all)) and high-magnification isolated mesas (lower, all) with an FLA intensity of 4.6 (left), 4.8 (center), and 5.0 J/cm^2 (right).

The lower row of images in Figure 3.5 shows a higher magnification of isolated mesas exposed to the same FLA pulses as the images immediately above each one. The textures appear visibly different from Figure 3.2 because the capping oxide has not been removed for these micrographs. By measuring the corner of each mesa to the beginning of the lighter-pink band of silicon, a radial reduction of 10% from 4.6 to 4.8 J/cm^2 and a further 6% from 4.8 to 5.0 J/cm^2 can be determined, indicating that the width this border exclusion region is a function of lamp intensity.

The impact of increased flash lamp intensity is more drastically seen in Figure 3.6, in which a wider spread of intensities is used to crystallize a series of samples with 100 nm-thick a-Si layers. Here, the significance of absorption as a function of sample thickness is displayed. When

compared with Figure 3.5 above, the mesa grids crystallized at 5.0 J/cm^2 and above are heavily overexposed to the point where even their sharp corners have been eroded. The relation of FLA intensity to silicon crystallization response is heavily dependent on the structure of the sample to be crystallized

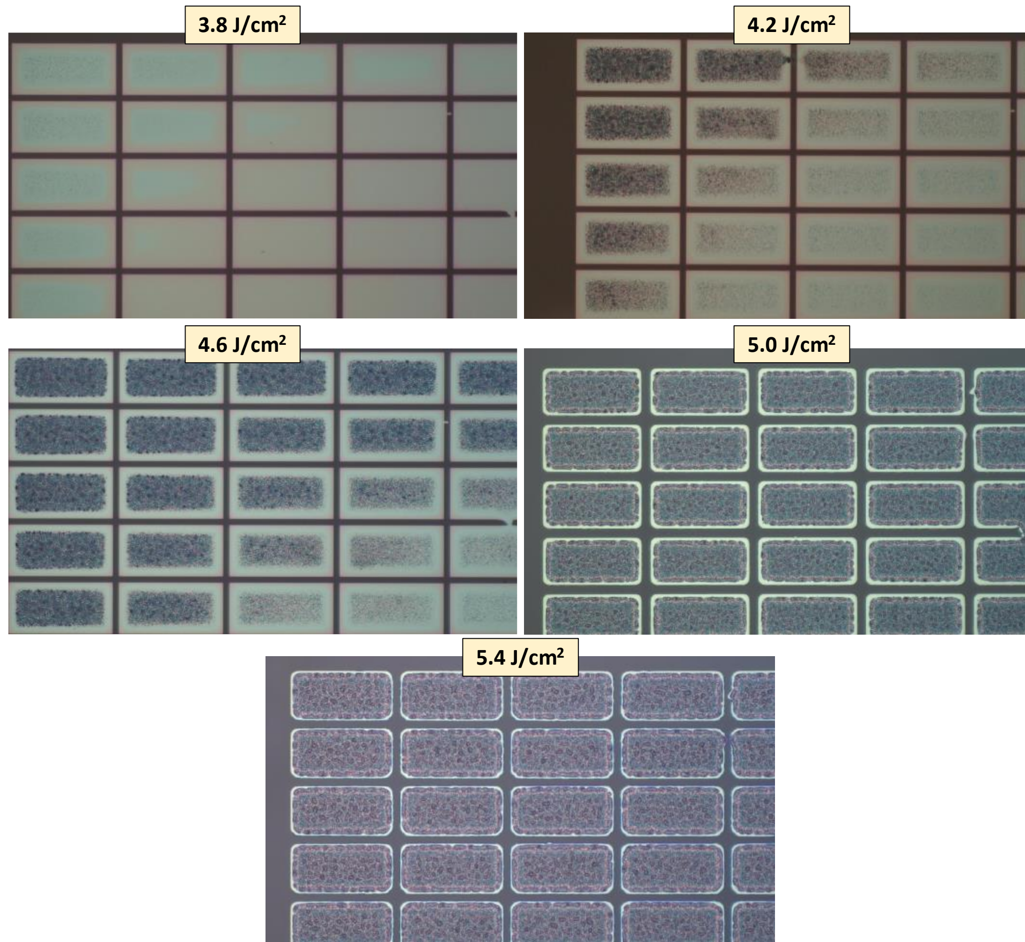

Figure 3.6: : 100 nm silicon mesa grids crystallized at FLA intensities between 3.8 and 5.4 J/cm^2. Each mesa is 100 μm × 200 μm with a 10 μm gap.

3.3.1 Nitride Barrier FLA LTPS

The previous examples have all incorporated a PECVD SiO_2 barrier layer. This material has numerous advantages: it has a similar composition to display glass for the purposes of strain balancing and thermal expansion, it has a high etch selectivity with respect to silicon, and it can

be deposited in the same PECVD tool as is used to deposit a-Si without breaking vacuum. However, interfacial energy between silicon and SiO_2, especially liquid-phase silicon, is estimated to be particularly high [86]. This may contribute to the pattern of randomized, high density void formation as liquid silicon is inclined to dewet at the barrier oxide interface.

Silicon nitride is a common interstitial or substitution material for applications requiring uniform silicon deposition in challenging situations [87], as well as being a common PECVD material for silicon PV passivation [88], [89]. It has a closer coefficient of thermal expansion to silicon than does SiO_2, making it a better match for applications involving rapid heating, while retaining ease of processing.

Unfortunately, these improvements appear to not translate into reduced void formation during FLA crystallization. Samples fabricated using a PECVD SiN_X barrier layer instead of SiO_2 showed a less-than-uniform texture even prior to crystallization, a texture that became much more apparent after FLA. Figure 3.7 shows microscope images of nitride-barrier samples crystallized at different FLA intensities. A new feature is apparent, manifesting as tiny dots extending throughout the entirety of silicon mesas. These imperfections are equally present in the center of crystallized mesas and within the border exclusion region where voids are not expected to form.

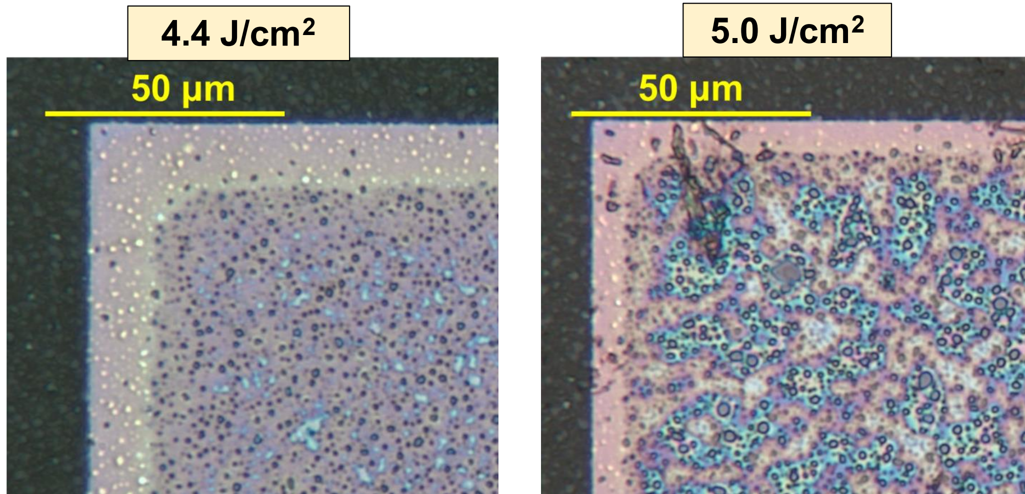

Figure 3.7: Optical micrographs of 60 nm a-Si on a silicon nitride barrier, crystallized with FLA at 4.4 (left) and 5.0 (right) J/cm^2. Pinprick voids are visible throughout the samples, with a similar texture noticeable in areas with no silicon.

The source of these new pinprick voids may be the more complicated procedure of successive plasma-enhanced chemical vapor depositions. While the SiO_2 and a-Si films used in this work both utilized a silane precursor, SiN_X used dichlorosilane, thus necessitating a different tool chamber. The time between barrier and silicon depositions and the resulting break in vacuum may have degraded the interface to the point where uniform nucleation was compromised. It is also possible that they are related to hydrogen bubbling, though these samples underwent the same dehydrogenation procedures as other experiments. Regardless of the mechanism of pinprick formation, the usual void-associated morphology is not significantly impacted by a silicon nitride barrier layer.

3.3.2 Metal/Ceramic Underlayer FLA

Metals and metal compounds are also commonly used as intermediary layers in film stacks to improve adhesion of subsequent films. However, the opaque nature of these materials interacts

poorly with the broad-spectrum emission and incomplete silicon absorbance of FLA. This can result in localized heating within metal underlayers, damaging the film integrity at FLA intensities that would otherwise not be sufficient to crystallize amorphous silicon. As thermally conductive material, metal can also act as a heat sink and reservoir, extending the duration in which thermal energy is retained in the system.

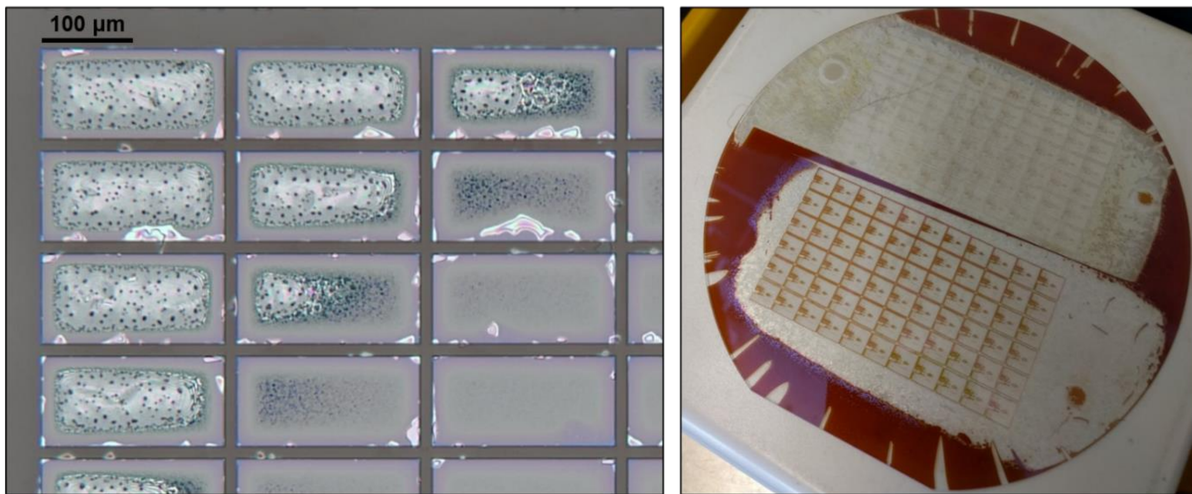

Figure 3.8: Left: Optical micrograph of FLA-crystallized silicon on a molybdenum underlayer with a pulse of 4.5 J/cm^2, demonstrating damage to the metal underlayer in the form of buckling around mesa edges. Right: Image of a 150 mm diameter glass wafer with silicon on ALD alumina underlayer after FLA crystallization with pulse intensities of 4.5 and 5.0 J/cm^2, demonstrating obvious wide-area loss of silicon.

Figure 3.8 demonstrates some unsuccessful attempts to use various metals as an adhesion-promoting underlayer. The image on the left is an optical micrograph of FLA crystallization of 60 nm a-Si on a 6 nm layer of DC sputtered molybdenum, chosen for its demonstrated compatibility with FLA in self-aligned devices (discussed in Chapter 4). Molybdenum readily forms silicon-compatible oxides and other compounds with an established Schottky barrier [90], [91], making it potentially valuable as an FLA stack inclusion for TFTs.

However, the extreme opacity of molybdenum, possibly coupled with its high reflectivity, resulted in a failure to effectively crystallize overlying a-Si. Significant damage was visible to the Mo underlayer even with a much lower FLA intensity than in other crystallization experiments, noticeable as sporadic buckling around mesa edges. This damage began at pulse energies lower than that needed to visibly crystallize the overlying silicon. In this process, the molybdenum acted as an absorbance center and thermal sink, resulting in a much higher energy absorbance that was not localized within the active layer.

To the right of Figure 3.8 is a photograph of a full 150 mm glass wafer originally formed with 60 nm a-Si on a 10 nm layer of atomic layer deposited alumina, chosen for its established properties as an adhesion promoter and apparent transparency. However, the absorbance spectrum of alumina is very heavily weighted towards the near-UV, similar to that of a-Si. This experiment resulted in an obvious large-area “explosion” of silicon, much of which did not remain on the sample after exposure to a moderate FLA intensity.

3.4 Summary of FLA Process Parameters

The structure and proportions of an a-Si film stack are the most important factors influencing its crystallization via FLA. Careful selection of AR capping layer thickness, silicon thickness and deposition parameters, and barrier layer material can significantly alter the produced LTPS. Some such combinations, however, can produce undesired results, especially if optical transparency is not sufficiently considered.

FLA LTPS has been shown in literature to demonstrate numerous morphologies, many of which are difficult to replicate due to a lack of complete information about the process used. The morphology shown here is very obviously altered by FLA pulse in the form of numerous dewetted

regions forming in the final LTPS. These randomized voids, though small, are present throughout each silicon mesa exposed to a high enough energy density, and their unpredictable structure can lead to problems with consistency in device operation when used to make TFT bodies scaled to smaller dimensions. In addition, the two-dimensional proximity impedance effect sharply curtails the usable area of FLA LTPS, though this issue may be mitigated with clever layout design.

The density of voids and degree of excluded border in an FLA LTPS mesa is most heavily impacted by the energy density delivered via FLA. Other notable parameters to consider are silicon thickness (which both increases absorption and requires more energy to fully melt), substrate heating (an effective linear offset to the temperature needed to melt a-Si at the cost of potential substrate damage), and duration of pulse delivery. Each FLA process must also be calibrated for the specific tool being used.

Chapter 4. ELECTRICAL DEVICE CONFIGURATIONS

The primary motivation for crystallization of thin amorphous silicon films via FLA is production of thin-film transistors as the logic plane for LTPS displays. In order for devices produced in this way to be considered complementary to extant display TFT semiconductors, they must be able to demonstrate a compelling combination of high carrier mobility, reliable operation and threshold voltage, and low off-state leakage, all without significant added process complexity. Research into FLA LTPS TFTs, having stagnated over the past few years, must begin from the ground up with an exploration of device structures and fabrication techniques for optimizing these metrics.

4.1 REQUIREMENTS FOR FLA LTPS TFTS

The value of FLA-crystallized LTPS is in its potential for electronic applications, such as TFT backplanes for flat panel displays. In order to prove the efficacy of this material in this field, numerous device benchmarks must be considered. Devices should demonstrate a high charge carrier mobility and thus a high current output at reasonable driving and gate voltages. They must also have low off-state leakage and uniform, predictable operation from one transistor to another. Given the demonstrated variability of this morphology of LTPS, other concerns regarding process compatibility are valid and must be dispelled.

Though it is unlikely that LTPS produced through FLA could reach the controllability and high performance of that of ELA, its advantages in industrial integration and throughput may help compensate for a moderate electrical showing. The exploration of these factors therefore

necessitates numerous experiments into strategies for thin film transistor fabrication on FLA LTPS.

4.2 CMOS FLA LTPS TFTs – Proof of Concept

With an untested and underutilized method of fabrication such as FLA LTPS, every experimental setup is likely to have minor differences and variations. These can be caused by incongruous or non-standardized tool sets, practices that are not carried out in identical ways, or even a failure to record certain basic assumptions. Therefore, the first step in continuing a global body of research should always be attempting to replicate existing work.

4.2.1 Methods

A general process flow was designed as a basis for all further experiments. Later experiments in this document will be explained mainly by how they deviate from this standard process, rather than exhaustively repeating every process.

Beginning with 150 mm-diameter wafers of Corning Lotus NXT display glass, 200 nm of SiO_2 was deposited by PECVD. This was followed by 60 nm of amorphous silicon, also using PECVD with a silane precursor and in the same chamber under vacuum. The a-Si layer was lithographically patterned into initial crystallization mesas with SF_6 reactive ion etch (RIE). A layer of 100 nm PECVD SiO_2 was deposited as a screen for upcoming ion implantation. Then, source and drain regions for PMOS devices were defined with a photoresist layer and the wafers were doped using ion implantation with 4×10^{15} ^{11}B ions/cm^2 at an acceleration voltage of 35 keV. Subsequently, separate source and drain regions for NMOS devices were similarly masked and doped with 4×10^{15} ^{31}P ions/cm^2 at an acceleration voltage of 70 keV. Implant parameters were selected based on tool

limitations with the intent of a peak concentration at the base of the silicon layer and verified with SRIM [92], as shown in Figure 4.1. SRIM simulations suggest that about 3/8 of the implanted dose remained in the 60 nm-thin semiconductor. Implant masks were then removed, and the wafers were crystallized with flash lamp annealing in a single-pulse regime of 5.0 J/cm^2 emitted over 250 µs (thus, 20 kW), with substrates first heated to 500 °C using a hotplate.

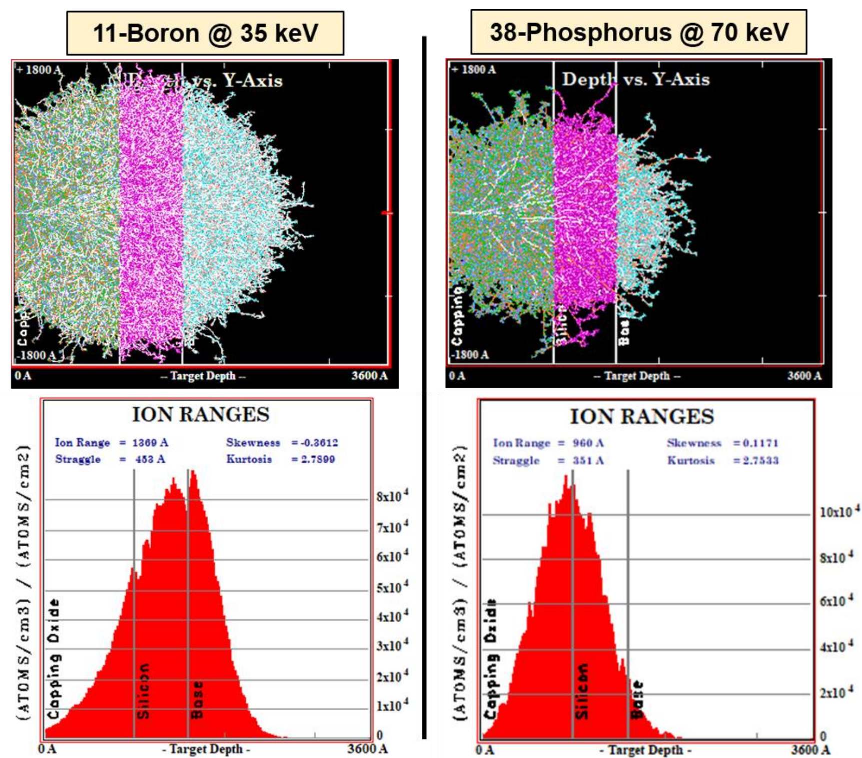

Figure 4.1: SRIM ion spread and ranges when implanted into a film stack of 100 nm SiO_2 on 60 nm Si on an oxide barrier. Left: 11-Boron implanted at 35 keV. Right, 38-Phosphorus implanted at 70 keV.

After FLA crystallization, the capping oxide layer was removed with buffered oxide etch (BOE) and the crystallization mesas were patterned and etched into smaller mesas that represented the final dimensions of the TFT devices. The silicon surface was cleaned with a modified RCA process of successive heated baths of sulfuric acid/hydrogen peroxide and hydrochloric

acid/hydrogen peroxide, with these modifications made to reduce the impact of the chemistry on the glass substrate. Then, a gate dielectric of 100 nm PECVD SiO_2 was deposited and densified with a 400 °C furnace anneal for 30 minutes. Contact cuts to the source and drain of each transistor mesa were lithographically defined and etched through the dielectric with BOE and the system was metallized with 0.75 µm DC sputtered aluminum patterned into gates and source/drain pads. Lastly, a sinter anneal was conducted in 5% H_2/N_2 ambient for 30 minutes at 450 °C to improve metal contact and help passivate dangling silicon bonds.

In total, both NMOS and PMOS TFTs were produced of varying mask-defined device dimensions between 96 µm and 2 µm in length. Devices were tested using HP 4145B and Keysight B1500A semiconductor parametric analyzers.

4.2.2 Results

Figure 4.2 demonstrates the crystallized morphology of LTPS produced in this manner, shown in a 400 µm by 400 µm square initial mesa still coated with capping oxide. A randomized texture of pockmarks and voids is clearly visible, with color differences indicating random variations in height as well. Chapter 3 describes this material in detail, including its physical characteristics and factors that influence its formation. When most of this mesa is etched away to reveal a final device mesa, the removed areas leave a texture on the underlying oxide layer due to uneven etching from the capping oxide removal, which propagates through the subsequent metal layers to produce a localized scratching effect.

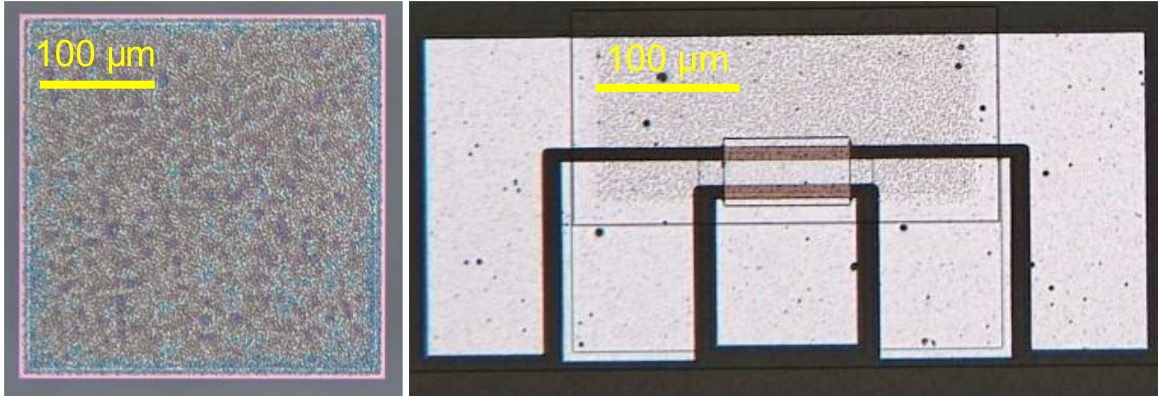

Figure 4.2: Microscope images of FLA LTPS material. Left – Directly after crystallization, taken with capping oxide. Note the randomized texture and coloration shifts indicative of a varying thickness. Right – A completed device with two linked gate contacts and two linked source contacts. Only the small center rectangle of silicon remains, the larger square is texture imbedded into the oxide underlayer.

Despite the randomized and void-laden morphology, this FLA LTPS material was used to produce thin film transistors that functioned similarly to those of more consistent structure. Both NMOS and PMOS TFTs were successfully demonstrated with encouraging electrical characteristics. Boron-doped p-type devices showed a threshold voltage of -2.82 V with a subthreshold slope of 140 mV/decade, while phosphorus-doped n-type devices showed a threshold voltage of 0.23 V and subthreshold slope of 118 mV/decade. Channel mobility for both charge carriers was extracted using the simple maximum-transconductance method. It is assumed that the low drain bias of ± 0.1 V causes devices to behave entirely in linear operation mode, following the relation:

$$I_{DS} = \frac{W}{L} C_{OX} \mu (V_G - V_T) V_D$$

(Eq. 7)

where I_{DS} is current from source to drain, W and L are the width and length of the channel, C_{OX} is the capacitance of the oxide dielectric, V_G and V_D are the voltages applied to the gate and drain,

and V_T is the threshold voltage at which current flow begins. Transconductance, g_m, or the rate at which a change in gate voltage changes the drain current, is obtained by differentiating the relation with respect to V_G. As V_T is independent of V_G, the relation simplifies to:

$$g_m = \frac{W}{L} C_{OX} \mu V_D$$

(Eq. 8)

Thus, a maximum channel mobility can be extracted as

$$\mu_{chan:max} = \frac{g_{m:max}}{\frac{L}{W} C_{OX} V_D}$$

(Eq. 9)

Using this extraction method, it was found that the maximum carrier channel mobility for these devices exceeded 140 cm^2/(Vs) for hole carriers and 380 cm^2/(Vs) for electrons.

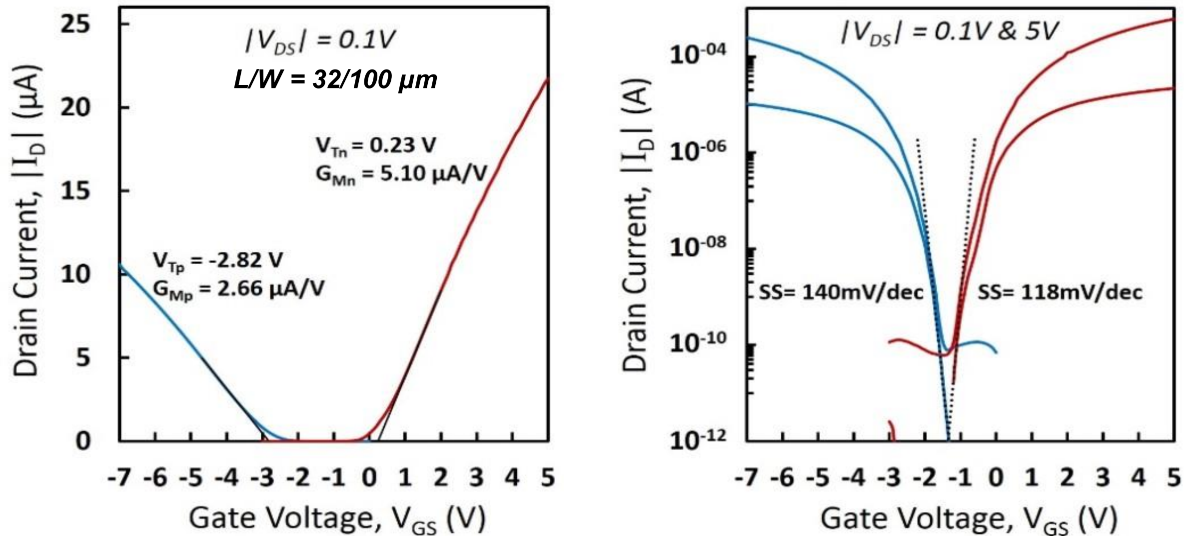

Figure 4.3: Left: Linear current-voltage transfer characteristics for a PMOS (blue) and NMOS (red) TFT of L/W = 12/24 µm , showing maximum transconductance and extrapolated threshold voltages. Right: Logarithmic current-voltage transfer characteristics of the same devices, highlighting reasonably steep subthreshold swing.

Though these devices show promising behavior and motivated much further study, several drawbacks must be noted. First, this method did not produce a reliable and repeatable process from sample to sample, or even from device to device on the same sample. The graphs shown in Figure 4.3 are an indication of best-case scenario behavior across numerous devices of similar dimensions. Given the variability of behavior, a measurement of yield is difficult to posit. The variation is likely a consequence of the inherent randomness of void density and size on the eventual channel area.

In addition, the fraction of failed devices increased as device dimensions were reduced until a point at which devices under a certain threshold uniformly behaved as resistors with no inducible gate modulation. A rough Terada-Muta analysis, with the output of multiple devices of varying lengths and constant widths compared around their respective threshold voltages, reveals this effect to be due to a drastic difference in mask-defined and metallurgical channel length. Assuming uniform behavior, the extracted reduction in channel length is greater than 6 μm for NMOS devices and greater than 13 μm for PMOS devices; all devices with a length smaller than these thresholds behaved as short circuits. This channel length reduction is dramatically larger than that of a typical thin-film or bulk silicon process, even considered as a proportion of channel length. It represents a critical flaw in this method of TFT fabrication.

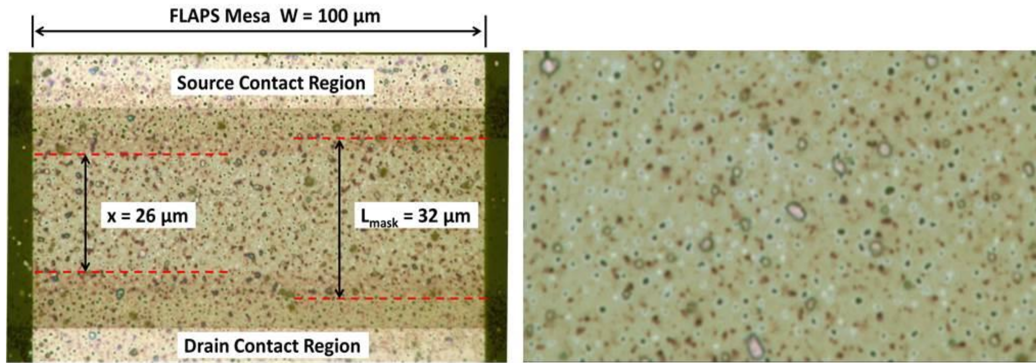

Figure 4.4: Left: demonstration of the reduction of channel length on a long NMOS device. Right: a close-up microscope image of a device channel with implanted junction barely visible.

4.3 SCALABLE FLA LTPS TFTS

The critical flaw underpinning the strategy detailed in Section 4.2 was a failure of scalability. TFT backplanes in modern displays, while nowhere near the extreme scaling of cutting-edge integrated circuitry, still require dimensional factors of < 4 micrometers for advanced pixel designs. The length reduction demonstrated renders this benchmark impossible.

This issue with poor device scaling in FLA crystallized LTPS is an unfortunate interaction that arises from two inherent factors of the technique. First, FLA is capable of bringing the full thickness of amorphous silicon films to a melt-phase transition without damaging or compromising glass substrates. Second, arbitrarily large areas of silicon are crystallized within a sub-millisecond time frame. These two aspects of FLA, though among the chief purported benefits of using this technique over other in-situ crystallization methods, result in a significant drawback to process integration: dopant migration is driven by liquid-state mass transport rather than diffusion. The brief hundreds of microseconds in which silicon remains in a liquid state is sufficient to allow any impurities or dopant molecules introduced prior to crystallization to travel throughout the liquid

medium by concentration gradient at rates that vastly outstrip those of conventional solid-phase diffusion at comparable temperatures and time scales.

The problem of liquid phase dopant transit is unique to FLA. Excimer laser annealing is an extreme surface-level technique that is unlikely to melt the full thickness of an a-Si film. Further, only very small areas of silicon are melted at once, limited by the laser spot size and pulse and scan rate. Continuous wave laser annealing and blue-light annealing are similarly restricted by area. On the other hand, bulk crystallization methods such as furnace annealing and metal-induced crystallization are constrained by the thermal stability of the substrate and therefore do not reach a melt-phase transition.

An obvious solution, truly more of a workaround, exists to this problem. If dopant migration during FLA is uncontrollable, simply introduce dopants into the silicon after crystallization. Since most or all channel length reduction is due to this single, brief liquid state transition, any doping into the post-FLA LTPS will have a negligible impact. This strategy, however, introduces a new complication as introduced dopants must be rendered electrically active by a secondary energetic step.

4.3.1 Methods

A modified experiment to verify this basic scalability strategy was designed using the experimental method in Section 4.2.1 as a starting point. In this variation, FLA crystallization was performed immediately after the formation of initial crystallization mesas and capping oxide deposition. After this, ion implantation was performed on the crystallized mesas through a 100 nm PECVD SiO_2 screen using the same dosage and energy parameters as previous. A significant degree of energetic damage to the polycrystalline lattice structure [93] is likely to result from

cascading kinetic transfer, which must then be healed with a subsequent thermal process to induce solid-phase epitaxial regrowth (SPER). In this experiment, activation and lattice regrowth were addressed with a furnace anneal at 630 °C in nitrogen ambient for 12 hours, the highest temperature able to be withstood by the glass substrates. After activation, devices were completed as in Section 4.2.1.

Figure 4.5 shows the final structure of typical devices prepared in this way, highlighting the impact of FLA intensity on apparent texture. The left image shows a device crystallized at 4.6 J/cm^2, showing slight color nonuniformities that could be the beginning of void formation during crystallization. This is an indication that the FLA intensity was insufficient to induce melting in the full thickness of the a-Si layer. The device on the right, however, was crystallized at 5.0 J/cm^2. Numerous irregular shapes are visible in the glass background surrounding this device, and a speckled texture is clearly visible on the overlaying aluminum gate and source. Both of these textures are confined to the area above the initial crystallization mesa, originally a 200 × 200 μm square. These patterns are a result of significant propagating roughness caused by etching into the SiO_2 underlayer due to voids forming in the silicon after melting and recrystallization; areas with voids allowed the buffered oxide etch intended to remove the capping SiO_2 to also etch down into the oxide below. Thus, roughness and imparted texture, an established source of gate leakage in LTPS TFTs [94] may be a significant factor hindering device integration.

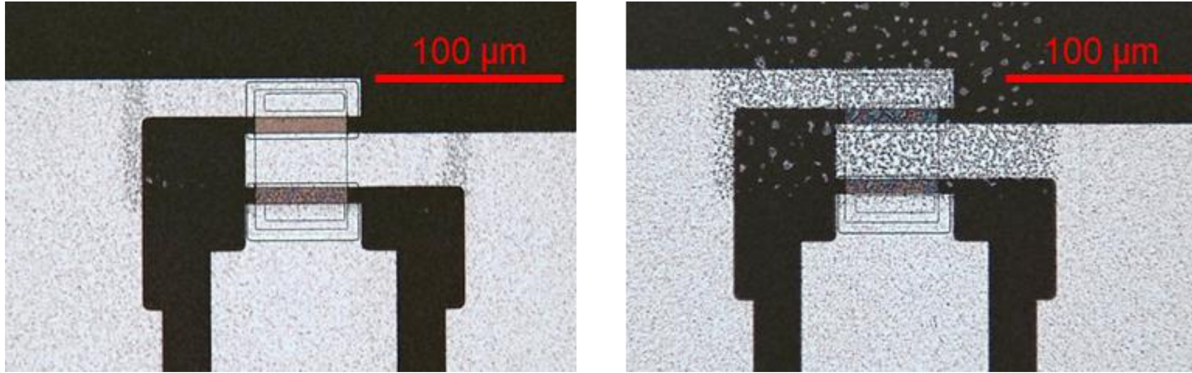

Figure 4.5: Micrograph images of completed 24/24 µm L/W TFTs using the scalable FLA LTPS method, crystallized with a single FLA pulse at 4.6 J/cm² (left) and 5.0 J/cm² (right). 5.0 J/cm² devices had far better electrical behavior.

4.3.2 Results

This process produced functional devices as shown in Figure 4.6, verifying the feasibility of dopant activation with a moderate-temperature furnace anneal rather than in-situ during crystallization. In this proof-of-concept method, phosphorus-doped n-type devices were constructed with an average threshold voltage of 4.55 V and a subthreshold slope of 2 V/decade, while boron-doped p-type devices had an average threshold voltage of -15.0 V and a subthreshold slope of 1.1 V/decade. Extracted maximum channel mobility was 12.3 $cm^2/(Vs)$ for electron-holes and roughly 33 $cm^2/(Vs)$ for electrons. Again, devices with smaller channel dimensions were less likely to be functional, but they varied in their dysfunctional behavior rather than consistently behaving as resistors.

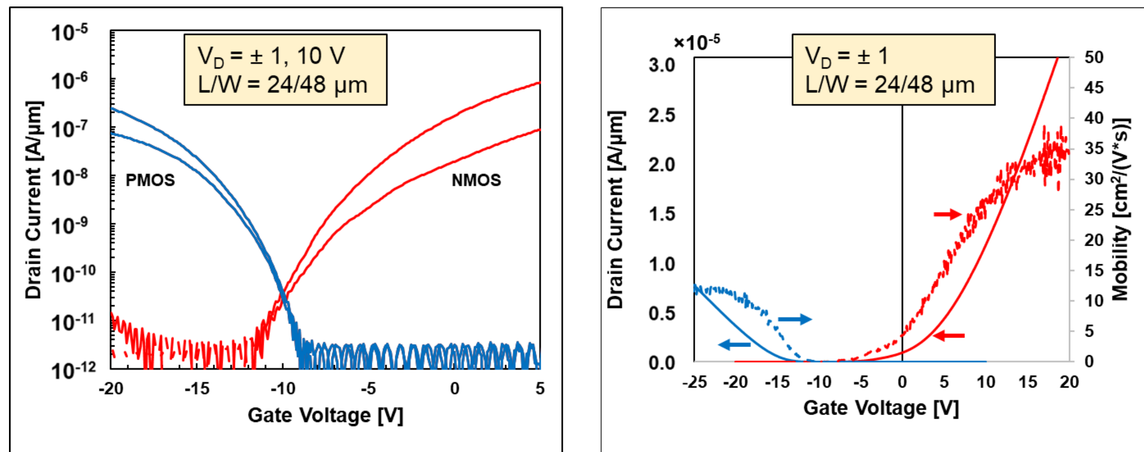

Figure 4.6: Left: Log-scale current-voltage transfer characteristics for PMOS (blue) and NMOS (red) FLA LTPS TFTs produced in the scalable alternative method. Devices had a length of 24 µm and a width of 48 µm. Note the significantly left-shifted and shallow switching characteristics, indicating a large amount of interface trap-states and possibly very resistive material. Right: linear-scale current-voltage transfer characteristics of the same devices. Maximum channel mobility for NMOS devices is an approximation to correct for roughness.

Terada-Muta analysis on the more consistently functional larger devices revealed an improvement in channel length reduction over the implant-first strategy. The difference in length between mask-defined and metallurgical channel was 3.6 µm for PMOS devices and 1.4 µm for NMOS devices.

This remaining channel length reduction is likely explained by inherent process bias and the capabilities of the lithography and etching processes utilized in this verification experiment; these issues can be easily solved with improved toolsets and more tightly-controlled fabrication methods. At the temperature used to activate these dopants, the diffusivities of boron and phosphorus in silicon is negligeable, even considering the extended duration of the anneal [95]. Any measurable presence of dopant in the mask-defined channel should be due entirely to the straggle of the implant volume and possibly segregation into the grain boundaries of the polycrystalline structure, especially in the case of phosphorus [96].

4.4 CO-IMPLANT AND SELF-AMORPHIZATION

The limited current of devices and high extracted sheet resistance demonstrated in the scalability-modified strategy of producing FLA TFTs suggests that this strategy of dopant activation is limited in effect. The main limiting factor in this study is the relatively low temperature of the furnace anneal used for activation. In bulk silicon IC applications, post-implant furnace treatments are undergone at temperatures ranging from 800 to 1200 °C in order to balance the efficacy of lattice regrowth and dopant activation with potentially unwanted dopant diffusion. Thin film devices, on the other hand, are thermally restricted by the material properties of the substrate, which is specific to individual applications.

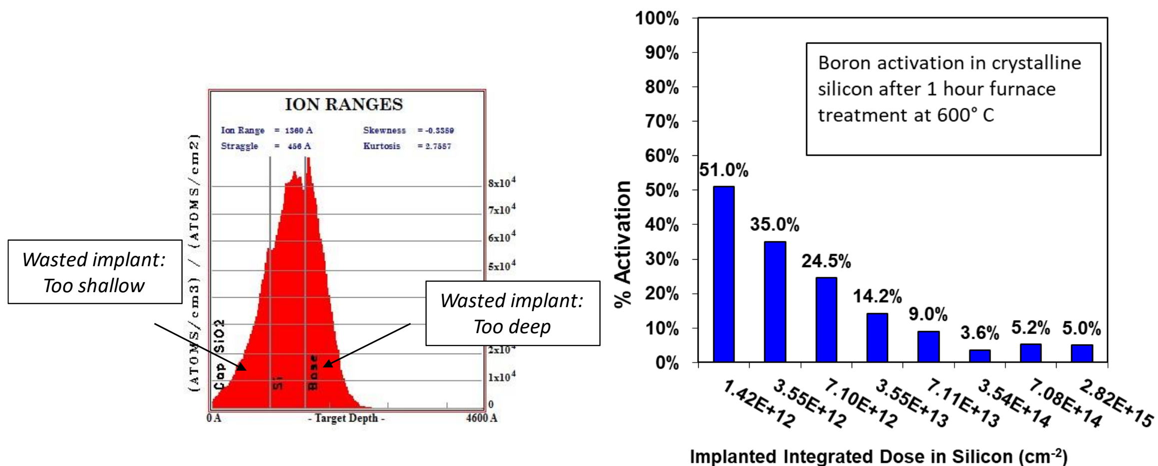

Figure 4.7 Left: SRIM demonstration of boron ion ranges in a thin silicon layer. Right: Activation percentage of implanted boron in crystalline silicon after a low-temperature furnace anneal demonstrating severely diminishing returns, from [97]

Glass is popularly considered to be "a frozen liquid" rather than a true, rigid solid. While this is not exactly accurate, it is true that the heating and cooling of a glassy solid is far less well-behaved than a classic crystalline solid. The thermal stability of a glass substrate is not limited by its liquid transition temperature but by its tendency to crack and warp. A substrate that bends or

breaks into two pieces, even if the break is clean and the pieces are sizeable, becomes incompatible with the handling and machinery designed to precisely align it to future fabrication and integration processes. With a glass substrate, it is not just the temperature reached and the duration held at temperature that can contribute to this failure, but also the rate at which that temperature is approached or disengaged [98]. Risk of cracking or warping can be partially alleviated by first subjecting glass substrates to a "pre-compaction" anneal at the highest temperature it is expected to reach during fabrication, though this is not a perfect solution [99]. It is far better to simply limit the thermal budget to a temperature that is lower than the maximum for which the glass formulation is technically rated.

Diffusion of dopants at glass-compatible temperatures is effectively negligible [95]; the overwhelming portion of lateral stray of dopant within the experiments in section 4.2 can be attributed to mass transport during melt-phase transition, with minor impacts related to implant straggle and lithography misalignment. When dopants are introduced into the silicon after crystallization and activated with a glass-compatible furnace anneal, this effect can be fully negated. However, activation percentage in this furnace anneal is equally limited. Of the dopant atoms which are introduced and then remain within the thin film of active polycrystalline silicon, most continue to occupy interstitial sites or are expelled from the lattice by interstitial silicon atoms.

The rate of incorporating dopant atoms to a lattice site at low temperatures is greatly increased by taking advantage of SPER [100]. During ion implantation, high-energy dopant ions impinge upon a surface, transferring their kinetic energy to the surrounding material as they penetrate the medium. This addition of energy can disrupt long-range order of crystalline structures, effectively "knocking" lattice atoms out of alignment. This causes a cascading chain of collisions by which a

single implanted ion can, with sufficient kinetic energy, result in many times more atomic vacancies than it directly causes. The result is damage to a crystalline material in the form of numerous unfilled, "dangling" bonds. Interstitial dopant atoms require much less energy to assume a lattice position in these pre-made empty sites than is required to displace a lattice atom [101].

4.4.1 Methods

In order to isolate the effects of physical lattice damage from any possible chemical or electrical effects caused by an introduced ion, an experiment was performed using a silicon implant as a preamorphization species. A self-implant of silicon ions into LTPS, unlike other available neutral species such as nitrogen or fluorine, is guaranteed to produce no additional electrical trap states or bonded compounds, fully isolating the kinetic impact of the implant from chemical effects. Two implant conditions were investigated, with one designed to partially amorphize the LTPS at the top of the silicon layer and the other designed to thoroughly amorphize the entire layer, effectively resetting it to its state prior to FLA crystallization; this experiment was modeled off existing analysis of amorphized layers via implant parameters [102]. Figure 4.8 demonstrates the intent and simulated results of these two conditions.

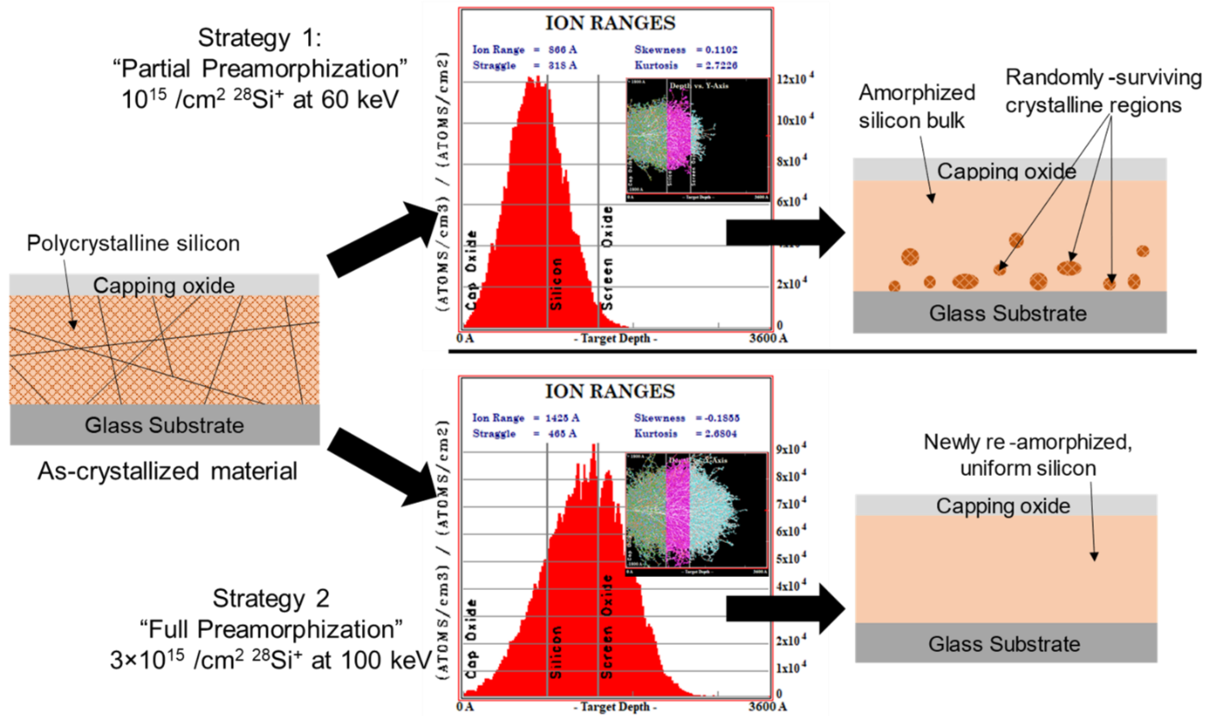

Figure 4.8: Diagrams and SRIM simulations of two silicon-ion preamorphization implant strategies. Upper path: "Partial preamorphization", with a dose of 1e15 cm^{-2} and an acceleration voltage of 60 keV targeting the leading edge of the silicon layer. Lower path: "Full Preamorphization", with a triple dose of 3e15 cm^{2} and an acceleration voltage of 100 keV targeting the base of the silicon layer.

This preamorphization implant was incorporated into the scalable FLA LTPS process immediately prior to dopant implantation. In addition, the glass substrate was switched from Corning Eagle XG to Corning Lotus NXT, a glass formulation optimized for very high thermal stability.

4.4.2 Results

Figure 4.9 demonstrates the electrical results of typical devices produced with these strategies. The addition of a partial preamorphization implant into a scalable PMOS FLA LTPS TFT broadly improved electrical behavior over the earlier experiment without any amorphization implant. This

strategy reduced threshold voltage from -16.3 V to -7.6 V, possibly by reducing the concentration of interstitial species and allowing more point defect trap states to heal through SPER. However, there was a noticeable increase in off-state leakage at higher drain bias, increasing by three orders of magnitude. In contrast, the full preamorphization strategy dramatically distorted electrical behavior, producing devices that barely showed any sort of transistor modulation with transfer curves that immediately flattened out. This suggests a strong component of series resistance degrading performance. Operation at low drain bias succumbed to this effect to the point that barely any drain current could be measured.

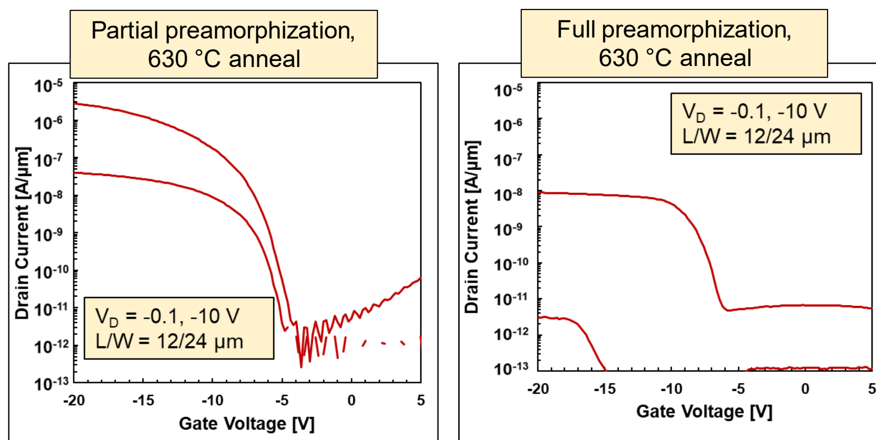

Figure 4.9: I_D-V_G characteristics of typical p-type transistors fabricated using a partial preamorphization (left) and a full preamorphization (right) strategy. Published in [103]

SPER is known to have an enhanced rate at higher temperatures in amorphized silicon [104]. To compare the impact of this enhanced rate with that of the preamorphization implants, a second set of samples was annealed at 700 °C after undergoing the same silicon ion pre-implants. This temperature approaching the point at which boron dopant migration is likely to be mediated by transient-enhanced diffusion (TED) [105], [106] which may cause boron in the tail of the implanted volume to diffuse at a faster rate. TED is mediated not by the concentration of boron

atoms, but by interstitial *silicon* defects; therefore, an increase in lattice damage by implanted silicon ions may dramatically improve boron activation. No higher activation temperatures could be investigated due to the thermal limitations of the substrates. The electrical results of devices built on these samples are shown in Figure 4.10.

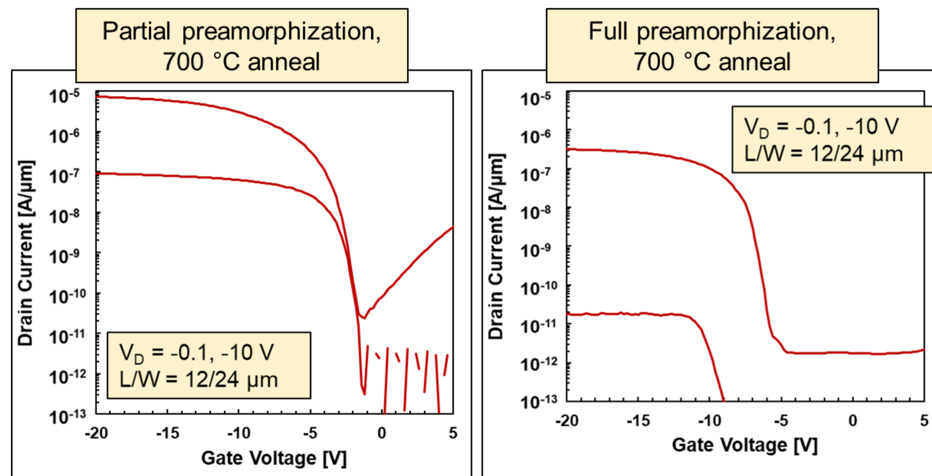

Figure 4.10: I_D-V_G characteristics of typical p-type transistors fabricated with a 700 °C activation anneal following a partial preamorphization (left) and a full preamorphization (right) strategy.

As compared with 630 °C activation, 700 °C-activated partial preamorphization devices showed excellent transfer characteristics with much sharper switching. Threshold voltage was further improved from -7.6 to -2.8 V as trap states near the channel could be healed with SPER. As a tradeoff, the off-state leakage at high drain bias was also increased and increased further with a stronger positive gate voltage. Meanwhile, the full preamorphization strategy activated at 700 °C showed a similar pattern to the 630 °C batch, with only the level of current plateau being noticeably different. Low drain bias operation became possible, but never crossed the threshold of nanoamps per micrometer of width.

The operation of devices subjected to a heavier silicon ion implant suggests that silicon recrystallization took place through a different mechanism than that of the partial amorphization strategy. This very high series resistance, exponentially mitigated at a higher-temperature heat treatment, suggests a nucleation-mediated solid phase crystallization method rather than epitaxial regrowth. It can thus be concluded that the "full amorphization" treatment truly does remove all significant presence of crystalline phases in the implanted regions, preventing SPER from taking place by eliminating any seed crystals from which to regrow.

Figure 4.11 demonstrates the carrier channel mobilities of partial preamorphization devices activated at 630 °C and 700 °C, extracted using the maximum transconductance. A partial preamorphization process with a higher temperature anneal consistently demonstrated channel mobilities in excess of 40 $cm^2/(Vs)$. Though Hall effect mobility extraction would be needed to properly decouple mobility from current, these channel mobilities can be compared with the current output at -10 V to suggest an average active charge carrier concentration of around

$8.4\times10^{18}/cm^3$, as compared with a carrier concentration of $1.6\times10^{18}/cm^3$ for the lower-temperature activation.

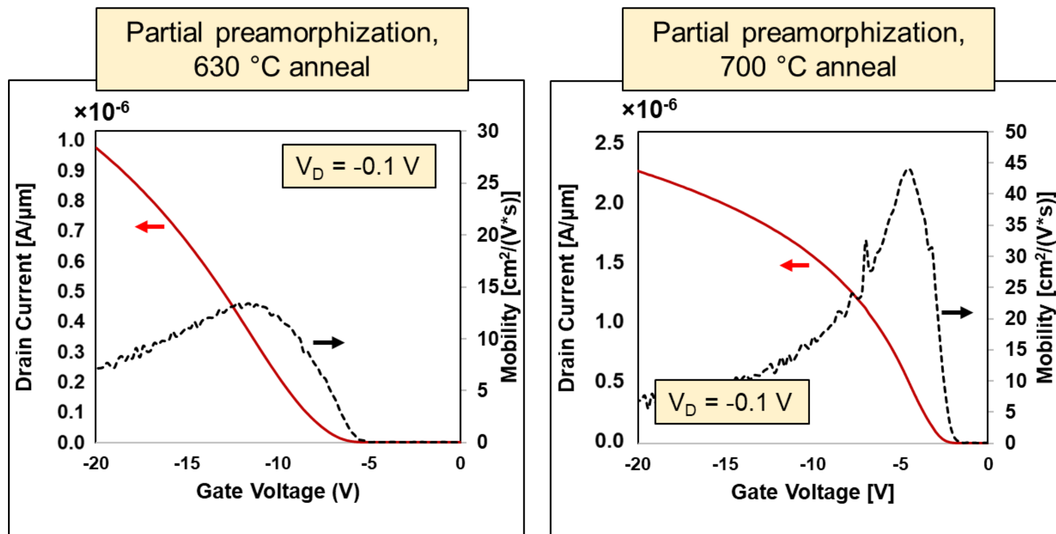

Figure 4.11: Linear, low drain transfer characteristics of partial preamorphization devices activated at 630 °C (left) and 700 °C (right), showing V_t of -7.6 and -2.8 V respectively and maximum channel mobility of 13.5 and 44.2 $cm^2/(V*s)$ respectively.

When these results are compared with those from Section 4.3, it is clear that a partial preamorphization has a minor positive impact on mobility and a significant impact on threshold voltage and total current output, with a slight increase in minimum leakage current. However, off-state leakage continued to increase with reverse gate bias, suggesting a gate-induced drain leakage (GIDL)-like mechanism. Significant improvements were also realized in yield, though this is likely due to better process controls. Table 2 compares full and partial preamorphization at 630 °C and 700 °C activation, along with non-preamorphized results from Section 4.3.

Table 2. Comparison of electrical parameters of L/W = 12/24 μm PMOS FLA LTPS TFTs with varying implant and activation treatments. Yield is defined as the fraction of devices that behaved within 50% of listed current and mobility

	Standard implant, 630 °C heat	**Partial Preamorph. 630 °C heat**	**Partial Preamorph. 700 °C heat**	**Full Preamorph. 630 °C heat**	**Full Preamorph. 700 °C heat**
Max chan. mobility [cm²/(v*S)]	12.8	13.5	44.2	(Very low)	0.04
Threshold Voltage [V]	-16.3	-7.6	-2.8	-14.4	-9.9
I_{On} @ -20 V V_G [μA]	0.25	66.7	174	0.21	7.5
I_{off} @ 10 V V_G [μA]	4.8×10^{-6}	8.7×10^{-3}	1.1	7.8×10^{-4}	4.1×10^{-4}
I_{On}/I_{Min}	5.2×10^{4}	2.5×10^{8}	7.4×10^{6}	2.3×10^{3}	4.4×10^{6}
Yield	55%	80%	88%	Very low	30%

The GIDL-like leakage mechanism is more easily explained through computer-aided simulation. Figure 4.12 shows a quasi-representative device simulated in Silvaco's ATLAS TCAD modeling software. Here, a p-channel TFT is constructed with a length of 12 μm and a gate dielectric thickness of 50 nm to closely resemble the devices fabricated in this chapter. When the device is reverse-biased by 5 V with -10 V applied to the drain, a significant amount of leakage current becomes visible. This leakage increases with the magnitude of either voltage; the physical devices shown previously used V_{DS} of -10 V and V_{GS} of up to 10 V, significantly increasing this GIDL effect. Off-state lateral electric field, shown in log scale in the upper right of Figure 4.12, is extremely pronounced just below the gate on the drain edge of the channel. This can also be seen in the energy band diagram in the lower right, where the sharp difference in voltage between

the channel and drain narrows the energy barrier to the point at which it is possible for electrons to tunnel from the drain into the body of the device.

In the physical devices shown in this chapter, this effect is much more pronounced due to trap-assisted tunneling (TAT). Defects can reduce the effective barrier of tunneling through the distorted energy barrier by providing intermediary states within the band gap for electrons to temporarily occupy. Rather than fully tunneling from valence to conduction band in a single leap, electrons may instead tunnel to a trap state part-way into the band gap, experienced as a lateral “hop” from which transition to the conduction band or a further trap is much more energetically favorable [107]. Polycrystalline silicon, due to its numerous grain boundaries and defect-dense regions, experiences a far greater degree of TAT than bulk silicon devices [108], [109]; this is one explanation for the process by which charge carriers can cross grain boundaries [110]. TAT is not included in the simulation shown in Figure 4.12.

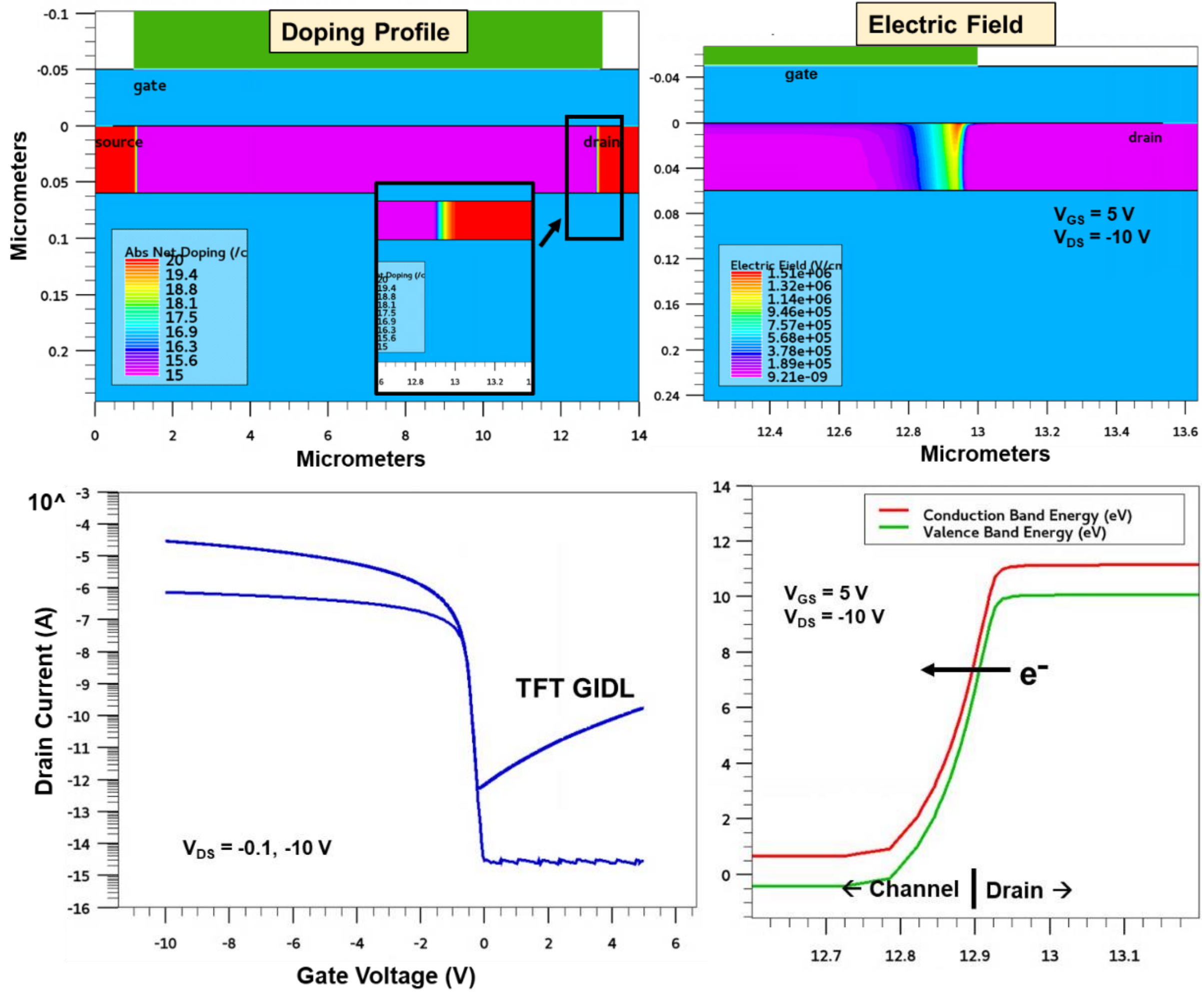

Figure 4.12: P-channel TFT TCAD simulation explaining how gate leakage is derived from band-to-band dunneling. Top Left: device structure of L = 12 μm showing dopant profile. Bottom Left: I_D-V_G transfer characteristics, indicating GIDL at higher drain bias. Upper Right: Electric field within the device at high-drain offstate conditions. Lower Right: Band diagram at the channel/drain junction, indicating a narrowed energy barrier through which electrons can tunnel.

4.5 SELF-ALIGNED DEVICES

The benefits of co-implantation suggest that dopant activation at low temperatures can be greatly enhanced. However, the presented devices were produced using lithographic design rules that far outsize those of a typical structure and application. A minimum feature distance of four micrometers is certain to prevent errors with poor metal etching or lithography misalignment, but

it leads to enormous areas of unnecessary overlap. Not only does this represent wasted area and inefficient spatial design, but it also leads to capacitive buildup in the dielectric between the silicon and the overshadowing metal layer, created by an electric field that does nothing to improve carrier flowthrough the channel. Overlapping metal area represents a waste of power that can impede switching rate and enhance leakage current when the gate is heavily reverse-biased [111].

Self-aligned (SA) device structure is a well-established method of eliminating lithography error while simultaneously reducing the number of lithography steps in a fabrication process. First described in [112] for thin film processing, the self-aligned structure uses a pre-made gate electrode as the channel mask for ion implant doping, rather than including a separate masking layer. Assuming the gate is sufficiently thick, dense, and made of a material that is not undesirably modified by ion bombardment, this strategy ensures that a minimal area of overlap is created between gate and doped wells. The extent of overlap is limited by the lateral straggle of the implanted ions and any lateral diffusion during subsequent thermal steps; this very minor area is sufficient to begin connection to the conductive inversion layer in the channel during device operation. In many applications of self-aligned gates in bulk silicon CMOS, the gate material itself is made of polysilicon which is heavily doped during the same ion implant.

4.5.1 Methods

Two additional factors must be understood to incorporate a self-aligned structure into FLA LTPS TFTs. First, the response and impact of this overlying gate material during FLA crystallization must be considered. As explained in section 3.3.2, the addition of any optically variant layer into the film stack will markedly alter how much incoming energy is reflected and absorbed by the sample. Further, the added material may act as a heat sink or retention volume, a

problem which is compounded by the geometric localization of top gate structures. Common self-aligned gate materials would either be, like metals, highly absorptive and reflective or, as in doped polysilicon, themselves impacted by the FLA crystallization process. For these reasons, it is unlikely that a self-aligned gate could be successfully built prior to crystallization.

If, as demonstrated, the self-aligned gate must be added after FLA crystallization, it means that ion implantation must also take place following crystallization. Therefore, the material and structure of the self-aligned gate must also be resilient to whatever thermal process is used for dopant activation. This process is already limited by the thermal budget of the glass substrate to below 600-700 °C depending on its specific material formulation; however, this still rules out many common wire metals. Molybdenum, with a melting point of above 2600 °C, is a readily available and easily processed material for this purpose, provided it can be safeguarded against oxidation.

To explore this, self-aligned devices were produced using a method similar to that of Section 4.3 but with the following modifications. After crystallization and formation of a gate dielectric, 100 nm of molybdenum was deposited with a DC sputter and patterned into gate structures across each mesa, with channel length being defined by gate structure width. An additional 50 nm of PECVD SiO_2 was deposited as a metal protection layer and wafers were implanted as before. The fraction of boron remaining in the silicon layer with this new, thicker screen oxide was hypothesized to be reduced from ~ 3/8 to ~ 1/4 based on SRIM simulations, but this is unlikely to have seriously impacted the concentration of activated dopants in the final product.

4.5.2 Results

Figure 4.13 shows the electrical behavior of self-aligned PMOS devices activated at both 630 °C and 700 °C, both of which also received a partial preamorphization of silicon ions. In comparison with non-SA devices, these transistors are much less left-shifted, with V_T of -3.2 and 0.2 V respectively. Note, however, that drain voltages shown on these graphs are limited to -3 V or lower, making on-state comparisons difficult.

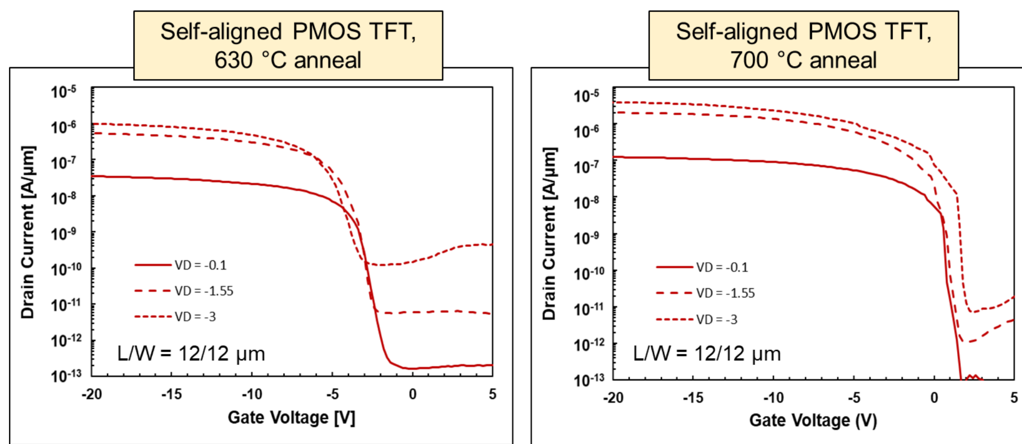

Figure 4.13: Log-scale transfer characteristics of self-aligned PMOS FLA LTPS TFTs incorporating a partial preamorphization, activated at 630 °C (left) and 700 °C (right). Note that drain bias is stepped from -0.1 to -3 V rather than -0.1 to -10 V.

Extracted parameters of these SA devices are shown in Table 3. SA devices were also produced using the full preamorphization strategy and their parameters are included in the table, but these devices behaved poorly and had an exceptionally low yield. It is more accurate to state that this combination of factors did not produce functional devices.

Table 3: Electrical parameters for L/W = 12/12 µm PMOS self-aligned configuration TFTs. Yield is defined as the fraction of devices that behaved within 50% of listed current and mobility.

	SA, Partial Preamorph. 630 °C heat	**SA, Partial Preamorph. 700 °C heat**	**SA, Full Preamorph. 630 °C heat**	**SA, Full Preamorph. 700 °C heat**
Max chan. mobility [cm²/(v*S)]	14.0	36.9	Very low	Very low
Threshold Voltage [V]	-3.2	0.2	-16.3	-14.4
I_{On} @ -20 V V_G [µA]	11.8	46.2	4.8×10^{-3}	1.9
I_{off} @ 10 V V_G [µA]	3.3	0.1	3.8×10^{-5}	4.0×10^{-5}
Yield	47%	20%	Very low	Very low

Despite the sharp switching, this method of fabrication is surprisingly non-resilient to an increase in drain bias. Figure 4.14 demonstrates this weakness with a stepped V_D between -0.1 and -10 V, the same range as the non-SA devices in Section 4.4. As the driving potential is increased, off-state leakage increases exponentially, until there is effectively no gate control over the conduction across the channel. This leakage can be explained as tunneling current similar to the GIDL-like behavior in Section 4.4, enhanced by a high concentration of point defects induced by ion implantation and incompletely healed in subsequent anneals. The impact of this defect-assisted tunneling is mitigated in non-SA devices due to the influence of the overlapping gate, which reduces energy band bending in a manner similar to a lightly-doped drain device. In SA devices, the region with the highest defect concentration coincides with the region of sharpest band bending, resulting in exceptionally high leakage through TAT. This particular weakness is demonstrated and explained graphically in Figure 4.14C

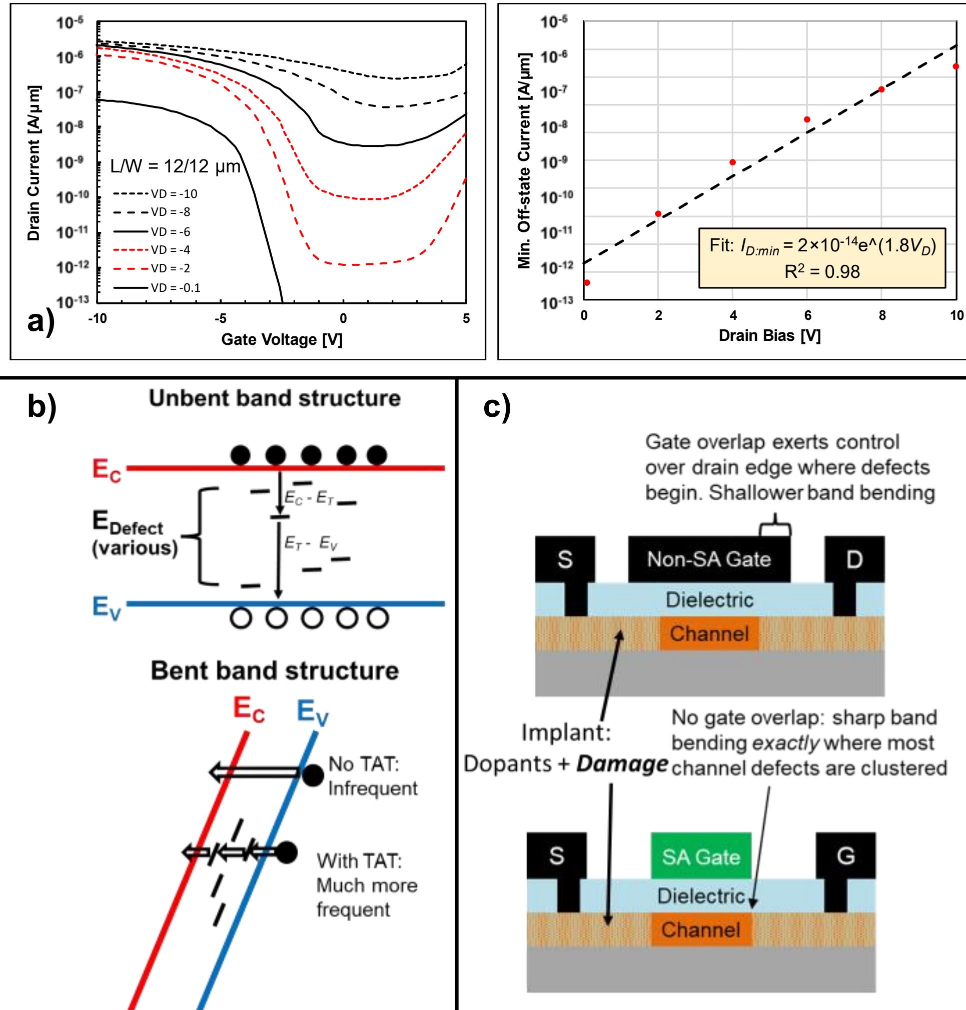

Figure 4.14: a) Left: Self-aligned, partially amorphized device with L/W of 12/12 µm activated at 630 °C, demonstrating the impact of increasingly-negative drain bias on off-state leakage. Note that the impact of gate modulation drops dramatically beyond VD = -4. b) Cartoon of the impact of defect states on TAT. c) Comparison of non-SA and SA devices, showing where TAT is clustered in relation to the gate's ability to control band bending.

Figure 4.15 demonstrates the repeatability in device operation between non-self-aligned and self-aligned devices with a sample size of near 20. The variation in operation of self-aligned devices may point to a large buildup of defects and damage at the edges of the channel, introduced by ion implantation. The fringes of the implant volume extend underneath the sides of the gate, damaging a region that should ideally remain intact after FLA crystallization. Though these fringes can regrow via SPER much like the source and drain, they have an outsized impact as undoped or

lightly doped areas that extend some distance into the channel. The non-uniform void-associated LTPS onto which the gate is constructed may also be a factor.

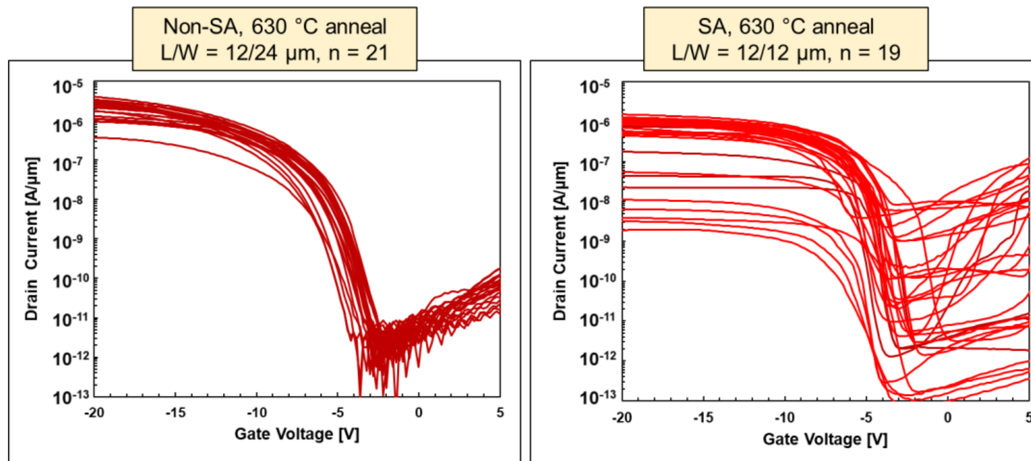

Figure 4.15: Yield comparison between non-self aligned (left) and self-aligned (right) devices otherwise fabricated in the same way, demonstrating the severe loss of replication and control caused by adding a self-aligned gate. In addition, roughly 80% of non-SA devices operated within a standard deviation of the median device, while only 47% of SA devices functioned as recognizable transistors at all

4.6 Full-FLA Scalable Devices

At a certain point, it becomes impractical to improve crystallization, dopant activation, and electrical function of FLA LTPS devices simply by increasing the temperature at which implanted dopants are annealed. Though partially amorphized devices function better than those with no preamorphization, and though self-aligned devices show improvements in scalable structure, these are not the most significant results of their experiments. The greatest improvement in functionality is attained by increasing the temperature at which furnace activation takes place. If 700 °C is better than 630 °C, it is likely that 800 or 900 °C would be even better at fully activating implanted dopants, healing implant damage, and potentially improving the crystallization of the channel in other ways. However, the temperatures used here in bulk furnace anneals already strain the

boundary of what can be considered "low-temperature" polycrystalline silicon. To rectify this, a surface anneal such as FLA can be used as an activation process as well as crystallization.

Most applications of FLA in literature and industry do not use it as a method of crystallizing a-Si; rather, it is a technique to heal damage and activate dopants in a crystalline solid. This suggests that the long furnace anneal used for dopant activation in scalable FLA LTPS TFT processes might be replaceable by a second FLA step. A "full-FLA" process such as this would limit the thermal strain of the glass substrate to the temperatures reached during FLA substrate heating or final device sintering: 400 °C in direct conduction and 450 °C by convection. This would certainly be a true low-temperature polycrystalline silicone process and is of interest for the broadening of design space and reducing the importance of a very thermally-resilient glass substrate.

4.6.1 Methods

The scalable FLA LTPS procedure detailed in section 4.3 can be easily modified to accommodate this process. After dopant ion implantation and implant mask removal, samples were exposed to a variety of FLA pulse intensities and repetitions. These pulses were set to a lower energy density so as not to re-melt the LTPS layer; though as Section 2.2.3 demonstrates, the absorbed energy needed to melt polycrystalline silicon is much higher than that of amorphous silicon. In addition, the substrate heating for both FLA steps was reduced to 400 °C to further limit deformation. The thermal limit for this experiment was thus 450 °C, though this can be reduced with alternative dehydrogenation and deposition methods [113], [114].

4.6.2 Results

Figure 4.16 demonstrates electrical data of both PMOS and NMOS devices produced with a two-stage FLA process for both crystallization and activation. PMOS devices were doped with a dose of 4e15 cm^{-2} 11-boron ion implantation at 35 keV, while NMOS devices were doped with 4e15 cm^{-2} 38-phosphorus @ 70 keV. Both processes experienced a partial preamorphization to encourage dopant uptake during activation, which was a single FLA pulse of 4.5 J/cm^2. Though lower activation intensities were explored, they showed significantly inferior results.

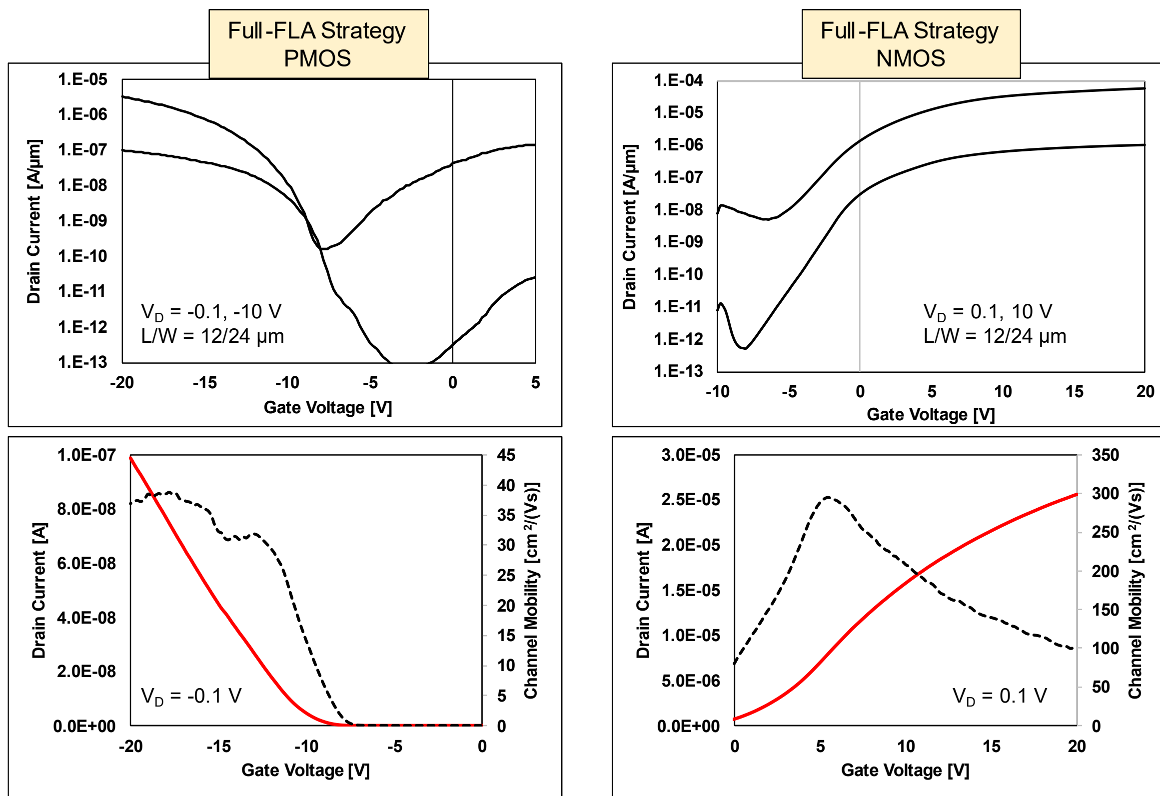

Figure 4.16: I_D-V_G characteristics (upper) and channel mobility extraction (lower) of PMOS (left) and NMOS (right) devices produced using a two-stage full-FLA strategy.

These transistors show promising device characteristics, though they represent more of a best-case in a set of high operational variance. The maximum p-type carrier channel mobility exceeded

40 $cm^2/(Vs)$, putting it in line with that of 700 °C furnace-activated samples. However, PMOS devices were all significantly left-shifted, with threshold voltages of ~ -12 V. NMOS transistors showed electron channel mobility greater than 300 $cm^2/(Vs)$ in some circumstances with V_T of ~3 V, though switching remained shallow. In all, both boron and phosphorus were proven able to be activated by FLA in already-crystallized FLA LTPS.

Off-state leakage remained the most significant downside for this full-FLA strategy. At high drain bias, PMOS TFTs regularly experienced drain leakage on the same order of magnitude as on-state current, indicating a failure of the gate to properly shut off the channel at these settings. Gate leakage, measured separately, was insignificant for these devices; all leakage flowed through the channel itself. The source for this leakage is likely similar to that of the self-aligned devices in Section 4.5 above, with additional severity due to the very low duration of post-implant anneal. A single 250 μs FLA pulse is unlikely to have sufficient time to completely regrow any energetic defects in the LTPS through SPER.

4.7 BOTTOM-GATE FLA LTPS DEVICES

The self-aligned process presented in Section 4.5 takes advantage of a top-gate TFT configuration, in which the dielectric and gate are deposited on top of the active material. This is in contrast to a bottom-gate configuration, in which gate and dielectric are deposited on a substrate first, followed by the semiconductor. Bottom-gate devices are broadly considered to be a superior TFT configuration due to improved interface control between semiconductor and dielectric layers and ease of back-channel passivation [115]. Additionally, a bottom-gate device is a necessary first step for fabricating a double-gate device, in which the semiconductor is sandwiched between two gates that can be either electrically tied together or biased independently for greater control.

Hydrogenated amorphous silicon and amorphous oxide semiconductor TFTs are easily able to utilize bottom-gate device configuration due to their simple and conformal semiconductor deposition steps. LTPS, however, requires an in-situ crystallization process, which can be significantly and situationally altered by the localized presence of underlying gates. Attempts to produce reliable ELA-LTPS bottom-gate devices have noted the difficulty of creating a uniform crystallization process when metal gates are regularly dispersed underneath, as this creates a variation in thermal response within the laser penetration depth that results in a change in optical response and local energy absorption [116], [117].

FLA LTPS, being inherently non-uniform already, can potentially benefit from exploring bottom-gate structures. It has been shown how the presence of different materials vertically and laterally near an area of a-Si can impact its degree of melting and recrystallizing. Since this property is difficult to entirely remove, it is of interest in seeing if it can be harnessed by using a bottom-gate structure to slightly enhance FLA response of silicon in the channel region, directly over the gate.

The gate material used for a bottom-gate FLA LTPS device is even more important than in other configurations. Additional materials added to the film stack during FLA will dramatically impact the silicon crystallization. An ideal gate material must be optically transparent across the broad spectrum emitted by a xenon flashbulb and have a refractive index reasonably close to the dielectric to avoid internal reflection, while still being sufficiently conductive to generate an electric field and induce inversion in the semiconductor. Additionally, it must be capable of withstanding moderate temperatures without deforming.

Indium Tin Oxide (ITO) is a transparent conductive oxide material that is often used in photovoltaic applications as a topside electrode. In PV, light must pass through a conducting

medium before reaching the photogenerative layer(s), allowing that medium to transport half of the resultant electron-hole pair further into the circuit. Since ITO has high transmissivity across much of the visible spectrum, it is ideal for this purpose and potentially useful as a bottom gate in FLA devices.

The ITO-BG process is a modification of the scalable FLA LTPS process in Section 4.3. Lotus NXT display glass wafers were coated with a thin 40 nm layer of ITO by pulsed DC sputter at 180 W onto a barrier SiO_2 layer. The ITO was then lithographically patterned into bottom gates of various sizes and etched with a dilute HCl solution before being annealed for two hours at 400 °C in air ambient to improve conductivity, transmissivity, and etch resistance. Figure 4.17 compares the transmissivity of bare glass, as-deposited ITO, and ITO after a curing anneal using a standard ITO figure of merit: transmission divided by average resistance, calculated at a wavelength of 740 nm [118].

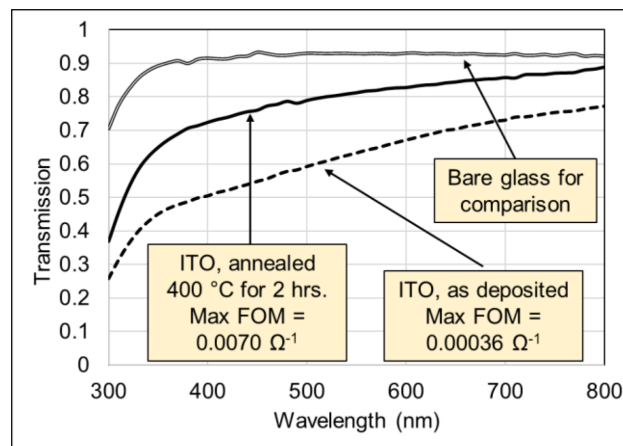

Figure 4.17 Comparison of transmissivity between bare glass, as-deposited ITO film, and ITO film after curing anneal.

Figure 4.18 shows the impact of an ITO bottom gate on an FLA-crystallized device. Larger silicon mesas with a narrow band of underlying gate structure demonstrated the most uniform

crystallization, at least from an immediate optical perspective. However, the difference in crystallization stability and remaining amorphous fraction is immediately apparent after ion implantation. Figure 4.18A shows such a structure after the amorphization effects of boron implantation. The bright center stripe represents the masked (and thus non-amorphized) LTPS channel, while the large lavender regions at top and bottom are implanted areas that did not benefit from underlying layer-enhanced crystallization; they appear to be significantly reamorphized. Between these regions are narrow bands of mottled pink, representing implanted areas which *did* benefit from underlayer-enhanced crystallization and were thus much more resistant to the kinetic damage of the boron ions. The presence of a fringed border, shown by the yellow arrows, indicates that this is not merely optical thin-film interference, as the areas of silicon near but not directly over the ITO gate also received some crystallization enhancement. This impact is still visible after dopant activation and recrystallization, as shown in the completed-device image in Figure 4.18B.

Bottom gates with a larger area had more of a significant impact on visible deformation of the overlying silicon, suggesting that this process would not be robust for an implementation that required many BG devices of varying dimensions. Figure 4.18C brings shows this effect clearly; as Figure 4.18D shows the consequence of an FLA exposure whose energy is not modified to take the somewhat-absorptive bottom gate into account. A melt-phase transition is attained in the source and drain regions far from the gate, but at a consequence of overabsorption and total silicon loss in the channel.

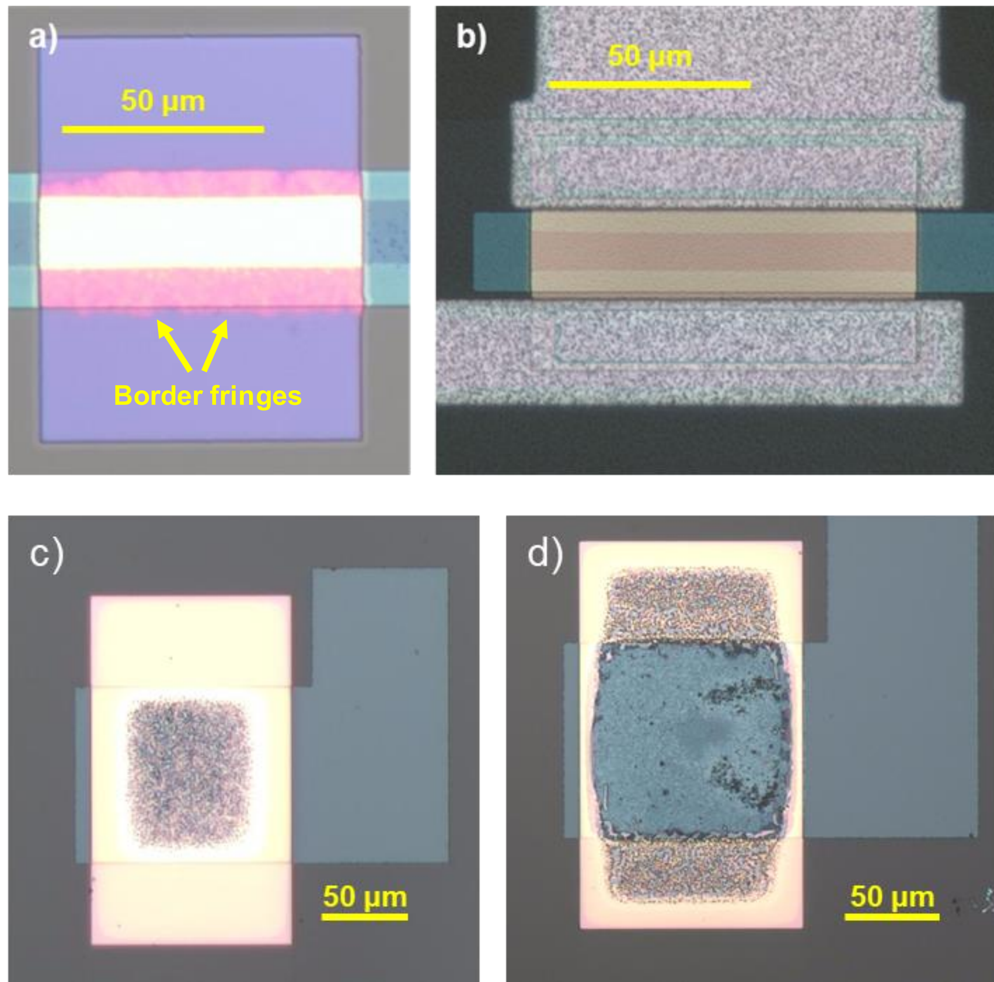

Figure 4.18: a-b) Optical micrographs of ITO bottom-gate devices taken a) directly after ion implant and b) as a completed device. As these silicon mesas were crystallized first, the impact of boron implant damage is readily visible in the three distinct stripes in a). c) Micrograph of a silicon mesa over a large-area ITO BG directly after FLA, crystallized at 4.4 J/cm^2, showing significant variation between on-gate and off-gate areas. d) Micrograph of another silicon mesa crystallized at 5.0 J/cm^2, demonstrating the consequence of excess energy with a locally-varying film stack.

PMOS devices produced in this manner had varying results, based on the area of their bottom gate. To ensure overlap, gates were four micrometers broader than the eventual channel towards both the source and drain. Devices with channel lengths of four micrometers demonstrated unexpectedly high channel mobility and sharp switching behavior at low drain bias, as shown in Figure 4.19. Threshold voltage was -4.8 V and maximum mobility was greater than 190 cm^2/(V*s).

However, a drain bias of V_D = -10 V resulted in significant off-state leakage, curve separation, and irreversible device failure.

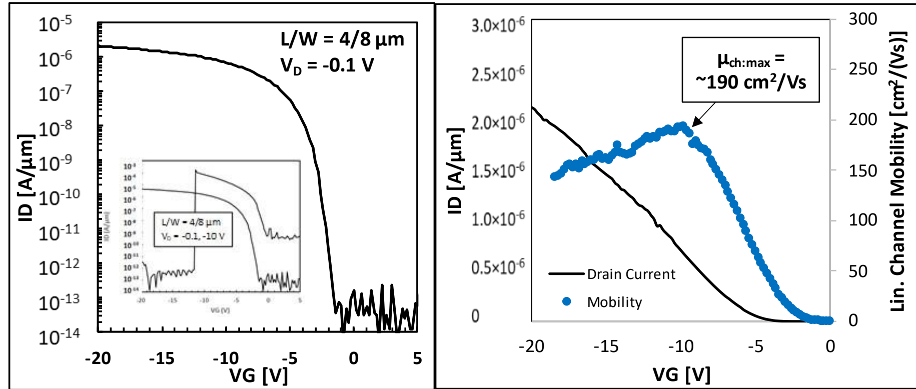

Figure 4.19: Low-drain transfer characteristics of an ITO bottom-gate TFT, demonstrating sharp transition, low leakage, and very high channel mobility prior to catastrophic breakdown. Mobility calculation uses a 15 point smoothing function. Inset: catastrophic breakdown of same device when tested at V_D = -10 V. Published in [119]

The breakdown of small dimension ITO BG devices at high drain bias may be due to the randomized morphology of heavily voided FLA LTPS. As channel dimensions get smaller and smaller, the conductive pathways across the channel become more stressed as charge crowds into smaller and smaller areas. If those paths are not an 8 µm-wide channel as intended, but rather a few strands of intact silicon, this current crowding may exceed the limits of the silicon. Alternatively, this could represent a device with a single grain of LTPS spanning the full length of the channel, which would account for the anomalously high carrier mobility.

4.8 DEVICE CONFIGURATION SUMMARY

Despite the disconcerting random-void structure of this FLA LTPS, functional and encouraging TFTs have been demonstrated in both n- and p-type. Initial devices showed extremely high mobility and sharp switching characteristics due to a fabrication method that maximized

dopant activation while minimizing defects. However, the loss of scalability in this process necessitated investigations into alternative dopant introduction and activation schemes. Improvements over initial scalable devices were attainable by promoting SPER in the source and drain through a silicon ion preamorphization implant, which was particularly effective when activation anneal temperature was increased to the highest temperature the glass substrates could withstand. Additional improvements in switching and scalability were demonstrated with a self-aligned configuration. Unfortunately, each of these processes resulted in a high degree of leakage current caused by trap-assisted tunneling, associated with point defects generated by the kinetic ion implant.

Further device configurations were explored, including a replacement of the high-temperature furnace activation anneal with a secondary FLA step. Though not ideal, both boron and phosphorus devices could be activated this way, demonstrating the feasibility of a full-FLA process. Lastly, bottom-gate devices were briefly explored with encouraging results, though the method and rate of failure at higher voltages rendered their operation rather frail. After this analysis, the timing of dopant introduction and the method of activation were conclusively identified as a key point of variability in producing high-quality FLA LTPS TFTs.

Chapter 5. MONOLAYER DOPING IN FLA

Ion implantation causes significant problems in FLA LTPS devices, warranting the exploration of other doping methods. Most LTPS TFTs are doped in-situ by adding dopant-containing molecules during chemical vapor deposition; however, FLA devices suffer if large quantities of dopants are present during flash lamp crystallization. Monolayer doping is a recently-developed alternative for harmlessly introducing a controlled concentration of dopant for ultra-thin junctions in bulk semiconductors, which shows promise as a doping method for FLA LTPS TFTs. N-type and P-type devices were produced using MLD phosphorus and gallium respectively.

5.1 MOTIVATIONS FOR MONOLAYER DOPING

Chapter 4 has demonstrated numerous negative factors that result from a reliance on doping by ion implantation. The kinetic energy associated with high-voltage ion bombardment can be deleterious to a thin semiconducting layer of polycrystalline silicon by causing atoms in lattice sites to become dislodged. This goes well beyond the formation of Frenkel defects; a high-dose ion implant can damage enough of the crystal structure to cause a significant percentage of it to return to an amorphous state, effectively killing any long-range order and the electrical benefits therein. This effect is much more severe in thin-film applications than in bulk silicon, as a bulk sample will always retain at least some distantly buried layer of crystalline material from which the crystal structure can be epitaxially reformed, no matter how energetic and sustained the impinging ions. If the polycrystalline structure of the silicon is fully eradicated, regrowth becomes impossible, and recrystallization is more likely to follow a pattern of randomized nucleation.

However, a certain degree of lattice damage and amorphization is necessary for dopant activation through a furnace anneal, particularly when the temperature of this anneal is limited by the thermal budget of a glass substrate. Lower doses of light ions, such as boron, are more likely to result in an amorphization fraction that cannot fully take advantage of solid-phase epitaxial regrowth. The targeting of precise energetic influence with a set of ion implants is both challenging and expensive. In short, ion implantation into thin LTPS comes with numerous difficulties and pitfalls that must be considered when designing a fabrication process.

Most industrial LTPS TFTs do not use ion implantation as the main method of introducing dopants into source and drain regions due to cost. It may be incorporated as a threshold voltage adjust or lightly doped drain, but these applications are much lower dose and therefore less costly and time-consuming. Instead, dopants are introduced into the silicon during a-Si deposition by incorporating a small fraction of dopant-containing molecule into the chemical vapor deposition chamber, such as phosphine for n-type phosphorus-doped a-Si or diborane for p-type boron-doped a-Si [120], [121]. This method is technologically mature, well-established, and able to be tailored to suit a wide variety of desired concentrations without damage or contamination to the silicon layer. Additional a-Si depositions can be added on top of this doped layer (or underneath and prior to it), allowing for *p-n* or *p/n-i-p/n* junctions as needed. These deposition-introduced dopants function in the same way as ion implanted dopants and can assume electrically active lattice sites if the amorphous silicon is crystallized.

Unfortunately, small FLA LTPS devices are wholly incompatible with in-situ deposition doping, as demonstrated in section 4.2. FLA crystallization necessitates the simultaneous melting of large areas of amorphous silicon in 100-microsecond timescales, which is a sufficient duration for any dopant molecules present to diffuse in all lateral directions by many micrometers. This

results in a supposedly intrinsic channel being encroached and shortened by diffusing dopants from the source and drain.

5.2 Physics of Monolayer Doping

Monolayer Doping (MLD) represents a recently-developed alternative method of introducing a precise concentration of dopants into a semiconductor surface. Originally presented by Ho *et al.* [122] for creating ultra-shallow boron junctions in bulk silicon, the structure and requirements for MLD make it well-adapted towards thin-film silicon applications.

In MLD, a bare silicon surface is chemically treated to populate its surface with hydrogen-terminated bonds. The surface is then submerged into a heated solution containing an organic molecule bearing both the dopant of interest and a reactive alkene or alkyne group. Over time, the Si-H surface bonds are chemically replaced with bonds between silicon and this organic group at the reduced alkene or alkyne in a process that propagates across the entire silicon surface. Figure 5.1 demonstrates the likely chemical mechanism for this replacement as stated in literature, in which these molecules replace silicon-hydrogen surface bonds to form a covalently bonded self-assembled monolayer [123].

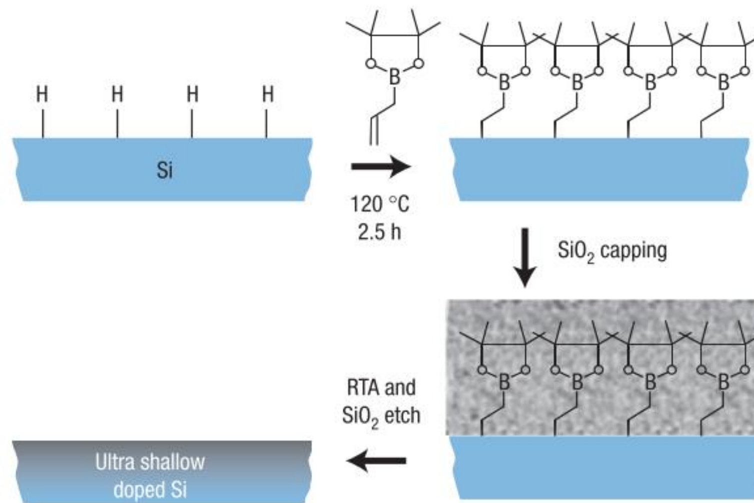

Figure 5.1: Mechanism of monolayer doping of boron through a self-assembled layer with an allylboronic acid pinacol ester precursor, from [122]

Once these bonds have formed, the surface is immediately coated with PECVD SiO_2 to encapsulate the dopant and prevent it from desorbing. An annealing process, such as RTA or furnace heating, is used to drive the dopants into the silicon bulk to a desired junction depth. The maximum dose of dopant that can be introduced through a single MLD process is thus strictly limited by the areal density of surface bonding sites, thus making it most effective as a technique for ultra-shallow junctions [124], [125] and the doping of nanostructures [126], [127].

5.3 Integration of Monolayer Doping and FLA

Figure 5.2 demonstrates how this technique can be introduced into an FLA LTPS TFT process. The monolayer adhesion process is surface-dependent, meaning that any thickness of consistent and non-permeable barrier between silicon and dopant solution beyond the thickness of native oxide growth is likely to be sufficient to prevent dopant molecule bonds from forming. Due to the

ease with which MLD can be blocked, selective regions can be masked off prior to solution immersion to allow intrinsic device channels to remain. Phosphorus, a convenient n-type dopant in silicon, can be introduced via MLD using a precursor of diethyl vinylphosphonate (DVP) [128].

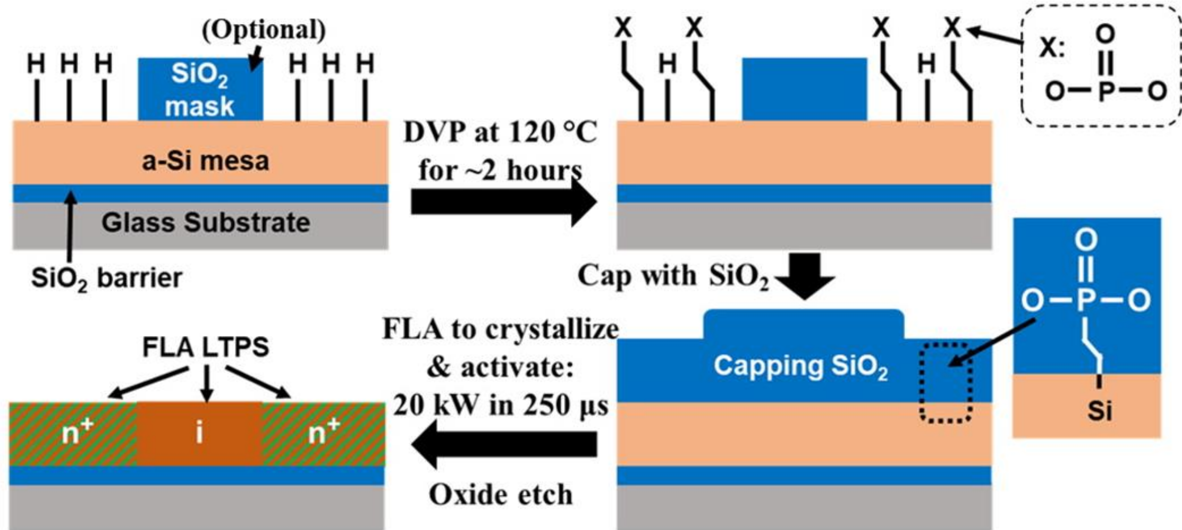

Figure 5.2: Diagram of the process for selectively doping, crystallizing, and activating thin LTPS via MLD with DVP. Published in [129]

Based on previous analyses of TFTs produced on FLA LTPS, two potential strategies for incorporating MLD become apparent; one in which amorphous silicon mesas are doped via MLD and then crystallized and activated with a simultaneous FLA treatment, the other in which FLA-crystallized LTPS is doped via MLD and activated with a separate thermal step. These strategies mirror those in Sections 4.2 and 4.3, respectively. Previously, it was determined that a significant presence of dopant atoms in amorphous silicon during FLA crystallization resulted in a large degree of channel-length reduction in the final devices, while dopants introduced into LTPS and activated at glass-compatible temperatures suffered from inextricable combinations of lattice damage and poor activation. The replacement of ion implantation with MLD may affect these drawbacks by providing a physics constrained dose that is non-energetically positioned at the

upper surface of the silicon layer, preventing significant lateral diffusion caused by an overabundance of dopants and eliminating kinetic lattice damage. For the purpose of expediently demonstrating compatibility with FLA LTPS, a single-FLA strategy was selected, mirroring that of Section 4.2.

5.4 PHOSPHORUS MLD FOR NMOS FLA LTPS TFTS

This experiment modifies the process design listed in Section 4.2 to replace ion implantation with a selective MLD self-assembly process as per Figure 5.2 above. Commercially-available DVP ($C_6H_{13}O_3P$) was used as a phosphorus-containing dopant source with a mesitylene (C_9H_{12}) solvent in a 1:25 ratio by volume, heated at 120 °C for two hours to produce silicon-vinyl phosphonate surface bonds, which were then capped with PECVD SiO_2 as both a dopant cap and antireflective layer. The MLD-exposed samples were then exposed to a single FLA pulse to simultaneously crystallize the silicon and incorporate the dopants adhering to the surface. Transistors were then compared with a similar but gateless structure (making a thin film "back-to-back diode") and a fully doped resistor. Figure 5.3 demonstrates the device structures produced in this experiment.

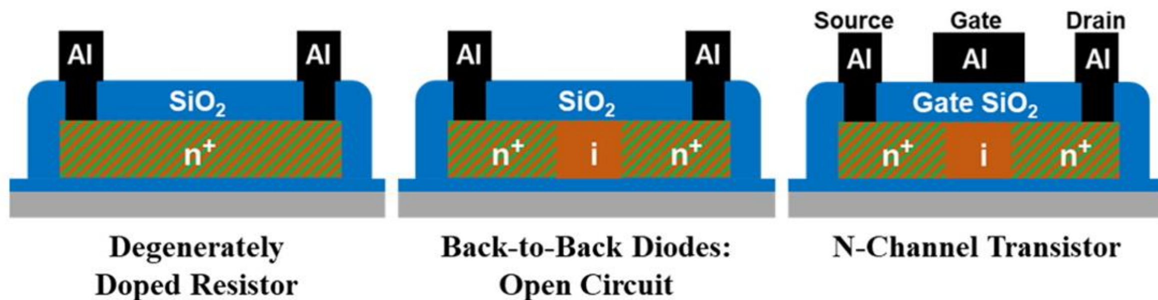

Figure 5.3: Three device structures produced by phosphorus monolayer doping and FLA.

Fully-doped resistors were subjected to secondary ion mass spectroscopy (SIMS) in order to confirm the physical presence of phosphorus in silicon after crystallization, as shown in Figure 5.4. It was found that an average concentration of around 8×10^{19} cm^{-3} was present throughout the film thickness, with a "hump" at the fore-edge of the sample which is a common characteristic of SIMS data on rough surfaces. Integrating across the ~60 nm depth of the mesa, this comes out to an estimated dose of 4.1×10^{14} cm^{-2}. To determine MLD efficiency, this number can be compared with the surface density of silicon atoms in common crystalline planes, which is 6.8×10^{14} cm^{-2} for the sparsest (100) plane and 9.6×10^{14} cm^{-2} for the densest (110) plane. Thus, the metallurgical doping efficiency of this process can be estimated as between 41% and 60% of the ideal factor. This suggests that MLD of amorphous silicon by FLA is an effective strategy and that there is no significant loss of dopant into the sacrificial oxide. Further, this demonstrates an effective full-thickness melting of the silicon layer during FLA. As dopant amount in MLD is dependent on availability of surface silicon bonds, increasing dopant concentration further would require multiple MLD and FLA iterations.

Selective dopant activation was confirmed by comparing 2-probe resistance measurements between fully doped two-terminal resistors and incompletely doped back-to-back diode devices: 96 μm wide and 120 μm between electrodes, with a 96 μm undoped "gap" in the case of the back-to-back diode. An average sheet resistance of 11 kΩ/□ was obtained on n+ doped regions and n+-i-n+ structure exhibited near open circuit. The sheet resistance of 11 kΩ/□ yields a resistivity value of 0.066 Ω·cm. This value corresponds to electron concentration-mobility product ($n\times\mu$) of $9.46\text{x}10^{19}$ $(cm\cdot V\cdot s)^{-1}$, which would translate to an electron concentration of $1.45\text{x}10^{17}$ cm^{-3} if the material was assumed to have the properties of bulk silicon. Therefore, this represents a lower bound of carrier concentration. In polycrystalline thin films, some active dopant is lost via dopant

segregation at the grain boundaries and mobility is lower due to the presence of grain boundaries in addition to surface scattering. This suggests a much higher active phosphorus concentration in this polycrystalline silicon MLD doped film, potentially on the order of 10^{18} cm^{-3}. Comparing with the SIMS data in Figure 5.4, it indicates a significant dopant activation resulting from MLD. The fully doped resistors displayed a lower resistance than back-to-back diodes by nearly six orders of magnitude, simultaneously demonstrating that the introduced phosphorus had become electrically active and that MLD could be limited to specified areas through selective silicon masking. Spreading resistance profile (SRP) data could not be measured on the isolated mesa structures of FLA LTPS, which must be patterned prior to crystallization as shown in Section 3.2.

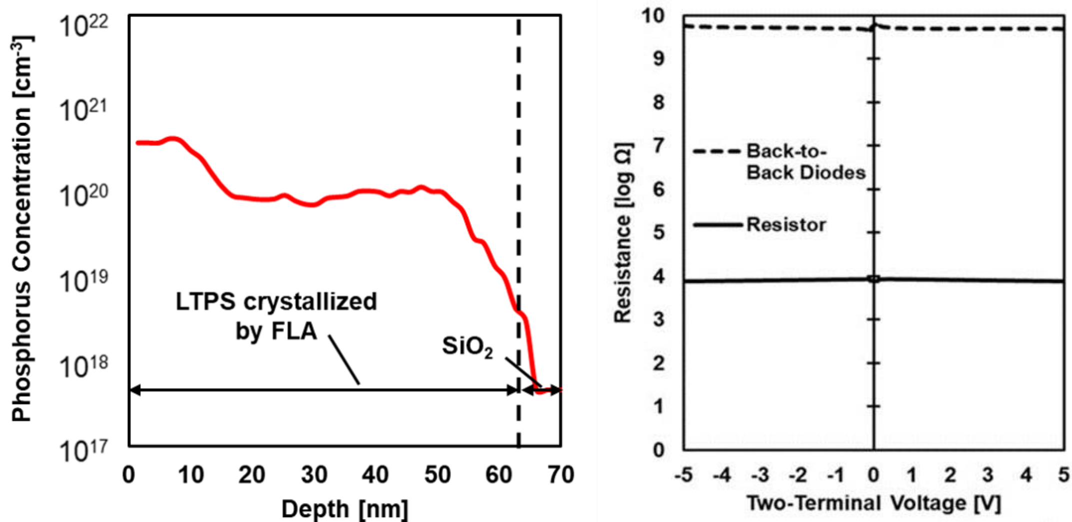

Figure 5.4: Left: SIMS data of an LTPS mesa doped with MLD phosphorus, showing a roughly uniform concentration across the thickness of the silicon film. Right: resistance comparisons between doped and undoped resistors (back to back diodes), demonstrating the phosphorus to be electrically active as well as metallurgically present.

Completed NMOS transistors were fabricated by adding a modulating gate to the back-to-back diode structures. Figure 5.5 demonstrates the typical electrical behavior of these n-type FLA MLD LTPS TFTs. In devices with mask-defined channel length of 96 μm, a threshold voltage of -1.2 V

and I_{On}/I_{Off} ratio of 10^5 were established. Electron channel mobility, extracted by the maximum transconductance method, reached a maximum of 61.3 $cm^2/(Vs)$. If this negative V_T is due entirely to trapped interface charge, roughly 5.5×10^{11} $/cm^2$ trap density exists at this interface.

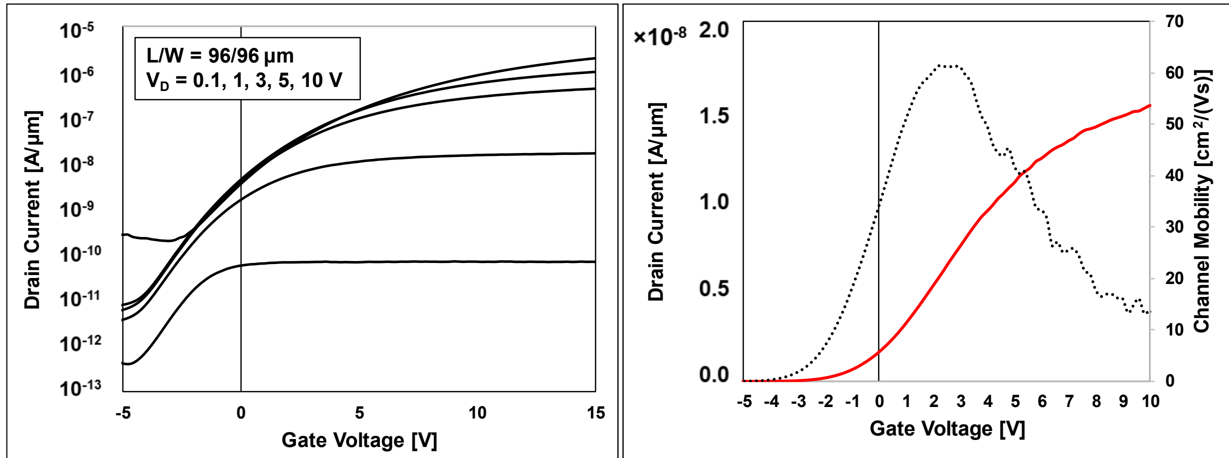

Figure 5.5: Left: I_D-V_G characteristics of a typical n-channel MLD FLA TFT at a series of gate voltages. Right: Extracted channel mobility and linear-mode low drain device behavior. The pronounced slump of low drain current suggests a high series resistance in the source and drain.

5.5 Gallium MLD for PMOS FLA LTPS TFTs

Monolayer doping with a boron dopant has been demonstrated fairly extensively in the literature. However, boron is not always the ideal p-type dopant due to its formation of light-sensitive boron-oxygen defects compounds, which degrade the lifespan of silicon solar cells [130], [131]. Gallium is another element in the boron group (Group 13) which is an acceptor material in silicon, and yet is not in common use in silicon PMOS or CMOS logic. Activation of high gallium concentrations is difficult, as the solid solubility of gallium in silicon is significantly lower than that of boron [132]. In addition, its diffusivity at common VLSIC process temperatures is very high in silicon and boron co-doped silicon [133]. The problems facing gallium as a dopant in silicon may be addressed by a doping method that generates an ultrashort junction of a specific

targeted concentration in a thin silicon film. Thus, a unified process of monolayer doping and FLA can potentially compensate for the problems classically associated with gallium dopants, or at least render them redundant. This is especially true in a thin film structure, as gallium cannot diffuse too deeply into a semiconductor body if that body is truncated to a few tens of nanometers.

To explore Ga-doped PMOS MLD FLA LTPS, the process in Section 5.4 was replicated with a gallium-containing precursor. Selected regions of amorphous silicon mesas were exposed to a solution of tris(2,4 pentanedionato)gallium(III) ($Ga(acac)_3$) in mesitylene in a 1:25 ratio by volume for two hours at 120 °C to cause gallium-containing compounds to bind to the silicon surface, after which the samples were capped with 100 nm PECVD SiO_2 and again crystallized with a single FLA pulse of 4.6-5.2 J/cm^2. This anneal was designed to simultaneously melt and recrystallize silicon, drive surface dopant into the silicon bulk, and provide enough energy for it to assume electrically active lattice positions. The efficacy of this process was analyzed with both SIMS and a SRP reading on a similar blanket sample of silicon-on-insulator (SOI) material, the dimensions of FLA LTPS mesas being not conducive to SRP. These results are shown in Figure 5.6.

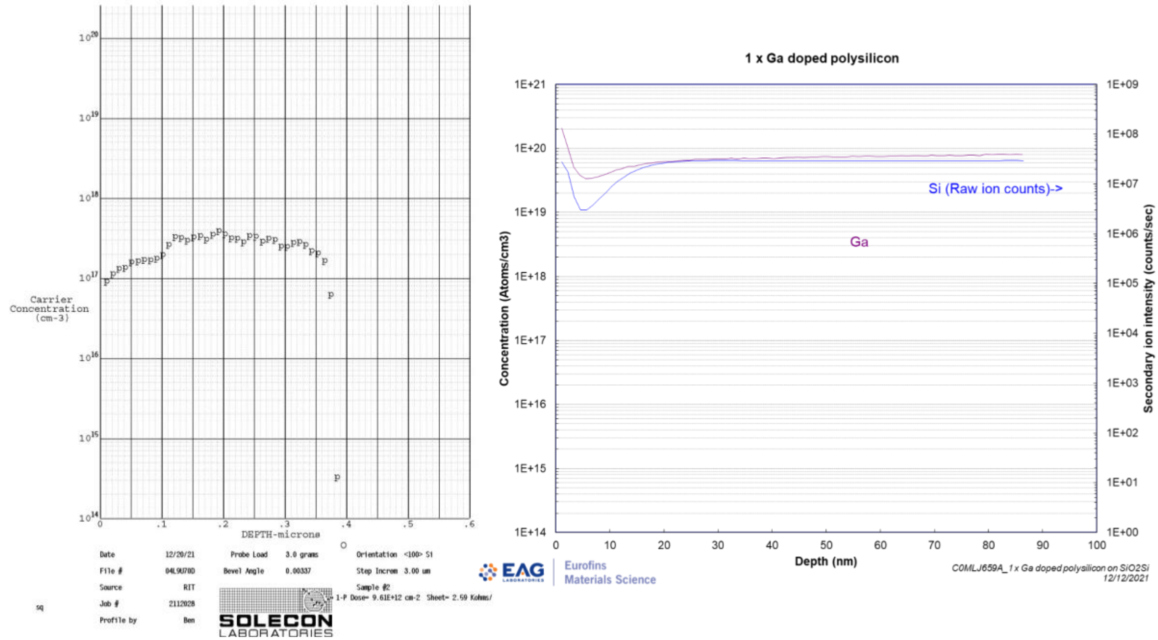

Figure 5.6: Left: SRP data of a silicon-on-insulator sample doped with MLD gallium. Right: SIMS data of a similar sample, indicating a much higher gallium concentrtion

From SIMS data, it is clear that MLD and FLA can cause a high dose of gallium, ~ 5×10^{19} atoms/cm^3, to enter the polysilicon. However, if the two structures of silicon sample are to be considered comparable, SRP data indicates that only a tiny fraction of that dose becomes electrically active, ranging from 1 to 5 percent of the metallurgical concentration. This is not unexpected given gallium's limited solid solubility in silicon and large atomic radius. Unfortunately, it suggests that even the thermal nonequilibrium aspect of FLA crystallization cannot easily overcome these obstacles. Given the regular crystal structure of SOI and thus higher surface density of silicon-hydrogen bonds, it would be expected that an even higher concentration of MLD gallium would be available in the SRP sample than these results show.

PMOS thin film transistors were fabricated on selectively-doped gallium MLD FLA LTPS in the manner demonstrated in Section 5.4. Electrical behavior for a typical (functional) transistor is

shown in Figure 5.7. A reasonably high output current is demonstrated, with off-state leakage significantly less than many boron-doped p-type FLA LTPS TFTs. However, this process was plagued by very low yield, suggesting that the FLA parameters necessary for an ideal device are very precise.

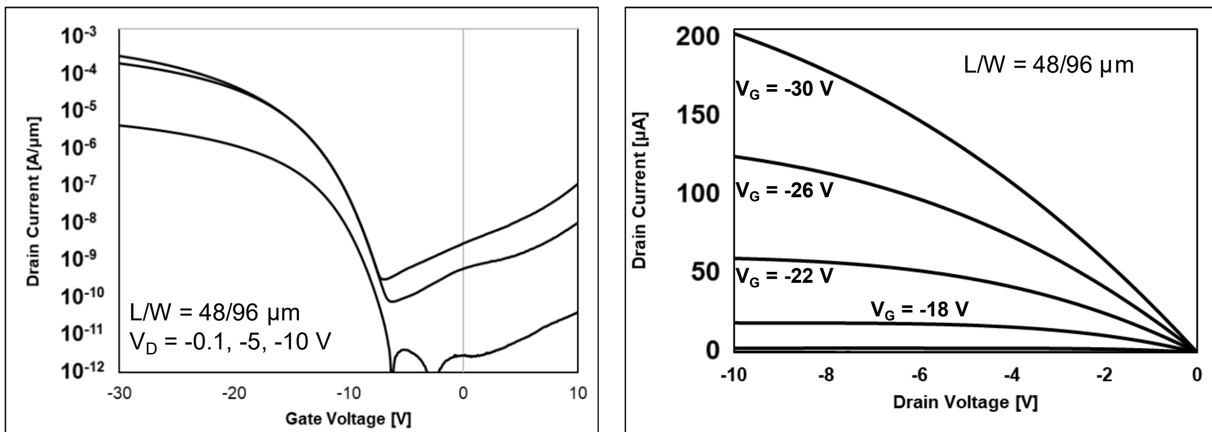

Figure 5.7: Electrical behavior of a p-channel gallium MLD FLA TFT. Left: I_D – V_G behavior. Right: Gate voltage family of curves.

Figure 5.8 shows further electrical data from this experiment. Using the maximum transconductance method, hole channel mobility was extracted to reveal a maximum of 33.0 $cm^2/(Vs)$. This value is comparable to that of FLA LTPS devices doped via boron ion implantation and activated with a furnace anneal. Using this peak, threshold voltage was calculated to be -16.5 V, indicating a much larger degree of interface charge than earlier FLA MLD experiments and potentially pointing to fixed charge associated with inactive interstitial species traveling laterally into the channel. This could be gallium or a carbon-based byproduct of the MLD process, which must be more fully understood before this technology is implemented industrially.

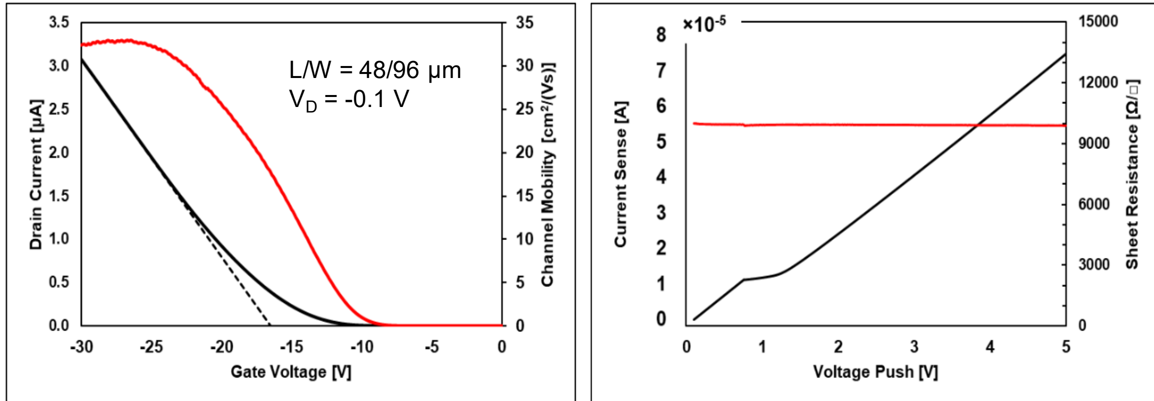

Figure 5.8: Left: Low drain transistor response with mobility and threshold voltage calculation of the device shown in Figure 5.7. Right: Van der Pauw measurements of a similar Ga MLD FLA LTPS mesa for sheet resistance comparisons.

To verify SRP data, sheet resistance was calculated on individual FLA LTPS mesas using the van der Pauw method to reveal an R_S of 9.9 kΩ/□. If activated gallium is assumed to be evenly distributed throughout the 60 nm LTPS layer, as suggested by SIMS data in Figure 5.6, this reveals a resistivity of 0.059 Ω·cm. This, combined with the mobility extracted from the TFT and the fundamental electron charge, reveals an active gallium concentration of 3.2×10^{18} cm^{-3}, somewhat higher than the concentration measured via SRP. It is therefore possible that the activation of gallium MLD via FLA is inconsistent from mesa to mesa, depending on the many geometric factors demonstrated in Chapter 3. Though devices and electrical analysis exhibited variance, Gallium MLD has been proven to be effective for the first time, both with conventional RTA activation [134] and activation via FLA.

5.6 FLA MLD SUMMARY

The mechanisms of FLA and MLD are proven to be compatible in the production of doped thin-film LTPS. Using these processes, both n-type and p-type devices were demonstrated using

phosphorus and gallium respectively. Electrical data supports the conclusion that a high percentage of MLD phosphorus is activated in LTPS, but the same cannot be said for gallium. MLD boron is almost certainly a better option for p-type FLA devices and has been extensively demonstrated by Ho and others [122], [123].

In these experiments, MLD was carried out on amorphous silicon patterned into initial crystallization mesas, then activated and crystallized simultaneously with a single FLA exposure. Previous experiments involving FLA on already-doped a-Si, as seen in Section 4.2, show a high dopant activation with a significant downside of many micrometers of lateral dopant migration. However, FLA activation of MLD without a concurrent liquid-phase transition has not been shown. The impact of the timing of these two techniques is thus of interest in further research.

Chapter 6. Cr-Enhanced FLA LTPS

FLA LTPS morphology with a random and void-heavy structure is not attractive for device integration due to variability of operation. Literature has demonstrated thick FLA LTPS with improved uniformity via the addition of a chromium underlayer. However, translation of this research into TFT thicknesses of silicon introduces the possibility of metal contamination within the silicon band gap, leading to recombination losses. Cr-enhanced LTPS at these scales is shown to be possible and produce functional TFTs, though the distribution of chromium after crystallization and further thermal process requires analysis so deleterious electrical effects can be minimized.

6.1 Literature Background

The randomized, void-laden morphology of all silicon devices presented in Chapters 4 and 5 presents significant problems that have been stated and hereto left unexamined. It is presumed that much of the electrical variability in otherwise identical devices can be explained by the random void distribution of the silicon. A lower-intensity FLA crystallization pulse results in numerous pinhole voids scattered across silicon mesas, with a higher fraction of remaining amorphous phase. Higher-intensity pulses generate a much higher crystallized fraction, but the physical consequences to mesa integrity are far more significant. Voids become large with respect to remaining silicon, forming narrow and isolated “bridges” in extreme cases. As scaling progresses into single-digit micrometer TFTs, the likelihood that individual devices will have differing effective widths increases dramatically, based on their varying fraction of remaining silicon across

an average channel length. The true channel dimensions of heavily void-laden devices are thus difficult to compute.

Chapter 3 discusses various methods to influence the morphology of FLA-crystallized LTPS, including adjustments to FLA intensity, silicon thickness, and modification of film stack. However, the random distribution of voids remains a constant throughout. Without a method of LTPS formation that is predictable and retains integrity, the variance in TFTs produced on this silicon will always be beyond what is acceptable.

Previous research, especially by that of the Ohdaira group at the Japan Advanced Institute of Science and Technology, has shown an underlayer of chromium to be an effective promoter of adhesion FLA silicon crystallization. Using samples of 3-4.5 μm amorphous silicon deposited on 100 nm of chromium coating a quartz substrate and crystallized with a single FLA pulse, they successfully eliminated wide-area silicon ablation and improved energetic response as compared with samples lacking this chromium insert. From here, the authors made numerous further advancements and explorations into this material [42], [48], [49], [80], [135]–[137]. A collage of some important findings of the Ohdaira group are shown in Figure 6.1.

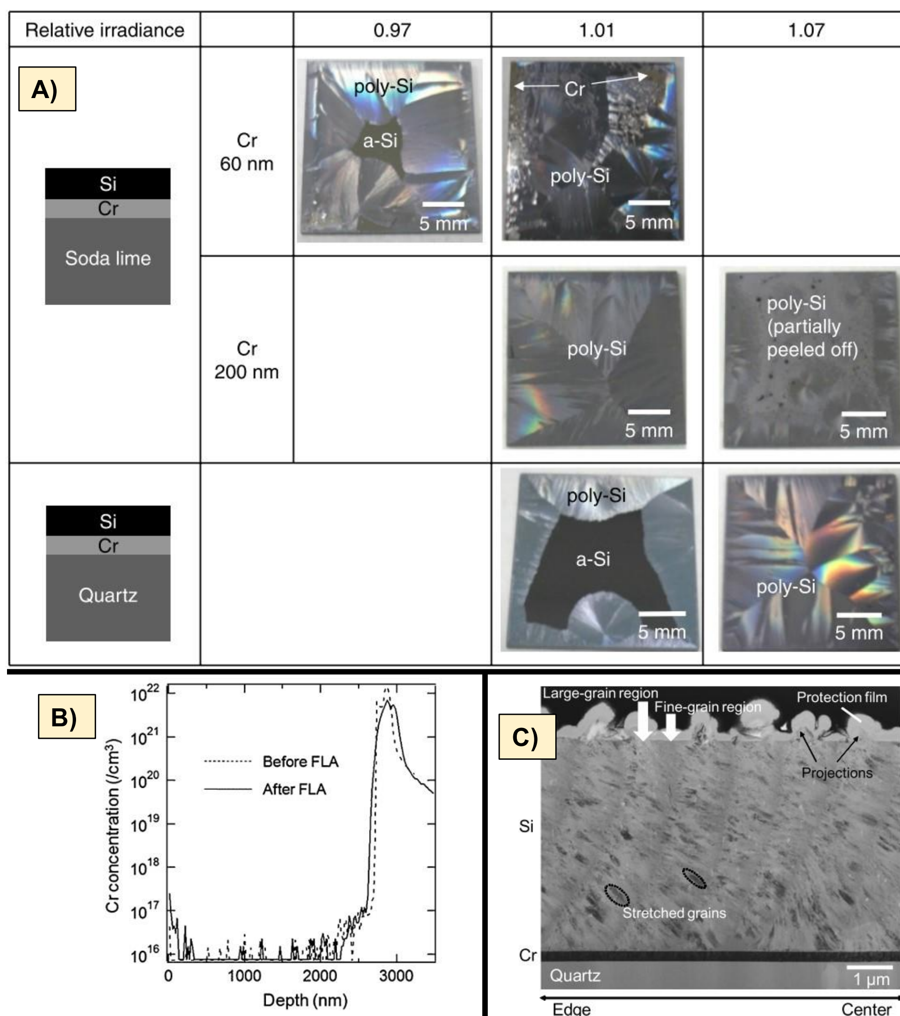

Figure 6.1: Collage of some of the work towards FLA crystallization of silicon performed by Professor Keisuke Ohdaira's research group at JAIST. A) Optical images of large-area 4.5 μm-thick LTPS films on Cr and quartz or soda lime glass crystallized with varying FLA energy densities, from [135]. B) SIMS data of a chromium underlayer used to promote adhesion in 4.5 μm-thick LTPS during FLA, demonstrating a negligible penetration of about 70 nm into the silicon after crystallization, from[42]. C) TEM micrograph of 4.5 μm-thick FLA-crystallized LTPS on a chromium underlayer, demonstrating buried elongated grains and periodic projections perpendicular to the lateral crystallization direction, from [136].

Using SIMS, Ohdaira *et al.* found that their underlying chromium layer had infiltrated the thicker silicon only to the order of ~70 nm, a negligible distance for thick-film applications. This also suggested that the improvements in crystallization were not due to metal-induced crystallization mechanisms, as this would have resulted in metal contamination throughout the silicon or even a metal layer exchange [13]. However, the Ohdaira group's research has been aimed

towards photovoltaic applications, which require a thick body of silicon for optimum absorption. This is in stark contrast to the thin silicon bodies preferable in TFTs to ensure the elimination of the "body effect" which can cause interoperation variations in threshold voltage as well as reduction of body capacitance. A chromium penetration distance of 70 nm may be negligible for an application several micrometers thick, but this same distance would extend fully throughout a 60 nm-thick TFT body such as those demonstrated in earlier chapters. The precise effects and mechanism of chromium in promoting silicon adhesion and generating a unique morphology are thus of interest towards expanding existing research on Cr-backed FLA LTPS photovoltaics into the realm of thin film transistors.

6.2 Thin FLA LTPS with Cr Underlayers

To extend the Ohdaira group's research with chromium underlayer LTPS towards much thinner silicon films, samples were produced in the following method. Glass wafers were coated with PECVD SiO_2 as a barrier, followed by a 6 nm layer of metallic chromium deposited by e-beam evaporation. This thickness was selected as an estimated minimum value necessary to ensure detectable, unbroken, and uniform deposition. Following this, 60 nm of PECVD a-Si was deposited and lithographically patterned into mesas with SF_6 RIE, then coated with an antireflective/capping layer of 100 nm PECVD SiO_2. These samples were crystallized with a single FLA pulse of a variety of intensities.

Crystallization with FLA revealed a marked and surprising difference in morphology, as shown in Figure 6.2. Large, elongated ridges of varying widths from 1 to 8 micrometers were present, forming a periodic pattern that extended perpendicularly away from all mesa edges. This

morphology was termed chromium-enhanced large grain (CrLG) to distinguish it from previous void-associated morphology.

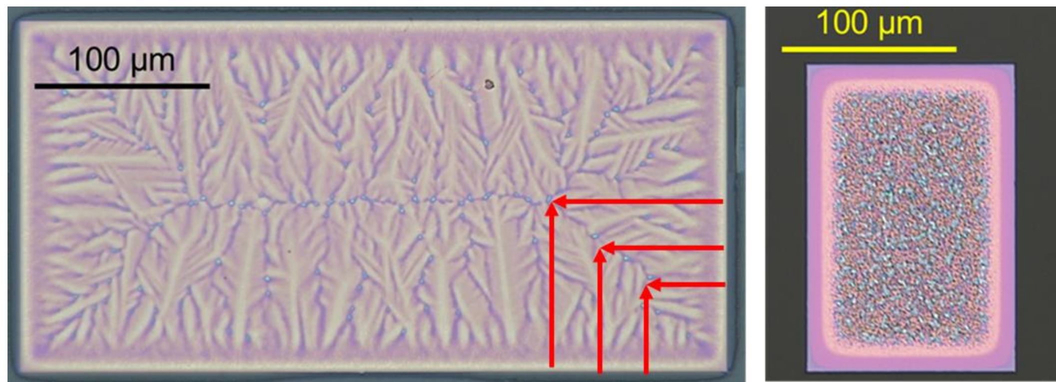

Figure 6.2: Comparison of FLA LTPS mesa crystallized with a chromium underlayer (left) and without (right), both crystallized under the same conditions with a single FLA pulse of 5.0 J/cm^2. Red arrows indicate the apparent direction of crystallization.

This chromium-enhanced large grain (CrLG) morphology is dependent on the geometry of the initial amorphous silicon mesas. Elongated regions form domains that are perpendicular to mesa edges and appear to travel inward, stopping only when they intersect with domains originating from a different edge. On rectangular mesas, a characteristic x-shape forms, while circular mesas form inwardly pointing domains with an elevated center. The orientation, length, and intersection of these grain structures can thus be guided by shaping the mesas prior to crystallization. Figure 6.3 demonstrates several ways in which varyingly-shaped mesas can influence and constrict grain growth, leading to different grain lengths and ridge patterns. For example, the addition of extended prongs to a mesa, as in the star-shaped CrLG formation, may help to constrain the number of initial crystals that form at the perimeter, increasing average grain size by reducing competition.

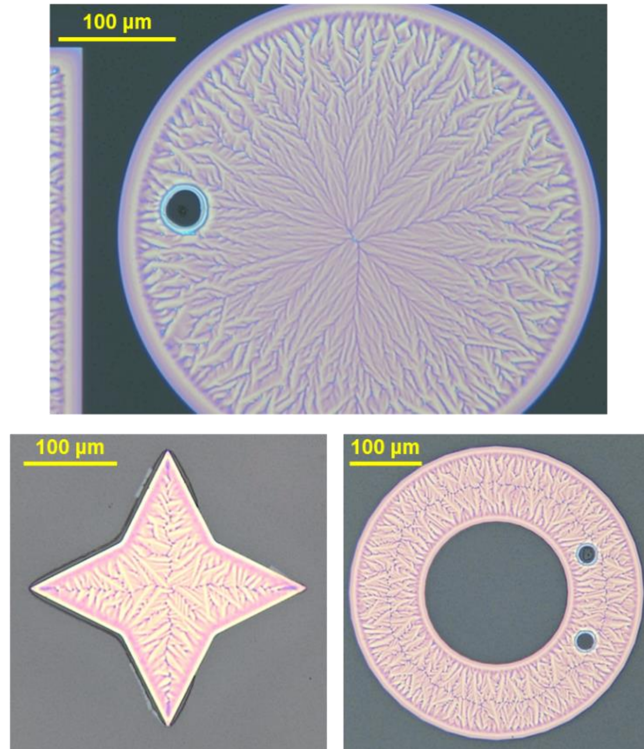

Figure 6.3: Demonstration of CrLG ridge pattern and formation on various shapes of initial crystallization mesa – circular (upper), star-shaped (bottom left), ring (bottom right)

Unlike previous FLA LTPS morphology, CrLG does not demonstrate randomly distributed voids. Where voids form in CrLG, they are on the order of tens of micrometers, often dominating individual mesas. These craterlike voids are far less common than those of void-associated LTPS and likely form at isolated imperfections within the silicon or metal films. An increase in FLA intensity resulted in a higher likelihood of crater void formation, suggesting these features to be caused by excess energy absorption in the thin chromium layer causing rapid localized buckling. Figure 6.4A demonstrates the structure of these voids. Importantly, their formation can be minimized by tailoring pulse intensity to the lowest output that still produces CrLG structure.

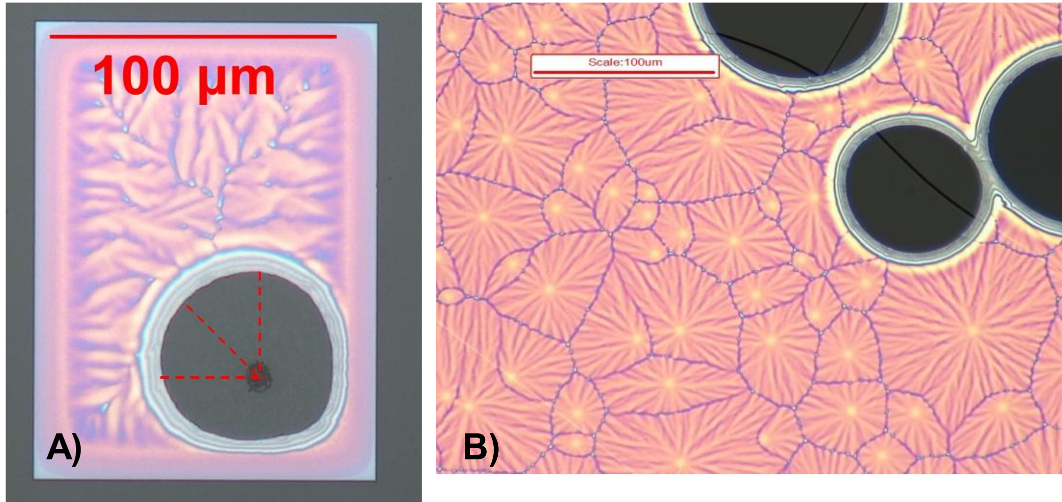

Figure 6.4: A) Demonstration of the pattern of void formation in a CrLG mesa FLA crystallized at 5.2 J/cm^2. A single large void appears to originate from a small defect in its center. The radius of this void is a constant 34 µm in the upwards and leftwards directions; in the other directions it is constrained by the mesa border. B) CrLG structure on a sample that did not undergo patterning into initial crystallization mesas prior to FLA.

Figure 6.4B represents a CrLG sample that did not undergo pre-patterning into initial crystallization mesas. It was instead crystallized as a blanket film and shows a more complicated texture as a result. Without geometric edges at which crystallization fronts can begin to propagate, the process instead appears to begin at random in numerous locations in a spiderweb-like cracking pattern. It is clear that if there are no edges from which these expanding domains can begin, edges will be violently created. However, without chromium enhancement, melt-phase blanket film crystallization is not possible at any FLA pulse intensity attainable with the system used in this research. Pre-patterning is a requirement for the production of void-associated morphology; this is another potential advantage of the inclusion of chromium into the FLA film stack.

The morphology of chromium-enhanced FLA LTPS is certainly not uniform. However, a material that forms nonuniform patterns in a predictable way is far superior in terms of device integration than one with a randomized and unpredictable nonuniformity. Void-associated FLA

LTPS can be tuned to produce more or fewer voids of a larger or smaller size but has little control over the distribution of those voids, and thus how many might be present in a given TFT. CrLG, on the other hand, can be directed in specific repeatable orientations, with smaller regions “cut out” in subsequent lithography and etching steps. This permits the formation of TFTs with parallel grain orientation across the channel and the avoidance of topographical extremes. More refined lithography and scaling techniques than those used in this research could isolate small TFTs onto single grain regions with a high degree of accuracy and confidence.

6.3 CrLG Devices

It is thus shown that a chromium underlayer can engender a new morphology of thin FLA LTPS with far fewer voids. However, its feasibility for electronic applications remains in doubt. Chromium is known to act as a deep-level trap state in the silicon band gap [138], which can compromise TFT operation by promoting carrier recombination within the device channel.

The devices produced in this experiment were PFETs doped via ion implantation and subsequent furnace activation at a 630° C, similarly to the Scalable FLA LTPS experiment shown in Section 4.3. An additional 6 nm chromium underlayer was added between the silicon and barrier oxide; all other processing steps were identical. By selectively carving out different regions of crystallization mesas to become the final device area, three forms of PFETs could be produced in a variety of device dimensions. These were separated based on the orientation of the channel with respect to the prevailing crystallization front direction, as shown in Figure 6.5. Type 1 was termed a Full Mesa (FM) device, Type 2 a With-Grain (WG) device, and Type 3 a Cross-Grain (CG) device.

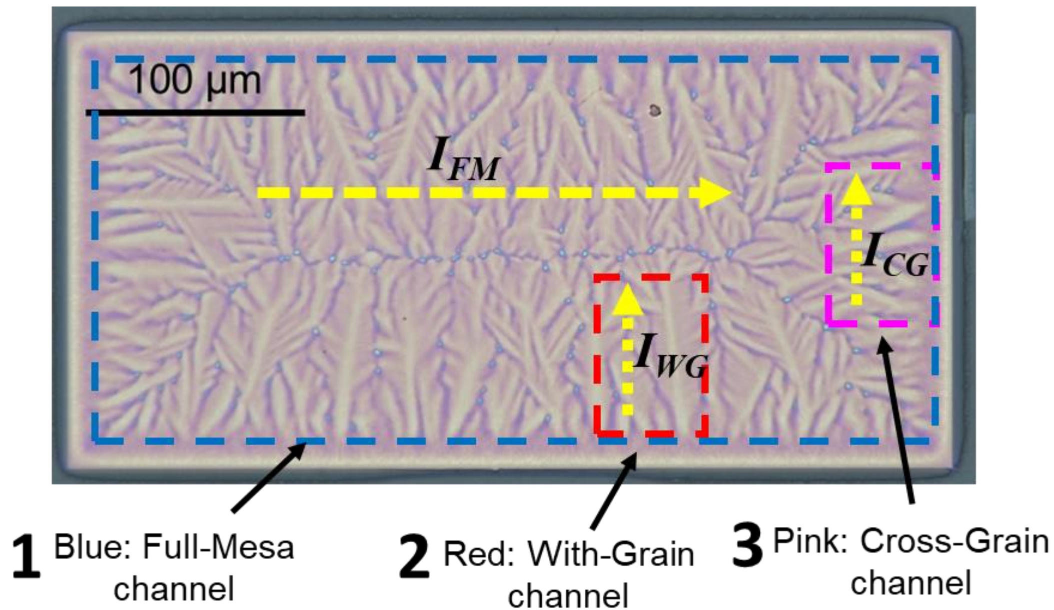

Figure 6.5: CrLG initial crystallization mesa depicting the three types of device channel structure that may be formed from it by lithography and silicon etching (though not all at once, as the full-mesa channel overlaps the others).

Of these, FM is the simplest to process, requiring no silicon etching after the crystallization step. On the other hand, this structure results in multiple directions of grain orientation present in the channel pathway. Figure 6.6D shows an overlay of transistor regions on one such crystallized mesa, where it can be seen that the channel pathway contains both parallel and perpendicular large grains as well as a long intersecting ridge. A sample FM device with length/width dimensions of 96/96 µm is shown in Figure 6.6A The device here has a threshold voltage near -7 volts, which indicates a relatively high level of interface charge. Additionally, these transistors tended to suffer from high leakage current at a drain bias of -10 V. Such issues are a common downside of LTPS devices which are exacerbated by the presence of active dopant segregation in grain boundaries; as a higher density of grain boundaries are present, the level of leakage can be expected to increase.

Figure 6.6B demonstrates the reproducibility of this device structure. The variability is quite low among twenty devices of the same dimensions as 5a, especially in on-state operation. The off-

state leakage behavior is not as consistent, with the variation most likely associated with the mechanism responsible for the enhanced magnitude. Figure 6.6C demonstrates the low drain bias operation of the device. Using the maximum transconductance method, a channel mobility of 35 $cm^2/(Vs)$ can be extracted.

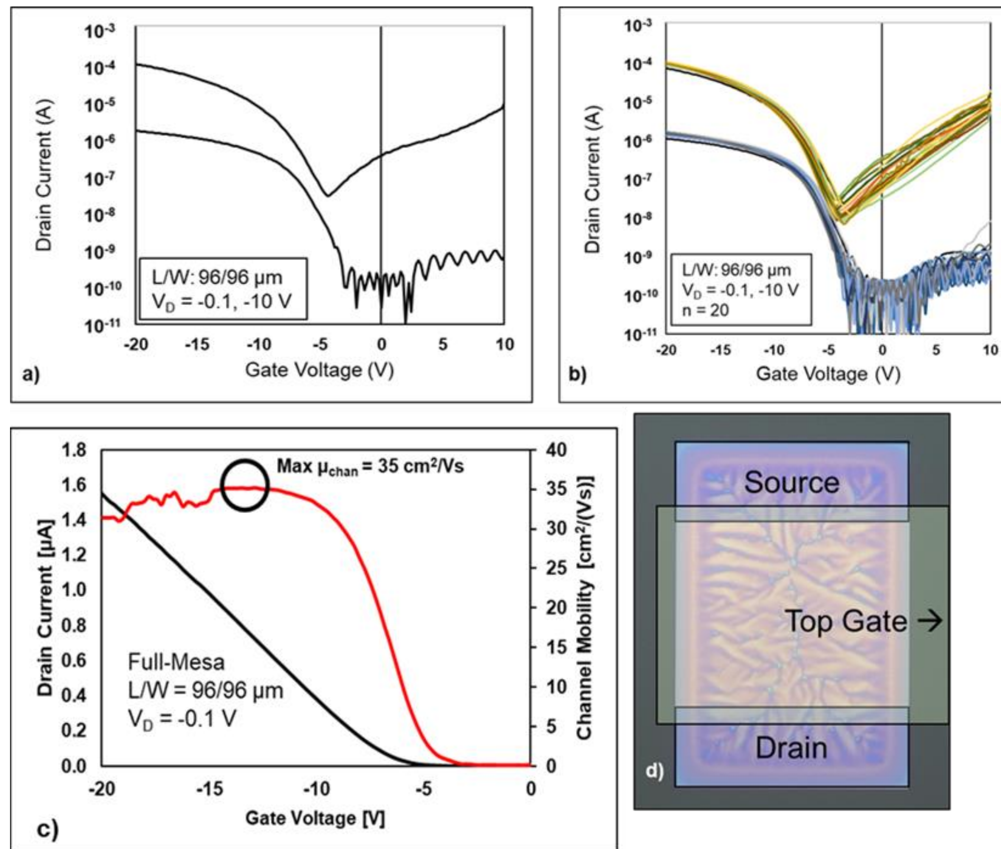

Figure 6.6: a) Transfer characteristics of a typical FM style transistor of L/W = 96/96 µm. b) Overlay of transfer curves of 20 such transistors. c) Linear-scale low drain bias and extracted channel mobility. d) Micrograph of FM-style structure indicating overlay of source, drain, and channel regions. Published in [139]

The effect of parallel vs perpendicular grain structure was investigated by producing TFTs of both WG and CG variety and identical dimensions. Figures 6.7A and 6.7B demonstrate these two schemes; of important note is the general direction of grain boundaries in between the source and drain shaded areas, as the channel is defined by the space between these wells. The CG structure

is thought to contain more boundaries that interfere with the flow of current, causing scattering events that impede carrier mobility. The WG structure, on the other hand, may have single grains that bridge the entire channel.

Figures 6.7C and 6.7D demonstrate the operation of a typical pair of such devices. Again, both suffer from a high leakage current at a drain bias of -10 V, mirroring the issues of the full-mesa device above. Interestingly, the lowest current attainable was nearly an order of magnitude lower for the WG device than the CG at high V_{DS}. Additionally, the switching characteristics of CG devices appeared "lumpy" and variable, as if they were a composite of many devices that exhibit slight differences in threshold voltage and subthreshold slope. This behavior is not seen in the WG devices, which have a generally higher transconductance and more closely resemble a bulk silicon transistor. Using the same maximum transconductance method, a maximum channel hole mobility of 34 and 31 $cm^2/(Vs)$ was extracted for these WG and CG devices, respectively.

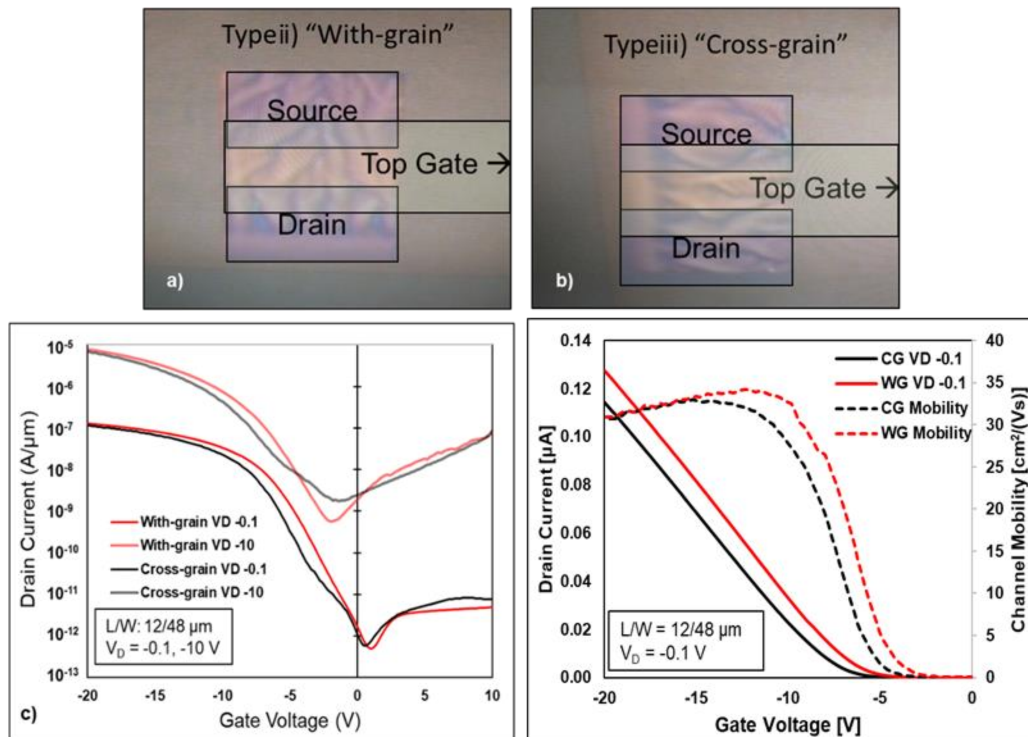

Figure 6.7: a) Micrograph of WG channel structure, highlighting the parallel direction of grain boundaries in the channel. b) Micrograph of CG channel structure, highlighting the perpendicular direction of grain boundaries in the channel. c) Transfer characteristic overlay of a typical pair of WG (red) and CG (black transistors of the same dimensions and processing history. d) Linear scale low-drain behavior of the device in c) and extracted carrier channel mobility.

It is clear from this experiment that chromium-induced, edge-directed FLA LTPS can be used to produce functional thin film transistors in spite of the conductive metallic underlayer used to aid in adhesion during crystallization. However, a significant amount of off-state leakage becomes apparent at high drain bias. This effect may be due to chromium contamination of the semiconductor channel, prompting further investigation into the distribution and behavior of the underlying metal during and after crystallization.

6.4 CrLG Material Characterization

The structure and surface texture of CrLG immediately after crystallization was further analyzed with Atomic Force Microscopy (AFM). A Bruker Multimode 8 AFM tool was used with antimony-doped silicon tips in tapping mode to reduce the strain caused by significant, clifflike variations in texture. Figure 6.8 shows an AFM scan of the central region of a mesa, demonstrating the variation in height between large visible ridges and the surrounding troughs. This texture is too pronounced to be interpreted as surface roughness.

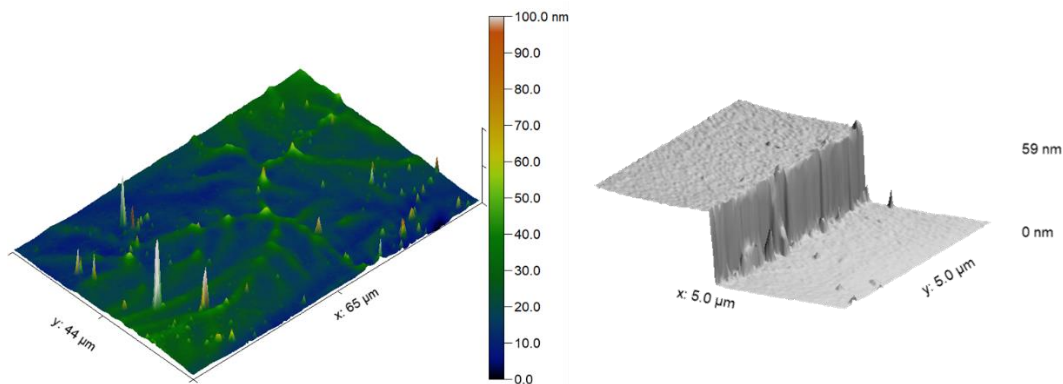

Figure 6.8: Left: Isometric AFM image of a CrLG mesa, showing texture in relief. Right: Absolute height of a mesa edge.

The rightmost image of Figure 6.8 demonstrates the absolute height of the mesas in a "stairstep" fashion. At the edge of each mesa there is an exclusion border of limited texture change, suggesting that melting may not have taken place across the full area. This stairstep has a total height of 59 nm, which indicates that the variations in height and corresponding variations in mass of the high peaks and ridges towards the center does not come from a loss of mass throughout the volume of the mesa, at least at the edges.

Closer inspection of the surface with AFM, shown in Figure 6.9, reveals the presence of a nanometer-scale texture distinct from the elongated grains and ridges that form the micrometer-scale texture. A pattern of trenches emerges, with rows of parallel voids between 20 and 70 nm in diameter. The depth of these voids cannot be adequately measured using AFM due to the curvature of the probe tip, but they extend at least 15 nm into the sample. Figure 6.9A-B shows this higher-resolution AFM scan in two different contrast scales to demonstrate that this "nanoscale" texture is simultaneously present within the "microscale" ridges and localized peaks. The nanoscale texture is not visible with optical microscopy.

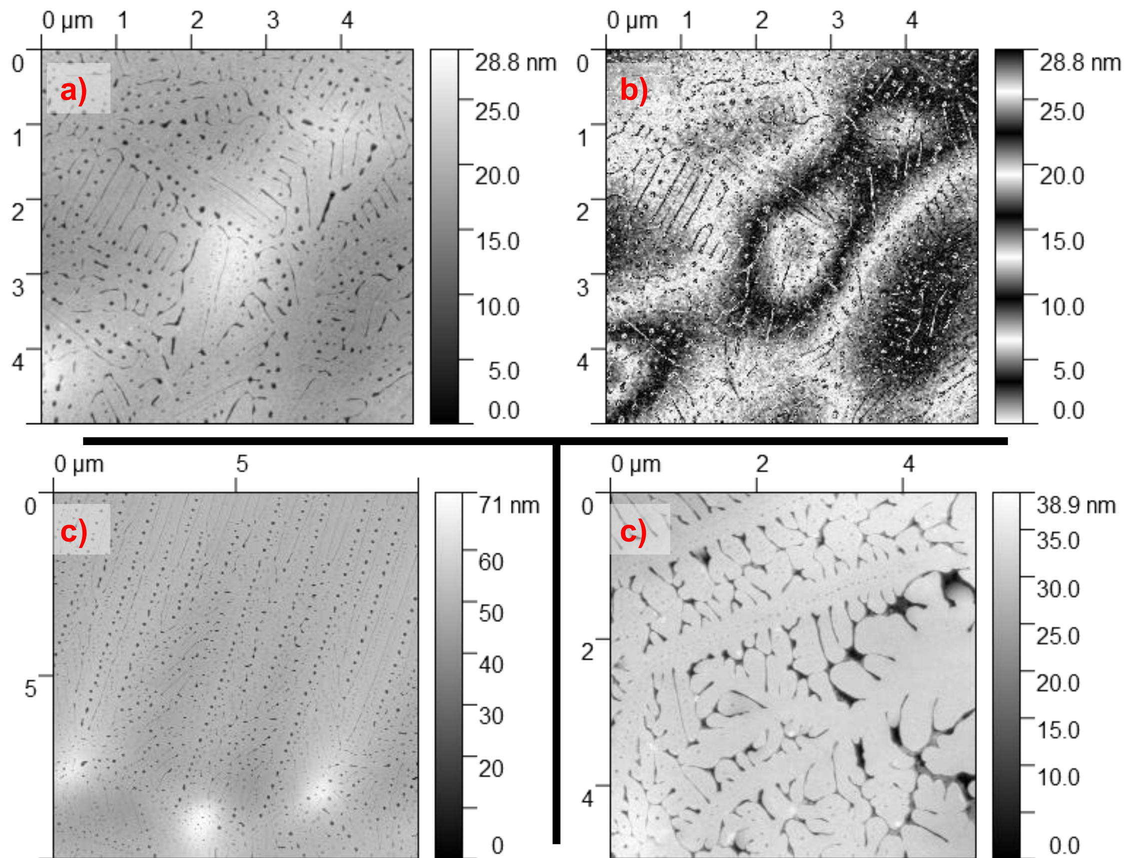

Figure 6.9: a) and b): A high resolution AFM image of CrLG in two different contrast scales, highlighting the non-interacting presence of both microscale and nanoscale texture simultaneously. c) CrLG AFM image showing a region of parallel trenches extending more than 10 µm. d) AFM image near the border of the CrLG mesa, showing the

transition into parallel trenches.

These “nano-voids”, with diameters of < 50 nm, are present all throughout the CrLG nanoscale texture, generally as a long chain of periodic voids equidistant between two trenches. Large domains of repeating parallel trenches and nano-voids are often visible in the nanoscale AFM texture. In some areas, these trenches extend beyond the bounds of the scan, at least 10 μm in length as shown in Figure 6.9C. The full extent and average size of these trench-bounded regions is difficult to measure. Towards the edge of a CrLG mesa, this pattern begins to break down and form a messy transition area as in Figure 6.9D. Here, some elongated parallel lines of nano-voids protrude into an area with no long-range patterns.

This surprising nanoscale structure is confirmed with scanning electron microscopy (SEM). CrLG mesas were imaged with TESCAN Mira3 SEM with a LaB_6 field emission source. Some samples were sputtered with gold for conductivity, though in most cases, the remaining chromium underlayer provided sufficient electron conductivity that a conductive sputter was not necessary. Figure 6.10 shows a high-resolution image of two areas of the same sample imaged with secondary electron SEM at ~65 kX magnification, showing a series of patterns similar to those presented through AFM. Regions of repeated, parallel trenches are visible, interspersed with rows of dark circular spots identifiable as the nano-voids from AFM. Most notably, there is an additional pattern of local high-contrast spots that tends to form in the same general region as the nano-voids between the parallel trenches, However, the nano-voids and high-contrast spots, henceforth called “bright dots”, differ in repeated frequency and apparent size. Additionally, a shadowy halo-like feature could be seen surrounding some voids and trench termina in a sparse and seemingly random distribution. These new features are not visible in AFM images, implying that they do not

contribute to the roughness or texture of the sample. They are likely confined to the subsurface region of the samples.

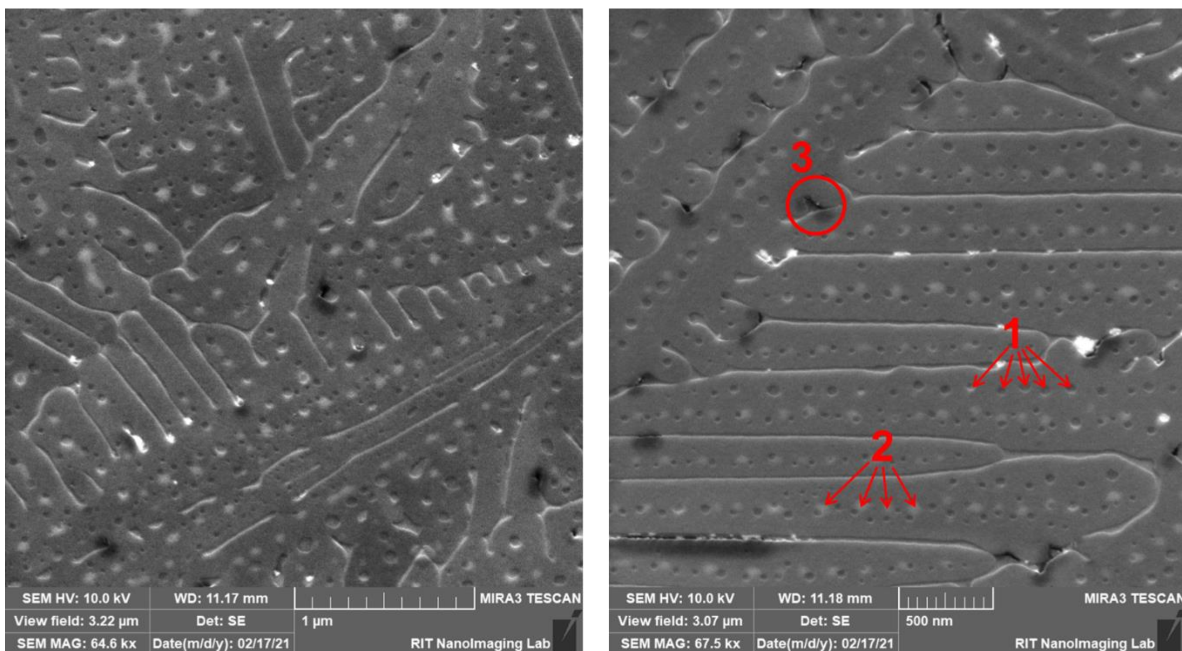

Figure 6.10: Left: High resolution SEM image of a CrLG mesa, showing not only nano-voids and trenches but also periodic "bright spots" as well as occasional dark, shadowy "halo voids". Right: another SEM image of a different region with callouts to 1) nano-voids, 2) bright dots, and 3) halo-voids. Sparse very bright specks indicate incompletely removed gold flakes.

In this case, the samples were previously sputtered with gold and then imaged in areas where the gold had flaked off, providing a convenient balance between high resolution, and charging reduction. This is not a standard method of SEM imaging and would be difficult to replicate in the future. Very bright specks indicate areas of remaining gold flakes.

Several variations of the CrLG-producing film stack were produced and crystallized via FLA and are demonstrated in Figure 6.11. One such film stack used chromium as an overlayer rather than an underlayer, with all other aspects and dimensions remaining the same. This modified

sample structure produced edge-directed CrLG morphology that has a strong optical resemblance to the underlayer samples detailed above. AFM imaging of this material was impossible due to probe damage caused by a combination of the extreme surface roughness and the relative hardness of the exposed chromium surface to the Sb-doped silicon probe tips.

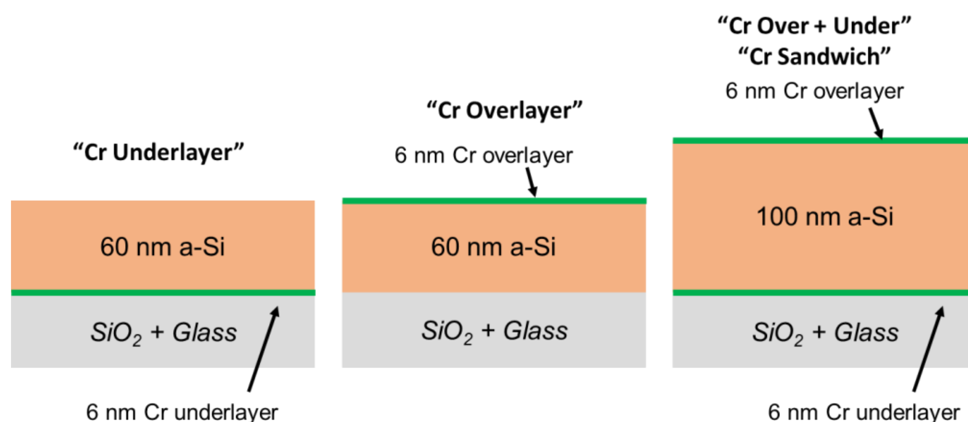

Figure 6.11: Depiction of three CrLG film stacks used in this analysis: Cr Underlayer, Cr Overlayer, and Cr Over+Under (or Cr Sandwich)

A cross-sectional sample of this material was inspected via transmission electron microscopy (TEM) to provide a clearer view of the distribution of chromium within the thickness of the silicon. The microscope used was a FEI Titan G2 80-200 kV ChemiSTEM system. Figure 6.12 demonstrates the TEM cross-section of this modified material stack in high-angle annular dark field (HAADF) imaging mode. A thin layer of intact chromium remains on top of the mesas, visible as a bright line contrasting with the dark carbon protection overlayer, added for sample preparation. However, there are several isolated regions in which metal appears to penetrate significantly into the semiconductor, forming shallow domes extending roughly 25-40 nm deep from the overlying layer. The diameter of these domes corresponds roughly to those of the bright dots visible in SEM images of underlayer-CrLG, if a random cross-section was to be taken through them. Additionally, evidence of chromium can be seen on the distal lower interface between the silicon and SiO_2

underlayer. This suggests that a full diffusion of chromium through the silicon occurs during its melt transition, after which the metal aggregates at interfaces.

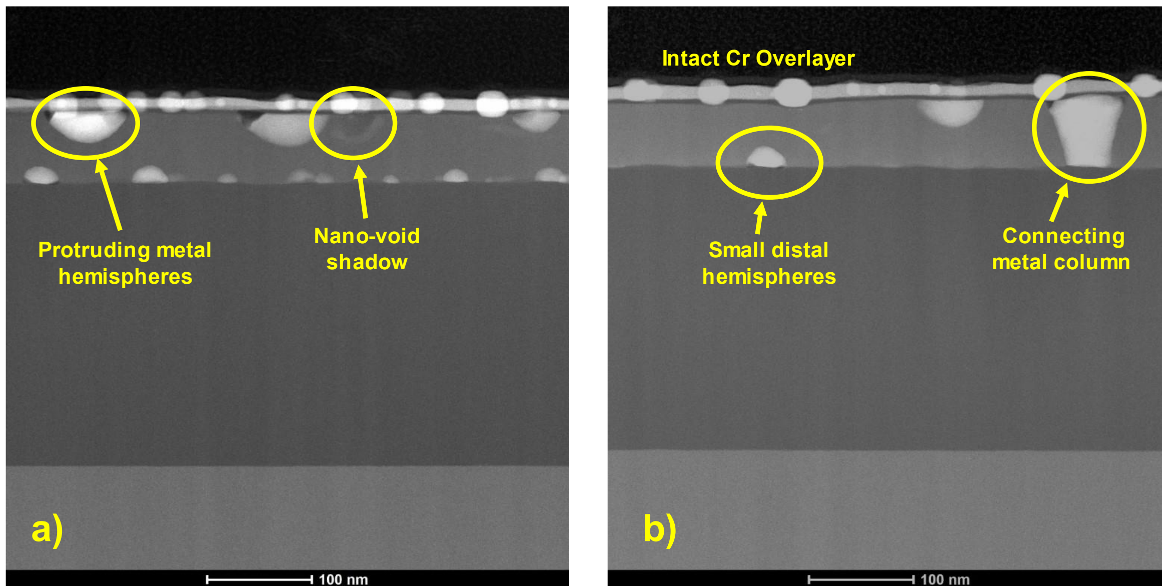

Figure 6.12: TEM images of Cr Overlayer CrLG mesa in two different regions of the same sample

A few uncommon events were also present in some areas. Figure 6.12A shows a faint shadow that may be the projection of a nano-void in the cross section, suggesting that they too do not extend all the way through the silicon thickness. Figure 6.12B shows a "column" of chromium extending fully from the top metal to the bottom oxide interfaces. This may indicate the coincidence of a chromium-rich bright dot near a void or a deep trench in the mesa, proving that there is certainly some distribution of metal throughout the silicon mesa, though it is rare.

Figure 6.13 shows a bright-field TEM image of a different area in the same sample which appears to include a grain boundary with different structures of silicon on either side. The left side shows distinct rows of crystal planes in a single, uniform phase, while the material directly to the

right of this boundary has very little apparent order. The quasi-randomness suggests a surviving area of amorphous silicon directly influenced by a nearby grain boundary [140].

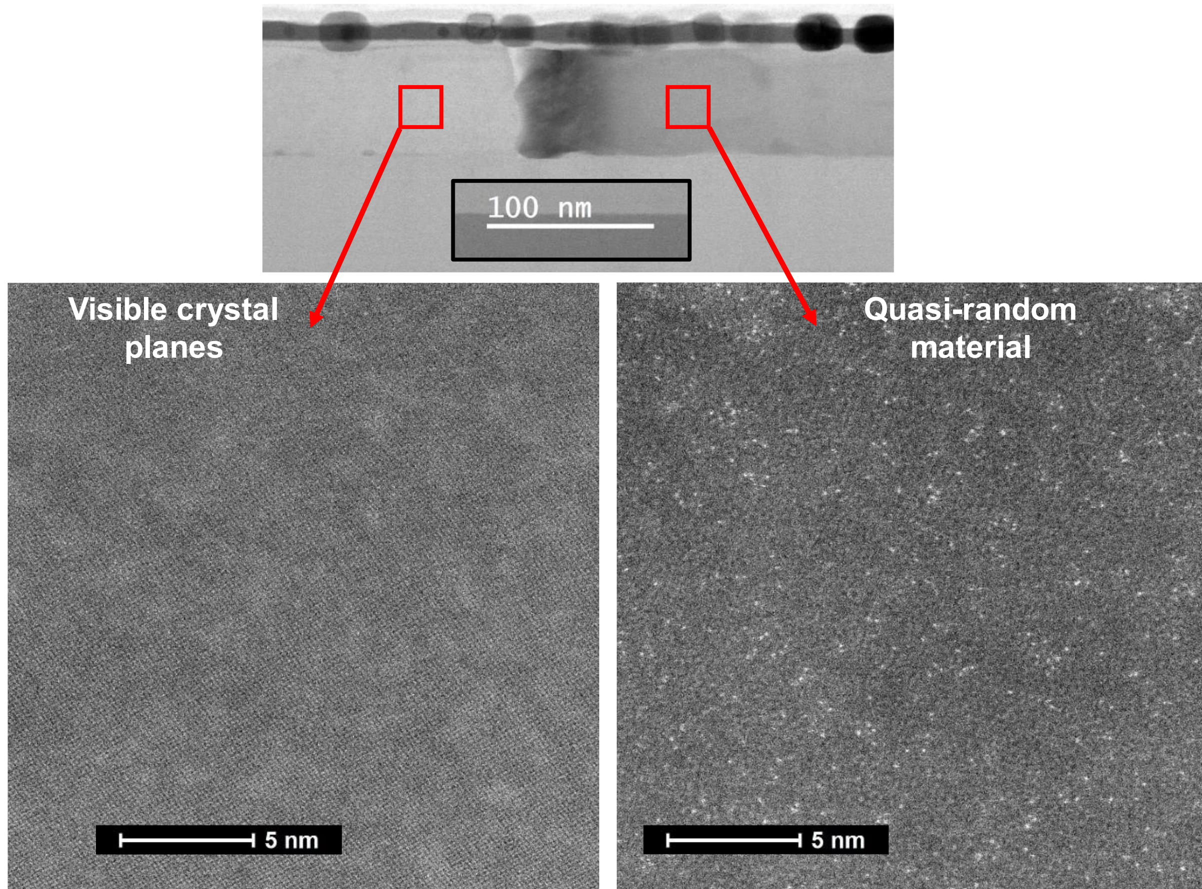

Figure 6.13: TEM of Cr Overlayer CrLG mesa showing the impact of a grain boundary on the surrounding silicon. To one side of the sharp boundary, silicon is visibly crystalline, but it becomes disordered and amorphous on the other side.

Energy-dispersive x-ray spectroscopy (EDS) confirms the identity of the bright metallic regions within the film stack to be chromium. The solid solubility limit of chromium in silicon is below the detection limit of EDS, meaning that an electrically-significant contamination within the semiconductor body is not ruled out by a failure to detect chromium there. Figure 6.14 shows EDS mapping of TEM images of the chromium-overlayer sample, comparing the relative density

of silicon and chromium in various regions within the stack. Both the bright interfacial protrusions and the intact overlayer register strongly as chromium, with no measurable signal anywhere else. Interestingly, the silicon-associated EDS signal is also uniform within the LTPS layer of the stack rather than being diminished in areas that show chromium protrusions. Since these protrusions are anticipated to be hemispherical in the z direction, have a diameter of at least 80 nm, and occur within a TEM sample that is less than 200 nm thick, this implies that the protrusions themselves likely also contain a significant quantity of silicon rather than being purely metallic. Chromium is known to form a variety of silicides: Cr_5Si_3, CrSi, Cr_3Si, and $CrSi_2$ [141]. All of these have a melting temperature much greater than that of a-Si and are thus thermodynamically favored. The proportionate stoichiometry cannot be estimated from this EDS data, but multiple species are likely to form.

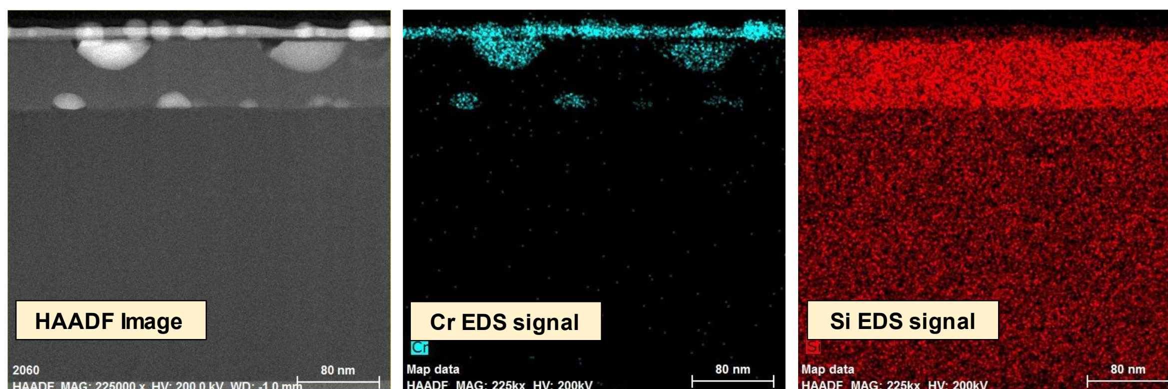

Figure 6.14: EDS signal of Cr Overlayer CrLG TEM, confirming the presence of chromium in the bright protrusions at the silicon interface.

This information was compared with EDS analysis from SEM imaging on Cr Underlayer samples for a confirmation of lateral chromium distribution across a sample. The primary EDS electron transition voltage for oxygen, O:Kα at 0.525 KeV, overlaps with chromium's strong Lα signal at 0.573 KeV, so the much weaker Cr:Kα peak at 5.41 KeV was used to differentiate the

elements. The > 16.2 KeV microscope overvoltage needed to effectively resolve this peak proved an obstacle to resolving the extremely high magnifications needed to differentiate these nanoscale features, rendering a full spatial EDS map impossible. Instead, numerous short scans were taken on several instances of individual nanofeatures, which were normalized to the nearby Ba:Lα peak found uniformly throughout the glass substrate. A normalized comparison of the chromium EDS signal between different features is shown in Figure 6.15.

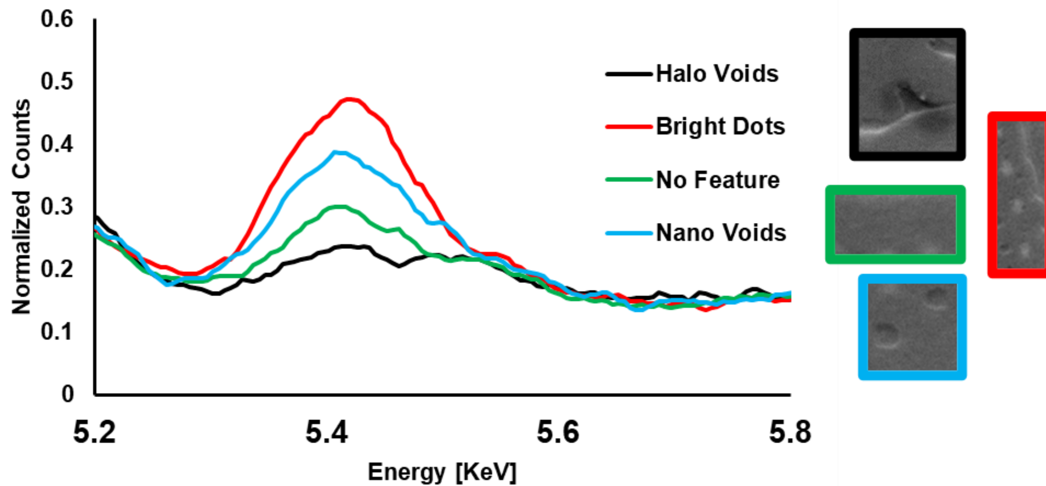

Figure 6.15: Comparison of chromium EDS signal, normalized to a nearby constant, between various nanofeatures (and a baseline "no feature" area)

From this graph, it is clear that there is a significantly higher chromium signal in scans that are limited to the "bright dot" nanofeatures than in other areas. This suggests that the regular pattern of bright regions in SEM corresponds with the occasional hemispherical protrusions of chromium at the interfaces shown in TEM images. Nano-void features also had a higher chromium signal when compared with regions selected due to no visible nanofeature presence ("No Feature" on Figure 6.15), suggesting that the underlying chromium layer is masked by less silicon in these

places. The lowest chromium signal of all was found in halo-void regions, implying that the underlying chromium is damaged or fully ablated in these places. Figure 6.16 provides a cartoon illustration of this hypothesized cross-sectional structure.

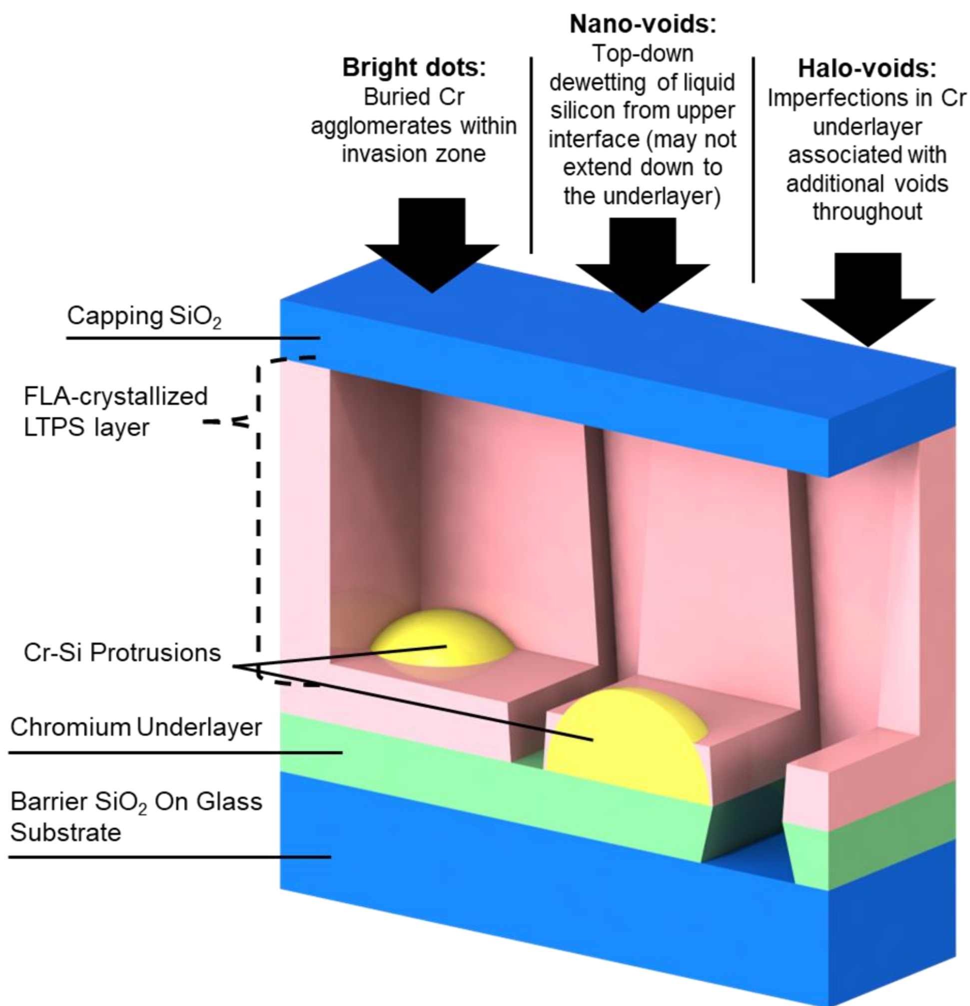

Figure 6.16: Cartoon demonstrating how each nanofeature visible in SEM and AFM manifests from a cross-sectional perspective of a Cr-underlayer mesa structure.

The universal and self-propagating pattern of trenches and voids within CrLG suggests it to be a response to internal factors within the material during formation, unrelated or only marginally related to the geometry-dependent microscale grain morphology. The formation of these recessed

patterns is most likely related to the balancing of strain within the various domains of the material during crystallization. Parallel trenches are produced along the edges of protruding polycrystalline grains acting as slip planes where the tensile strain in the crystalline lattice overcomes the energetic barrier needed to dislocate. This is displayed as a series of lateral "cuts" into the crystal structure, likely in crystallographically significant angles away from the direction of grain formation.

Nano-voids form once there is a critical area of unbroken surface at the silicon-capping oxide surface, causing a buildup of surface energy from an unfavorable interface. The rapidly solidifying liquid silicon pulls away from this upper interface, resulting in small divots which do not extend through the entire layer because the silicon-chromium lower interface is much more thermodynamically favorable. As the parallel trenches also result in a broken interface, the nano-voids are automatically confined into the median between trenches, though the mechanism of formation is different. Therefore, lattice strain, a 3D bulk property, is relaxed through the formation of 2D trenches along grain edges, while high surface energy, a 2D interface property, is mitigated through the formation of 1D pits.

6.5 CrLG Post-Process Structure

Unlike the prepared as-crystallized samples imaged in section 6.4 for material analysis, the devices presented in section 6.3 experienced several processing steps that could have potentially altered the distribution of chromium within the silicon stack. After crystallization, areas of the devices were implanted with boron ions, then subjected to a twelve-hour furnace anneal at 630 °C furnace anneal to activate these dopants, in addition to many other, less invasive procedures. To explore and compare the impact of these steps, a sample of completed and functional TFTs were deprocessed by removing the metallization with aluminum etchant and the gate dielectric with

BOE. These "post-process" samples, formerly functional devices, were analyzed with electron microscopy to compare with "as-crystallized" samples.

It became immediately clear that post-process samples lacked the global conductivity that allowed as-crystallized samples to be properly imaged in an SEM; charging effects due to electron trapping dominated and resolution became impossible. This suggests that some stage of TFT processing or deprocessing interferes with the intact conductive chromium layer underneath the mesas and throughout the sample, thus allowing devices to function as transistors rather than thin metal resistors. After a thin gold sputter, post-processing samples could be effectively imaged with SEM. Figure 6.17 shows these results in various regions and magnifications.

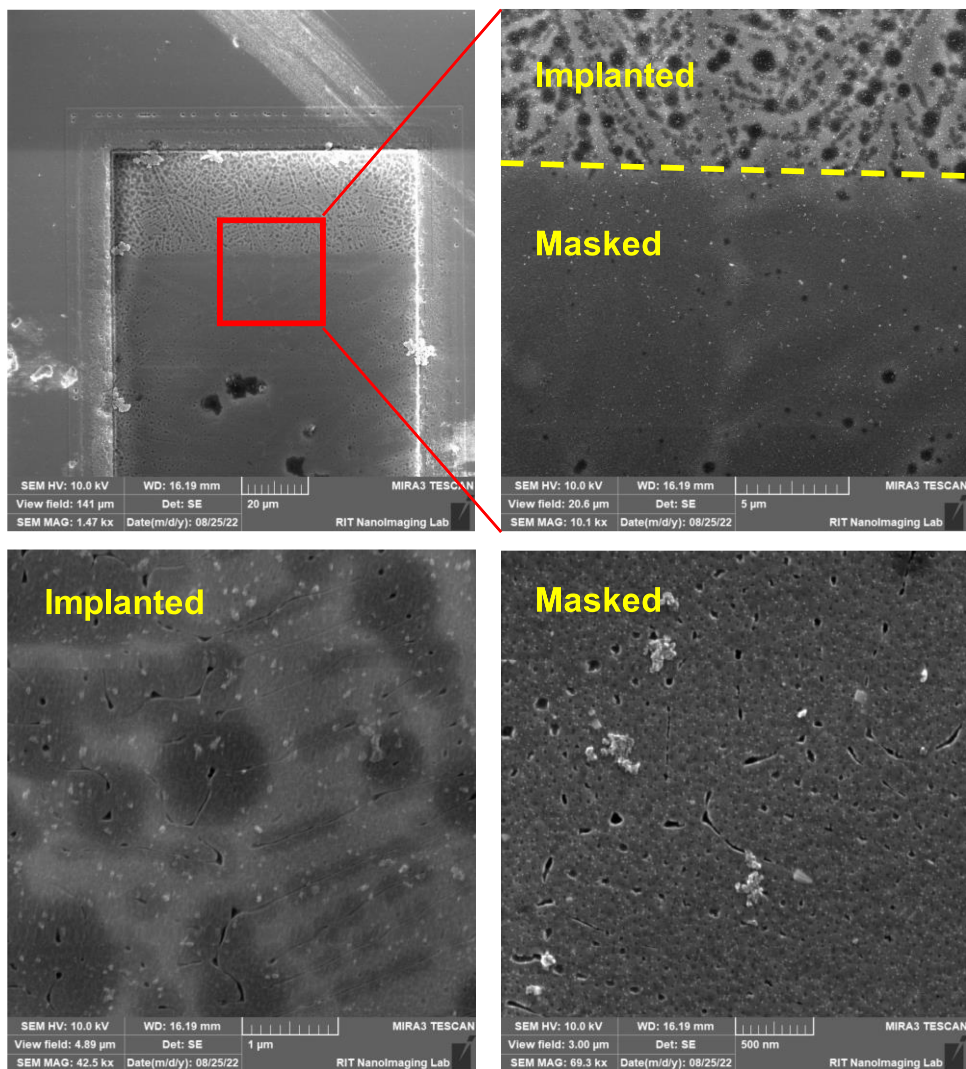

Figure 6.17: SEM images of a post-processing Cr overlayer CrLG mesa. Upper Left: Wide-area image highlighting the difference between ion implanted source/drain and masked channel. Upper Right: Higher magnification of that same boundary. Lower Left: Region subjected to ion implant. Lower Right: Channel region, shielded from ion implant.

There is a stark contrast in the material of Figure 6.17 between regions which had been masked during ion implantation and regions which were fully implanted. Implanted regions showed a marked increase in halo-style voids, visible as circular shadows surrounding nearly every intersection of trenches. This pattern was not visible in areas that had been shielded from ion implant, suggesting that this change is brought about by damage to the thin metal underlayer

caused by kinetic impact. Areas that are sufficiently damaged may then become origin points for further loss of chromium in the subsequent furnace anneals. Crucially, neither masked nor implanted regions displayed the regular pattern of bright dots identified as chromium aggregates in the as-crystallized samples. This is unlikely to be caused by shadowing from the conductive sputter, as the increased halo formation in the implanted regions is so clearly visible. Rather, this suggests that chromium distribution following a moderate-temperature anneal is significantly impacted in all regions of the CrLG LTPS.

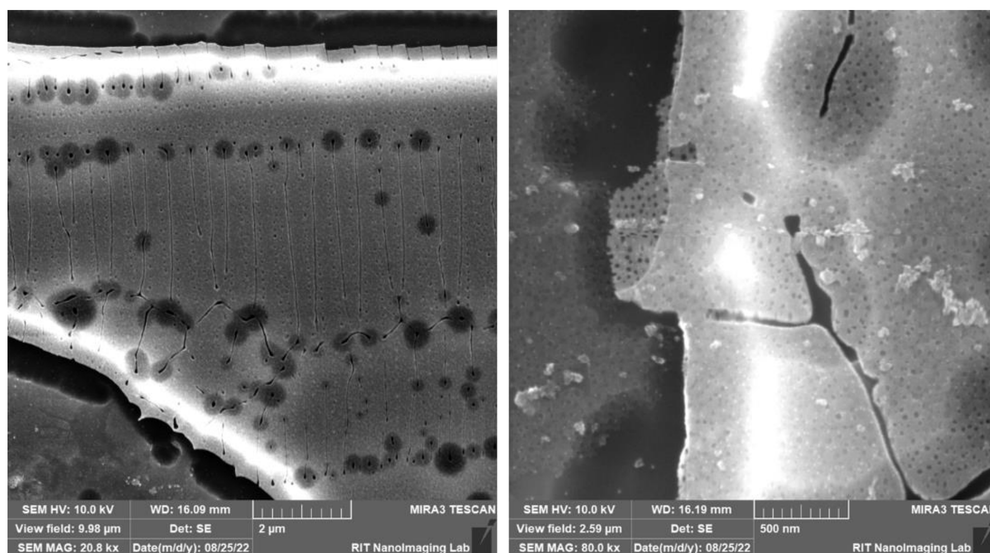

Figure 6.18: SEM images of a post-processing Cr Overlayer CrLG sample, focused on borders of mesas that have been etched after crystallization. A frayed and jagged edge is visible around the ends of cut-off elongated trenchs.

Figure 6.18 demonstrates the impact of etching CrLG mesas into smaller mesas after crystallization. With sufficient magnification, the edges of etched mesas show a jagged pattern with occasional protrusions that follow the nanoscale domains of individual trenches and columns. This is unlikely to be caused by the lithographic patterning, which projects straight lines. Rather,

the resilience of the CrLG material to the SF_6 RIE varies locally, based on the proximity of nearby trenches. RIE is known to etch amorphous phases much more quickly than crystalline [142]; it is possible that the interfaces between elongated trenches have a higher amorphous content.

TEM analysis of these deprocessed samples confirms a change in structure and metallic distribution after TFT processing steps. Figure 6.19 demonstrates TEM of a post-process Cr Overlayer sample that experienced additional thermal steps but was masked from ion implant. Where previously there had been intermittent hemispherical metallic protrusions extending from the chromium overlayer, the high-contrast chromium signal is now sparsely distributed along the lower stratum of the silicon layer on the opposite interface. The material forms rounded agglomerates that appear discrete and separate from the interface, extending some 25-35 nm into the silicon layer. These agglomerates show crystal planes and have both a strong Cr and Si EDS signal, implying a silicide structure. Meanwhile, the overlayer remains consistent and intact at the upper interface, still in a visibly amorphous state.

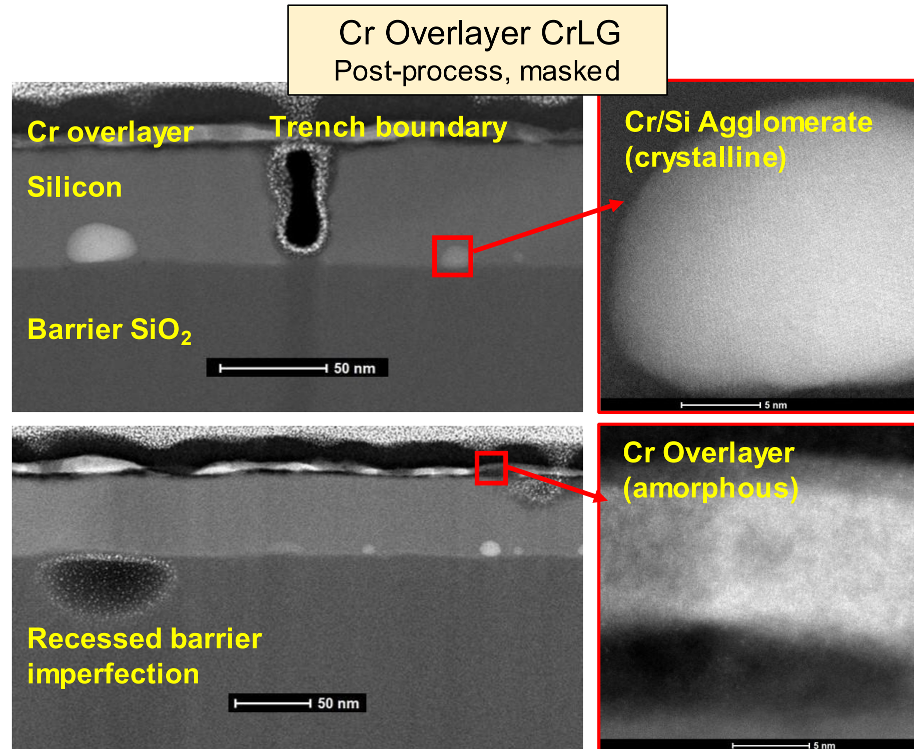

Figure 6.19: Left: TEM images of two regions of a post-process Cr Overlayer CrLG film stack protected from ion implant, showing that the hemispherical protrusions have fully redistrubted into a layer of sparse, discrete agglomerates. Upper Right: Closeup TEM of a single agglomerate revealing crystal planes. Lower Right: closeup TEM of remaining Cr overlayer film.

Some imperfections in the film stack are visible in this TEM analysis, though they are uncommon. Within the silicon layer, there is a narrow 10-15 nm-width gap extending almost throughout the full thickness of the film. This area shows no significant EDS signal of any of the elements relevant to the system, implying a void within the material. This may be the cross-section representation of a nanoscale trench extending perpendicularly out of plane. Additionally, a wide 70 nm recessed void is visible within the SiO_2 barrier, potentially the result of an overzealous capping oxide etch interacting with a pathway through the LTPS.

Areas of post-process Cr Overlayer samples that were exposed to ion implant in addition to subsequent thermal steps were difficult to image, due to unexpected enormous, micrometer-scale

voids extending throughout the barrier SiO_2 and even well into the glass, as shown in Figure 6.20. This is likely the cross-section representation of the proliferation of halo-voids within implanted regions. However, the silicon film, chromium-rich agglomerates, and chromium overlayer were not affected by these sublayer caverns and appear similarly to their counterparts in the masked area. From this, it can be concluded that the operation of Cr overlayer devices is not impacted by the numerous halo-voids in implanted areas; these may be caused by an error in sample preparation.

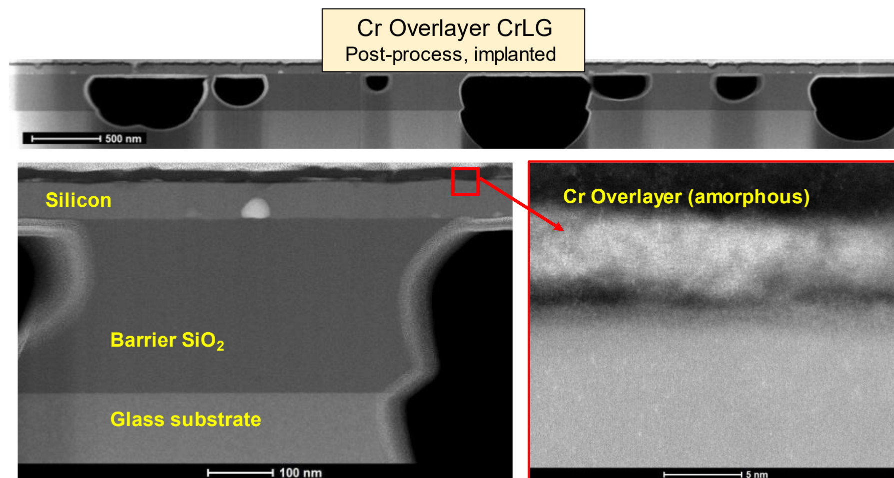

Figure 6.20: TEM images of a post-processing Cr Overlayer CrLG film stack exposed to ion implant, showing a similar structure as the masked region in addition to enormous voids in the SiO_2 barrier and glass.

TEM revealed a markedly different structure in post-process CrLG produced with a Cr Underlayer film stack, as shown in Figure 6.21. Similar to the overlayer sample, there is no evidence of hemispherical metallic protrusions from the thin chromium film, but rather a layer of discrete chromium-rich agglomerates. However, the Cr Underlayer structure shows this agglomerate region to be clustered near the lower Si-Cr interface as opposed to on the opposite interface. Additionally, these bodies are far more numerous and randomly clustered than either the hemispheres or the overlayer-associated agglomerates. Most of the agglomerates again appear to

be fully detached from the interface and extend 25-35 nm into the silicon layer. These agglomerate regions display visible crystal planes, in sharp contrast to the indistinct silicon bulk immediately surrounding it.

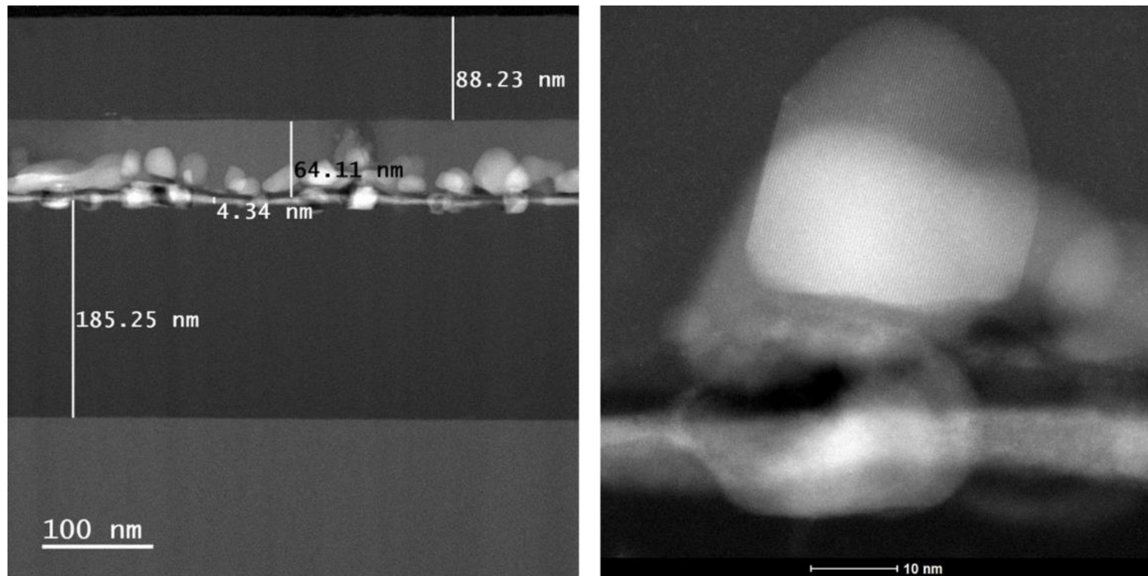

Figure 6.21: Left: TEM image of a post-process Cr Underlayer CrLG film stack, showing that chromium intrusion into the silicon layer has reorganized into a region of small, discrete agglomerates. Right: Close-up TEM of a single agglomerate revealing crystal planes.

EDS analysis of post-process TEM structures clearly identifies the high-contrast agglomerations as being rich in chromium. In addition, there is an intact chromium underlayer between 4 and 6 nm in thickness that has survived both implantation and anneal. In SEM imaging, as in Figure 6.16 above, there were numerous areas that appeared to show damage to this layer, but they are not visible from a cross-sectional view. Additionally, a small but significant chromium reading is present at the upper interface between the silicon and the capping SiO_2, suggesting that chromium is diffusing throughout the entire mesa and lightly precipitating at this interface. From this it can be further confirmed that the silicon is broadly contaminated with metal. However, the

localization of chromium to the far surface of the silicon also suggests that it is segregating out of the liquid solution at this interface, which may act as a refinement process to reduce the chromium concentration to its level of solid solubility in silicon.

EDS confirms that these new agglomerate features are rich in chromium, as in Figure 6.22. The sparse nano-void structures visible in SEM are still present after post-processing, shown as a round ~50 nm divot into the upper interface of the silicon layer which is filled in by SiO_2 from the conformal dielectric deposition. However, there are no visible agglomerates far from the Cr/Si interface, even though as-crystallized TEM shows Cr signals on the far interface as well.

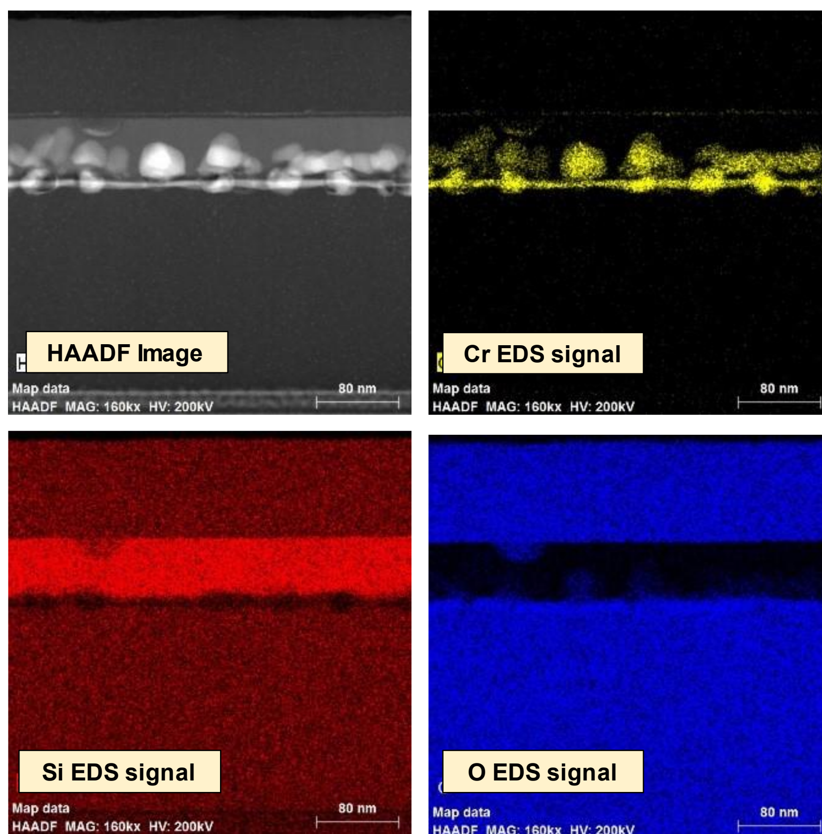

Figure 6.22: TEM EDS of post-processing Cr Underlayer CrLG sample, confirming the agglomerate layer to be rich in chromium. Ntoe the nano-void divot on the upper left of the scan, which has a stronger oxygen signal but less Si and Cr.

From a perspective of mass balance, it is implausible that the bright agglomerates at the base of the silicon are comprised entirely of chromium. Only a 6 nm film of chromium was deposited in the initial film stack, yet the agglomerates have penetrated the LTPS layer a distance of 30-40 nm with a saturation fraction of 40-60%. Naturally, the thickness of the TEM sample exceeds the diameter of even the largest agglomeration, but the most conservative assumptions regarding in-plane density suggest that more than a 2 nm loss of Cr film thickness would be needed to compensate for these structures. From this, it can be concluded that the agglomerations are a chromium-rich silicide. This is further supported by the silicon EDS signal in Figure 6.22, which is not attenuated in agglomeration regions.

Some regions in post-process samples, namely those that formed device channels were masked from ion implant in fabrication steps. These areas, clearly visible due to their intact aluminum gates, were similarly analyzed with TEM and EDS to isolate the impact of ion implantation from that of annealing. Figure 6.23 shows HAADF and multi-species TEM images of a masked region, with a very thick aluminum upper layer to demonstrate the proportional dimensions of a completed device. The chromium-rich aggregate layer in this sample shows the same structure as the implanted sample, suggesting that the chromium redistribution is mainly a consequence of the anneal rather than of the implant. The metal underlayer also appears to be intact and comparable with the implanted region.

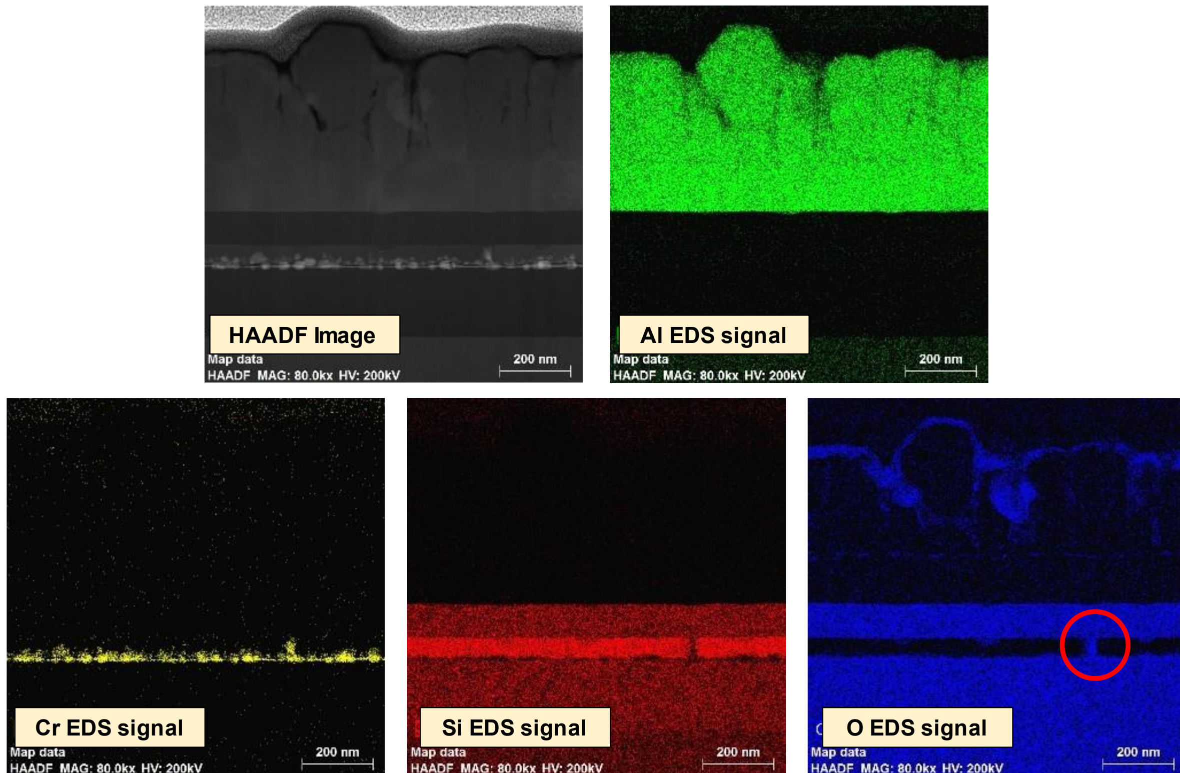

Figure 6.23: TEM EDS of post-process (but not deprocessed) Cr Underlayer CrLG device channel, not subjected to ion implant. Cr-rich agglomerates are still present in this region, proving that the ion implant is not the cause of chromium redistribution. An unexpected oxygen signal is circled in red.

On the rightmost side of the LTPS layer in Figure 6.23, a small pillar-like feature is present. Comparative elemental EDS indicates that this feature is comprised of chromium and oxygen, with a reduced silicon component compared to its immediate surroundings. This may represent a grain boundary in the polycrystalline structure. Much as chromium self-segregates to the upper silicon-oxide interface, grain boundaries offer another set of interfaces throughout the silicon which can attract impurities. It has long been understood that large dopants in polycrystalline silicon have a strong tendency to segregate to boundaries, impacting resistivity through carrier trapping [96]. A similar mechanism may be present here, resulting in a high density of carrier recombination centers at the edge of LTPS grains. It is also possible that areas of chromium that are exposed to SiO_2 due

to random LTPS imperfections can oxidize into CrO_x-group compounds during high-temperature processes, which would explain the very strong oxygen signal in this area.

Figure 6.24 is a cartoon demonstration of the structure of post-process CrLG formed from a chromium underlayer, to be compared with Figure 6.16 above. The broad distribution of chromium-rich agglomerates results in the loss of “bright dot” structures visible in SEM. These bodies are not fully vertically distributed throughout the silicon layer, but instead extend to a certain average distance away from their underlayer source. The appearance of nano-voids is unaffected by post-processing: the structure and distribution of these features are not impacted by chromium mobility. Halo-voids, still caused by gaps in the metal underlayer, are much more numerous in ion implanted regions of post-process CrLG due to the combined effects of kinetic implant damage and subsequent thermal treatments. Lastly, there is significant, TEM-visible segregation of chromium to interfaces and grain boundaries during post-crystallization anneals.

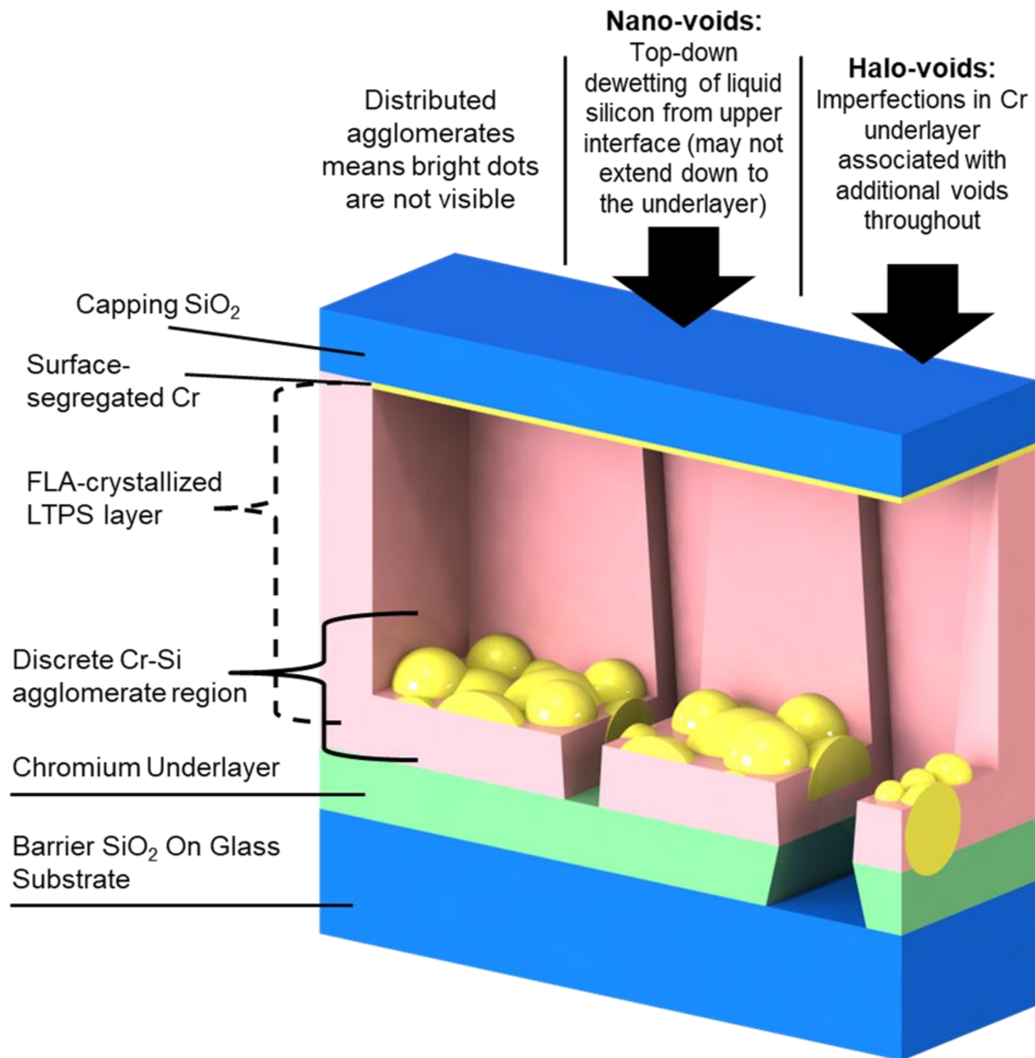

Figure 6.24: Cartoon demonstrating the cross-sectional structure of post-process CrLG, showing how nanofeatures visible in SEM and TEM are impacted by TFT processing. This structure more closely resembles that of finished CrLG devices than that shown in Figure 6.15

6.6 Chromium Distribution and Device Performance

It is clear from microscope characterization that the silicon body of CrLG devices contain chromium in three forms: a remaining, though attenuated, thickness of deposited metal; a region

of dense, isolated metal-rich agglomerates; and a degree of evenly-distributed metallic contamination. The impact of each of these forms on the electrical characteristics of TFTs must be understood to properly evaluate the efficacy of CrLG as a semiconductor material for display applications. Despite the advantages of predictability and uniformity over void-associated FLA LTPS, an inability to account for electrical impact of metal contamination could render this material unusable.

The conductivity of the remaining underlayer material is clearly limited in one of two ways, or else no functional transistor-like behavior would be possible, and all devices built on CrLG would be electrical short circuits. It is possible that the remaining underlayer material has been oxidized from the available oxygen in the SiO_2 barrier layer to form one of the many possible chromium-oxide compounds. This would be difficult to detect with TEM EDS due to the overlap of chromium and oxygen's main emissive peaks. Another possibility is that the chromium-silicon junction forms a Schottky barrier, providing electrical isolation and preventing conduction when applied potential is insufficient to surmount this barrier. This is unlikely to be significant, as the barrier height between chromium and intrinsic silicon is 0.28 eV, as compared with 0.89 eV between the aluminum metal lines and p-type silicon. However, a more complicated concentration profile with a sharp delta layer near the bottom metal could increase the size of this barrier significantly, as Schottky barriers are often governed by interface states [143], [144].

CrLG produced in a chromium-overlayer film stack is structurally similar to underlayer material with the additional advantage of keeping the remaining metal layer exposed, which can be removed with a chromium etchant. However, TEM imaging demonstrates that the majority of Cr-rich agglomerations exists in close proximity to the chromium layer, implying that a device produced with a chromium overlayer would have more of its aggregate region present near the

semiconductor-dielectric interface where the majority of conduction takes place in classical transistors. In order to explore the balance of these effects, p-type TFTs were produced on 60 nm-thick CrLG with an originating 6 nm Cr overlayer, similar to that shown in the TEM images of Figures 6.12-14 above, which was then subjected to a 5-minute etch in Transene Chromium Etchant 1020 at room temperature to remove any exposed overlayer metal. Devices were then implanted with boron ions, activated with a 12 hour furnace anneal at 630 °C, and metallized with aluminum. A more detailed explanation of these process steps can be seen in Section 4.2.

Figure 6.25 demonstrates the typical behavior of an overlayer-sourced CrLG device, first in a “standard” drain sweep of -0.1 V to -10 V, then with a much shallower step up to -5 V. A marked loss of modulation occurs as drain potential increases, culminating with a complete loss beyond -5 V. This may suggest that the high aggregate-density of the conduction region acts as a series of individually conductive islands which can be bridged with sufficient field applied at the drain. Notably, this behavior persisted regardless of device length, with shorter devices retaining modulation at higher drain bias than longer devices. A summary of electrical properties in relation to drain voltage is shown in Table 4.

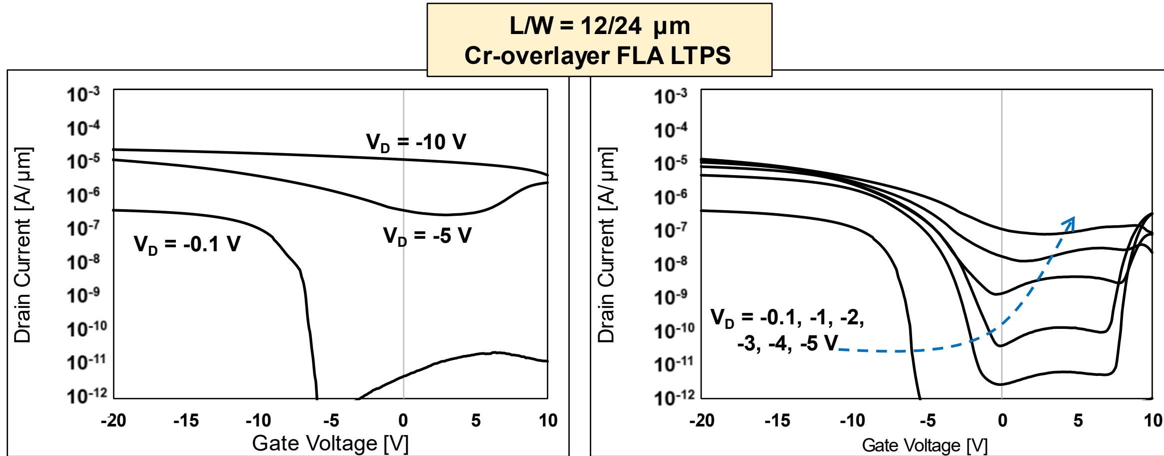

Figure 6.25: Electrical characteristics of CrLG PMOS TFT made on a Cr Overlayer sample with chromium etched away after crystallization. Left: I_D-V_G characteristics with standard drain voltage sweep. Right: Finer drain voltage sweep to explore loss of gate modulation.

Table 4: Comparison of electrical parameters of CrLG Overlayer device at different drain biases

V_D [V]	V_T [V]	I_{ON}/I_{Off}	$I_{VD=10}/I_{Off}$
-0.1	-7.6	7.96	2.50
-1	-6.3	6.07	4.95
-2	-7.1	5.21	3.85
-3	-7.6	3.86	1.75
-4	-7.5	2.95	0.25
-5	-6.7	2.18	0.04
-10	0*	0.84	0*

** Devices lost all modulation at V_D = -10 V*

By comparing these metal overlayer devices with the initial, test-case metal underlayer CrLG devices shown in Section 6.3, a hypothetical trend emerges. Although it may be possible to remove the remaining metal-rich overlayer after crystallization, there is no clear benefit to doing so. Instead, CrLG devices modulate more effectively when the depth of primary conduction is

separated from regions with significant chromium agglomeration density. This explanation supports the hypothesis that agglomerate penetration into the silicon is independent or only weakly dependent on the thickness of that silicon or the original location of the chromium layer, a concept that is also demonstrated in TEM comparisons. Figure 6.26 shows a side-by-side TEM depiction of a 60 nm-thick CrLG stack with an underlayer metal source after TFT processing, a > 100 nm-thick CrLG stack with a sandwiching metal source, and a > 60 nm-thick CrLG stack with an overlayer metal source, the latter two immediately after crystallization. Both samples, regardless of structure and processing differences, display an average agglomerate invasion distance *z* of 35-40 nm from each metal source.

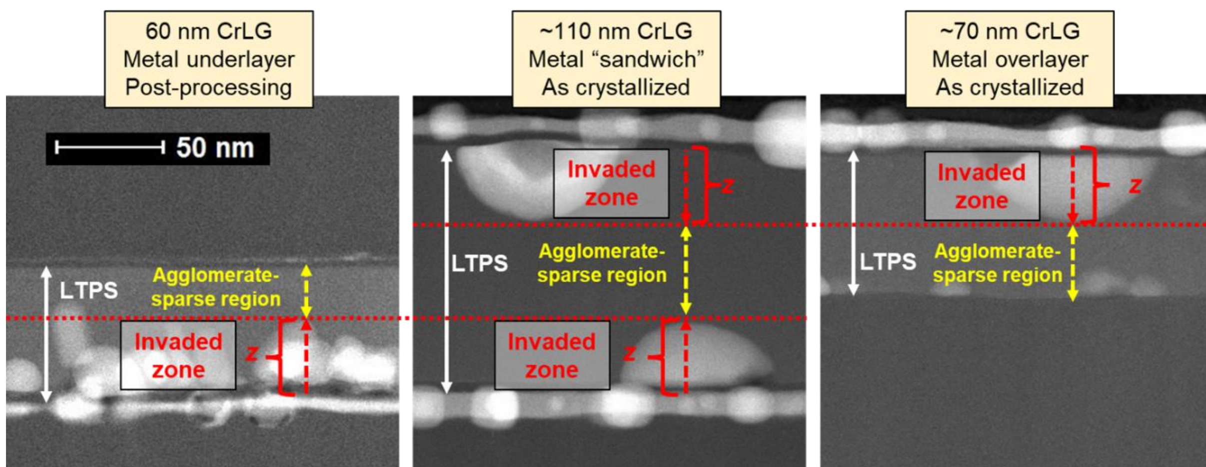

Figure 6.26: Demonstration of invasion distance z across TEM images of three CrLG film stacks.

This comparison demonstrates that each sample stack of CrLG LTPS can be split into zones adjacent to the metal source layer into which there has been significant metal-agglomerate invasion and a distal layer which is mostly agglomerate-free. This invasion distance, *z*, is not dependent on silicon thickness or stack structure; each of the samples in Figure 6.26 were crystallized with the same FLA settings and have similar invasion distances.

The relation between silicon thickness *t* and invasion distance *z* in CrLG TFTs was explored with an additional experiment. Building off the chromium-underlayer structure demonstrated in section 6.3, a series of a-Si/Cr/SiO_2/glass substrate samples were fabricated, with initial a-Si thicknesses varying between 20 and 100 nm. These samples were crystallized with FLA, doped with boron ion implantation, furnace activated, and metallized to produce PMOS CrLG TFTs following the procedures in section 4.2.1. Based on the hypothesis of thickness-independent invasion distance, these samples would each display a different fraction of aggregate-free LTPS over a Cr aggregate-dense buried LTPS layer. An explanatory cartoon of the various samples in this experiment can be shown in Figure 6.27.

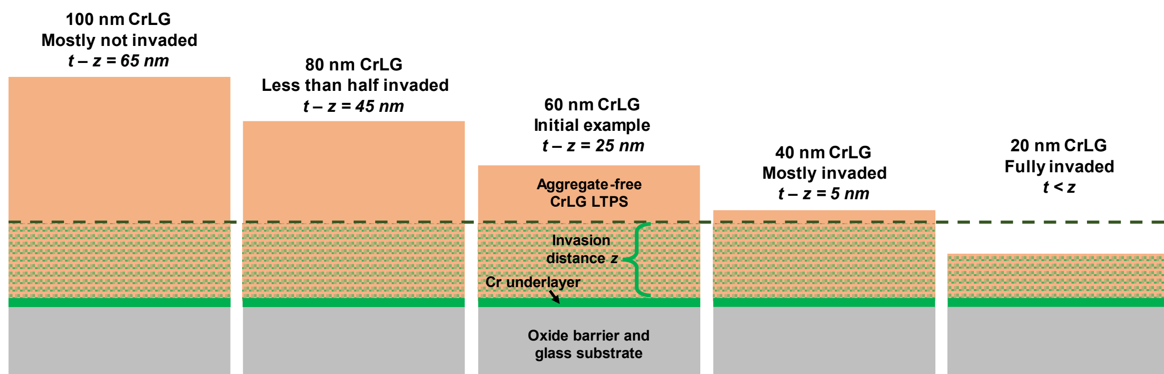

Figure 6.27: Diagram of the hypothetical silicon thickness-independent invasion distance z as it interacts with film stacks of varying silicon thickness: z and t are to scale

The efficacy of FLA crystallization is dependent on total energy absorbed, which is dependent on silicon thickness. As such, a broad spread of single-pulse FLA energy densities between 4.8 and 5.6 J/cm^2 were used to crystallize different regions of each sample. The lowest energy setting that produced optically identifiable CrLG was used as the primary example of that thickness for electrical characterization and comparison. Figure 6.28 shows comparative optical micrographs of

each sample after FLA crystallization, with contrast and saturation adjustments to demonstrate CrLG structure.

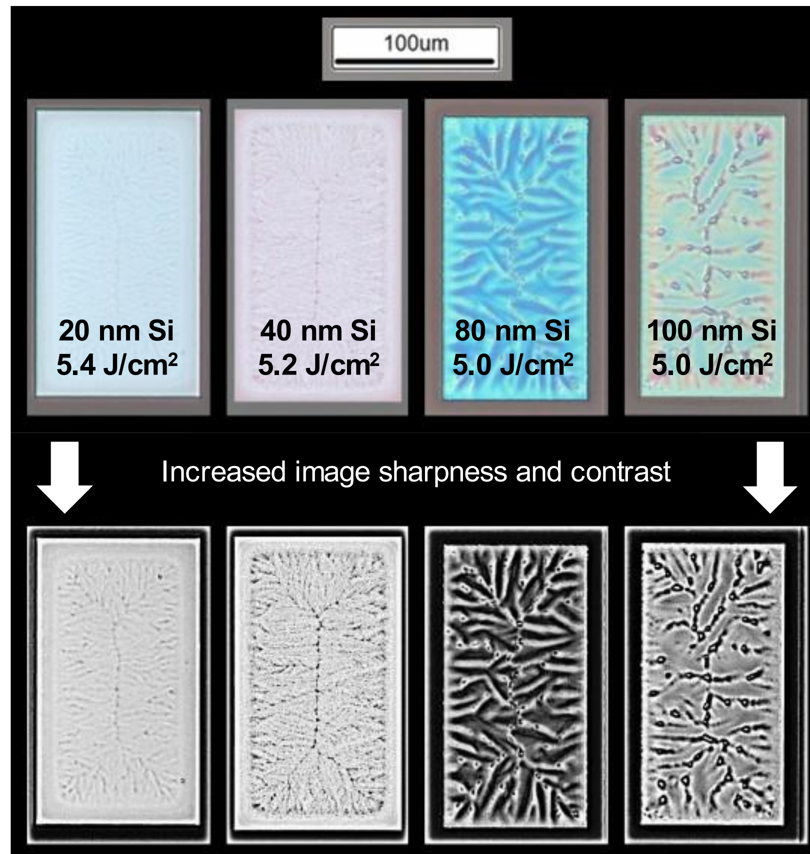

Figure 6.28: Upper: Optical micrographs of CrLG Cr underlayer mesas of varying silicon thickness after crystallization. Lower: The same images manipulated with software to increase contrast and make CrLG texture more noticeable.

Figure 6.29 demonstrates a comparison between typical p-type FLA CrLG TFTs of equal 12/24 µm length/width dimensions fabricated on varying thicknesses of LTPS. All measured devices are crystallized at the lowest FLA intensity that generates visible CrLG structure in an attempt to negate the effect of thickness variations on FLA pulse absorption. All devices appear to have similar switching sharpness and off-state leakage at high drain bias. A threshold voltage of ~-5 V

is common to the two thicker devices, while the two thinner devices have a threshold voltage of -9 to -10 V. For each device, channel mobility was extracted with the maximum transconductance method. Most devices show a similar maximum mobility of just under 30 $cm^2/(Vs)$; however, the 20 nm thick device has a significantly reduced maximum mobility of 17 $cm^2/(Vs)$. These parameters are displayed in Table 5.

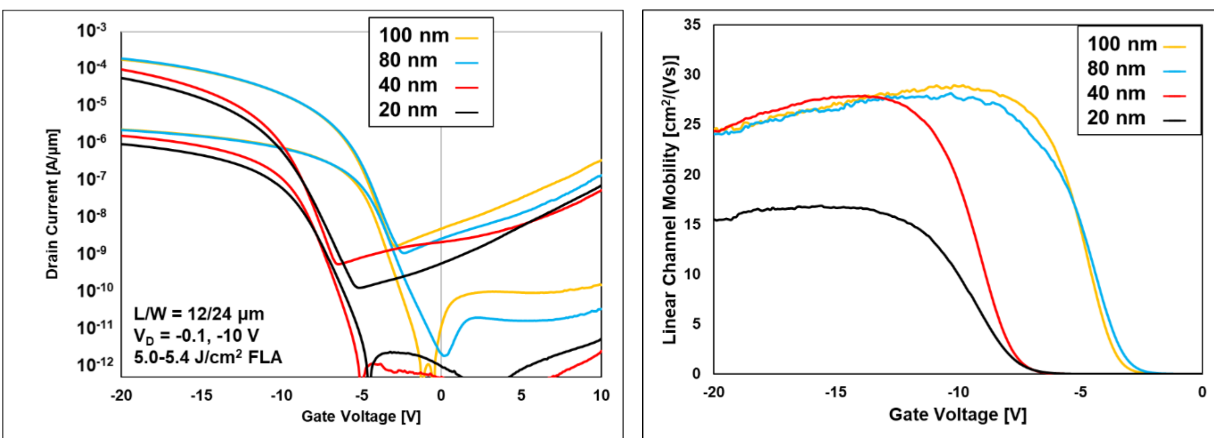

Figure 6.29: I_D-V_G characteristics (left) and extracted channel mobility (right) of CrLG underlayer TFTs of L/W = 12/24 µm channel dimensions and silicon thicknesses between 20 and 100 nm.

Table 5: Relevant device parameters of varied-thickness CrLG underlayer devices in Figure 6.29

Silicon thickness *t* [nm]	**Maximum channel mobility [cm²/(Vs)]**	**Threshold voltage [V]**
100	29.0	-5.3
80	28.1	-5.2
40	27.9	-9.5
20	16.8	-9.9

This pattern of device operation would normally have little bearing on a comparison of TFTs of different thicknesses. When the hypothesis of a consistent agglomerate invasion distance is introduced, however, a pattern begins to emerge. In this case, the varying regimes of these CrLG device operation may be considered as a factor of their thickness with respect to the 30-35 nm invasion distance. Figure 6.30 is a schematic to help illustrate this concept.

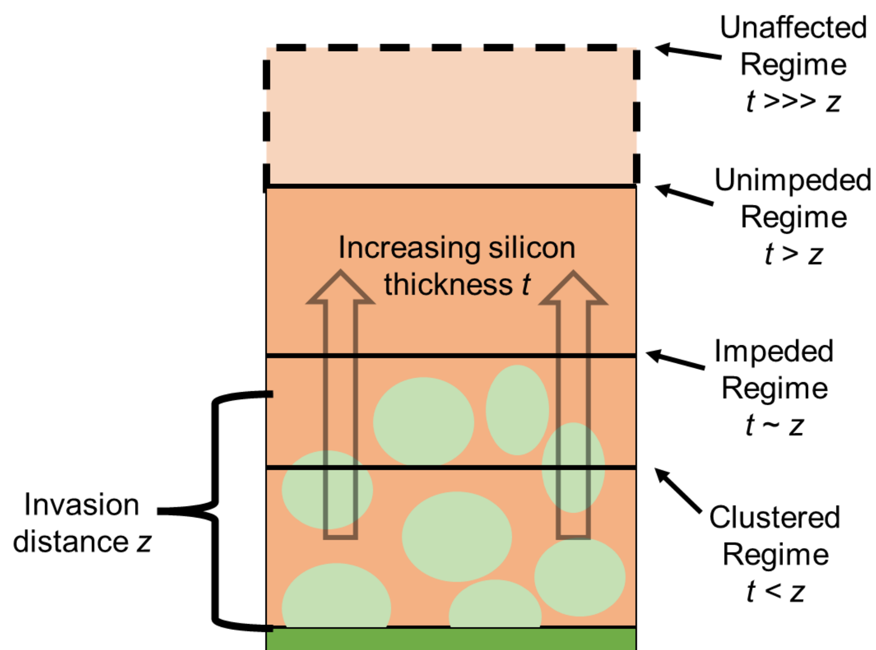

Figure 6.30: : Cartoon schematic of the different regimes of CrLG TFT operation based on the relation of silicon thickness and invasion distance.

When silicon thickness is much larger than invasion distance, chromium has effectively no electrical impact on the stack. Most of the silicon layer is free of contamination. This is the regime in which the Ohdaira group's work likely takes place; silicon thickness is in the order of micrometers and Cr invasion has been measured by SIMS to be less than 100 nm. This is the Unaffected regime. If t is larger than z, but within the same order of magnitude, a device operates

in the Unimpeded regime. Here, the body of silicon is contaminated with chromium up to its solid solubility limit, as evidenced by the clear traversal of Cr regions across the Si layer in TEM images. However, there is a large band of silicon which is free of agglomerates, in which electrical conduction can take place. The 80- and 100-nm thick transistors in this experiment operate in this regime.

As t is further reduced and begins to approach z, CrLG devices enter the Impeded regime. Here, buried fixed charge or additional interface traps in the channel surrounding the Cr agglomerate layer becomes significant as the conduction pathway is squeezed into a narrow region above z. Threshold voltage is impacted by this layer of charge, but mobility is mostly unchanged. This is the operation regime of the 40-nm thick TFTs. Finally, if thickness is reduced to below the invasion distance, there is no longer a conductive pathway that is clear of agglomerates. The additional scattering centers obstructing the channel result in a sharply reduced carrier mobility in addition to V_T degradation, as is seen in the 20-nm thick TFT. This behavior is the Clustered regime, representing a conduction mechanism that is heavily hampered by invading particles. Beyond this point, there is a critical thickness below which the formation of CrLG by FLA is not possible due to limited light absorbance in the silicon.

6.7 CrLG Conclusion

Chromium-enhanced FLA LTPS represents a morphology of polycrystalline silicon that is predictable, geometry-mediated, and produces fewer micro-scale dewetted areas than the randomized void-laden material demonstrated in Chapter 4. The consistent behavior of CrLG allows the production of TFTs with much more replicable behavior from device to device, a significant drawback shown in previous FLA LTPS devices. Though this material has been shown

previously in micrometers-thick structures to have negligible chromium contamination, the novel thin CrLG displays metal invasion in a variety of forms, resulting in unique nanoscale textures visible in high-resolution SEM and AFM and independent of the edge-directed textures visible through optical microscopy.

Immediately after crystallization, chromium intrudes into the silicon layer in the form of hemispherical protrusions at the Si/Cr interface. Once exposed to further thermal treatments, these protrusions redistribute into a layer of discrete agglomerates of chromium silicide. The agglomerate region invades the silicon to a distance that is broadly independent of geometry, though it may be affected by aspects not varied here, such as FLA intensity, anneal time and temperature, and thickness of the metal layer. This behavior persists whether chromium is introduced as an underlayer, an overlayer, or both simultaneously. From this, a relation between device thickness and electrical behavior can be explained as the degree to which the agglomerate layer interferes with conduction through a TFT channel.

This interpretation helps explain the impact of chromium presence in CrLG devices and suggests some mitigation strategies. The simplest solution to any fears of contamination would be to simply produce thicker devices, on the order of 200 nm or more. This is not ideal for many applications, but is worth exploring. Additionally, efforts could be made to getter or prevent the formation of these agglomerates with targeted device engineering.

Chapter 7. COMPARATIVE STUDY ON INTEGRATED STRATEGIES

The experimental methods presented in chapters 4, 5, and 6 discuss several fabrication methods which can be implemented into a full procedure for producing FLA LTPS TFTs. Each of these are worth considering independently and in conjunction with other strategies to determine their impact on device performance and electrical behavior. Of these, three specific strategies are singled out as ideal candidates for a comparative experimental design.

7.1 COMPARATIVE FABRICATION STRATEGIES

Chromium-underlayer large grain FLA LTPS, as described in chapter 6, represents a morphology of LTPS that is not plagued with large, randomly distributed voids. Though it is still visibly nonuniform and demonstrates variance in surface texture on the order of the full thickness of the film, CrLG formation is an edge-directed process; its formation can be directed by shaping the geometry of the a-Si mesas prior to crystallization. This permits specific areas of predictable morphology and high uniformity to be carved out of post-crystallization mesas, bypassing areas with the most grain boundaries and largest ridge textures. However, there is evidence that the impact of residual chromium within CrLG may degrade electrical performance.

Within the experiments presented in Chapter 4, the stage at which dopants are introduced to silicon to delineate source and drain regions of TFTs has been identified as an important factor in device performance. If amorphous silicon is doped prior to FLA crystallization, the melting-solidification transition ensures a high degree of dopant activation. However, the freedom of a liquid phase allows dopant atoms to laterally travel a significant distance in the sub-millisecond

crystallization timeframe. On the other hand, LTPS can be doped after crystallization to avoid this lateral transit, but this necessitates a separate, lower-temperature dopant activation anneal which will likely have a reduced activation percentage. The decision to introduce dopants before or after crystallization is thus an extremely important factor in process design and cannot be left out of a comprehensive comparative study.

FLA can also be used as a method of dopant activation on already crystallized LTPS; in fact, this is a much more common use of the technology. This makes it a valuable replacement for the activation method used elsewhere in this document: long furnace anneals at temperatures just below the limitations of display glass substrates. By replacing these furnace anneals with a secondary FLA step, fabrication more closely resembles a truly low-temperature process. The highest temperature experienced by the substrate at thermodynamic equilibrium then becomes the 450 °C furnace anneals used to dehydrogenate amorphous silicon after deposition and sinter the final devices, both of which are significantly shorter processes.

Chapter 5 dealt with MLD, an alternative method of dopant introduction for thin film and ultra-shallow junction applications. Ion implantation is often disfavored in industrial settings due to its high cost; instead, dopants are incorporated into amorphous silicon during deposition. In FLA LTPS, the melt-phase crystallization transition can render this impractical, as demonstrated by the large lateral diffusion shown in section 4.2. Any large quantity of dopant present throughout regions of the initial a-Si layer will likely spread far beyond those regions after FLA crystallization.

MLD offers an opportunity to strictly limit dopant concentration based on the physical constraints of available surface bonding sites, which can mitigate the extent of effective lateral diffusion. Additionally, MLD is a technique that does not induce kinetic damage to target samples, which may be of importance with the unique crystal structures of CrLG LTPS or ensuring the

consistency of the metal underlayer. The comparison of MLD with an established ion implant process will shed light on its interaction with other FLA LTPS TFT techniques.

The efficacy of each of these fabrication methods: chromium-underlayer edge directed LTPS, monolayer doping, and dopant introduction prior vs. after crystallization, all with full FLA activation, can be studied as part of a broad experimental design with eight potential combinations. By selecting parameters for which control data already exists, a simpler and more parsimonious design can be realized. All experiments in this design are built on a thin chromium underlayer, with non-CrLG data coming from earlier studies. Phosphorus dopants are used for these experiments to produce n-type TFTs, mainly for comparison to existing MLD data. All other parameters are as stated in the "default" sample listed in Section 4.2.1

Figure 7.1 demonstrates the experimental breakdown of these combined factors into four pathways. Each pathway is further split by varying FLA intensity between 4.0 and 5.2 J/cm^2 to explore how crystallization is impacted by various modifications and to ensure the optimal energy density is located. Unless otherwise stated, each result shown below uses whichever intensity was optimal for that setting and result, which will vary based on equipment setup.

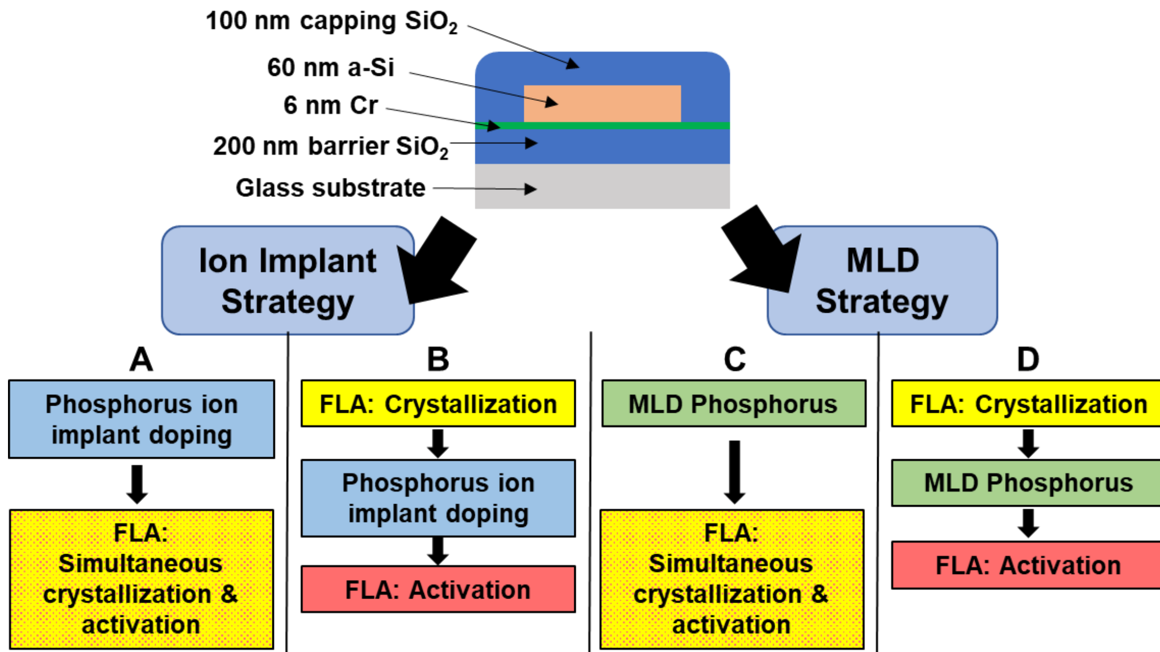

Figure 7.1: Flowchart of the critical process steps of the four experimental "pathways" in this document section.

7.2 NMOS CRLG FLA LTPS TFTS

7.2.1 Pathway A: Combined Crystallization & Activation FLA

Pathway A, from Figure 7.2, demonstrates the first instance of n-type FLA TFTs built on chromium-underlayer large grain polysilicon. A layer of 60 nm PECVD a-Si is deposited on a thin chromium underlayer, then doped with phosphorus ion implantation prior to FLA crystallization. The single combined crystallization and activation FLA step used a spread of flash lamp intensities between 4.6 and 5.2 J/cm^2. Ion implantation into a-Si is intended to be effectively the same as dopant introduction during deposition; it is used for convenience. This combination of strategies is directly comparable to n-type devices shown in Section 4.2, with the only difference being the inclusion of a chromium underlayer.

Figure 7.2 shows a comparison of optical images of Pathway A mesas after FLA crystallization at varying intensities, as well as electrical results of NMOS TFTs constructed on these or similar mesas. It is clear that only a narrow band of flash lamp energy density is effective at producing undamaged CrLG LTPS. An intensity of 4.8 J/cm^2 or below is insufficient and does not result in a full melt phase across the center of the mesa. However, an intensity of 5.2 J/cm^2 results in a high frequency of large voids overtaking a majority of mesa area. A “sweet spot” of successful CrLG formation without significant damage is apparent; it is around 5.0 J/cm^2 in this equipment setup, though doubtless may vary based on individual FLA systems.

From these micrographs, it is also clear that the process used to introduce dopants to these mesas prior to crystallization has an impact on crystallization. Each intensity shows a visible distinction between the ion implanted top and bottom region of the mesas and the central channel region. This distinction is particularly apparent in samples crystallized at 4.8 and 5.2 J/cm^2, in which the silicon in these regions is heavily damaged. This effect may be due to implant disturbance of the underlying chromium layer, reducing its integrity and thus its adhesion efficacy. A more complete analysis of this effect could be performed by comparing samples doped by ion implant with in-situ deposition doping. However, the integrity of the silicon crystallized in the “sweet spot” is sufficient for the purpose of this analysis.

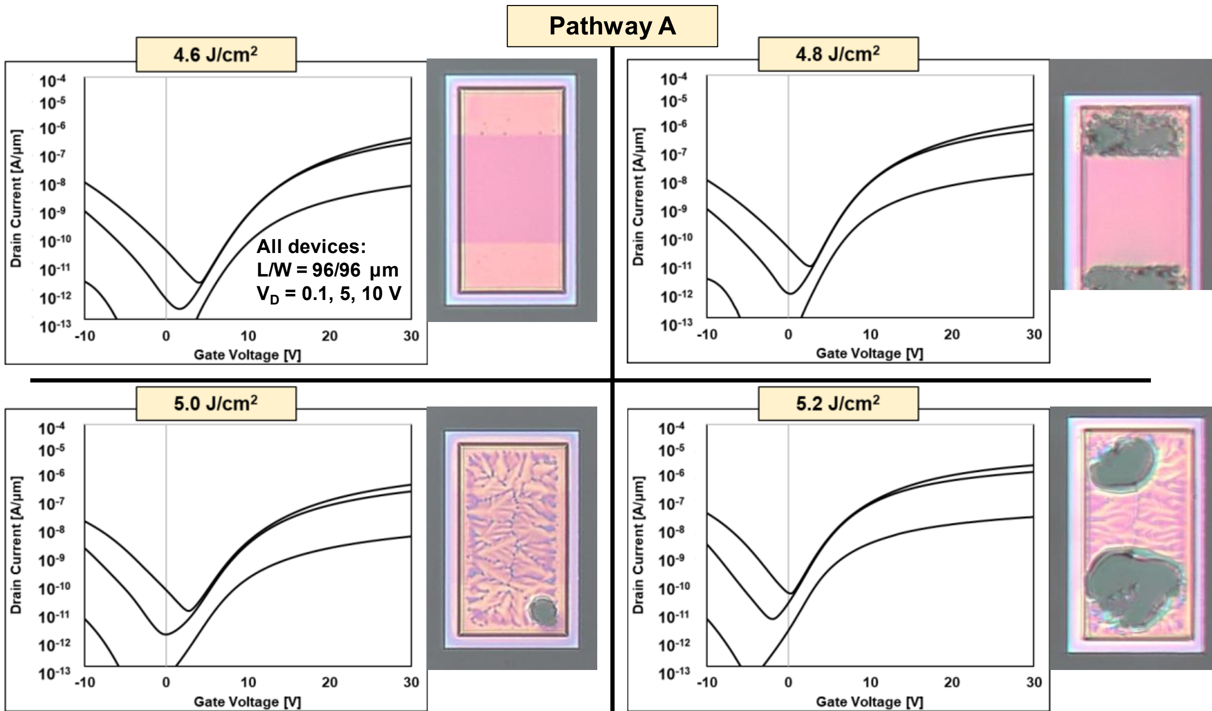

Figure 7.2: Data from Pathway A. For FLA intensities from 4.6-5.2 J/cm²: optical micrograph of L/W = 96/96 µm device mesas after crystallization/activation and final mesa lithograph. $I_D - V_G$ characteristics of devices fabricated on these mesas.

Regardless of silicon integrity in the source-drain regions, each of these FLA conditions is sufficient to crystallize a-Si, at least partially, as well as activate the implanted dopants. NMOS TFT characteristics of large, 96 × 96 µm devices shown in Figure 7.2 indicate that functional transistors can be produced even when source-drain silicon is heavily damaged, though this may result in problems with yield fraction.

A better comparison of device behavior can be made by looking at smaller devices. Figure 7.3 compares devices with mask-defined channel dimensions of 12 µm in length and 24 µm in width. Low-drain transfer characteristics are used to extract channel mobility and threshold voltage through the maximum transconductance method. However, the device crystallized at 5.2 J/cm² shows very high off-state current, especially at higher drain biases. This likely indicates that lateral

diffusion of phosphorus during FLA crystallization has reduced the metallurgical channel length, inflating the extracted channel mobility.

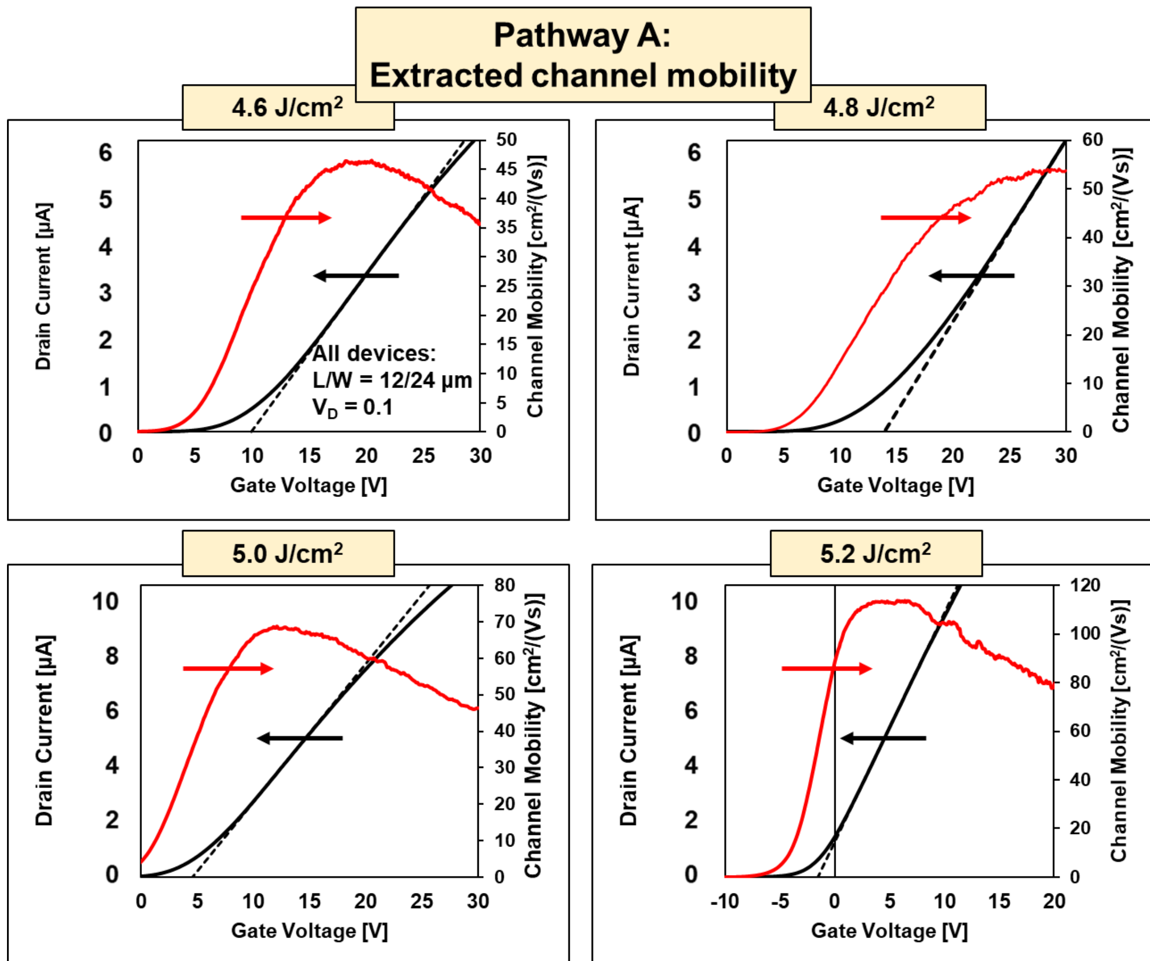

Figure 7.3: Channel mobilities and low drain bias operation for mask-defined L/W = 12/24 µm devices fabricated through Pathway A using FLA pulses of 4.6-5.2 J/cm^2.

Table 6 lists some important electrical parameters of these devices. A decrease in threshold voltage shift can be seen with an increase in FLA energy, pointing to a reduction of fixed charge in the channel, likely indicating larger grain size and thus fewer grain boundaries. Each boundary acts as a scattering center as well as a location for both chromium and MLD phosphorus to segregate, so their minimization is important for electrical operation. The chromium distribution of these single-FLA devices is likely dissimilar to those demonstrated in Chapter 6, as they did not

experience a long furnace activation anneal after crystallization. The chromium present within the invasion distance remains as hemispherical protrusions rather than broadly distributed discrete agglomerates, so its impact on threshold voltage is not as significant. These devices more closely resemble the "as-crystallized" structure shown in Section 6.4; the presence of distal agglomerations at the silicon-SiO_2 surface may result in additional interface traps.

Table 6: Relevant electrical parameters of Pathway A TFTs of L/W = 12/24 μm. The starred mobility value may be inflated due to lateral dopant diffusion, which may also distort V_T calculations.

FLA Intensity	**4.6 J/cm^2**	**4.8 J/cm^2**	**5.0 J/cm^2**	**5.2 J/cm^2**
V_T (V)	9.9	13.9	4.6	-1.5*
$\mu_{chan:max}$ (cm^2/Vs)	46.4	54.2	68.6	113.8*
$I_{(VT+10)}/I_{min}$	3.8×10^5	6.2×10^5	1.0×10^5	4.0×10^3
SS_{Min} (V/dec)	2.09	1.89	2.17	2.77

7.2.2 Pathway B: Successive Crystallization and Activation FLA

Pathway B demonstrates a modification of n-type CrLG FLA TFTs in which dopants are introduced after crystallization and activated with a second flash lamp anneal. In this strategy, the initial crystallization anneal followed the same spread of intensities as Pathway A, while the secondary FLA activation was conducted at 4.5 and 5.0 J/cm^2 for eight possible combinations. Figure 7.4 shows micrograph images of mesas after crystallization and prior to implant, indicating that the presence of localized crystallization differences, voids, and loss of silicon integrity seen in Figure 7.2 is due entirely to the phosphorus ion implantation. Without a pre-FLA implant, crystallization is uniform across the mesa following the patterns laid out in Chapter 6. Further, a FLA intensity of 5.2 J/cm^2 results in the most distinct large-grain morphology with the least degree of border exclusion.

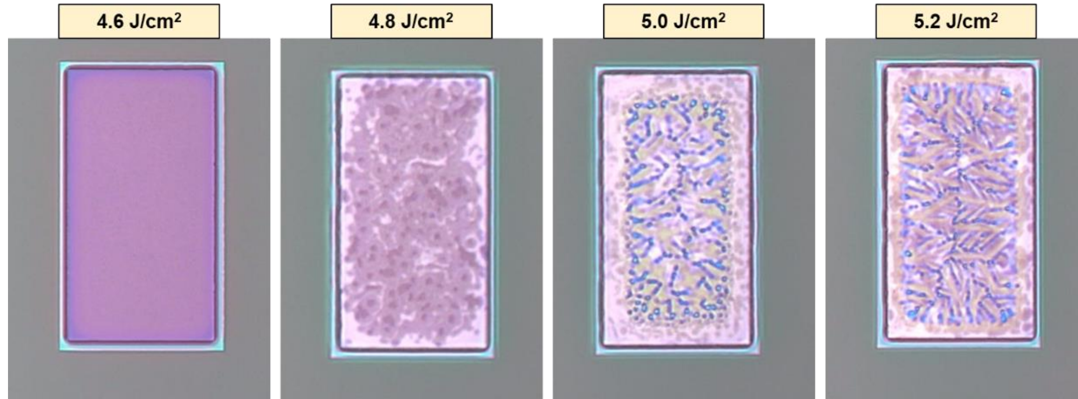

Figure 7.4: Optical micrograph of Pathway B mesas of 120x208 µm after initial FLA crystallization, showing CrLG when FLA intensity is at 5.0 J/cm^2 or above. (The spotty texture is due to an incomplete photoresist removal which was corrected prior to device completion)

Not all combinations of FLA crystallization and activation energies resulted in reliably functional NMOS TFTs, especially with shorter device dimensions. Figure 7.5 shows the full array of crystallization and activation FLA intensity combinations and the typical behavior of NMOS TFTs (L/W = 12/24 µm) processed under those conditions, with their electrical parameters summarized in Table 7.

Table 7: Relevant electrical parameters of Pathway B TFTs of L/W = 12/24 µm. "FLA 1" indicates the intensity of crystallization FLA performed prior to doping, while "FLA 2" indicates the intensity of activation FLA.

FLA 1*	**4.6 J/cm^2**		**4.8 J/cm^2**		**5.0 J/cm^2**		**5.2 J/cm^2**	
FLA 2*	**4.5 J/cm^2**	**5.0 J/cm^2**	**4.5 J/cm^2**	**5.0 J/cm^2**	**4.5 J/cm^2**	**5.0 J/cm^2**	**4.5 J/cm^2**	**5.0 J/cm^2**
V_T (V)	19.4	--	18.4	17.0	--	14.7	14.6	17.8
$\mu_{chan:max}$ (cm^2/Vs)	22.7	--	8.8	32.5	--	30.1	41.3	37.9
I_{VT+10}/I_{min}	8.7×10^7	--	5.1×10^4	1.3×10^6	--	1.9×10^5	1.8e5	1.8×10^5
SS_{Min} (V/dec)	0.92	--	2.20	0.70	--	2.50	2.37	2.64

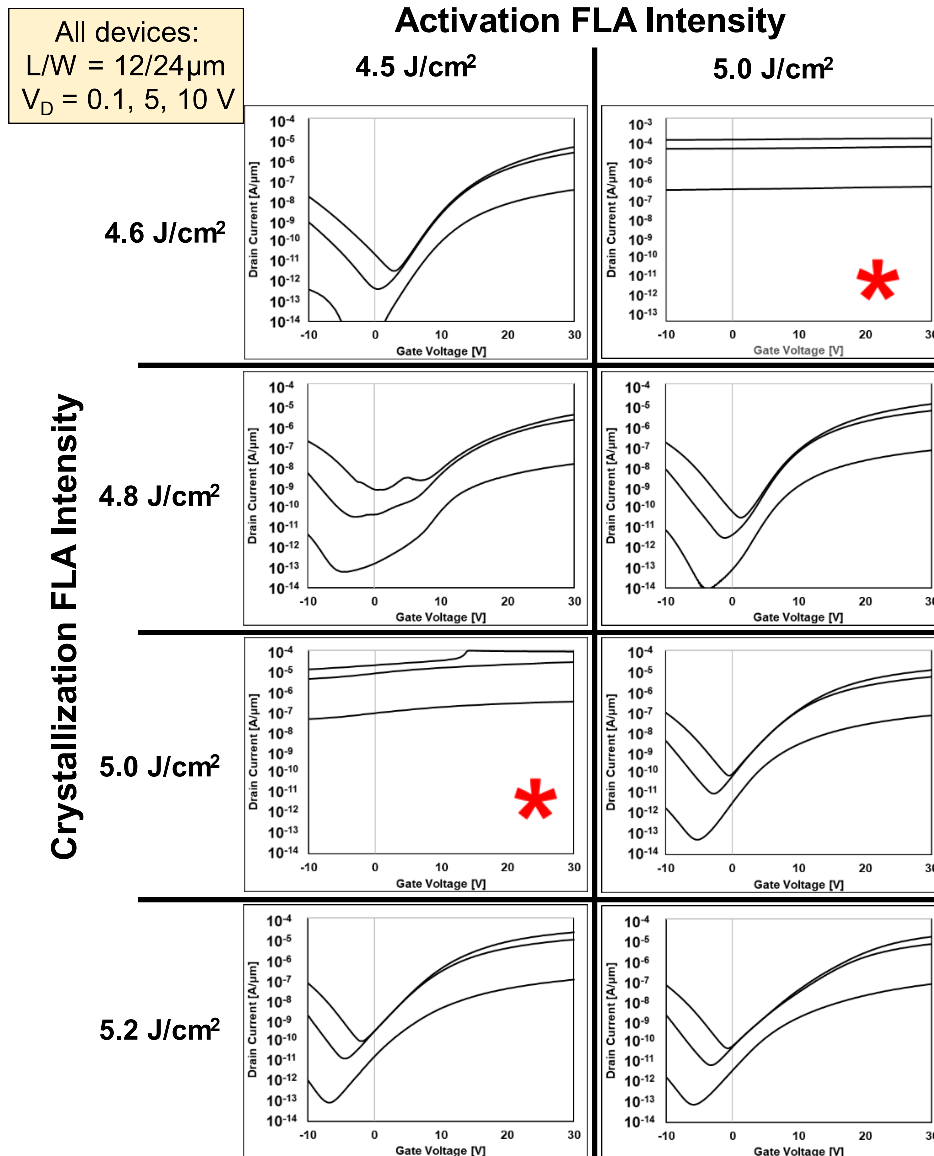

Figure 7.5: Array of I_D – V_G characteristics for Pathway B TFTs crystallized with FLA 4.6-5.2 J/cm^2 and activated with FLA at 4.5 or 5.0 J/cm^2. Starred graphs represent treatment combinations that did not result in consistent transistor-like behavior.

Two samples shown in Figure 7.5 show anomalous, resistor-like behavior rather than transistor modulation. This may be explained by poor process control and variance in fabrication, especially with the sample crystallized at 5.0 J/cm^2 and activated at 4.5 J/cm^2. However, the sample crystallized at 4.6 J/cm^2 and activated at 5.0 J/cm^2 demonstrates a limitation of FLA as a method of dopant activation in thin-film silicon. In previous multi-stage FLA experiments, the intensity of

activation exposures has been kept at or below that of earlier crystallization exposures. Because amorphous silicon has both a lower melting temperature and a higher absorbance in the visible light range than that of polycrystalline silicon, a second FLA exposure at a similar energy density will not greatly impact the silicon's structure and phase. However, a much higher-energy activation pulse following a low-energy crystallization pulse is likely to cause complicated re-melting behavior, which counteracts the benefits of a multi-stage FLA process by allowing lateral dopant diffusion.

7.3 NMOS MLD CrLG FLA LTPS TFTs

Pathways C and D explore the doping of NMOS CrLG devices with monolayer doping instead of ion implantation. These procedures utilized the same chemistry as explained in Chapter 5: a divinylphosphonate bath heated to 200 °C for two hours, carefully washed off with mesitylene and toluene sequentially before immediate capping with 100 nm of PECVD SiO_2.

7.3.1 Pathway C: Combined Crystallization & Activation FLA

The single-FLA Pathway C incorporates monolayer doping prior to FLA crystallization, allowing activation to take place simultaneously in a manner similar to Pathway A. Samples of 60 nm PECVD a-Si with a 6 nm Cr underlayer were patterned into initial crystallization mesas, then capped with a mask of 100 nm PECVD SiO_2. Source and drain windows were then etched into this mask, allowing selective regions to be exposed to MLD chemistry. Because SiO_2 was used as a dopant mask and because MLD also requires a capping layer to be deposited immediately after deposition to prevent loss of adhered dopant, the final thickness of the oxide layer after these stages varied between 100 nm in doped regions and 200 nm in masked regions. This was the layer

used for antireflective and capping oxide during FLA. Thus, a variance in the reflection of incoming light is anticipated between these regions. Figure 7.6 demonstrates this variation in thickness and the change in reflectance that would result in an ideal situation. The differences in the UV range may be significant as a-Si absorbs most strongly in that range.

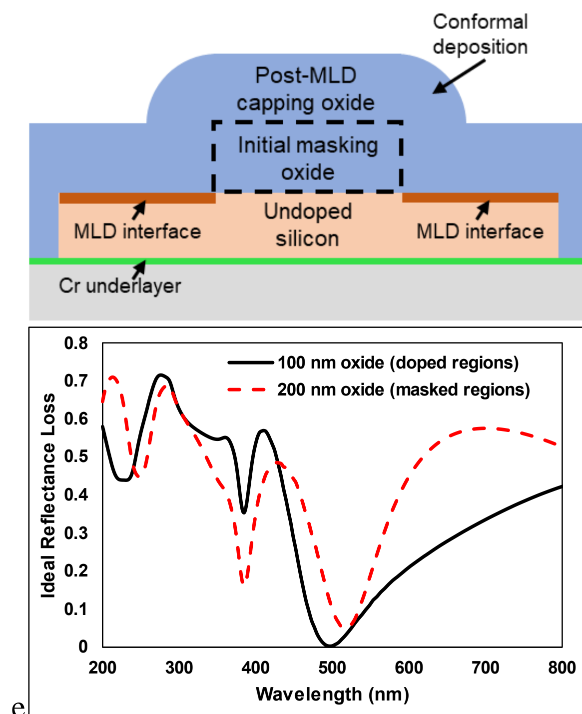

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Figure 7.6: Above: Cartoon of undesirable capping oxide thickness variation during FLA caused by MLD procedures. Below: Impact of oxide thickness variation on the visible spectrum of light in ideal circumstances.

Figure 7.7 contains micrographs of LTPS mesas of this pathway immediately after crystallization. An obvious difference in color between doped and undoped areas is due to the remaining capping oxide layer. Beyond that, there is a decrease in border exclusion radius within the doped areas, which is most noticeable in the sample crystallized at 5.0 J/cm^2. The avoidance of damaging ion implantation has resulted in a greater degree of mesa integrity. As compared with samples from Pathway A in Figure 7.2, very few dewetted areas are present. Further, there is no localization of the few noticeable voids to the doped regions, which provides additional evidence

that monolayer doping is a much less damaging method of dopant introduction than ion implantation. The chance and size of void formation increases with crystallization energy density, but their distribution is random

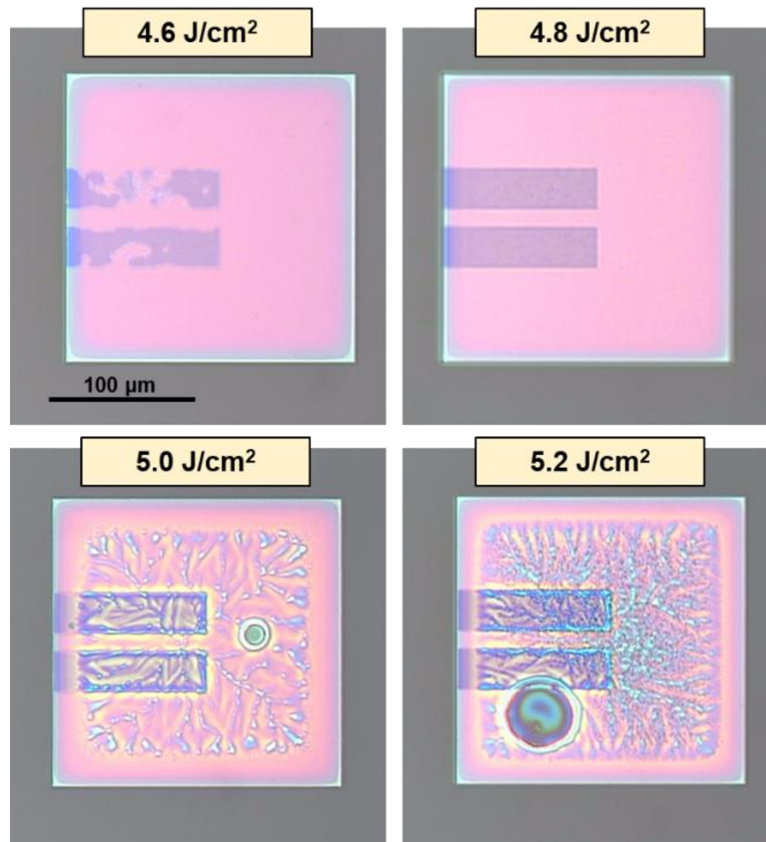

Figure 7.7: Optical micrographs of silicon mesas after FLA crystallization for Pathway C: CrLG + phosphorus MLD in a combined crystallization/activation FLA step. Higher energy density samples demonstrate a pattern of randomly distributed voids.

Electrical data for n-type TFTs produced through Pathway C is shown in Figure 7.8. Only samples that reached a CrLG morphology demonstrated consistent electrical behavior. Without a full mesa melt, MLD-adhered dopants may not have become incorporated into the final silicon mesa. Samples intended to be crystallized/activated below 5.0 J/cm^2 are not shown here due to low and variable yield.

Based on this comparison, the device crystallized at 5.0 J/cm^2 shows clear advantages over its counterpart crystallized at 5.2 J/cm^2. Channel mobility is significantly higher and threshold voltage is less exaggerated. It is possible that FLA crystallization in the presence of MLD can rapidly overheat and desorb surface dopants before they can be activated, resulting in an even lower concentration than MLD is normally capable of providing. A monolayer of optically dense organic compound atop the a-Si layer may also alter the depth profile of energy absorbance during FLA, but this is beyond the scope of this document.

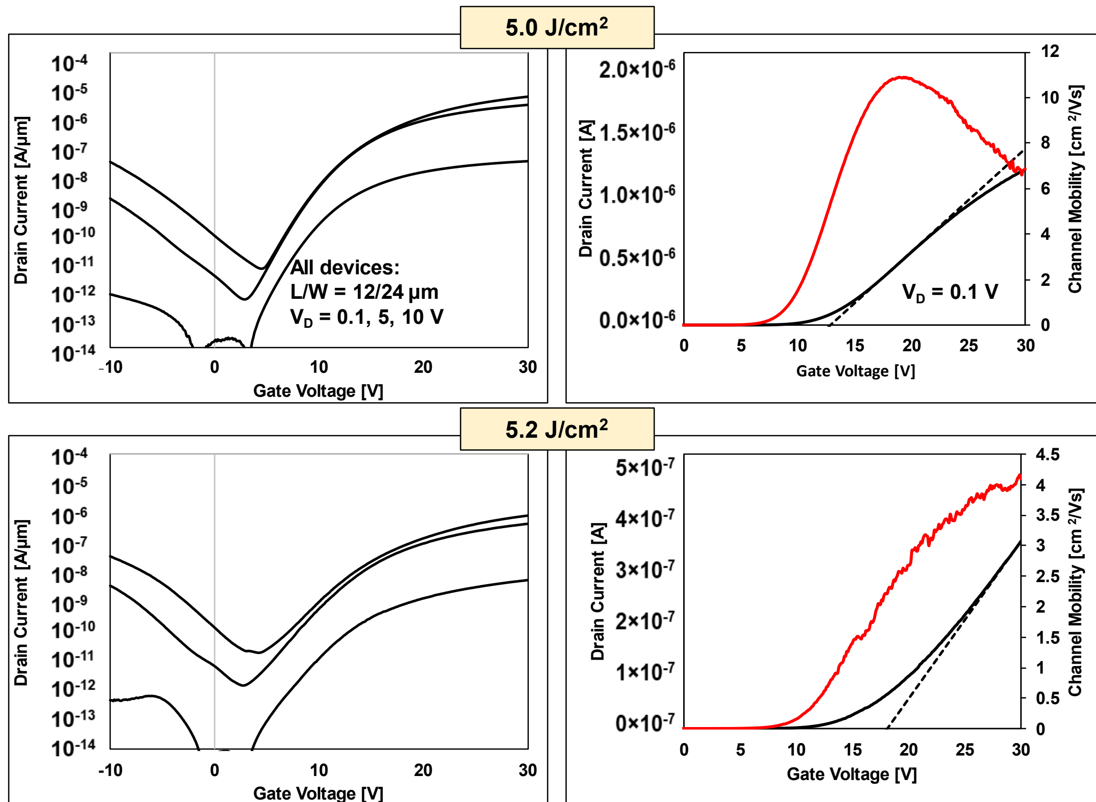

Figure 7.8: Electrical characteristics of Pathway C CrLG MLD NMOS devices crystallized and activated using a single FLA pulse at 5.0 J/cm^2 (upper) and 5.2 J/cm^2 (lower), including I_D – V_G characteristics (left) and channel mobility calculations (right)

Table 8: Relevant electrical parameters of Pathway C TFTs of L/W = 12/24 µm compared with a 96/96 µm non-CrLG device from earlier work

	CrLG: FLA 5.0 J/cm^2 (Pathway C)	**CrLG : FLA 5.2 J/cm^2 (Pathway C)**	**No CrLG (Initial MLD, Ch. 5)**
V_T (V)	12.9	18.1	-1.5
$\mu_{chan:max}$ (cm^2/Vs)	10.9	4.16	61.3
I_{VT+10}/I_{min}	9.61×10^6	1.15×10^6	5.8×10^3
SS (V/dec)	0.719	1.02	1.40

Table 8 displays relevant electrical parameters of the functional *L/W* = 12/24 µm Pathway C devices, FLA crystallized at or above 5.0 J/cm^2. The maximum mobility of 5.2 J/cm^2 devices is artificially low, as a maximum transconductance was not reached in the gate voltage sweep, which reached up to 30 V in these extended $I_D – V_G$ tests. These results are compared with the MLD FLA devices shown in Chapter 5.4, which did not use CrLG material. The device size for this comparison was also much larger: *L/W* = 96/96 µm; this may obscure the impact of lateral dopant diffusion during melt. Initial experiments using phosphorus MLD and FLA were not successful in devices smaller than *L/W* = 48/96 µm.

7.3.2 Pathway D: Successive Crystallization and Activation FLA

Pathway D incorporates monolayer doping, chromium large-grain morphology, and a double-FLA process with dopants introduced after crystallization. Samples of 60 nm PECVD a-Si on 6 nm Cr were lithographically patterned into initial crystallization mesas and coated with 100 nm PECVD SiO_2 as a capping layer before being crystallized with single-pulse FLA at bolometer-defined energy densities of 4.6, 4.8, 5.0, and 5.2 J/cm^2. After this, the capping oxide was selectively etched to create source and drain windows and the samples underwent MLD in the same chemistry

as Pathway C. Following the post-MLD capping oxide deposition, an activation anneal was carried out via FLA using intensities of 4.5 and 5.0 J/cm^2.

Figure 7.9 shows optical microscope images of Pathway D samples directly after the activation flash lamp anneal for each of the eight combinations of FLA intensities. Some differences in apparent silicon color are likely due to the SiO_2 capping layer, which has not been removed in these images. As in Pathway C, the thickness of capping oxide in the second FLA step varied between 100 nm in the doped regions and 200 nm in masked regions, resulting in optical distortions. Still, significant differences in crystallization behavior are obvious both from the radius of border exclusion in lower-intensity samples and the increased prevalence of large-area dewetting in doped regions. The increase in reflectance loss in masked regions is certainly a contributing factor; however, a change in light absorption due to surface modification by MLD cannot be ruled out. Interestingly, the increased likelihood of voids in doped regions appears to increase with *higher* initial crystallization intensity and *lower* FLA activation energy, suggesting more complex interactions with MLD-impacted surfaces.

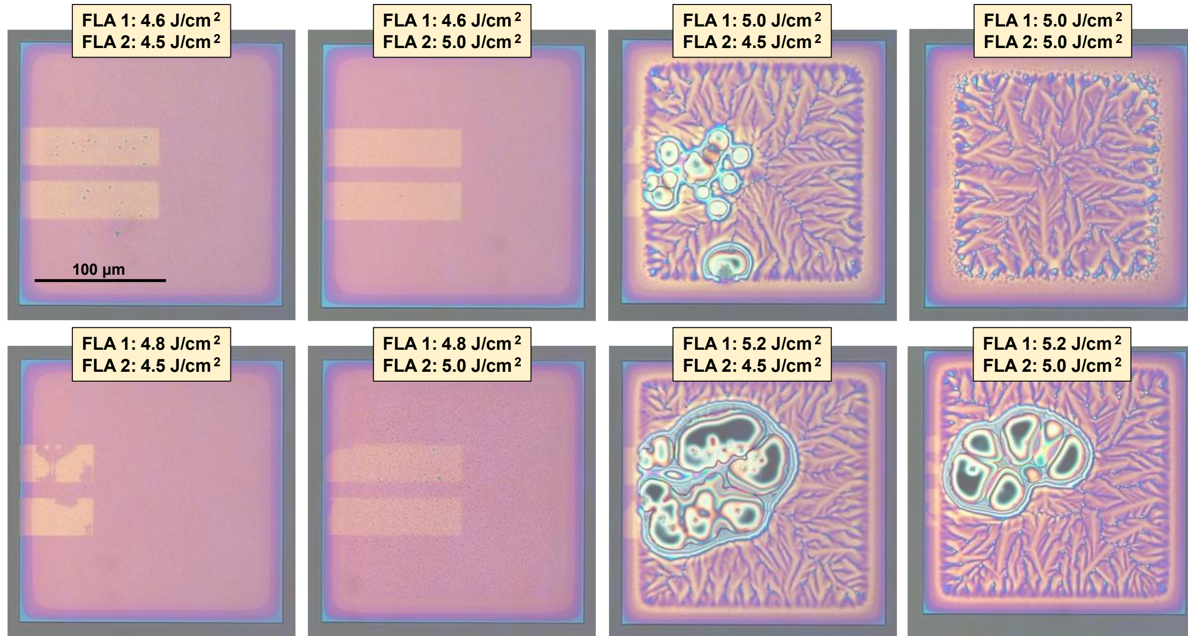

Figure 7.9: Optical micrographs of Pathway D mesas, CrLG MLD with separate crystallization and activation FLA stages. Crystallization FLA took place at 4.6 – 5.2 J/cm^2, while activation FLA was at either 4.5 or 5.0 J/cm^2.

Devices produced using Pathway D did not behave as anticipated; no repeatable and sensible electrical data could be obtained. When anything approaching transistor-like behavior was found, it behaved as a p-type device rather than the n-type function expected of a silicon device doped with phosphorus. Figure 7.10 shows this anomalous electrical behavior, which may be the result of chromium contamination in the silicon acting as a p-type dopant or invasion of the aluminum contacts into the silicon source and drain. As this unintended source of holes is present throughout the entire silicon mesa, it is likely a contributing factor to the elevated off-state leakage of all CrLG devices. The fact that it is the dominating behavior of Pathway D devices indicates that very little of the intended n-type dopant has activated.

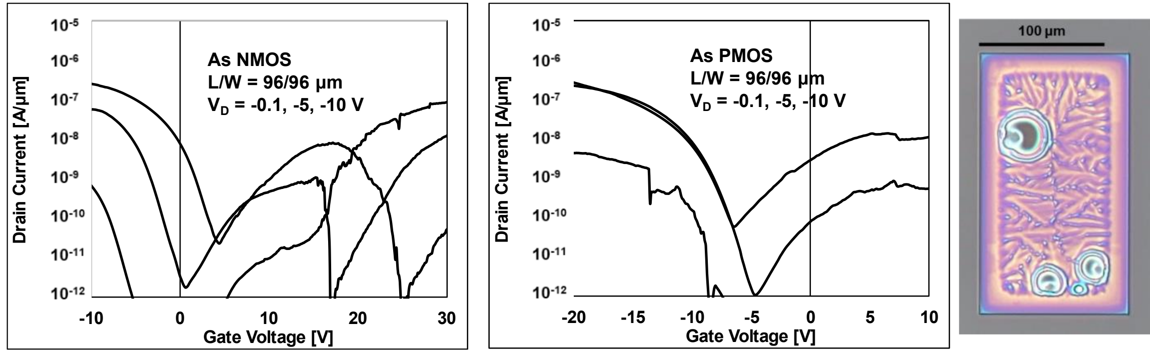

Figure 7.10: Anomalous and irregular p-type behavior demonstrated by the presumably n-type Pathway D CrLG MLD devices, indicating a total failure of MLD phosphorus to activate in these conditions.

The significant difference in behavior between devices produced via Pathways C and D suggests that monolayer doping is not easily activated with flash lamp annealing. Merely increasing the temperature of the LTPS layer for a sub-millisecond duration does not provide surface-adhered dopants with enough force to both incorporate into the bulk of the solid phase silicon film and reach electrically active lattice sites. Pathway C successfully activates MLD phosphorus by taking advantage of the melting and recrystallization of amorphous silicon. The free mass transfer of the brief liquid state allows dopant molecules on the surface of the silicon to become incorporated into the silicon body. From this position, dopant activation becomes possible. Unfortunately, this mechanism of dopant transfer is the same process by which large-scale lateral diffusion causes dopants in FLA to invade a purportedly-intrinsic channel, significantly hindering device scaling.

In Pathway D, the energy densities for the activation FLA were set below the level needed to re-melt an already crystallized silicon layer. Without melting, there was no driving force to facilitate dopant atoms at the surface interface to enter the silicon. It is likely that the remnants of the MLD layer after the second FLA step were removed from the sample along with the capping

oxide removal. Monolayer doping of thin silicon films, especially CrLG, is not compatible with post-crystallization FLA activation.

A secondary FLA step with a much higher intensity might succeed in activating MLD on thin LTPS by re-melting some or all of the silicon layer. However, the energy delivered through FLA would need to be significantly greater, as polycrystalline silicon is more transparent than amorphous silicon in the visible light spectrum and also has a higher melting temperature. This tactic would thus be self-defeating by irreversibly damaging the CrLG structure. The frequent presence of voids and dewetted areas in the doped regions of Pathway D suggest that the consequences of multiple FLA exposure may already be a factor in mesa integrity.

7.4 INTEGRATED STRATEGY SUMMARY

Four different pathways of producing n-type FLA LTPS TFTs have been explored here, representing different combinations of three integrated fabrication strategies. These pathways are compared again for clarity in Table 9, selecting devices that were crystallized and activated with FLA pulses of 5.0 J/cm^2. As mentioned immediately prior to here, Pathway D devices were regrettably nonfunctional due to a lack of redistributive force driving the surface-adhered dopants into the already-crystallized CrLG body.

Table 9: Comparative results of devices produced from each strategy in this chapter, with FLA settings of 5.0 J/cm²

	Path A: **Single-FLA implanted CrLG**	**Path B:** **Multiple-FLA implanted CrLG**	**Path C:** **Single-FLA MLD CrLG**	**Path D:** **Multiple-FLA MLD CrLG**
Dimensions (L/W)	12/24 µm	12/24 µm	12/24 µm	--
V_T (V)	4.6	14.7	12.9	--
$\mu_{chan:max}$ (cm^2/Vs)	68.6	30.1	10.9	--
$I_{(VT+10)}/I_{min}$	1.0×10^5	1.9×10^5	9.6×10^6	--
SS_{Min} (V/dec)	2.17	2.50	0.719	--

Each of these pathways utilized CrLG LTPS morphology for its consistency and resistance to dewetting. The experiments shown here are comparable to previous results demonstrated in Chapters 4 and 5, which are collected in Table 10. Again, FLA energy density is kept consistent at 5.0 J/cm^2, and no furnace activation steps are incorporated, making these true low-temperature processes. Though promising and comparable electrical results were shown with long furnace anneals of 630-700 °C, this temperature range strains both the thermal limitations of the glass substrate and the credibility of the term “LTPS”. Thus, furnace-activated results are not included in this comparison.

Table 10: Comparative results of devices demonstrated earlier in this document, produced in methods similar to that of Table 9 but without CrLG morphology.

	Comparison with Path A: **Proof of Concept**	**Comparison with Path B:** **Full-FLA Scalable Process**	**Comparison with Path C:** **Initial MLD Phosphorus**	**No extant comparison with Path D**
Presented in:	Section 4.2	Section 4.6	Section 5.3	--
Dimensions (L/W)	32/100 µm (25/93 eff.)	12/24 µm	96/96 µm	--
V_T (V)	0.23	3	-1.5	--
$\mu_{chan:max}$ (cm^2/Vs)	380	300	61.3	--
$I_{(VT+10)}/I_{min}$	~8×10^6	1.59×10^6	5.8×10^3	--
SS_{Min} (V/dec)	0.118	~2.8	1.4	--

Comparing these results, it is clear that FLA-only CrLG LTPS suffers from significant interface traps which heavily affect its threshold voltage. The rightward V_T shift in CrLG strategies is frequently over 10 V, as compared with < 3 V for similar non-CrLG experiments. This may be due to two factors which were not considered prior to this comparison. First, phosphorus is very likely to segregate out of silicon and into interfaces and grain boundaries during a melt-phase transition. The edge-oriented crystal growth and sharp boundaries of CrLG discourages phosphorus from staying in the silicon body and may even push more dopant into grain boundaries in the channel. Second, the CrLG devices shown in Chapter 6 all experienced a furnace anneal for dopant activation. While FLA is clearly capable of activating phosphorus in CrLG, the long heat treatment at > 600 °C is needed for chromium present in the silicon layer to redistribute into discrete agglomerates. It seems that the as-crystallized chromium distribution of large hemispherical protrusions and smaller regions on the upper Si-SiO_2 interface may have a larger impact on the device's electrical behavior.

Interestingly, the single-FLA MLD Pathway C shows demonstrable improvements over the initial experiments with MLD phosphorus, especially in subthreshold swing and on/off ratio. Though this may be attributed to improved process control and increased experience with a novel technique, it could also suggest that CrLG is a superior LTPS morphology for MLD dopant activation when compared with randomized void material. This, again, can be explained by phosphorus's tendency to segregate to the interfaces of LTPS: The perimeter of each void in randomized-void LTPS is effectively another interface at which phosphorus can accumulate, thus preventing it from acting as a donor source. This is more significant in an MLD strategy than in ion implant because the phosphorus dose is much smaller and limited by the physics of a-Si surface chemistry. With MLD phosphorus, a loss of 90% of introduced dopants may reduce active donor concentration to levels that impede device operation. However, channel mobility in the MLD CrLG device is still much lower, most likely due to the additional scattering centers of non-redistributed chromium at the Si-SiO_2 interface.

In short, the impact of chromium redistribution in CrLG is more significant to device operation than previously considered. Without a furnace anneal to convert the LTPS from as-crystallized to post-process structure, increases in interface traps and scattering centers in the channel conduction pathway significantly impact threshold voltage and carrier mobility. This effect persists whether a single- or multiple-FLA process is used. Though MLD and CrLG techniques were proven to be compatible with phosphorus n-type devices when doped prior to FLA crystallization, a multi-stage FLA process has yet to produce measurable activation with surface-adhered monolayer dopants.

7.5 ADDITIONAL FABRICATION STRATEGIES

Several other fabrication strategies which have been introduced in this work were left out of this experimental design for reasons of coherence and narrowness of scope. Each of these are worth further analysis in a future experiment.

Preamorphization implants, as discussed in Section 4.4, were shown to improve device mobility and current output in void-associated LTPS morphology, likely by allowing a more thorough regrowth through solid phase epitaxy. Silicon ion self-implant, in particular, allows for increased dopant activation at glass-compatible furnace temperatures without changing the chemical makeup of the LTPS. However, the reliance on a complicated ion implantation of an non-traditional implant species makes this technique less valuable for eventual industrial application, even more so than standard ion implant doping.

Concurrent with preamorphization, self-aligned devices were demonstrated in section 4.5. This device structure was explored to improve scalability by eliminating opportunities for lithography error and using gate formation to define channel areas. Using this process, relatively small TFTs could be produced with more consistency and sharper operation at low drain bias. However, the loss of gate control at drain biases greater than 3 V represents a significant downside that has not yet been addressed. Further, the molybdenum used as a gate material has unknown compatibility with MLD and would certainly interfere with crystallization in an initial-doping strategy.

Bottom gate devices, as discussed in section 4.7, represent an alternative TFT configuration with many desirable traits. Using transparent ITO as a gate material, very high carrier channel mobility was obtained in devices with channels shorter than 8 μm. This form of bottom-gate LTPS TFT is an underexplored strategy that may help open up a very limited design space in p-type BG

TFTs. However, the fragility and variability of these devices, even on randomized void-associated LTPS, would make effective comparisons difficult when combined with other techniques. The addition of gate structures underneath the silicon layer presents a significant degree of procedural complication for chromium-underlayer crystallization and was not addressed in this comparative experiment.

Finally, chromium was shown to encourage edge-directed crystallization as a thin overlayer as well as an underlayer. In this configuration, the distribution of TEM-visible chromium after crystallization was mostly confined to a layer of hemispherical protrusions at the upper surface of the silicon layer. The intruding metal is thus physically accessible and may be able to be removed with a targeted etch, reducing the degree of electrical impact. However, comparative EDS suggests that this chromium is likely bound up in silicides which are difficult to selectively remove from polycrystalline silicon. Removal of the upper chromium-aggregate region would require shaving down the thickness of the entire silicon layer, which is challenging at these dimensions. Further, distribution of some metal to the lower silicon/SiO_2 interface indicates that minute metallic contamination is likely throughout the silicon body.

Chapter 8. CONCLUSIONS

The focus and intent of this work was to explore and characterize crystallization of LTPS by FLA at a morphological and electrical level, towards its potential implementation as a technology for TFT backplanes on unconventional substrates. The following accomplishments demonstrate this goal to be attained.

- Unified and characterized the existing, neglected field of FLA LTPS by continuing existing research and identifying areas of improvement. By exploring the variations of crystallization morphology produced in various implementations of this technique, a standardized process can be identified.
- Demonstrated numerous TFT configurations and fabrication strategies on FLA LTPS, including scalable self-aligned devices, preamorphization-enhanced activation, ITO bottom gate structures, and a single vs. multiple FLA crystallization and activation process for the reduction of processing temperatures.
- Introduced the emerging techniques of monolayer doping to FLA activation and used its unique factors to address existing challenges in FLA LTPS. Through this, demonstrated gallium MLD for the first time; using it, produced functional p-channel LTPS devices.
- Developed the novel material system of thin film silicon-chromium crystallization as a predictable and edge-directed alternative to existing FLA LTPS morphology. Characterized this material in depth to determine the distribution of chromium at various stages of fabrication and its impact on TFTs.

This chapter summarizes some of the findings demonstrated in this body of research and recommends future areas of study to establish FLA LTPS as a complementary technology for thin film semiconductors.

8.1 KEY CONTRIBUTIONS

8.1.1 Preamorphization-Enhanced Activation

Extending the research of Saxena and Jang [50], [51], a high-performance CMOS-compatible device process for FLA LTPS TFTs was demonstrated. However, lateral diffusion of dopants during crystallization was identified as a fatal flaw towards producing these devices at smaller, industry-required scales, necessitating the development of a scalable alternative. This was accomplished with a two-stage crystallization and activation scheme, which suffered from low dopant activation at temperatures friendly to display glass substrates.

To solve this issue, a pre-amorphization implant of silicon ions was introduced prior to doping to enhance activation by promoting solid-phase epitaxial regrowth. A partial amorphization improved device operation in a variety of ways, most notably increased channel mobility and reduced threshold voltage shift. This effect was verified to be caused by enhanced SPER by comparing it with a much more intense amorphization process to destroy surviving crystalline phrases. This resulted in extremely weak crystal regrowth during activation due to the dominance of nucleation as a crystallization mechanism.

This technique was extended to a more glass-friendly FLA-only strategy, proving that a multi-stage FLA process can take the place of the established furnace activation method. This

dramatically reduces the thermal budget and temperature limit of samples and moves closer to a true “low-temperature” process.

8.1.2 Monolayer Doping in FLA

MLD is a fairly recent technology [122] allowing a self-assembled layer of dopant-containing molecules to penetrate a crystalline surface. FLA was demonstrated to be capable of activating dopant layers produced on thin silicon films by this technique. MLD-doped phosphorus n-channel TFTs on FLA LTPS were demonstrated and characterized as a proof-of concept, thus enabling an alternative method of dopant introduction into this structure of device. The use of MLD to selectively dope regions of an amorphous solid was also demonstrated as a novel concept; FLA was able to simultaneously crystallize a-Si into LTPS and activate MLD-adhered dopants.

In addition, monolayer doping of gallium into silicon as a p-type dopant was demonstrated both in a bulk sample and a thin film. Using this technique, Ga-MLD p-channel TFTs on FLA LTPS were fabricated and characterized. This technique may be useful for producing thin film solar cells that are less vulnerable to light degradation at end-of-life.

8.1.3 CrLG – Chromium Distribution and TFT Impact

Though chromium has already been used as an underlayer for much thicker FLA LTPS [42], the extension of this system to the dimensions of thin film electronics resulted in many surprises and challenges. CrLG offers a significant advantage over a more randomized LTPS structure, as it is a predictable morphology that can be directed into various orientations by adjusting the geometry of initial a-Si mesas. In addition, the extent of its grain sizes is large enough to potentially

produce LTPS TFTs entirely on single grains, which would reduce unwanted scattering events at grain boundaries.

TFTs were produced on CrLG material to verify its utility as a semiconductor material. Though these devices were promising, a high degree of off-state leakage was noticeable along with other deleterious factors. CrLG was subjected to in-depth characterization to determine the potential causes of this device degradation. It was found that chromium distribution within this material took the form of hemispherical protrusions of chromium silicide out of the metal source layer after crystallization. Following further thermal treatments used to activate dopants in these TFTs, these $CrSi_X$ protrusions reconfigured into discrete agglomerations penetrating a consistent distance into the silicon thickness. To determine the impact of this agglomeration layer on TFT operation, devices were produced on CrLG of varying thickness. It was shown that as thickness approaches agglomerate invasion distance, a shifted threshold voltage precedes a sharp drop in carrier mobility, suggesting both the presence of buried charge around this layer and scattering centers within it.

8.2 FURTHER WORK

The breadth of topics addressed in this research necessarily result in areas that would benefit greatly from further investigation. The lateral proximity impedance effect of FLA crystallization, highlighted in Chapter 3 as a challenge to consider, has been discounted in the rest of this document by limiting focus to well-isolated LTPS mesas. However, a potential industrial integration of FLA would not have this luxury, needing instead to optimize production by maximizing available space.

Therefore, efforts to better understand this problem through advanced physical modeling and comparative experiments are still needed to create strategies for limiting its impact.

Regarding the structure of CrLG, it has been demonstrated that the redistribution of chromium in LTPS during post-crystallization anneal is both much greater than expected and much more significant to final electrical behavior. This suggests that gettering or physical removal strategies may be of interest following crystallization, at the point where invading metal is more mobile. Strategies involving long furnace anneals or very thick layers of LTPS are not feasible for TFT applications. Further, these investigations must be backed up with SIMS and deep level transient spectroscopy to truly quantify the metallurgical and electrical contamination caused by chromium. This analysis would also greatly benefit from X-ray photoelectron spectroscopy (XPS), especially for determining the bond structure between chromium and silicon as a vertical profile. Ion beam etching XPS is particularly suited to the isolated mesa requirements of FLA LTPS. Additionally, x-ray diffraction, though briefly attempted without success, may still be of use for determining favored crystal planes in CrLG material if analyzed from a statistical standpoint.

Lastly, several fabrication strategies have been highlighted in Section 7.5 as worthy of further research. The conjunction of preamorphization processes and self-aligned device structure has shown promising results in FLA LTPS TFTs, though this was limited to processing strategies that included long furnace anneals. A similar advancement may be possible using a full-FLA method, perhaps also with MLD replacing the costly and damaging ion implant. Most MLD chemistry is not compatible with the metal SA gates used here; however, thin polysilicon gates doped in the same process may be an effective replacement. The analysis of MLD by XPS would also greatly improve the understanding of when and how introduced dopants are bonded to the silicon surface and bulk, as well as highlighting any organic contamination.

In addition, ITO bottom-gate FLA LTPS TFTs may be promising when coupled with stricter FLA control and techniques to increase the robustness of the silicon channel, such as thicker metal-overlayer CrLG. As bottom-gate LTPS TFTs are extremely challenging through conventional laser annealing means, a consistent FLA-crystallized method would be a valuable expansion of the TFT backplane design space.

8.3 CLOSING REMARKS

It's no great surprise that the TFT research community is losing interest in LTPS, replaced with advanced amorphous oxide semiconductors and hybrid materials. After all, silicon has been the reigning champion of transistor materials for decades, and millions of pages of research have already been penned on its properties. In the eyes of many, LTPS is a solved problem. However, new advancements in AOS, especially p-type AOS, are piecemeal and sporadic, sometimes proudly boasting a hole mobility of nearly 10 $cm^2/(Vs)$ [145]. In the meantime, the existing methods of producing consistent, high-quality display LTPS struggle to keep up with demand, limiting throughput and usable substrate size on the manufacturing level.

FLA LTPS, for all its faults in spatial consistency and material replicability, represents a material which can be made with an appreciable fraction of the quality of laser-annealed LTPS and a much more efficient, overall cost-effective throughput rate. It's important to remember that the goal of consumer electronics is not to make the best device, but the best value for electronics manufacturers and consumers both. The problems associated with FLA LTPS material are solvable through numerous approaches, from advanced doping mechanisms to the inclusion of novel adhesion layers. Certainly, many strategies will prove to be ineffective and should be discarded after careful consideration, but the investigations must proceed before that consideration can be

made. The demand for larger, better, and more non-traditional format displays is only going to increase, and it is the job of research and industry to meet it.

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APPENDIX I: SAMPLE PREPARATION

The following is a detailed rundown of the processing steps used to produce FLA LTPS TFTs. Individual studies may have used slightly differing processes, as listed in the text.

- Begin with a substrate of 150 mm diameter, 500-600 μm thickness commercially-available display glass.
    - Corning Eagle XG for applications with thermal limits up to 600 °C or Lotus NXT for applications up to 700° C
- Deposit 200 nm PECVD SiO_2 with a silane precursor at a temperature of 400 °C as a barrier layer.
- In the same reaction chamber and without breaking vacuum, deposit 60 nm a-Si with a silane precursor at 400 °C.
- Anneal samples in a furnace at 450 °C for 30 minutes in nitrogen to dehydrogenate the a-Si.
- Pattern the a-Si layer into initial crystallization mesas using conventional photolithography and SF_6 RIE – 75 sccm, 100 W, 130 mTorr for 60 s (a significant overetch, but highly selective to SiO_2). Remove photoresist as usual.
- **IF DOPING PRIOR TO CRYSTALLIZATION**, go to doping section.
- Clean samples with a modified RCA clean to remove contaminants:
    - Piranha solution (H_2SO_4 spiked with H_2O_2) at 130 °C for 10 minutes
    - RCA SC-2 (300 ml each of HCl and H_2O_2 in water) at 75 °C for 10 minutes
- Deposit 100 nm PECVD SiO_2 with a TEOS precursor at a temperature of 390 °C as a capping layer.
- Crystallize silicon with FLA (more details can be found in Appendix 2 and in the section on activation by FLA)
    - Use external bolometer calibration to determine correct voltage settings for desired energy density. Drift is possible over a span of weeks.
    - Preheat sample to 400 °C with hotplate.
    - Expose sample to a single FLA pulse of 250 μs with desired voltage setting.
- **IF DOPING AFTER CRYSTALLIZATION**, go to doping section, then activation section.
- Remove capping/screen oxide with 10:1 BOE for 2-3 minutes, if applicable.
- Pattern the LTPS layer into final device mesas using photolithography and RIE as above.
- Clean samples with a modified RCA clean as above.
- Deposit 100 nm PECVD SiO_2 with a TEOS precursor at 390 °C as a dielectric layer.
- Anneal samples in a furnace at 400 °C for 30 minutes in nitrogen to densify the SiO_2 dielectric.
- Etch contacts through the SiO_2 dielectric using photolithography and 10:1 BOE for 4 minutes. Remove photoresist as usual.
- Metallize by depositing 500-800 nm aluminum via DC sputter, using a chamber pressure of 5 mTorr, 20 sccm Ar flow, and 1000 W sputter power.

- Etch aluminum into gate/source/drain lines using photolithography and Fujifilm 1961 aluminum etchant (or whichever etchant is preferred). Inspect samples prior to removing photoresist.
- Sinter samples in a furnace in 5% H_2/N_2 forming gas, first at 300 °C for 30 minutes and then at 450 °C for 30 minutes.

Doping section

Dopant introduction in this work was mostly performed through ion implantation for the sake of convenience. Implant settings were selected using Stopping and Range of Ions in Matter (SRIM), designed by James F. Ziegler and available online at www.srim.org, to ensure uniform dopant concentration in a 60 nm-thick silicon target through a 100 nm-thick screening SiO_2 overlayer. Roughly 1/4 to 3/8 of introduced dopants remained in the target layer; this can only be improved with lower energy implant, which was not possible with the system used.

The tool used in this experiment was a Varian 350D ion implanter set up for individual 6" wafers.

For ion implant:

- Ensure that the sample film stack consists of 100 nm SiO_2 on top of 60 nm silicon, depositing this screening oxide layer by PECVD if necessary.
- Create an implant mask with photoresist and conventional lithography, such that areas intended to be shielded from implant are blocked with > 500 nm of organic polymer.
- For p-type implant, select the ^{11}B peak from a boron trifluoride source gas with a beam current below 150 μA and acceleration voltage of 35 keV. Implant a dose of 4×10^{15} ions/cm^{-2}.
- For n-type implant, select the ^{31}P peak from a phosphine gas source with a beam current below 150 μA and acceleration voltage of 70 keV. Implant a dose of 4×10^{15}.
- Remove photoresist in oxygen plasma. Inspect before continuing to ensure complete removal.
    - For samples requiring both p- and n-type regions, remove and reapply photoresist mask as needed between implants.

For monolayer doping:

- Ensure that the sample film stack consists of 100 nm SiO_2 on top of the silicon layer, depositing this masking oxide layer by PECVD if necessary.
- Pattern the oxide layer with conventional photolithography and buffered oxide etch to expose the areas of silicon intended to be doped.
- Remove photoresist as usual. Subject wafers to a *very* brief HF dip to remove any native oxide growth from unmasked regions. (Native oxide does not grow quickly on thin a-Si layers)

- Immediately immerse samples into a prepared bath of MLD solution (detailed below) heated to 120 °C in a sealed argon environment. Ensure sufficient liquid exposure of surfaces to be doped.
    - For n-type phosphorus MLD: eight grams of Diethyl vinylphosphonate in 300 mL of mesitylene, sparged with argon for 15 minutes.
    - For p-type gallium MLD: four grams of Tris(2,4 pentanedionato)gallium(III) in 300 mL of mesitylene, sparged with argon for 15 minutes.
- Briefly wash samples in successive baths of toluene, acetone, methanol, and water, then dry with nitrogen gas.
- Immediately cap samples by depositing an additional 100 nm of PECVD SiO_2

Activation section

IF DOPING PRIOR TO CRYSTALLIZATION, do not use this section. This section is only necessary for process flows in which dopants are introduced into already-crystallized LTPS.

For furnace activation:

- Ensure all photoresist has been fully removed from samples with oxygen plasma or piranha solution.
- Anneal samples in a wafer furnace for 12 hours at 600 – 700 °C in nitrogen.
    - Do not exceed the thermal limitations of the glass substrate.
    - Ramp temperature up to activating temperature *slowly*, including a 30-minute stabilization step at 600 °C if higher temperatures are used.
    - Ramp temperature down to room temperature *slowly*, preferably for more than four hours. Rapid temperature shifts will cause the substrate to warp.

For flash lamp activation:

- Load samples, one at a time, onto a 400 °C hotplate for preheating, using an unpolished silicon wafer as a carrier.
    - Anneal only a quarter of a 6” wafer at once, centering that quarter under the quartz exposure window. Other areas should be masked with silicon wafer pieces.
- Expose samples to a single FLA pulse of between 4.0 and 5.2 J/cm^2 with a duration of 250 µs.
    - Multiple pulses are possible and may improve crystal regrowth, but can also lead to dopant deactivation.
- Unload samples to a separate surface or chill plate, handling only the silicon carrier wafer. Allow samples to cool fully before handling directly. Glass may visibly flex or contract if cooled too quickly.

APPENDIX II: FLA SYSTEM AND SETTINGS

Flash lamp annealing in this work was performed with a NovaCentrix PulseForge 3300 photonic curing system. This tool is equipped with two quartz-jacketed xenon flashbulbs in a reflector chamber designed to direct as much light vertically through the exposure window as possible. Each lamp is powered by a bank of five high-voltage capacitor drivers, with one driver emitting a low-power simmer current while the capacitors are charged to improve consistency during high-frequency pulse repetition. The system is continuously cooled with deionized water.

As in all systems, there is a tradeoff between the total amount of energy delivered in a single pulse and the duration of the pulse in which it is delivered. A longer pulse duration can deliver a larger sum of energy, but in doing so the rate of absorbance and heating is counterbalanced by the increased degree of heat dissipation through natural cooling. In this research, a pulse duration of 250 μs was chosen for consistency and a total heating-cooling cycle bounded by one millisecond. The PulseForge 3300 is capable of safely delivering a maximum of 6 J/cm^2 within this duration, corresponding to a power of 24 kW.

The shortest pulse duration possible using this tool is 100 μs, though this resulted in greater variation in energy output. A maximum energy density of ~4 J/cm^2 was deliverable under these settings. Pulse energy density cannot be directly adjusted; it is a function of lamp voltage and pulse duration. The energy density of a pulse is measured using an external bolometer with a blackbody absorbing sensor, assuming no losses to reflectance or absorbance. Thus, all FLA settings listed in J/cm^2 are significantly greater than the amount actually absorbed by the silicon layer. An absorbance percentage of 30-40% is expected, with variance based on sample preparation and geometry.

The exposure window in the PulseForge 3300 is a 7 cm by 13.5 cm rectangle, though variations in incident light angle can result in annealing nonuniformity at the edges of this area. For uniformity, 150 mm-diameter circular samples were annealed with a multiple-shot approach by physically masking off non-focus areas with pieces of silicon wafer. The maximum area annealed in a single exposure was less than 5 cm by 10 cm.

Samples were preheated to 400-500 °C using a separate hotplate, the accommodation of which required some adjustment to the PulseForge structure. A blank silicon wafer was used as a carrier to prevent handling of glass wafers during thermal stress and to promote uniform heat distribution from the hotplate.

Appendix III: Microscopy Data

SEM

- The imaging tool used is a TESCAN Mira3 Scanning Electron Microscope equipped with a lanthanum hexaboride field-emission source.
- Samples were cleaned with oxygen plasma prior to imaging.
- Conductive sputter was avoided unless electron charging significantly impacted imaging. The text indicates when gold sputter became necessary
    - Sputter thickess is unknown but presumed < 60 nm
- Magnification and acceleration voltage were significantly varied between images and are listed on the label of each individual image.

TEM

- The imaging tool used is a FEI Titan G2 80-200 kV ChemiSTEM system.
- Samples were prepared with a FEI Quanta 3D FEG 600 focused ion beam. Some samples are coated with carbon, platinum, or both as protection layers. These elements do not factor into any chemical analysis.
- Magnification for all EDS and "wide-angle" images is 160 kx, with a 200kV accelerating voltage. For higher magnification images, consult sizebars.

AFM

- The imaging tool used is a Bruker Multimode 8 AFM system operating in tapping mode.
- AFM tips were Bruker RTESPA-300 antimony-doped silicon tips with a rectangular tip radius of 8 nm and a frequency of 300 KHz.
    - These were selected due to their high spring constant of 40 N/m. Triangular silicon nitride tips showed a high degree of failure and breakage.
- Samples were cleaned with isopropyl alcohol and oxygen plasma prior to scanning and affixed to magnetic pucks with adhesive tabs.
- After scanning, AFM data was processed with Gwyddion software package, available at www.gwyddion.net, to level scans and remove particulate errors.