7-5-2023

RF Device Characterization of Graphene Transistors

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RF DEVICE CHARACTERIZATION OF GRAPHENE TRANSISTORS

By

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Thesis

Submitted in Partial Fulfillment of the Requirements for the Degree of MASTER

OF SCIENCE IN ELECTRICAL ENGINEERING

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July 5, 2023

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ACKNOWLEDGEMENT

Three people I would like to thank without whose support this thesis would not have been possible. Firstly, my thesis advisor Dr. Ivan Puchades whose continuous guidance and help in making me reach and stretch my thinking and analysis on the characterization of the transistors and his assistance in making me learn every step of the measurements done in the Semiconductor Device Characterization Laboratory possible. Secondly, Dr. James E. Moon who has been a pillar in making me learn semiconductor device physics and transistors. His constant help in clearing my doubts and rectifying my faults at every instant along with his immaculate detailing, understanding of the subject and patience has always been an inspiration for me to reach the unknown and made the electrical and microelectronic education so much meaningful and worthy. Thirdly, Dr. Santosh K. Kurinec who has not only taught but walked me literally through each and every step of fabrication the knowledge which she imparted has been indelible in making this thesis come together. Her dexterity in fabrication has helped me learn and explore the world of semiconductors from the very onset. Lastly, PhD. Candidate in our research group William Huang without whose design and fabrication of the devices they would not have been characterized in the first place. Additionally, Dr. Sean L. Rommel for always believing in me and guiding me throughout.

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ABSTRACT

Radio Frequency performance of field-effect transistors has been explored in depth, experimented and industrially in use since a long time. Whenever one thinks of transistors which could take us to the regime of more than 1 THz in frequency it would always be the High Electron Mobility Transistors (HEMTS) as the perfect solution to that. The Graphene transistors have been very much in research from 2010 and promise equal results due to their huge potential in mobility. In the Semiconductor Manufacturing And Fabrication Laboratory at the Rochester Institute Of Technology our research group has been designing, fabricating and characterizing the graphene transistors of top-gated and back- gated varieties of which the former has been more explored and characterized because of its potential in high frequency performance.

In this thesis characterization of both the top-gated and the back-gated varieties will be discussed in intricate detail with different permutation and combinations in experiments in order to depict the efficiency of these transistors in terms of their frequency characteristics and the possible ways to optimize the mobility and transconductance, thereby changing the hysteresis behaviours of the top-gated transistors. The maximum oscillation frequency has been explored for the top-gated variant where it can be estimated how they are in performance and exhibit unique nature compared to that of the PMOS and the NMOS devices along with this distinctive hysteresis behaviours by application of a polymer on GFETs has been investigated.

Chapter I. Introduction

Graphene as a material has been a subject of research for more than a decade ever since its discovery by Andre Geim and Konstantin Novoselov who were awarded the Nobel prize for the same in 2010 [1]. Starting with the developments made in the field of wearable electronics such as biosensors and other such wearable sensors as such especially those used in healthcare have proved to be helpful. Graphene proves as the material which is the heartstring of such sensors. The Graphene sensors prove to be most useful because of their adaptability to be made into different types of structures [2]. The growth process for the sensors based on Graphene is somewhat different from that which are used for the Graphene transistors (GFETs) in general.

Here CVD forms the main process of growth and there is no such transfer process as is common for that of the GFETs. Research has shown that for detection of body motion and acoustic waves [2] CVD-grown Graphene on Ni foam is more useful that that grown on Cu foils.

Further down the line if research be conducted then the Graphene-based sensors show huge potential for telemedicine [3]. The unique properties of this one atom thick material such as high carrier mobility or high electron velocity has propelled researchers across the world to probe further into making field-effect transistors with this material. Such devices are used for high frequency response GFETs with frequency ranges up to 1 THz. The reason for this high frequency is obviously the mobility close to 200,000 $cm^2\,V^{-1}s^{-1}$ and 350,000 $cm^2\,V^{-1}s^{-1}$ of

these GFETs [5,67].

A lot of work has been conducted to generate high values for the cut off frequency (f_t) and maximum oscillation frequency (f_{max}). The immediate comparisons of these GFETs can be done with High Electron Mobility Transistors (HEMTs). To achieve the THz range is to work on the plasmonic for these transistors which are to create a 2D electron gas channel which can be used to excite the plasmons at THz frequencies by means of oscillation.[15] DC current excites the plasmons to drift with the 2D electron fluid in the HEMT channel. This results in the electron drift which causes the Doppler Shift in the plasmon dispersion.

The Doppler Shift is principally a change in frequency of a wave in relation to the observer moving in relation to the source. Here the electron drift is the main cause for the Doppler Shift as it is moving relative to the plasmon dispersion and hence a change in frequency takes place. Reversal of the Doppler Shift maybe caused by the plasmon reflection and hence an enhancement in plasma wave amplitude may occur.[15] Dyakanov and Shur have an instability theory which states that if the plasmon reflection conditions are asymmetric, the amplitude of the plasma wave increases exponentially provided that the plasma wave gain exceeds the damping losses. In this process the energy of the dc current passes to the plasma wave [16]. This type of instability is the most pronounced among all the other instabilities. The asymmetry required to produce this instability is produced by the reactive impedances between the gate and source contacts as seen in Fig. 1 [16]. All the above phenomena can be eased with Graphene as this material has the potentiality to have great plasmonic resonances with its great carrier mobility. Various

recent experiments have been conducted to explain this theory. Some have even reported resonant detection of THz radiation in GFET resonant cavities [16]. Unfortunately, the studies are largely theoretical in nature at the most.

In the case of GFETs the spectra of the plasma waves are linearized from the hydrodynamic equations in the presence of the steady electron drift with a particular velocity [16]. Jornet et al. produced comprehensive studies on the numerical and hydrodynamic analyses for the GFETs which was useful for generating on-chip plasma generator for wireless communications.

The motivation for our research group is to fabricate and characterize the GFETs to have a high value for the cut off frequency (f_t) and maximum oscillation frequency (f_{max}). The first point for this comes from the HEMTs as was mentioned earlier. The reason behind this is that the cross section of these transistors is very similar to our GFETs without the use of such complex crystallography that we want to fabricate as well as the fact that the mobility of these transistors is what Graphene is capable of reaching to further enhance the values of the f_t and f_{max} to the region 1 THz. We have found from our prior experiments that the gain of the GFETs made in our SMFL matches with the commercially available HEMTs in some ways. Also our motivation extends to the NMOS that have a value as high as the HEMTs in such cases and we intend to compare and study the characteristics with them as well for better understanding and analysis.

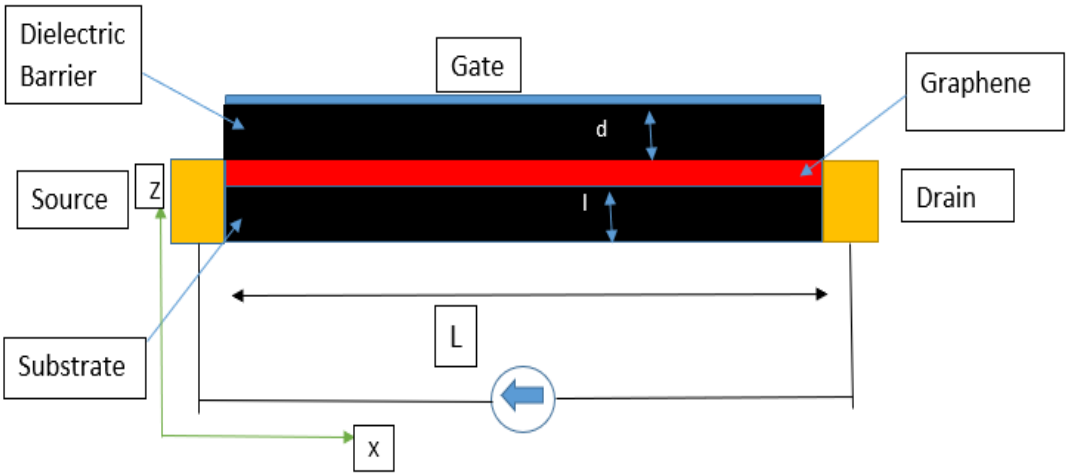


Fig. 1:- Schematic explaining the Dyakanov Shur instability in a GFET[16]

The small signal model has duly been adhered to follow the characterization of the GFETs manufactured at RIT SMFL. Instead of going into further adjustments of the gate length, channel length or a change in the dielectric the effort to bring changes to the nature of the mobility has been explored by the application of an electron donating amine rich polymer by means of coating on the devices. The objective behind that was three-fold that this step would trap the interface trap charges, reduce Coulombic scattering at the Graphene interface and reduce the capacitances henceforth which serve as a major impediment in case of frequency measurements.

Chapter II. Literature Review

A plethora of papers and books have been reviewed to study in detail the effects of Graphene, its usefulness in field effect-devices and all its transfer characteristics. Fabrication has been studied quite extensively where a lot of motivation for the author has come regarding the transfer process of the material. This is because the study of the transfer process will lead to the minimization in the defects produced in Graphene such as wrinkling. Study has also been conducted on the nature of the f_t and f_{max} whose characterization is the goal of the author. Fundamental explanation of an E-K diagram with the Dirac Point on the right has been shown in Fig. 2.

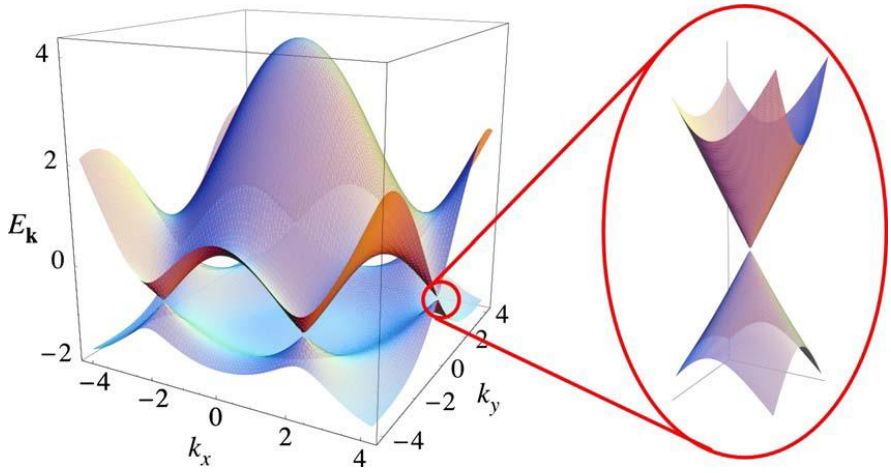


Fig 2 :- Electronic dispersion in the honeycomb lattice. Left: energy spectrum (in units of t) for finite values of t and t', with t = 2.7 eV and t' = −0.2*t*. Right: zoom in of the energy bands close to one of the Dirac Points. [66] Reprinted figure with permission from The electronic properties of graphene by Neto, A. H. Castro; Guinea, F; Peres, N. M. R ; Novoselov, K. S; Geim, A. K Reviews of modern physics, 01/2009, Volume 81, Issue 1 Copyright (2009) by the American Physical Society.

2.1 Discussion of MOSFETS and Comparison with GFETs

Starting with Lillienfield and Heil's patents in 1926 and 1934 with much momentum gathered after Atalla's work in 1959 MOSFETs were a subject of interest research and form the basis of any electronic device that we use today. A normal NMOS or a PMOS transistor is composed of three terminals source, drain and gate with a dielectric layer between the gate and the substrate which is usually Silicon Dioxide with a particular dielectric thickness. The role of this layer of dielectric is to support the electric field that enables the inversion of the carrier type at the Si surface [18]. The mention of the inversion layer is very important because it comes into play when a gate bias is applied. A positive gate bias on a NMOS transistor places a lot of positive charges on the gate of the transistor and hence these charges cause the repelling of the holes present at the surface which are positively charged. This application of a positive gate bias also makes the surface susceptive to the entry of more number of electrons through the n+ regions of the transistor where the concentration of them is already in quite a huge number there [19]. This is what is known as the inversion phenomena where in a p-type substrate instead of holes being present now is replaced by electrons. The intensity of inversion is weak, moderate or strong with the amount of V_{gs} which is applied. The reason for the three regions to be named so is because every one of them show distinct characteristics [19]. The inversion phenomenon is the same for PMOS transistor as well except for the fact that the gate bias now to be applied will be negative instead of positive. The current in this inversion layer is made up of two components namely the drift current and the diffusion current.

Considering the case of the drain source voltage V_{ds} and its value being gradually increased

from ‘0’ then at the smaller values of the V_{ds} the impact on the drain current is large but however when the value of the V_{ds} is large then the drain current tends to saturate which means that the value of the V_{ds} is so large that it drains all the available electrons from the channel for a given value of V_{gs} [19]. This is a phenomenon which is a characteristic for both the PMOS and the NMOS. Fig. 4 shows the schematic and mechanism of an NMOS device.

In a stark contrast to both the PMOS and the NMOS, GFETs do not saturate at all for any given value of the V_{ds}. This happens due to the fact the GFETs do not have any band gap for them which is largely responsible for saturation and a channel pinch off [29]. So, saturation in GFETs does not occur normally citing the works of previous people like Han et. al who has proved that the presence of a very thin dielectric full drain current saturation takes place in GFETs [55]. This thinness in dielectric is very much responsible to make the gate bias V_{gs} be comparable to the drain bias V_{ds} and the Dirac Point which is the point where the conduction and valance bands meet shift in the positive or negative direction indicating that there is the presence of saturation [29]. The role of different dielectrics for the GFETs shall be discussed in detail later. Another method which has recently been adopted by a group of researchers at UC Irvine led by Liu et al. in 2013 found the mechanism of the Negative Differential Resistance (NDR) to be more effective than the conventional methods of introducing an artificial band gap like application of an electric field, quantum confinement of carriers in nanometer scale ribbons, surface functionalization with various atoms etc to be more effective [30]. The fabrication procedures were quite similar to the normal methods of fabrication like transfer of exfoliated Graphene on Si/SiO_2 substrate and applying the thin film deposition of Al_2O_3 by ALD and ultimately creating a dual-gated structure with the heavily doped Si substrate acting as the back gate [30]. At larger values of the back gate voltage V_{bg} the reduction of the Dirac Point conductivity was

shown but more than that what induced the NDR to take place was to set one terminal at variable input while the other terminals were fixed at constant values. For the ID VG measurements keeping the V_{ds} and the V_{bg} are fixed while the top gate voltage V_{tg} is swept to control the I_D. The NDR effect is revealed when the V_{ds} and the V_{tg} are swept simultaneously. Fig. 3 shows how NDR decreases if the drain and gate are connected [30]. In other research it also suggests that the NDR also depends on how fast the carriers are depleted in the channel. That is to say the total number of carriers decreases as the V_{ds} increases [31].

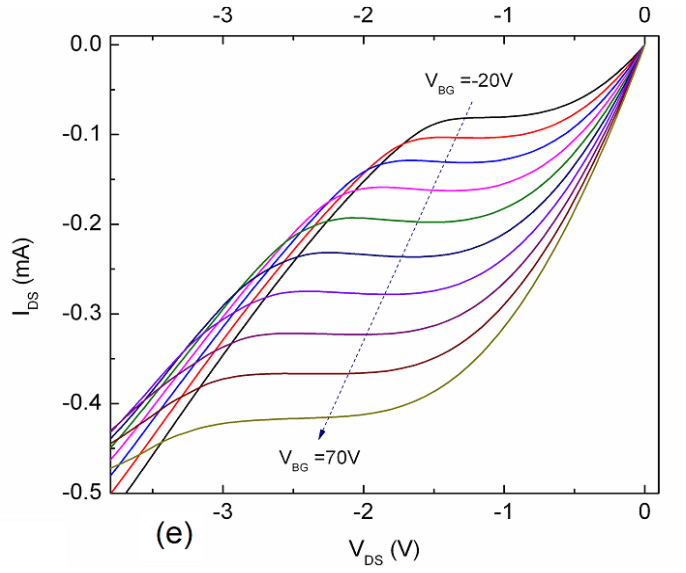


Fig. 3:- Connecting the drain with the gate, and applying the bias *VDS=VTG* from 0 to -4 V. The NDR effect becomes much weaker.[30] Reproduced from Liu, Guanxiong, et al. "Graphene-Based Non-Boolean Logic Circuits". Ithaca: Cornell University Library, arXiv.org, 2013. *ProQuest.* Web. 20 June 2023, with the permission of AIP Publishing.

The governing equations of current for a p-channel MOSFET and a n-channel MOSFET are as follows.

N - Channel MOSFET

$$I_{DS} = \mu C_{ox} \frac{W}{L}[(V_{GS} - V_T)V_{DS} - V_{DS}^2](1 + \lambda V_{DS}) \quad \{\text{NON-SATURATION}\} \quad (1)$$

$$I_{DS} = \frac{1}{2}\mu C_{ox} \frac{W}{L}(V_{GS} - V_T)^2(1 + \lambda V_{DS}) \quad \{\text{SATURATION}\} \quad (2)$$

P - Channel MOSFET

$$I_{DS} = \mu C_{ox} \frac{W}{L}\left[\{(V_{GS} - V_T)V_{DS} - \frac{{V_{DS}}^2}{2}\}(1 + \lambda V_{DS})\right] \quad \{\text{NON-SATURATION}\} \quad (3)$$

$$I_{DS} = \frac{1}{2}\mu C_{ox} \frac{W}{L}(V_{GS} - V_T)^2(1 + \lambda V_{DS}) \quad \{\text{SATURATION}\} \quad (4)$$

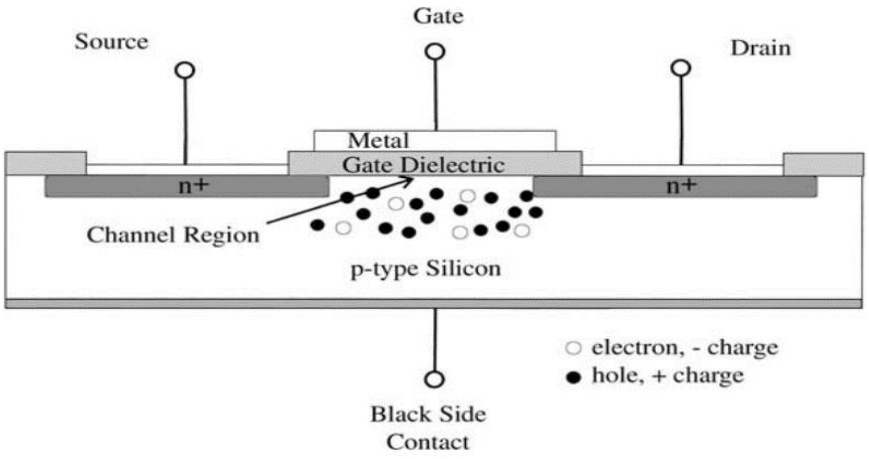


Fig. 4 :- Standard schematic diagram of a N-Channel MOSFET [18] Reproduced with permission from Springer-Verlagberlin / Heidelberg

Similar to the PMOS and NMOS the GFET as shown in Fig. 4 also has the three structures source, drain and gate but the topology of the transistor is different for that in comparison with that of the MOSFET. But in this case the transistors can be made back-gated as well as top-gated. A further in-depth discussion of the two types of the structures will be carried out in the

following sections (2.2 and 2.3) which will elucidate the fact how the GFETs function and further make clear how they are different in operation despite having many similarities with the MOSFETs. The current governing equation for the GFETs both top and bottom gated are as follows.

$$I_{DS} = \mu \frac{W}{L} \int_{VCS}^{VCD} Q_{TOTAL}(V_C) \frac{dV}{dV_c} dV_c \quad (5)$$

The quantity $\frac{dV}{dV_c}$ is defined as $1+\frac{C_q(V_c)}{C_t + C_b}$ and the total charge is given by $Q_{total} = \frac{q\pi(kT)^2}{3(\hbar v_F)^2} + \frac{q^3 {V_c}^2(x)}{\pi(\hbar v_F)^2} + \boldsymbol{\eta}_{puddle}$ where '$\boldsymbol{\eta}_{puddle}$' is defined as $q\Delta^2/\pi(hv_F)^2$.

In the above equations '$C_q(V_c)$' is the quantum capacitance at the voltage drop across the Graphene layer, $'C_t' \, and \, 'C_b'$ are the top and the bottom gate capacitances, respectively, further having the expressions of $C_t = \frac{\varepsilon_0 \varepsilon_t}{L_t}$ and $C_b = \frac{\varepsilon_0 \varepsilon_b}{L_b}$. [25] Here $'V_c(x)'$ is the voltage drop across the Graphene layer and x = 0 at the source end and V(x = L)= V_{ds} at the drain end of the channel, 'k' is the Boltzmann's constant, 'T' is the temperature, $'\hbar$' is the reduced Planck's constant 'v_F' is the Fermi velocity which is defined as $v_F = {}^{3a\gamma_0}/_{2\hbar}$ where γ_0 = 3.16 eV.

The drain current equation is usually obtained by integrating over the length of the channel using V_C as the integration variable. However, it is to be noted that $\frac{dV}{dV_c}$ is specified here for a top and bottom gated structure and not individually. If a top-gated structure is considered then $1+\frac{C_q(V_c)}{C_t}$ will be the expression and if a bottom-gated structure be considered then $1+\frac{C_q(V_c)}{C_b}$

will be the expression. As mentioned earlier there is no saturation that takes place for GFETs, hence only a single equation is defined.[25]

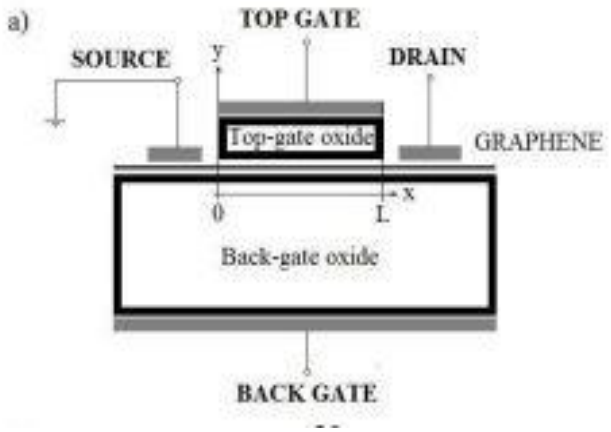


Fig. 5 :- Cross section of a top-gated GFET [25] © July 2016 IEEE.

2.2 Capacitances of MOSFETS and GFETS which influence the Frequency response

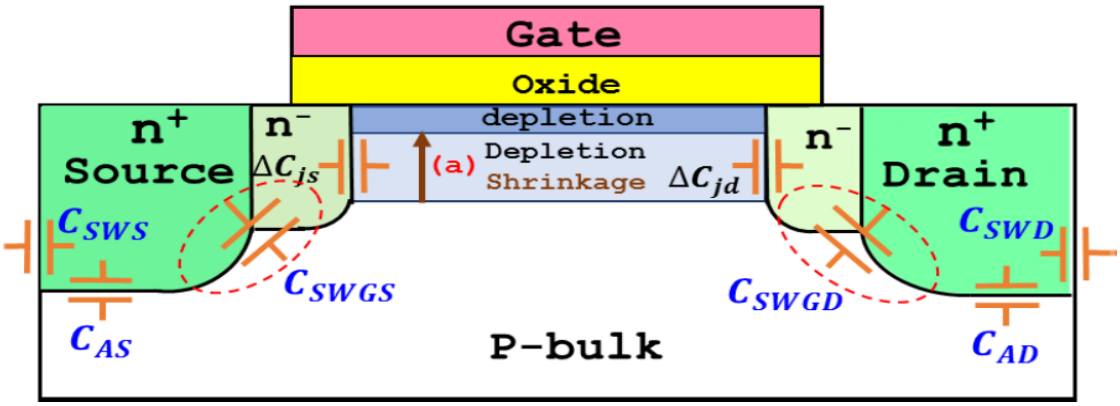


Fig. 6 :- Schematic of a bulk NMOSFET structure in the OFF-state region. The arrow (a) indicates that the channel depletion depth X_d is shrunk from the maximum X_{dm} at $V_{gb} >= V_{th}$ when V_{gb} goes to negative [20] © October 2021 IEEE

In Fig. 6. as the value of the V_{gs} goes to the negative at the off state there is an increment in the values of C_{js} which is the source-drain bulk junction capacitance and C_{jd}

which is generated by the increase in the source-drain bulk junction area in the gate edge sidewall of the n-LDD region. This happens due to channel shrinkage as depletion depth is added to the C_{SWGS} and C_{SWGD} [20]. The value of the C_{jd} is dependent on the value of C_{jdo} which is the zero-bias drain-bulk junction capacitance and it rises due to the increment of the drain bulk junction sidewall area along the gate edge due to the shrinkage of the channel depletion depth X_d or junction depth which is added to the C_{SWGS} and C_{SWGD}. [20] In Fig. 3, the CSWGS (CSWGD) is the gate-edge sidewall source (drain) junction capacitance, CSWS (CSWD) is the isolation-edge sidewall source (drain) junction capacitance and CAS (CAD) is the bottom area source (drain) junction capacitance. The values of ΔC_{JS} and ΔC_{JD} cannot be neglected as the n-LDD junction capacitance as mentioned earlier is much higher than any other components as shown in Fig. 6 [20]. This is due to much higher channel doping than in the p-well of the NMOS. So, the junction capacitance C_J needs to be accurately designed for RF based performance as it is dependent on the V_{gb} and also on ΔC_{JS} and ΔC_{JD}.

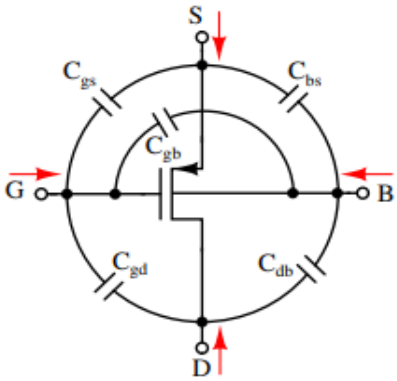


Fig. 7:- The respective parasitic capacitances of a PMOSFET transistor by V. K. Sharma, J. N. Tripathi and H. Shrimali, "Deterministic Noise Analysis for Single-Stage Amplifiers by Extension of Indefinite Admittance Matrix," in IEEE Open Journal of Circuits and Systems, vol. 1, pp. 124-139, 2020, doi: 10.1109/OJCAS.2020.3016017 is licensed under CC BY-ND 2.0.[26]

In case of the PMOS as shown in Fig. 7 similar to that discussed for the NMOS the overlap capacitances dominate here as well namely the C_{gs} and the C_{gd}. These capacitances are proportional to the channel width being dependent on the gate bias voltage because of the modulation of the overlap region charge density [19]. The gate body capacitance C_{gb} is also another parasitic capacitance which is present along the channel length 'L' and proportional to it. Both sides of the channel must be taken into consideration while calculating its value [19]. Similar to that of the NMOS junction capacitance explained in the earlier paragraphs, for the PMOS the junction capacitances namely the C_{bs} and C_{db} are formed due to the depletion charge surrounding the drain or source diffusion regions which have been embedded in the substrate. Under normal conditions both the junctions that is, the source drain and the source body junctions are reverse biased for a positive voltage.

To take into consideration the case of the Graphene Transistors (GFETS) it is very much needed to describe the quantum capacitance of these transistors which is a derivative of the total charge (Q_g) present in a low Density Of States (DOS) of Graphene with respect to the channel voltage (V_{CH}) along with the Fermi Dirac distribution is $f(E_F) = \frac{1}{1+e^{\frac{(E-E_F)}{kT}}}$ where 'E_F' is the Fermi Energy 'k' is the Boltzmann's constant and 'T' is the temperature. Independently the DOS has the equation $g(E) = \frac{2}{\pi(\hbar v_F)^2}$. This DOS is with respect to the local electrostatic channel potential $V_{ch} = \frac{E_F}{e}$. It is to be kept in mind that the Graphene in consideration is of pristine nature [28]. This is given by the equation as follows,

$$C_q = \frac{\partial Q_g}{\partial V_{ch}} = \frac{8\pi e^2 kT}{(h v_F)^2} \ln\left[2 + 2\cosh\left(\frac{E_F}{kT}\right)\right] \quad (6)$$

In the above equation E_F is the Fermi Energy, 'k' is the Boltzmann constant, 'v_F' is the Fermi velocity and 'T' is the temperature. The total gate capacitance of a GFET is reduced to the quantum capacitance in series with the geometrical capacitance, $C_{ox} = \frac{\in_{ox}}{t_{ox}}$ and thus becomes,

$$C_t = \frac{C_{ox} C_q}{C_{ox} + C_q} \quad (7)$$

In cases where the dielectric is thicker one of the above quantities becomes very much larger than the other one such as,

$$C_q \gg C_{ox} \rightarrow C_t \approx C_{ox}$$

The above discussed quantum capacitance is very much dependent on the DOS of Graphene and hence any changes in that affects it greatly.[28] This is the fact for which the transfer process of Graphene is very much to be handled carefully as the wrinkles forms in the Graphene changing its lattice structure during that affects the quantum capacitance indirectly. This might also be caused due to doping of Graphene with impurity atoms and also due to the formation of nanoribbons [28].

Charge defects can also induce potential fluctuations across the Graphene sheet which can be reduced by Gaussian distribution of the potential.

The hysteresis measurement of the C-V indicates that quantum capacitance is being influenced by oxide charge trapping. An increase of the minimum capacitance gate voltage in the back sweep measurement points to the presence of interface traps which traps the charge carriers at the gate oxide gate or due to the adsorbents being present on Graphene [28]. This above

problem can be mitigated by the application of a coating or extrinsic doping which shall be discussed in the later sections. So, the effect of the capacitances for the two types of transistors discussed previously that is, PMOS and NMOS are very much different to that of the GFETs.

Apart from the above discussed quantum capacitance there is the gate capacitance (C_g) and the gate drain capacitance (C_{gd}) which are expressed as follows,

$$C_g = -w^2\, q[d\int_{\varphi_{ss}}^{\varphi_{sd}}(\boldsymbol{\eta}_e - \boldsymbol{\eta}_h)\sigma(\varphi_s)/i_{total}\frac{dV(x)}{d\varphi_s}d\varphi_s]/\mathrm{d}V_{gs} \quad (8)$$

$$C_{gd} = w^2\, q\ [d\int_{\varphi_{ss}}^{\varphi_{sd}}(\boldsymbol{\eta}_e - \boldsymbol{\eta}_h)\sigma(\varphi_s)/i_{total}\frac{dV(x)}{d\varphi_s}d\varphi_s]/\mathrm{d}V_{ds} \quad (9)$$

'w' is the channel width, q is the total charge, 'φ_{sd}' source drain potential, 'φ_{ss}' is the symmetric surface potential, 'η_e' is the electron density, 'η_h' is the hole density, 'σ' is the conductivity, 'φ_s' is the surface potential, 'i_{total}' is the total current, 'V(x)' is the voltage at point 'x' on the surface which was defined earlier to be '0' at the source end and 'L' at the drain end where V(x=L)= V_{ds} ,'V_{gs}' is the gate source voltage and 'V_{ds}' is the drain source voltage, 'φ_{sd}' and 'φ_{ss}' are the surface potential of the drain and source respectively [35].

The electron concentration is given by,

$$\boldsymbol{\eta_e}(E_F) = \int_0^{\infty} g\,(E)f(E,E_F)dE \quad (10)$$

The hole concentration is given by,

$$\boldsymbol{\eta_h}(E_F) = \int_{-\infty}^{0} g(E)\big(1 - f(E,E_F)\big)dE \quad (11)$$

Hence, the expression '$\eta_e - \eta_h$' multiplied by the elementary charge $\frac{4\pi {E_F}^2}{(\hbar v_F)^2}$ gives the total charge [28].

When the Fermi level is at 0 eV then the density of sates for both holes and electrons are the same. As Fermi level shifts towards positive energies the carrier concentration will be dominated by the electrons 'η_e' and this shift in the Fermi level can occur through electrical gating [28]. The expression 'i_{total}' can be explained further to be the summation of two long and short-range disorder scattering mechanisms and hence the 'i_{total}' expression can be split up into three components which are as follows [35],

$$i_{long} = \frac{w}{l_{eff}} \frac{q^2(\hbar v_f + 2m\sqrt{g_s g_v})^2}{\sqrt{3}(\hbar {v_f}^2) n_i 2\pi m^3 [sgn \int (n_e(\varphi_s) + n_h(\varphi_s)) \varphi_s \frac{dV(x)}{d\varphi_s} d\varphi_s]_{\varphi_{ss}}^{\varphi_{sd}}} \quad (12)$$

$$i_{short} = w/l_{eff} \frac{2 g_s g_v \hbar}{q m n_d {v_o}^2 \pi} [sgn \int (1 - e^{-\frac{\varphi_s}{\beta}}) \frac{dV(x)}{d\varphi_s} d\varphi_s]_{\varphi_{ss}}^{\varphi_{sd}} \quad (13) \quad \text{and,}$$

$$i_{disorder} = \frac{w}{l_{eff}} \sigma_{min} [sgn \frac{\int (\frac{\beta}{4} e^{-2\varphi_s/s} - \frac{2\beta}{\beta + s})}{s - \beta} + 1) \frac{dV(x)}{d\varphi_s} d\varphi_s]_{\varphi_{ss}}^{\varphi_{sd}} \quad (14)$$

In the above expressions the expression 'sgn' is represented by $\frac{V_{gs} - V_{Dirac} - V(x)}{\sqrt{(V_{gs} - V_{Dirac} - V(x))^2 + s_m}}$, $s_m = 1e-6$, 'q' is the charge, 'ħ' is the Planck's constant, 'v_f' is the Fermi velocity, 'g_s' and 'g_v' are the spin and valley degeneracies, respectively. 's' is the disorder parameter, β = $k_B T$ where 'k_B' is the Boltzmann's constant and 'T' is the temperature, 'n_i' is the impurity density, 'm' is an experimental parameter having a value of 0.35 which is variable depending on the experiment conducted.

Hence, the 'i_{total}' expression has a value of $((i_{long}{}^{-R1} + i_{short}{}^{-R1}) -_{R1}^{R2/} + i_{dis}{}^{R2})^{1/R2}$. It can be deduced from all of the equations stated above and especially the 'sgn' equation that the choice of the gate bias or the offset is the main deciding factor behind the value of the 'C_g' and 'C_{gd}' along with the value of the 'V(x)' as the value of the Dirac voltage is assumed to be fixed. It is quite elementary for any kind of RF measurement to be taken for the determination of the 'f_{max}' that the value of the offset or the bias point is to be chosen close to the Dirac point because the value of the mobility and the transconductance remain the highest in the Id-Vg curve. It is to be noted that ID-VD curves unlike the PMOS and the NMOS for choosing a value in saturation for the picking of the bias point isn't of much use in the case for the GFETs as they do not saturate. If an ideal case of the Dirac point that is 0V is to be considered here and the value of the 'V_{gs}' be taken at the Dirac voltage keeping the value of 'V(x)' also the same i.e., all of them at 0 V then the whole expression for the 'sgn' turns to '∞'. The value of 's_m' is negligible and can be neglected. If that is the situation then 'i_{short}' and '$i_{disorder}$' turn to '∞' and 'i_{long}' turn to '0' and consequently the entire expression of 'i_{total}' turns to '∞' as well. So plugging in the value of 'i_{total}' in equations (8) and (9) we have the whole values of the capacitances of the gate and drain reduced to '0' which is the not the desirable form of minimization required for RF performance. From this line of deduction one can build two cases,

CASE I (When Dirac Point is Negative)

If the Dirac Point is negative then, the value of 'V_{gs}' assumed to be a negative whole number (usually negative biasing is taken for a negative Dirac Point) keeping the value of 'V(x)' at a negative or positive decimal number in the range of -1 to 1 V(as that is assumed to be the best

values for RF measurements) then the value of 'sgn' turns to be a 1. However, if the value of the 'V(x)' or 'V_{gs}' is chosen to be such that the entire numerator gets nullified then the value of 'sgn' turns to '∞' which happened when all of the three terms were equal to '0' as mentioned in the above paragraph. Plugging the 'sgn' into the capacitance expression will render it to be '0' as was the case mentioned earlier.

CASE II (When Dirac Point is Positive)

If the Dirac Point is positive then, the value of 'V_{gs}' is assumed to be positive (as positive Dirac Point gets a positive gate biasing) opposite that of CASE I keeping the value of 'V(x)' at a positive or positive decimal this time in the same range. The value of 'sgn' again turns to be a '1' and will turn to be '∞' if the value of 'V_{gs}' or 'V(x)' is chosen such that the numerator turns to '0'. Plugging in the value of the 'sgn' yields the same result for the capacitance as in CASE I. The above two cases have been mentioned in order to establish the importance of the bias points and the 'V(x)' in the minimalization of the parasitic capacitances of the gate and the drain. In mentioning so it must be noted that the best and ideal Dirac Point case is obviously at 0v as that is the perfect balance of the electrons and holes when the Fermi level remains at '0'. So, we see that the 'sgn' term has quite a significant role in the calculation of the capacitance to reduce it to the minimal possible value.

Hence to make the value of the 'sgn' to bare minimum and not '0' or '∞' the choice of the biasing voltage is absolutely important as that will multiply the capacitance to a large or small amount and hence the value of the f_t and f_{max} gets magnified or diminished in accordance if one looks carefully at their Figures of merit mentioned below.

2.3 Maximum Transit Frequency (f_T) and Maximum Oscillation Frequency (f_{MAX})

When explained in simple words maximum transit frequency 'f_t' is the frequency at which the small-signal short-circuit current gain of the transistor in question drops to unity or 0 dB and 'f_{max}' is the frequency at which the short-circuit voltage or power gain drops to unity or 0 dB. Popularly they are the Figures of merit for the three types of transistors that can determine the value of the 'f_t' and 'f_{max}' which are defined as follows.

For PMOS and NMOS

$f_t = \frac{g_m}{2\pi(C_{GS}+C_{GD}+C_{GB})}$ and

$f_{max} = \sqrt{\frac{f_t}{8\pi R_G C_{GD}}}$. It is to be noted here that 'C_{GB}' is often neglected in approximate or practical calculations for the 'f_t' however the exact equation for both are

$f_t = \frac{g_m}{2\pi[(C_{GS}+C_{GD})\left(1+\frac{R_D+R_S}{r_0}\right)C_{GD}.g_m(R_D+R_S)+C_p}$ and

$f_{max} = \frac{f_t}{2\sqrt{g_{ds}(R_D+R_S)+2\pi f_t R_G C_{GD}}}$. Here, '$C_p$' is the parasitic capacitance, R_G is the gate resistance, R_D is the drain resistance and R_S is the source resistance. However useful these Figures of merit are for calculating theoretical and experimental values they do not give accurate results all the time and are quite difficult to estimate as well given the number of variables. This is the reason why S parameters come into use being generated from a Vector Network Analyzer. These parameters are useful to denote the Maximum Available Gain (MAG) which when reduces to 0 dB gives the value of 'f_{max}'(though $'f_{max}'$ does not provide a constant range if extracted

from the MAG), Maximum Stable Gain (MSG) where the transistor is said to be unconditionally stable, Mason's Unilateral Gain which when plotted against the frequency gives the value of the 'f_{max}' when it drops to 0 dB and the H_{21} which is the current gain and when it reduces to 0 dB it gives the value of the 'f_t'. All of the above four mentioned quantities in details and in terms of the S parameters will be explained in later sections with the measurements of the three types of transistors in question.

For GFETS

For the Graphene transistors the Figures of merit are as follows,

$$f_t = \frac{g_m}{2\prod(C_{GS} + C_{GD})][1/1+g_{ds}(R_S + R_D) + \{C_{gd}g_m(R_S + R_D) / C_{GS}+ C_{GD}\}]} \text{ and}$$

$$f_{max} = \frac{g_m}{4\prod C_{GS}} \frac{1}{\sqrt{g_{ds}(R_i + R_S+ R_G)+ g_m \frac{R_G C_{gd}}{C_{gs}}}}$$

$'R_i'$ is the charging resistance, $'R_S'$ is the source series resistances, 'R_D' is the drain resistance and 'R_G' is the gate resistance, 'C_{GS}' and 'C_{GD}' are the gate-source and gate-drain capacitances respectively, 'g_m' is the transconductance and 'g_{ds}' is the drain conductance. In these transistors the S parameters come into great use and are calculated to obtain the values of the 'f_t' and 'f_{max}' same as in the case for the MOSFETS.[42]

2.4 Examples of f_T and f_{MAX} in case of MOSFETS and GFETS

Coming to discuss how these capacitances influence the $'f_t'$ values we can refer to the group of researchers led by C.P. Chao who in order to reduce the capacitances divided the transistors into multiple identical sections connected in parallel. The area of the MOSFET was being saved

by finger gates because adjacent diffusion sections share same source/drain fingers with Si-wafer and a nitride gate oxide and CMOS process technology [21]. The gate drain capacitance ie $'C_{gd}'$ is proportional to the number of fingers. The maximum value of $'f_t'$ is reached at the gate bias where transconductance has the maximum value.

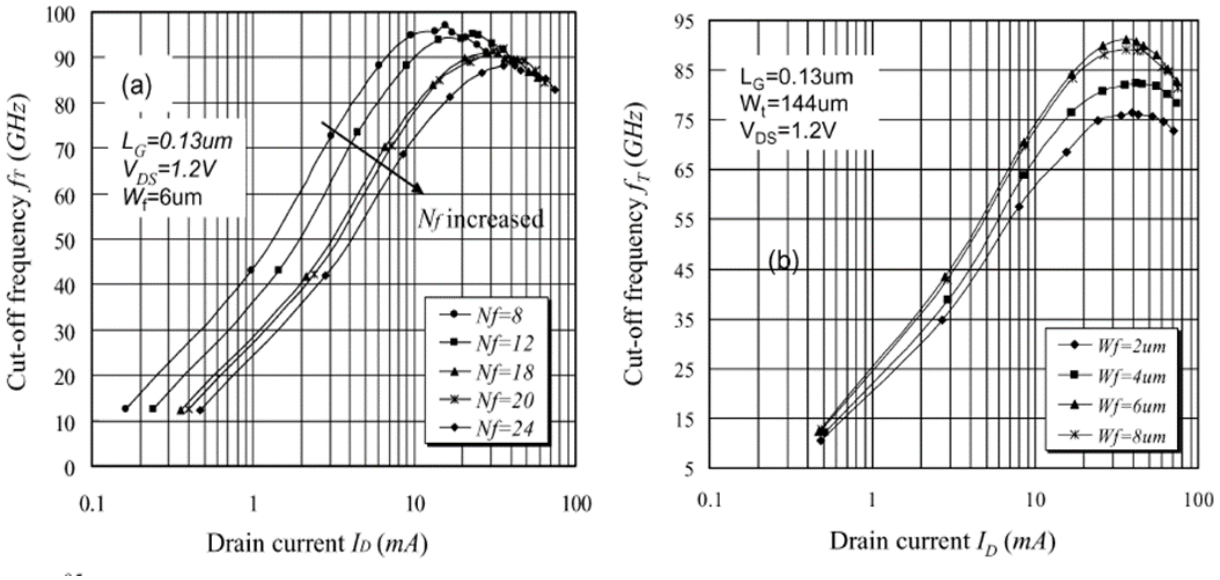


Fig. 8 :- f as a function of drain current I with (a) various finger-gate number (N) and (b) finger-gate width (W), the total gate width (W) is 144 μm [21]. © September 2005 IEEE

This approach however did not yield much result as initially the value of $'f_t'$ kept on increasing with the drain current but decreases with the increased voltage drop across the source/drain regions. Also, the fact was evident that with the increase in the number of fingers the source drain resistance as well as the gate to bulk capacitance also increased [21]. However, they found that the value of $'f_t'$ increases with the width of the finger but that in turn leads to an increment in the gate to bulk capacitance which degrades the RF characteristics as shown in Fig. 8. The value was 6 um for the gate to bulk capacitance for which the value of f_t was the highest. That is to say that the $'f_t'$ decreases from 97 to 88.2 GHz as the number of fingers increases from 8 to

24.

Lam and Chan who reviewed and evaluated MOSHEMT structures [58-61] with a regrown layer of InGaAs in the channel also faced the same decrease in the values of f_t when their FETs were with 30 fingers with increase in gate capacitance [22]. The same phenomena was observed for the case of f_{max} as well but more stable. So, it might be safe to assume that the number of fingers decreases the values of the f_t and f_{max} instead of enhancing them.

Comparing the influence of capacitance with the GFETs here also gate/source and gate/drain capacitances dominate frequency response of the transistors. But unlike the case of the MOSFETs here the contact resistances have a role to play. These dominate the values of f_t and f_{max} [23]. When the resistances are too high then the parasitic capacitances can be disregarded. The extrinsic capacitance of the device might be reduced but still the gate capacitance will be dominating the frequency performance of the transistor, especially the value of f_t [23] The value of the gate capacitance is expressed as the series of the top gate oxide capacitance for dual-gated GFETs and the quantum capacitance. The gate oxide capacitance is obviously a constant, but the quantum capacitance is something which is related to the voltage drop across the channel of the transistor. The back-gate oxide capacitance can be disregarded as it is short-circuited by the dc gate source voltage at the back [23].

The gate oxide capacitance is dependent on V_{gs} and V_{ds} both, the latter being more dominant as it has a huge impact on the maximum speed of the transistor. This is in stark contrast with the MOSFETs that have the C_{gd} value which is independent of the biasing voltage and the C_{gs} value which is relatively constant at the saturation region of the transistor.

2.5 Extraction of f_T and f_{MAX}

These values have been extracted in various experimental methods as well. Some have used measured amplifiers with the devices under test while some have used multiple transistors connected in parallel to give a capacitance value.

Although the method did not yield many results for the f_t and the f_{max} it did result in the extraction of the capacitance [24]. Another factor which comes into being is the device fringing capacitance which was a major impediment in finding the C_{gd} increment for the researchers O.Ozawa and H.Ishuichi in determining an effective length for a given gate width. The change in C_{gd} is again proportional to the gate width and the effective length can be found by plotting change in C_{gd} versus gate length or gate width.

However, to do this the subtraction of C_{gd} at V_{gs} = 0 required to find the change in C_{gd} eliminates from the C_{gd} data both the measurement setup capacitance and as mentioned earlier the fringing capacitance. The fringing capacitance which depends on V_{gs} and is very relevant in short channel devices could not be obtained and hence the method proved to be unfruitful. However, researchers M. Sadowski and D. Tomaszewski deciphered the fringing capacitance by using the accumulation range of $C_{gs}(V_{gs})$ and $C_{gd}(V_{gs})$ characteristics of MOSFETs [24].

Now coming to the extraction of the values of f_t and f_{max}, as mentioned earlier using the figure of merit to determine their values is the best option. That is why the extraction of capacitances were limned in the earlier few paragraphs. However, using the figure of merit is just an estimation of the values of f_t and f_{max} and the totally accurate values which are needed.

Matlab calculation can lead to accurate values of f_t and f_{max} by the determination of the impedance and admittance matrices of the small-signal circuit equivalence. The extrinsic series resistances found by the Z matrix of the two-port network are then converted and subdivided further into the S and H matrices to get the value of the Maximum Available Gain (MAG) and short-circuit current gain which shall be discussed later [24].

2.6 Back Gated Graphene based Devices

There have been many approaches throughout the decade from 2010 to present into fabricating the GFETs. The most popular and adopted methods by various groups working with GFETs are the top-gated and the back-gated structures. The back-gated structures are very useful for the purposes of photodetection as they can modulate the photocurrent by applying a gate voltage which enables the photodetection [17]. This has its drawback, too, as Graphene has a zero bandgap structure. A large amount of dark current is generated which produces less sensitivity. At the regions where Graphene is in contact with the metal the Fermi level is close to that of the metal due to charge transfer while the other regions are uncontrolled and can be easily controlled by the back-gate voltage. As a result, a built-in electric field is generated which at the transition region is intermediate and has a role to play in enabling high speed of the charges and is with zero gate bias and no dark current [17]. Still the low absorption of Graphene make it difficult for photonic applications. Similar to photodetectors in photodiodes the Fermi level difference between Graphene and the semiconductor is the electric field that separates electron and hole pairs. Operating on the principle of reverse bias in dark condition maximum majority carriers are around the Fermi level. Under forward bias condition the carriers flow from

the semiconductor to the Graphene but under reverse bias condition the majority carriers cannot surpass the Schottky Barrier Height. Hence the reverse bias current or the dark current decreases exponentially at the interface [17]. The photocurrent which is the main component of the reverse bias is mainly due to the absorption in the semiconductor as clearly shown in Fig. 9.

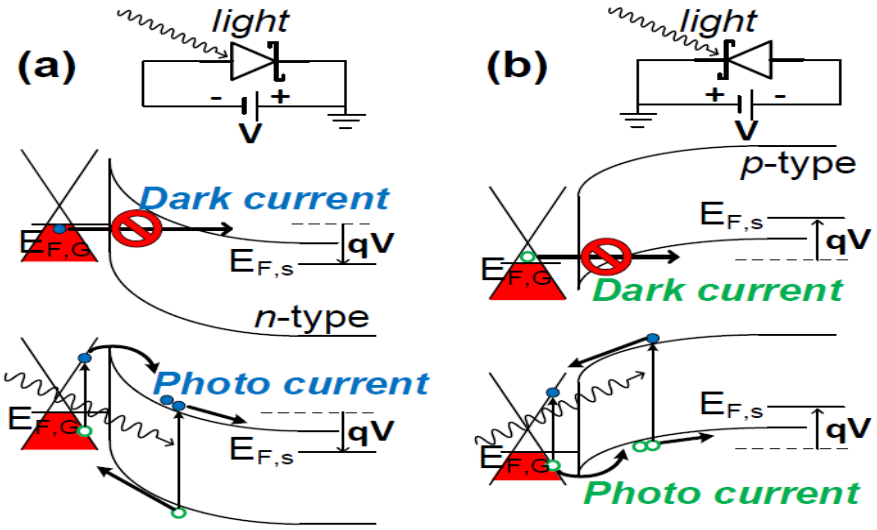


Fig. 9 :- Graphene/semiconductor photodiode without and with visible light (a) Left column: Graphene/n-semiconductor Schottky diode. In this case majority carrier is electron.(b) Right column: Graphene/p-semiconductor Schottky diode. In this case the majority carrier is hole [17]. Reproduced with permission from the author.

2.7 Top-Gated and Back-Gated GFETS

Now when we discuss the case of Graphene transistors or GFETs here also the bottom and top gate structures are fabricated. The deposition of Graphene as a film over the gate dielectric is usually done by the PMMA transfer method after the Graphene is prepared by the Chemical Vapor Deposition method [4]. The gate oxide layer which is the back gate as mentioned above is deposited by Atomic Layer Deposition (ALD) on the Si substrate. Two metal contacts are usually fabricated composed of two metals with the same or different thicknesses for the source/drain contacts. Lithography then patterns the Graphene channel due to plasma etching by oxygen [4]. In some cases the flakes of Graphene deposition instead of the CVD grown Graphene and PMMA transferred method are also utilized [5]. In those cases however the etching due to oxygen plasma is typically avoided for the development of the channel [5]. This is to avoid the probability of having dangling bonds at the edge of the Graphene and also to avoid some defects such as Graphene wrinkling, etc. Fig. 10 shows the SEM, AFM and device schematic very elaborately. After ALD many other processes have been reviewed for the treatment of the graphene surface such as deposition of oxide seed layers, polymer coating and ozone treatment [68-73]. In our fabrication of the GFETs we have applied passivation of the dangling bonds by hygrogen which shall be discussed in Chapter VII.

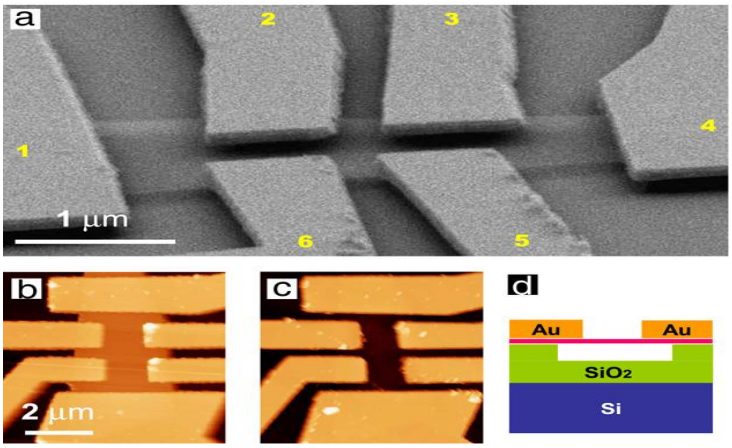


Fig. 10 :-(a) Scanning Electron Microscope (SEM) image of a typical suspended six-probe Graphene device taken at 15 degree with respect to the sample plane. (b) Atomic Force Microscope (AFM) image of the suspended device #1 before the measurements. (c) AFM image of the device #1 after the measurements with Graphene removed by a short oxygen plasma etch (same z scale). (d) Device schematic, side view. Degenerately doped silicon gate (blue), partly etched SiO2 (green), suspended single-layer Graphene (pink) and Au/Cr electrodes (orange) [5]. The choice of dielectrics in the case of these bottom gated structures is a crucial parameter. Reprinted from K.I. Bolotin, K.J. Sikes, Z. Jiang, M. Klima, G. Fudenberg, J. Hone, P. Kim, H.L. Stormer, "Ultrahigh electron mobility in suspended graphene", Solid State Communications,Volume 146, Issues 9–10, 2008, Pages 351-355, ISSN 0038-1098, https://doi.org/10.1016/j.ssc.2008.02.024. (https://www.sciencedirect.com/science/article/pii/S0038109808001178) with permission from Elsevier.

All the structures mainly mentioned above have SiO_2 as the main dielectric with varying thicknesses. However, studies have proved other dielectrics such as Aluminum Oxide (Al_2O_3), Hafnium Dioxide (HfO_2) and Titanium Dioxide (TiO_2) for GFETs which are specifically aimed for high frequency response. The choice of dielectric plays a vital role that is to say the lower the gate oxide capacitance the higher is the transconductance as well as the cut-off frequency (f_t) [6]. Hence among the above mentioned dielectrics Hafnium Dioxide has been the choice for many GFETs because of its high value of dielectric constant. Due to thermal instability TiO_2 is not a great option for a dielectric but having a

low dielectric constant Aluminum Oxide still is a good choice since it has low value of breakdown voltage [6]. All of these oxides and their properties become useful in both the back-gated and top-gated structures of Graphene. The back-gated structures are not ideal for RF performance [6]. This is because of the fact that these transistors have small gate capacitance and therefore, make it difficult to achieve a high value of transconductance. It is also impossible to achieve the current saturation for the Graphene transistors along with a good DC voltage gain (A_V) and large channel conductance as is visible in Fig. 11 [27]. As a result huge control voltages are required to reach a good value of transconductance and indirectly to achieve a good value for the f_{max}. So to improvements are needed to parameters such as the bandgap which leads to low carrier mobility ($\leq 0.05 m^2 V^{-1} s^{-1}$) or the increase in the velocity saturation or to improve the saturation current (20 A m^{-2}) [27].

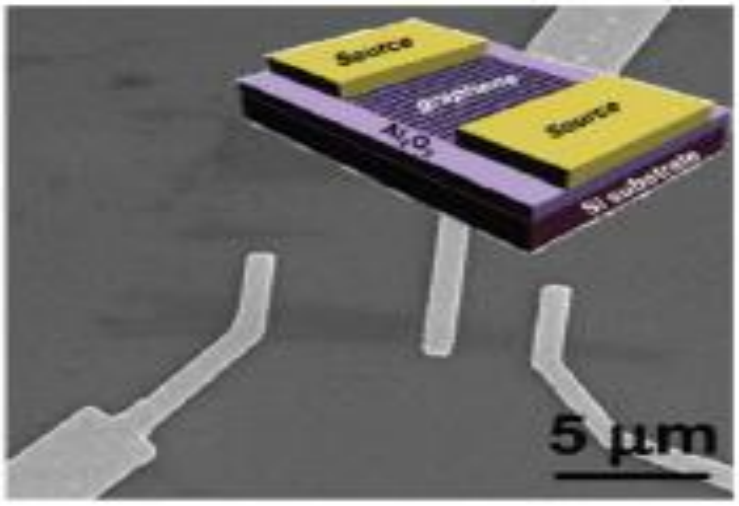


Fig. 11:- Example Of A SEM image of a back-gated GFET on a 72 nm Al2O3/Si substrate, and the inset display schematics of the device and a schematic of a top-gated GFET with HfO2 gate dielectric by Saeed, M., Palacios, P., Wei, M.-D., Baskent, E., Fan, C.-Y., Uzlu, B., Wang, K.-T., Hemmetter, A., Wang, Z., Neumaier, D., Lemme, M. C., Negra, R., Graphene-Based Microwave Circuits: A Review. *Adv. Mater.* 2022, 34, 2108473. https://doi-org.ezproxy.rit.edu/10.1002/adma.202108473 is licensed under CC BY-ND 2.0 [27].

Still, if we want to investigate as to which dielectric is the best for construction of GFETs used for RF performance be it back-gated or top-gated, then it is seen that Al_2O_3 has the least degree of strain while Hafnium Dioxide (HfO_2) and TiO_2 show more degrees of strain for the Graphene here which can be a detrimental factor for the other parameters in question. Previous experiments have proved that the stability of Hafnium Oxide is better for Transconductance [6]. Comparison of the devices showed values of f_t and f_{max} for the HfO_2 layer devices while the TiO_2 and Al_2O_3 devices showed lower values of these two parameters.

Another dielectric which has been a preferred one for some time for the GFETs is Hexagonal Boron Nitride (HBN) which is mainly because it has got minimum dangling bonds and is free of interface charge traps. Devices fabricated with this dielectric have higher carrier mobilities which are far higher than the other dielectrics discussed so far. The hindering part of this dielectric is the charge scattering that takes place due to the presence of Graphene in it [7]. Recent experiments done on the channel length performance of these HBN transistors have showed that the shorter the channel length the greater is the instability factor [7].

Another factor observed is that, if the width of the transistor is large enough then the gate resistance is inversely proportional to the channel length [7]. This is important as the increment of the gate resistance is therefore detrimental in the ultimate goal for a higher value of f_{max}. Ultimately the RF performance of such transistors always depend on the biasing point which the group took as V_{ds} = 0.6 V and $V_{gs} - V_{ds}$ = 2V. V_{ds} is the Dirac Voltage, out here which is the necessary voltage to turn off the channel and also gives an estimate about the doping present in

the Graphene [3]. The maximum slope gain was hence observed to be around 10 dB/dec and channel length reduction by a factor of 2 increases the power gain to 5.4 dB and also the value of f_{max} increases by almost 10 GHz from 6.5 GHz to 16 GHz [7].

Considering the GFETs with channel lengths of 1.8 µm and 900 nm with and without defects and impurities the frequency increases with an increase in the power gain. For the GFET on HBN different Graphene quality scenarios are considered. Instability implies that the GFET amplifier is unusable at this particular bias point. The chosen bias point was $V_{gs} - V_{ds}$ = 2 V and V_{ds} = 0.6 V.

The reason for the scaling of the channel length is that the value of f_{max} increases for shorter channel lengths by the factor of $\frac{1}{L^2}$. However due to saturation velocity effects the g_m or transconductance becomes insensitive to the length (L) and hence the value of f_{max} increases by a factor of 2 which is also dependent on the quality of the Graphene used and the scaling factor decreases from $\frac{1}{L^2}$ to $1/L$. But in cases of longer channel lengths the scalability is in the order of $\frac{1}{L^n}$. So, the THz region objective for the value of f_{max} can be realized with shorter channel lengths.[7] Lower values of the V_{ds} is used to increase the device stability a lot and to lower the channel length. The main factor is the choice of the biasing point, which plays the vital role in the value for the determination of f_t and f_{max}.

From other experiments we see that with a Dirac Point (the meeting of the conduction and valance band where the electron affinity is the highest and density of states is the

lowest) at 49 V the field-effect carrier mobility of the GFET is around 767 cm^2/Vs and the value for f_t is at 1.6 Ghz. The GFETs which had the above mentioned parameters were made as Graphene silicon heterojunction ones which were back-gated with a 90 nm of SiO_2 and the Al gate being 100 nm. The source drain contacts being Cr/Au 5/100 nm [3]. So we can safely assume that the width has a vital role to play along with the channel length in determining the value for the f_t and f_{max} as mentioned above because even with the structure being back-gated it offers high value for f_t.

Let us now discuss the case of Graphene top-gated transistors in terms of their usefulness for the values of f_t and f_{max}. Lemme, et al. demonstrated a top-gated Graphene transistor in 2007 which had a thin film of SiO_2 deposited above the Si wafer and below the Graphene layers. This type of transistor offers higher value of gate oxide capacitance. The electron and hole mobilities were greatly reduced and hence it proved to be ineffective as a whole [8].

A group of researchers from Nanjing University in 2016 reported values of f_t and f_{max} to be at 70-255 GHz and 106-200 GHz respectively. This was done by a different method altogether. For example, the transfer method was done by Au and not the conventional PMMA. The purpose of this was that the film of Au forms Ohmic contact with the GFETs and also enables a self-aligned gate process that minimizes the Graphene region and also, the transistors have the gate structured as a 'T' of 60 nm. The purpose of this is to diminish the value of the resistance which has been mentioned earlier to have a bad effect on the value of f_{max} [9]. The self-alignment Au transfer and the 'T' gate structure have contributed to the above stated values for the cut-off and the maximum oscillation frequencies respectively. The dielectric being used is

Al_2O_3 which is 8 nm thick and the gate electrodes are Ti/Au which are 50 nm/450 nm as is quite visible in Fig. 12. This process also minimizes the parasitic resistance.

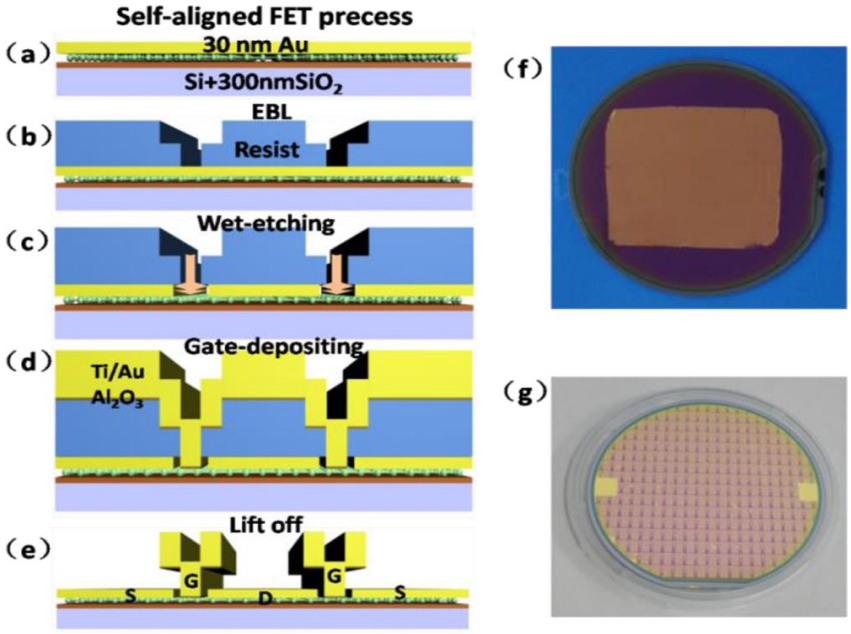


Fig. 12 :-. Schematic illustration of the fabrication of self-aligned GFETs by solution-etching. (a) 30 nm Au/Graphene on Si substrate with 300 nm SiO_2; (b) Trilayer photo resist for T-gates are patterned by EBL; (c) Gold film under the T-gates is wet etched away concomitant transverse etched space; (d) Ti/Au is deposited on top as the gate metal after 8 nm Al_2O_3 is deposited by ALD as dielectric with 1 nm Al self-oxidized seed layer; (e) After lift-off, GFETs are formed; (f) Photo image of transferred Graphene with Au film on 3 in Si substrate; (g) Photo image of GFETs on 3 in. Si substrate.[9] Reprinted (adapted) with permission from Yun Wu, Xuming Zou, Menglong Sun, Zhengyi Cao, Xinran Wang, Shuai Huo, Jianjun Zhou, Yang Yang, Xinxin Yu, Yuechan Kong, Guanghui Yu, Lei Liao and Tangsheng Chen, "200 GHz Maximum Oscillation Frequency in CVD Graphene Radio Frequency Transistors" *ACS Appl. Mater. Interfaces* 2016, 8, 39, 25645–25649 Publication Date:September 19, 2016 https://doi-org.ezproxy.rit.edu/10.1021/acsami.6b05791 Copyright {2016} American Chemical Society

The values of the f_t were found to be at 70 GHz before the de-embedding process and after the de-embedding process it was found to be at 255 Ghz. These two values were obtained from the

same device after the two processes were conducted on them [9]. The device had the same gate length mentioned above and with values of V_{gs} and V_{ds} at 0.6V and 0.35 V. The values for the gate length, V_{ds} and V_{gs} remain the same as for f_t [9].

2.8 Other high Frequency Transistors (HEMTS)

High Electron Mobility Transistors (HEMT) are known for their exceptional mobility and hence high values for cut-off frequencies and maximum oscillation frequencies. Among the family of HEMTs, InP based ones exhibit best RF properties known. Miguel, et al. demonstrated the first InP transistor with a maximum oscillation frequency more than 1 THz [10], the transistors being ideal for submillimeter and THz power generation having high available current. To achieve such results high quality low resistance ohmic contacts need to be made on the semiconductor layer which are thermally and electrically stable. InP transistors achieve much higher bandwidths with twice the breakdown voltage than any normal SiGe transistor. The InP transistors is guided by non-equilibrium electron transport in the collector space charge region. But with all that said there are two major hindrances in the fabrication of these transistors extrinsic parasitic capacitance and base metal sheet resistance. The highest ever reported f_t and f_{max} values for these transistors were 610 GHz and 1.5 THz, respectively, enabling amplifier gain at 1 THz. This was done on a 25 nm gate [10].

Coming to their usability in terms of RF power these transistors are most useful in generating RF power. These transistors can be used to generate wireless network speeds of up to 92-95 GHz for use in military and mobile applications [10].

For GaN transistors the values of the f_t and f_{max} reported are 454 GHz and 444 GHz, respectively by Tang et al. [56] on a AlN/GaN/AlGaN HEMT device. Shinohara et al. has reported values of maximum frequency being 600 GHz with a gate length of 20 nm [57]. The more the scaling takes place for these transistors the higher is the frequency which is recorded, which is up to 2 THz. When we discuss the case of Gallium Nitride (GaN) transistors in terms of the RF power performance we see that there is a degradation in the power performance of these HEMTs. This occurs because there exists the problem of charge trapping which interferes with the stability of the device. The underlying Aluminum Nitride has the potential of a high polarization effect which yields high power and high frequency [11].

Another impediment that these transistors face is the parasitic effects which usually arise from the generation of available energy states in the semiconductor energy gap which appears as traps or holes as such from the channel or gate contact [11]. These traps maybe due to crystal irregularities or impurities present in the layers and can be eliminated by the presence of an electric field. Sometimes growth of a passivation layer such as SiN atop the AlGaN/GaN layer also helps reduce these parasitic effects to a great extent. Another great factor of impedance to be mentioned here is the contact resistance which is offered due to the ohmic contacts and large source to drain resistance. In order to reduce this a Molecular Beam Epitaxy (MBE) process was used to grow the contacts to minimize the resistance by a factor [12]. The research group led by Yue et al. demonstrated the highest value of f_t recorded to date that is 370 GHz for any GaN transistor. For their devices they resorted to the idea of a rectangular gate in order to reduce the values of the C_{gs} and the C_{gd}, clearly demonstrated in Fig. 13 and 14 [12]. The main reason, however, remains in the key factor of having a reduced gate length which gave a high value of f_t and also kept the parasitics a lot lower. This similar approach might be taken for GFETs as well

to achieve a high value of f_t.

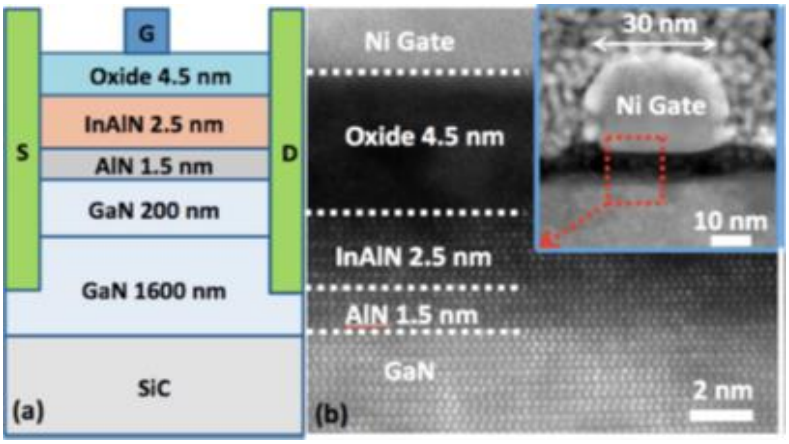


Fig. 13 :- (a) Schematic of the InAlN/AlN/GaN HEMT cross section and (b) High-resolution Transmission Electron Microscope (TEM) and (inset) scanning TEM images confirming the HEMT layer structures and the 30-nm gate length after device fabrication.[12] Reproduced with permission from the author.

When we discuss the case of the GaAs transistors the T gate shape and the ohmic contacts have a huge role in the value of the f_t and f_{max}. Elgaid et. al demonstrated such transistors which had the structures as stated above with a f_t value of 440 GHz and f_{max} value of 400 GHz [13]. The 'T' gate alignment had a definite role in this too.

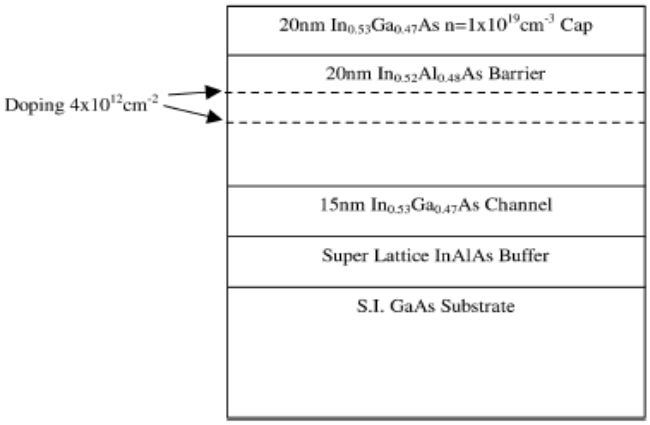


Fig. 14 :- Double-delta-doped InAlAs/InGaAs Metamorphic on a GaAs substrate. [13] © November 2005 IEEE

2.9 Comparison of HEMTs with GFETs

Comparing the properties of the above mentioned HEMTs with GFETs we see that that increment in the gate width has a direct relation with increasing value of the gate resistance. The reduction in gate width is directly proportional to the parasitic pad capacitances which in turn affects f_{max} and reducing oxide thickness can be a way of amelioration, but then again doing that may increase f_{max} but increase parasitic capacitances. Usually instead of the 'T' gate approach done by many researchers for the HEMTs the GFETs are subjected to using a thicker layer of SiO2 in order to reduce these parasitic capacitances shown in Fig. 15 [14]. Similarity to the HEMTs also in GFETs a gate length of 50 nm or below yields a higher value for the f_t but then again unlike the HEMTs we have a lot of other factors.

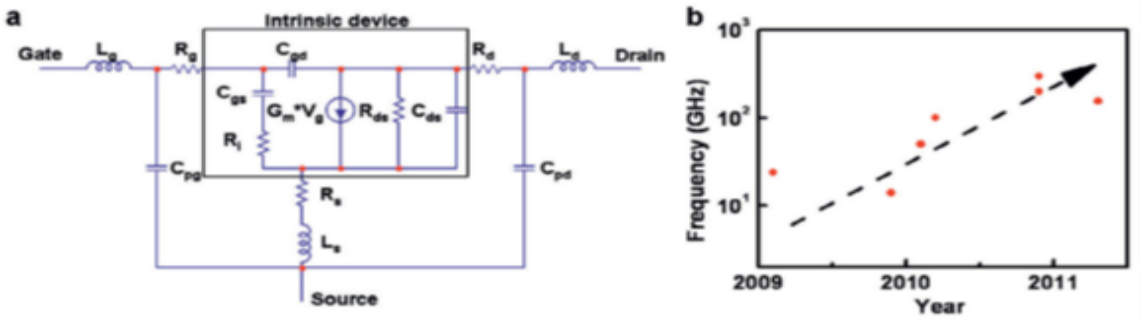


Fig. 15 :- Graphene RF transistors. (a) The equivalent circuit topology of a Graphene transistor. The C_{pg} and C_{pd} are the gate and drain parasitic capacitances, R_s, R_d and R_g are the resistances of the source, drain and gate electrodes. Ls, Ld, and Lg are the inductance of the source, drain and gate electrodes. C_{gs}, C_{gd} are the top-gate to source and top-gate to drain capacitance, C_{ds} and R_{ds} are the capacitance and resistance between drain and source. R_i is the resistance of dielectrics (gate-charging resistance). (b)The demonstrated cut-off frequencies of Graphene transistors versus time.[14] Reprinted from Publication title, Lei Liao, Xiangfeng Duan, "Graphene for radio frequency electronics", Materials Today, Volume 15, Issues 7–8, 2012, Pages 328-338, ISSN 1369-7021, https://doi.org/10.1016/S1369-7021(12)70138-4. (https://www.sciencedirect.com/science/article/pii/S1369702112701384) with permission from Elsevier.

Table 1:- **Highest Reported Values for F_T and F_{MAX} for Different Types of Transistors**

TYPE OF TRANSISTOR	f_t	f_{max}
InAs	644 GHz [62]	681 GHz [62]
GaAs	688 GHz [63]	800 GHz [63]
InP	610 GHz [64]	1.5 THz [64]
GFET	427 GHz [65]	8 GHz [65]

In accordance with the small signal model taken into consideration for the GFETs the value of the V_{ds} and V_{gs} forms the most crucial in evaluation for the f_t apart from the capacitances of the transistors as mentioned earlier. One can attribute the gate length and oxide thickness which has been discussed before but the drain conductance is another important parameter which plays a considerable role as it disconnects the extrinsic output from its input [74]. In such a case however the mobility increment goes in vain as the competing effect of the transconductance (g_m) and the drain conductance on both the values of the f_{max} and f_t. Henceforth, although g_m increases but then subsequently increase of the drain conductance nullifies the beneficial effect it can have on the f_t and f_{max} [74]. This is why the source and drain resistances also play an important role as they reduce the drain conductance if they have lower values themselves [74]. Researchers have also attributed the presence of a capacitive dipole layer between the metal and the graphene as to affecting the value of the f_t [75]. Hot carrier effects in top gated GFETs has also been attributed to reducing the f_t value where the reduction of the electric field in the emitter base insulator interface increasing the barrier height and in turn reduces the g_m and the f_t value [76]. This is very much dependent on the nature of the gate oxide used, that is a stable gate oxide will be much better a choice than an unstable one and also the thickness of the emitter base insulator as was the reason proposed in [76].

CHAPTER III. Experimental and Preliminary Results

3.1 PMOS

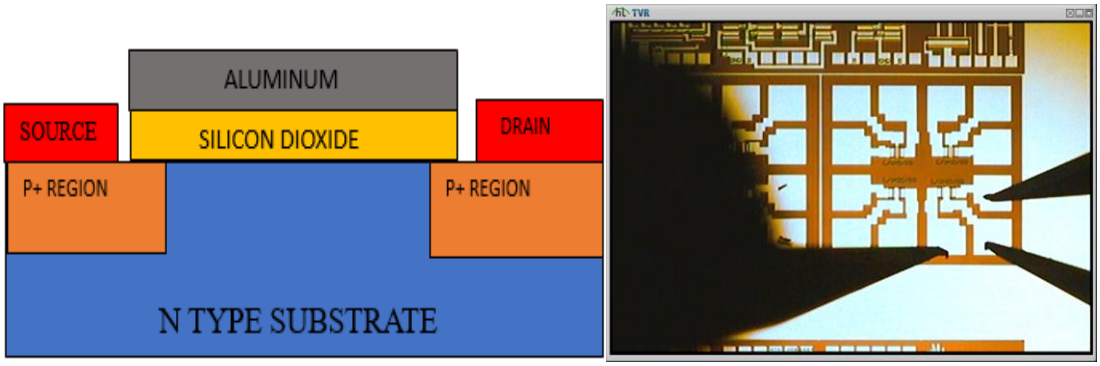


Fig. 16 :- Diagram of a typical P type MOSFET fabricated at RIT (Left) and a 8 PMOS transistors of different W/L ratios fabricated at RIT (Right)

To establish and characterize the Graphene transistors we have made an approach to first study extensively the characteristics of the metal gate PMOS and NMOS fabricated in the RIT SMFL as illustrated in Fig. 16 (left). To do that we have studied various lots of fabricated PMOS and NMOS in the last two years and obtained the family of curves as well as the ID-VG curves from them. This has been done to estimate the value of the output voltage (V_{ds}), the gate source voltage (V_{gs}) and to have an idea of the input frequency as well as the amplitude for testing these transistors for high-frequency applications.

To begin with four variants of the PMOS transistors which are shown in Fig. 17 (right) were chosen from both the lots with W/L ratios of 80/80 µm, 80/40 µm, 80/20 µm and 80/10 µm. The reason behind choosing four variants and not a single one is that we wanted to observe whether the transconductance value which is an intrinsic factor in the transit frequency (f_t) as well as the maximum oscillation frequency (f_{max}) is affected by the change in length or not.

For our testing purposes a particular value of I_d was chosen in saturation for a particular V_{gs}. This is to determine the value of the load resistor to be used in the single transistor amplifier circuit to test for high frequency. The value of the resistor is very important for this purpose as that is the main component which regulates or controls the voltage in the circuit and indirectly is essential in measuring the frequency in an oscilloscope or a network analyzer. The load resistor as mentioned was chosen for a voltage drop of -2.5 V across the resistor.

On the basis of the above assessments the following table in Table 2 explains the values of the resistors chosen for the corresponding transistors.

Table 2 :- **Table showing Operating Conditions of the PMOS Transistors under test**

Operating Conditions	For A 10x80 µm PMOS	For A 20X80 µm PMOS	For A 40X80 µm PMOS	For A 80x80 µm PMOS
Threshold Voltage	- 2.5 V	- 2.5 V	- 2.5 V	- 2.5 V
Gate Bias Voltage	- 2.79 V	- 2.79 V	- 2 V	- 2 V
Drain Source Current At Gate Bias	- 14 µA	- 56 µA	- 21 µA	- 99 µA
Value Of Load Resistor	17.48 KOHM	44.4 KOHM	119 KOHM	251 KOHM

As mentioned in the above paragraphs the high frequency measurement was done with the help of waveform generators and oscilloscopes for the transistors in consideration. The parasitic capacitance of any transistor is the main hindrance for lowering the frequency values for any transistor in question. This can be avoided by a load resistance as mentioned before and

measurement of the voltage gain. The voltage gain and phase are measured with the oscilloscope. The voltage gain and the phase are simultaneously measured with the increment of the input frequency and with respect to the input signal. The f_{max} is thus measured when the gain decreases to 1 or 0 dB. It is an important point to be noted here that the main difference in the voltage gain can be done by changing the offset value of the respective transistors to have a higher or lesser gain depending on the size of the transistors.

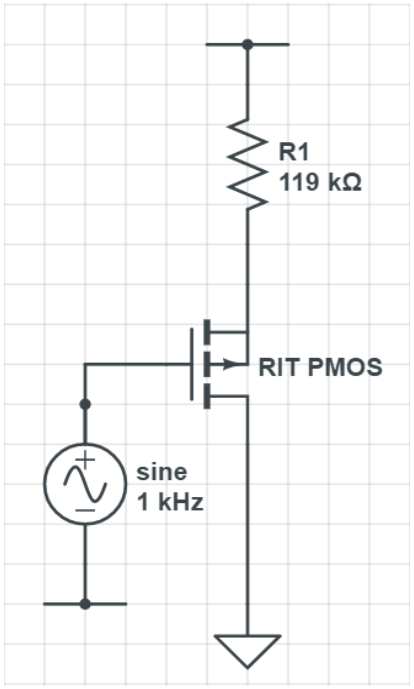


Fig. 17:- A typical circuit diagram for a PMOS transistor amplifier with a V_{gs} of -2 to -3 V

The circuit shown above in Fig. 18 was tested using a waveform generator to drive the gate voltage at the V_{gs} bias with a small ac signal of 100 mV amplitude with a 119 KOHM resistor and an input frequency of 1 KHz. The ac voltage output from source to drain was measured with an oscilloscope. The gain was calculated as $A_V = V_{out}/ V_{in}$ and the phase difference was measured in the oscilloscope.

Two different devices with 80/20 µm W/L ratios was measured as shown below

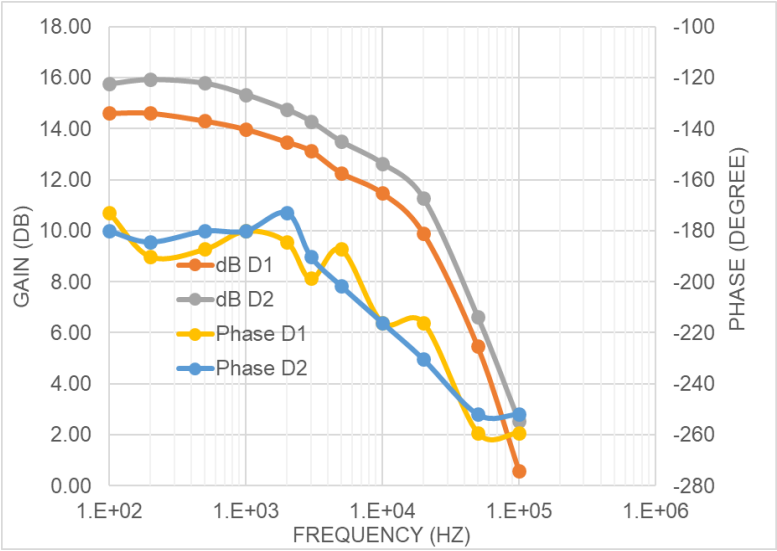


Fig. 18 :- Gain and phase of 80/20 µm metal gate PMOS transistor fabricated at RIT as a function of frequency.

As shown in Fig. 18 the gain at low frequencies is between 14 and 16 dB (5x to 6x) for both devices and the phase is about -180 degrees as this is an inverting amplifier configuration. As the frequency is increased the gain decreases and the phase starts to increase, indicating the transistors have a hard time keeping up with the frequency of the input voltage at the gate. The gain decreases to unity (0 dB) at about 10 KHz for both devices. A HP network analyzer was used.

Table 3 :- **Table shows the Values of Different Dimensions of PMOS and their f_{max} Values.**

DIMENSIONS OF PMOS TRANSISTORS	VALUE OF THE f_{max}
80/80 µm	8.31 kHz
40/80 µm	41.68 kHz
20/80 µm	100.07 kHz
10/80 µm	149.13 kHz

We observe an increasing value of the f_{max} with the decrease in the channel length.
A more efficient method is to use the network analyzer for the frequency measurements of the transistor. In the network analyzer the amplitude, input frequency and the offset voltages are set while the analyzer sweeps the frequency of the input signal and the output is monitored. This way it is easier to estimate the value of the f_{max} when the gain is plotted against the frequency. The phase shift is also calculated from the analyzer. Table 3 shows the list of four dimensions observed. We have observed that the characteristic values for the f_{max} all range within 60 kHz and not more than that at 0 dB.

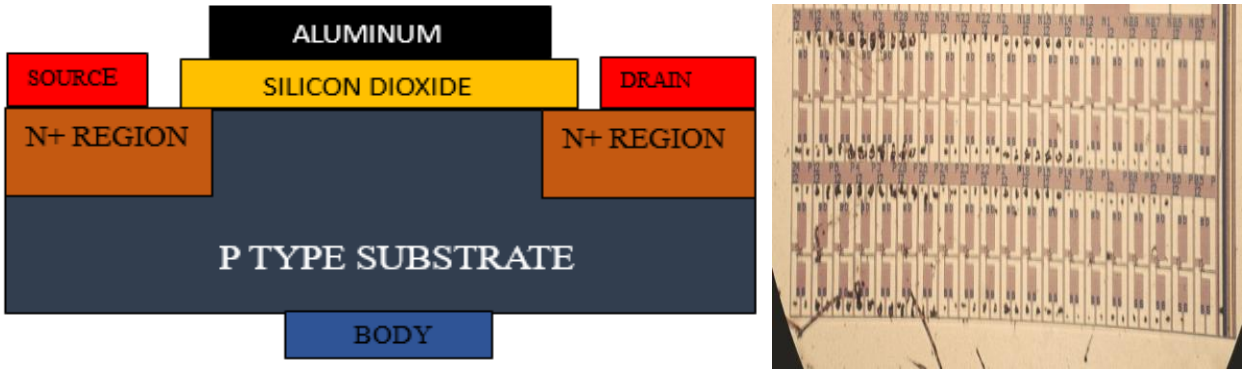


Fig. 19 :- Schematic diagram of a typical N TYPE MOSFET fabricated at RIT (left) and microscopic view of a series of NMOS transistors fabricated at RIT (right)

3.2 NMOS

As mentioned earlier we have taken the example of the NMOS a schematic and microscopic view as shown in Fig. 19 to characterize our Graphene transistors. As in the case of PMOS we took a variety of dimensions for our analysis of the frequency and the gain for the NMOS devices. The dimensions were 24x12 µm, 12x12 µm, 6x12 µm, 3x12 µm and 1.4x12 µm for a single wafer instead of taking two separate wafers and then comparing the values. Upon determination of the ID-VD curves with VGS of 1V steps the value of IDS in saturation was

obtained for a V_{out} of 2.5 V and a V_{gs} of 3V for each device. The gate source voltage was kept constant for all devices because at the preliminary stage we wanted to see what the values of the gain and the corresponding frequencies are for the particular V_{gs} of 2-3V. The testing method and the circuit topology as shown in Fig. 20 was the same as for the NMOS. The circuit diagram for the devices is as shown below.

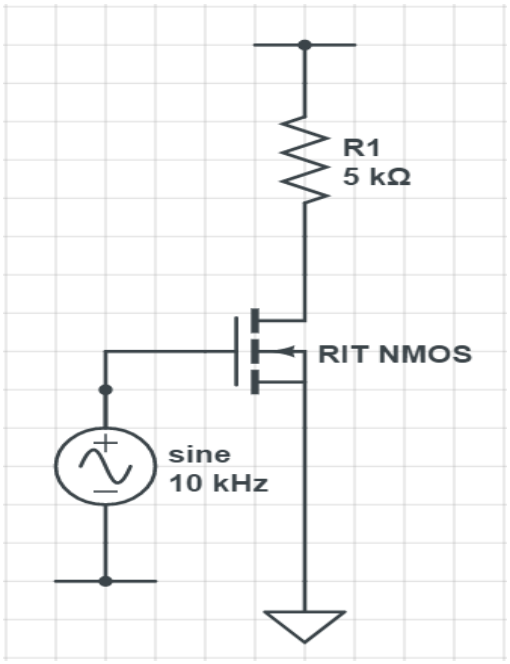


Fig. 20:- A typical circuit diagram for a NMOS transistor amplifier with a V_{gs} value of 2 to 3V

The corresponding Table 4 for the individual values of the NMOS transistors are as follows.

Table 4 :- **Table showing different operating conditions for the NMOS transistors under test.**

Operating Conditions	For a 24x12 µm NMOS Transistor	For a 12X12 µm NMOS Transistor	For a 6X12 µm NMOS Transistor	For a 3X12 µm NMOS Transistor
Gate Bias Voltage	3 V	3 V	3 V	3 V

Drain Source Current At Gate Bias	50 µA	88 µA	191 µA	357 µA
Value Of Load Resistor	50 kΩ	28.4 kΩ	13 kΩ	7 kΩ

The input frequency for the 24x12 µm was set to 10 KHz with the same amplitude as the PMOS i.e 100mV and a VGS of 3V. The results for the observation in the network analyzer are shown below in Fig. 20 where the gain is plotted against frequency.

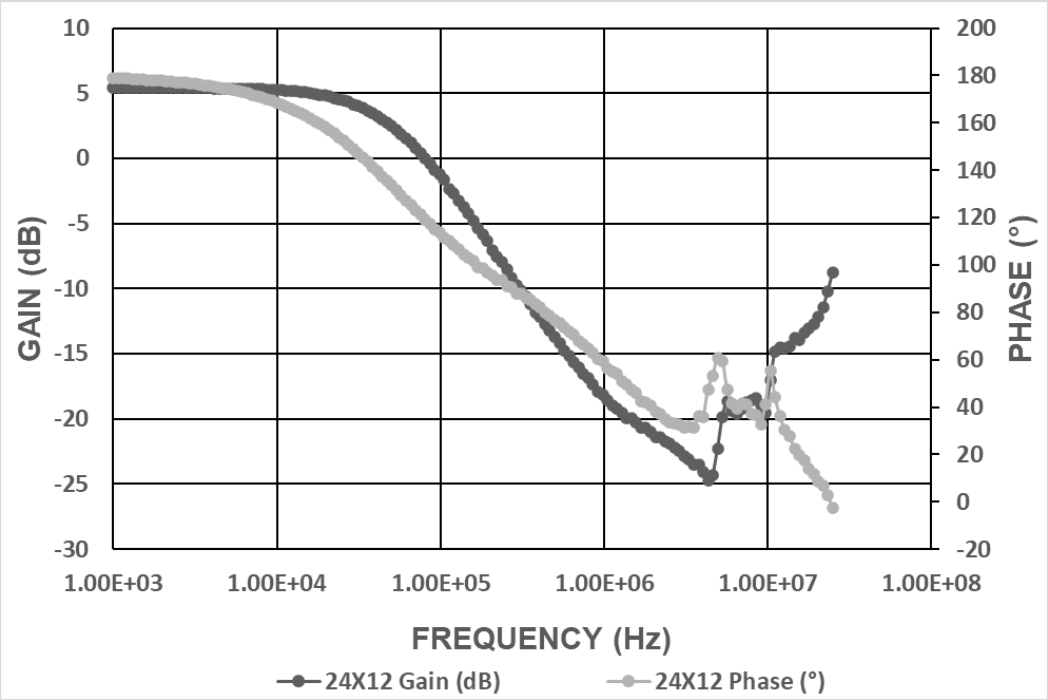


Fig. 21:- The gain vs frequency of a typical 12x24 µm NMOS transistor along with the phase in degrees and gain in dB.

We observe that the gain falls uniformly with the increase in the frequency for the transistor with a uniform phase shift that is, the transistors have a hard time keeping up with the increment in the input frequency, the same as was observed in the case for the PMOS. The value of the f_{max} for this transistor was determined to be at 80.49 KHz.

Moving forward to test the 12x12 µm dimension transistor a similar nature was observed and the same was repeated in the case of the others as well as we kept going down for the channel lengths.

It was observed that the values of the f_{max} for the transistors kept on increasing as we went down in the length of the channel. We theorize that the gate overlap capacitances of the NMOS transistors were decreasing and hence resulting in an increase in f_{max} . We can estimate that at this point as we have also observed that the transconductance for all the transistors goes up and the gain remains constant which also infers the fact that the mobility of the electrons is increasing with the shortening of the channel length. It is also a matter of fact that variation in the value of the V_{gs} may have an influence in the increment for the value of the f_{max} . In future experiments it has to be determined what different results are obtain in varying that value. We have kept the value strictly between 2-3 V as mentioned before for all of the above-mentioned transistors so maybe with a decrease in the overlap capacitances if the value of V_{gs} be increased to somewhere in the midpoint or higher between 3-4 V then we can observe a higher value for the f_{max}.

All of the above being said it is important, however, to consider the mobility of these transistors. It is quite naturally assumed that with the decrease in the channel length the mobility always increases and hence gives an appraisal in the value of the transconductance.

The below graph in Fig. 22 will show all our results we have obtained for the gain vs frequency for the NMOS transistors and Table 5 shows increase in value of the f_{max} with decrease in the channel length.

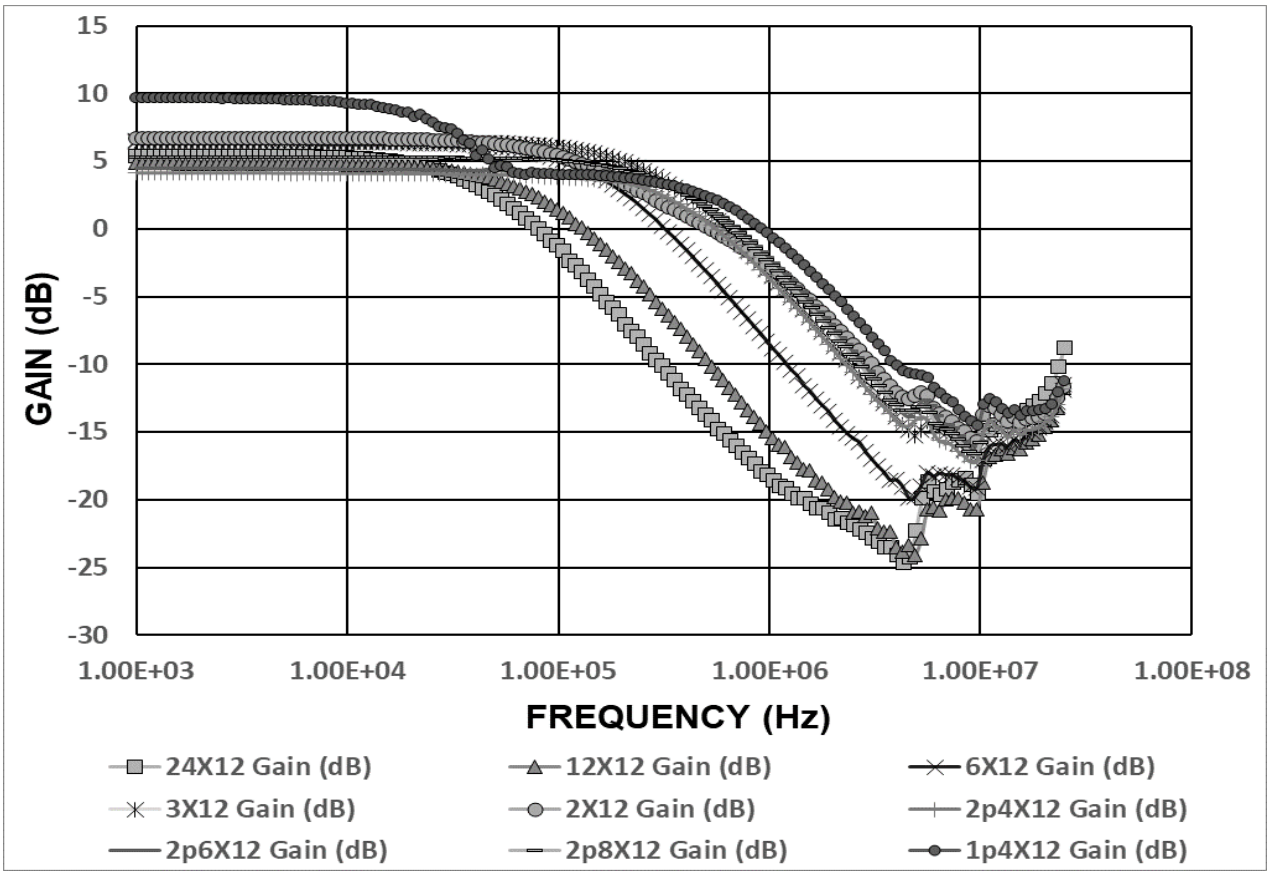


Fig. 22:- Gain Vs Frequency graph plotted for the NMOS of all the various sizes fabricated at RIT

Table 5 :- **Table shows the Increase of f_{max} with the Decrease in Channel Length.**

DIMENSION OF NMOS TRANSISTORS	VALUE OF THE f_{max}
24X12 µm	80.49 KHz
12X12 µm	128.56 KHz
6X12 µm	308.99 KHz
3X12 µm	606.57 KHz
1.4X12 µm	914.70 KHz

Taking all of the above into account to study for our GFETS made at RIT with a multitude of

different structures we have observed a variety of similarities with that of both the PMOS and the NMOS in terms of the offset voltages as well as with the value of the gain of the transistors. However, to date the value of the determined f_{max} is undecided as the uniformity of the Gain vs Frequency graph for our GFETs has not been observed to make a device characterization and comparison. We then worked to improve the mobility of the GFETS in order to increase the value of the transconductance and in turn to increase the value of the f_{max}. The GFETs which have been fabricated have a phase shift which was varying very much with the slightest change in frequency.

3.3 GFETS

In our SMFL at RIT we have fabricated both top-gated and bottom-gated GFETs whose Dirac Points have seemed promising for the top-gated GFET variant but not for the bottom-gated ones. The top-gated GFETs have a Dirac Point close to 4 V. However, in the testing phase of these transistors for the f_{max} values we have found the gain of the channel to be in the negative and increasing towards the positive for almost all the transistors. Along with this we have noticed that there is too much noise in the output channel from the oscilloscope. Consequently, the phase shift in the network analyzer is almost non-conclusive for us to be estimating anything that we have read from the literature to date.

The above being said, on a positive side we have investigated a commercially available Graphenea GFET S-10 chip for sensing applications with back gated transistors. We have noticed some very particular characteristics from that which are worthy to mention here. Although there was the absence of top-gated transistors we can still estimate the gain and phase

shift of GFETs and have an idea of what we are aiming to fabricate from their data sheet.

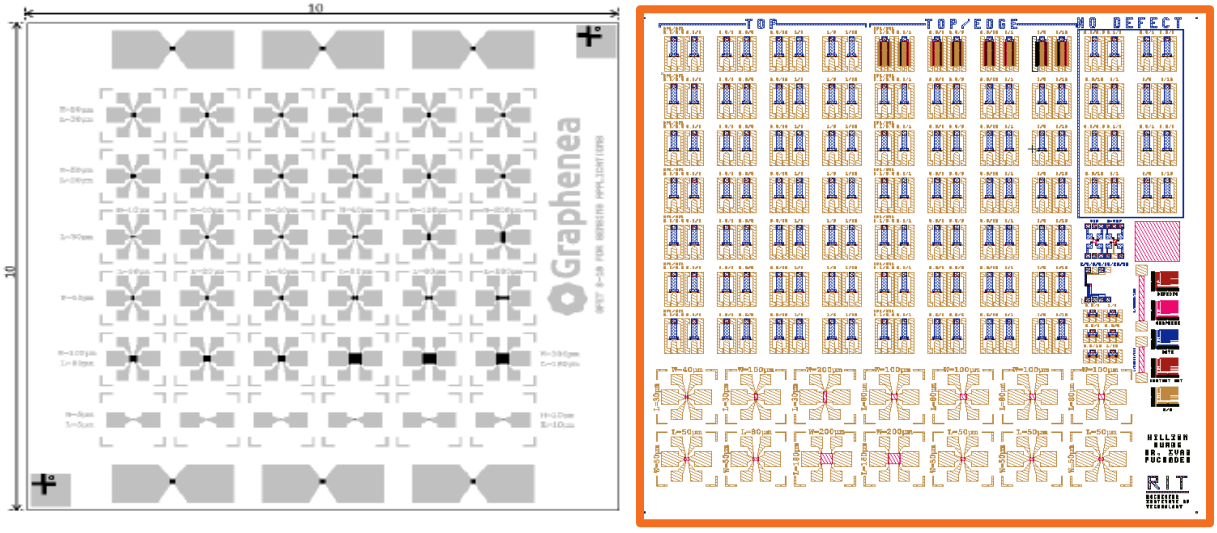


Fig. 23 :- The layout of a typical GFET S-10 Graphenea chip for sensing applications (left) and a layout of a RIT fabricated chip with top-gated and back gated GFETs. Bottom two rows are top-gated and the upper seven rows are top-gated. (right)

Table 6 :- **Table above shows the Values of Fmax and the Dimensions of the Commercially Available Sensor Chips**

DIMENSION OF THE GRAPHENEA BACK GATED GFETS (µm)	VALUE OF THE f_{max}
50 X 50 µm (First Variant)	2.14 KHz
100 X 80 µm (First Variant)	3.24 KHz
50 x 50 µm(Second Variant)	7.43 KHz
100 x 80 µm (Second Variant)	13.27 KHz
5 x 5 µm	21.83 KHz

Again, the testing method is the same for the GFETs as it was the PMOS and NMOS shown previously. The difference here is as there is no saturation presence in GFETs due to the absence of a band gap as mentioned before, therefore we have taken the ID-VG curves of these back-

gated transistors for picking up the particular value of I_d to find the appropriate value of the load resistor. We have gate biased all of the transistors for 1.8 V. The load resistor as mentioned was chosen for a voltage drop of 1 V across the resistor.

We can see here that an increasing trend in the value of f_{max} has been found with decrease in the channel length. So, it can be inferred that the comparisons we have made to date with the PMOS and the NMOS regarding the decrease in channel length leads to increase in the value of the f_{max} will work for our GFETs as well when they are fabricated to perfection in the best possible way. Although it has been said in the previous sections that back-gated transistors are not good for RF performance, it will be still good to fabricate them first and see the gain and the phase change graphs in order to estimate the value for the top-gated GFETs. The frequency response schematic and comparison table is as is shown in Figures 23, 24 and Table 6.

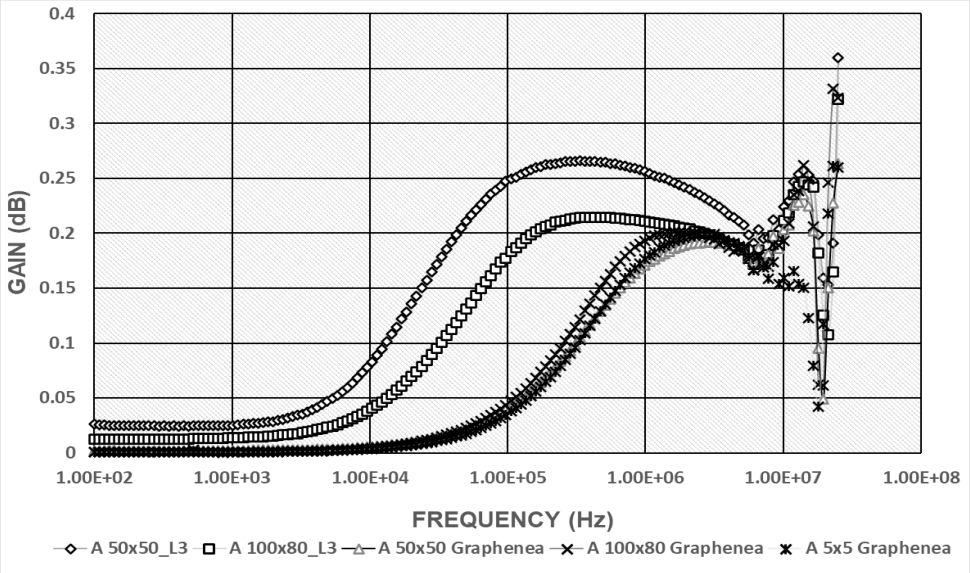


Fig. 24 :- Gain and frequency for all the different dimensions of the back gated transistors are shown for the Graphenea chip.

3.4 Effect of the Parasitic Capacitances of a PMOS and NMOS theoretically and experimentally on F_{MAX}

I. PMOS

Theoretical

As it is quite well known that the gate overlaps capacitances C_{GS} and C_{GD} play a very vital role in the evaluation of the f_t and f_{max} value, both theoretically as well as experimentally.

The Figure of merit for C_{GS} is,

$$C_{GS} = C_{OX} W L_{OV} = 8\ X\ 10^{-5} X\ 4.93\ X\ 10^{-9} X\ 1\ X\ 10^{-5} = .004\ fF$$

The Fig. of merit for f_{max} is ,

$$F_T = \frac{gm}{2\pi(C_{GS} + C_{GD})} = \frac{0.5}{0.0502} = 100\ KHz$$

$$F_{MAX} = \sqrt{\frac{f_t}{8 \prod R_G C_{GD}}} = 118\ KHz$$

The above value of f_{max} is extracted keeping in mind that the CGS and the CGD values are the same for the PMOS of W/L 80/10 µm. The g_m value has been taken from the difference between two points from the ID-VG curve obtained for the transistor.

Experimental

The value for the same transistor experimentally was obtained to be the same as shown in the Fig. 20. However, varying the value of V_{gs} changes the frequency by some KHz but that value is certainly not a noticeable one. It is to be noted that the transconductance value has been taken from the ID-VG slope of the 80/20 µm transistor. Different transconductance values leads to different values of the f_{max} . In our experimental considerations we have taken two adjacent values from the steepest part of the slope that is to say two points in saturation which are remaining constant and the points after that are not varying much in value with the ones taken.

II. NMOS

Theoretical

$C_{GS} = C_{Field} \times L \times G_{FOX} = 5.31 \times 10^{-9} \times 1 \times 3 \times 2 = 1.8$ fF

$C_{GD} = 1.8$ fF

$F_T = \frac{gm}{2\pi(C_{GS}+C_{GD})} = \frac{2.09}{36.48} = 92.47$ KHz $\quad F_{max} = \sqrt{\frac{f_t}{8\prod R_G C_{GD}}} = 522$ KHz

Experimental

The same procedure was followed in case of the NMOS as well where the transconductance was taken from the ID-VG slope of the 3 µm x12 µm transistor and the value was found to be 606.57 KHz which is slightly higher than the theoretical values. This is because in all the cases the value for the g_m or transconductance is not always constant in experiment and hence the experimental value is slightly higher than the theoretical values. The same is observed for the variants of the PMOS except for the 10/80 µm variety as specified above.

Multiple wafers from different lots were measured and compared to publish the given results in order to get a definite idea about the variation in the frequency range. It might be noteworthy that not much of a variation in all the values were seen for both the PMOS and the NMOS.

CHAPTER IV. Transfer characteristics of Top-Gated and Back Gated GFETS

As Graphene is such a material in which saturation is practically absent except in the case of the Negative Differential Resistance (NDR) which has been discussed earlier, the transfer characteristic curves are mainly referred to as the ID-VG curves instead of the ID-VD or the family of curves. These curves are especially beneficial for the choosing of the bias point or Q point for the determination of the values for the f_t and f_{max} similar to that of the PMOS and the NMOS. In addition to what has been discussed in the previous sections regarding the absence of this bandgap, the potential of Graphene in terms of bringing a change to the transistor is very much diminished as it fails to create the "off" state necessary for the transistor. Physicists have found that stacking two layers of Graphene on top of each other, that is to say formation of bilayer Graphene with the appropriate biasing also leads to the formation of the bandgap [37-38].

The application of the gate voltage on GFETs brings about a shift in the Fermi level due to the application of an electric field and hence there is a shift in the Dirac Point as well. This can be more pronounced and observed if a hysteresis sweep is done on a given voltage range. The value and range of the sweep is the most important and that can be determined by the steepness of the slope of the initial I-V curve. That is to say if the Dirac Point is at positive and falling a higher sweeping range is to be applied and if is steep then equal sweeping range on both sides is the most preferrable. Studies by Han et al. suggested that channel scaling from 5 μm to 90 nm also has a role in shifting the Dirac Point, hinting at the short-channel effects in GFETS [39] and further proved to be the influence of hot carriers (holes) by influence of the high electric field by Shi et al. with devices having channel lengths of 2 μm [40]. Influence of hot carriers for Dirac

Point shift may be attributed to photoluminescence as shown by Matsumoto et al. in Graphene phototransistors which was abnormally large and equal to 20 V [41].

4.1 Transfer characteristics of ID-VG Curves of RIT top & Back Gated GFETS

I. Back Gated Variety

At the SMFL at RIT there have been two significant lots which have been fabricated as discussed in the previous sections in their process flows with monolayer graphene. The ID-VG curves have been duly obtained for the various individual chips of the lots. All of the lots contain local or top-gated transistors and global or back-gated transistors. The lots were tested under various conditions over a period of time and observations on the transfer characteristics were made. The first lot for which the back-gated transistors were found to be having good transfer characteristics as compared to the top-gated devices. There is no thickness variation observed in the graphene layer.

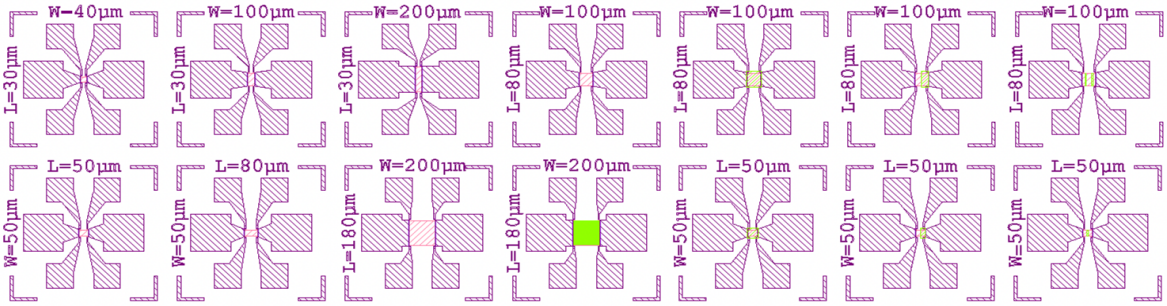


Fig. 25:- 7 Species of back gated Graphene transistors fabricated at RIT SMFL.

The back-gated transistors were tested for all the seven variants as illustrated in Fig. 25 above for the ID-VG curves using a HP 4145B D.C parameter analyzer where the Dirac Point was

observed to be in the range of 20V-30V for a constant V_{DS} of 0.01V and the slope was seen to be falling on the electron dominant region of the curve indicating a fall in the mobility and in turn a decrease in the transconductance value for all the transistors. It is interesting to note that all of the transistors regardless of the length and width exhibit the same nature that is to say an imbalance of electrons and holes occurring on both sides of the Dirac Point, the '100x30'µm variant having the least number of holes in it. Such an imbalance is mainly due to the domination of the holes for all the variants and insignificant electron presence so much that the slope is seen to be falling off on the positive side of the Dirac Point where the Fermi level is positive. RF performance of such back-gated transistors with such a large Dirac Point is hence not viable because of the reasons discussed earlier of which the very small value of the gate oxide capacitance (3.84 E-8) is attributed as the main reason which prevents the transistors from having a high value of transconductance. Application of huge control voltages is required for the transconductance and hence f_{max} to have a considerable value.

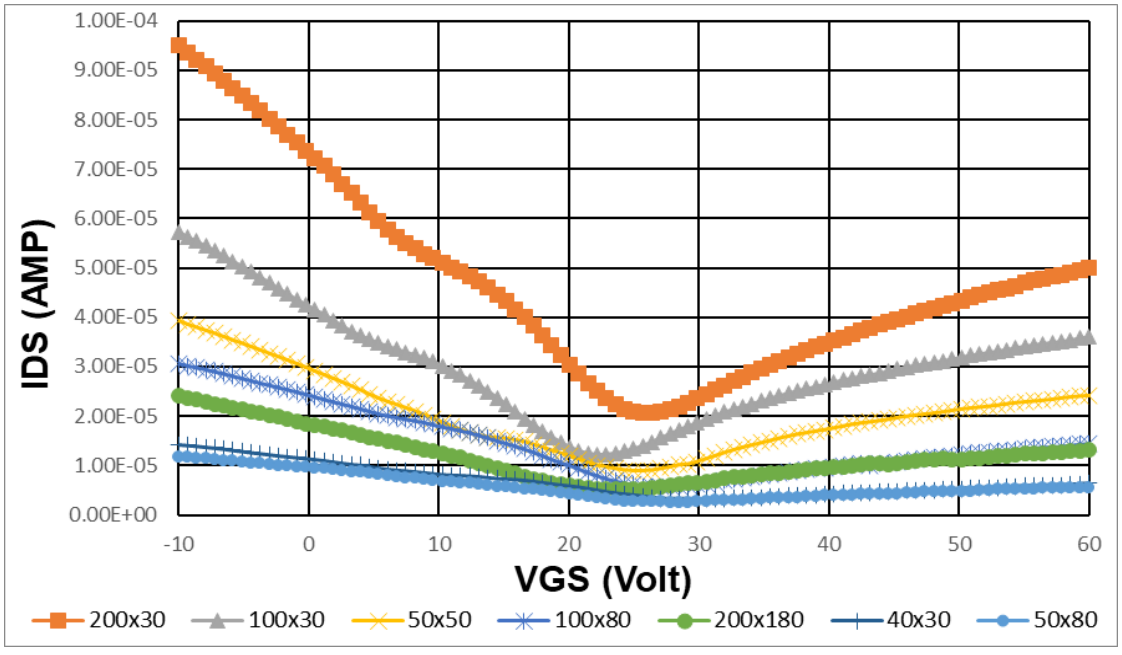


Fig. 26:- ID-VG Curves of 7 variants of back gated GFETs fabricated at RIT SMFL.

As is illustrated in Fig. 26 in all the curves shown it is quite impossible to obtain current saturation as well as obtain a DC voltage gain and a large channel conductance out of these seven variants. A very poor value of maximum transconductance was achieved for all the variants which was 1.36 E-6 µS/cm for the electrons and 2.72 E-6 µS/cm for the holes.

II. Top Gated Variety

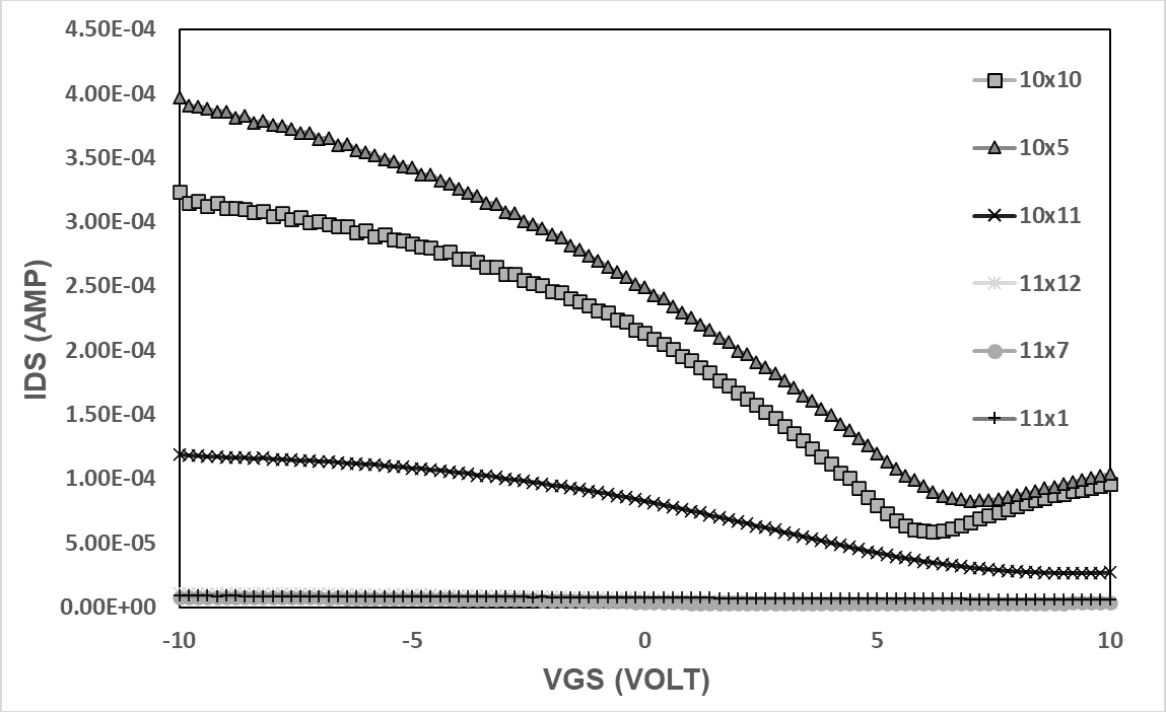


Fig. 27 :- ID-VG curves of 6 variants of top-gated GFETs fabricated at RIT SMFL

The fabricated lots had seven variants of top-gated transistors which were measured the same way as for the back-gated variants. As observed in the case of the back-gated transistors the top-gated ones also exhibit the same nature that is, all of the six tested variants as shown in Fig. 27. have depicted a very low electron mobility or electron dominance and a considerable mobility or hole dominance. The values of the Dirac Point range from 2.80V – 8.20 V for all the six variants with a constant V_{DS} of 1V, the '11x1'µm variant indicated at the bottom in Fig. 27 having no

Dirac Point as the electron mobility of that transistor was obtained as zero. The mobility of electrons for the said variants were found to be in the range of 0-10 cm^2/Vs and that for the holes was 35-100 cm^2/Vs The transconductance ranged from 0-6 µS/cm for the electrons and 0-10 µS/cm for the holes for all the devices under consideration. The top-gated variety is usually considered very good for RF performance due to the presence of the very thin layer of dielectric which in our case was Al_2O_3 of 15 nm in thickness as described in the earlier sections. The choice of the dielectric as mentioned earlier is the most crucial parameter and hence the most commonly used Al_2O_3 was selected and not others like HfO_2 or TiO_2. However, modulating the thickness of the layer is the most important for RF performance because it offers better control over the carriers in the channel and channel modulation can be achieved with application of low gate voltages [27]. In our case even with making the oxide layer as thin as possible the balance of electrons and holes on both sides of the Dirac Point was not possible for both of the above discussed variants and hence RF performance even with applied low gate voltages was not viable. This was the reason why in the preliminary stages of frequency measurements the f_{max} was not achieved with the top and bottom gated varieties. The mobilities extracted followed the Figure of merit, $\frac{g_m}{\frac{W}{L} X\ C_{OX}\ X\ V_{DS}}$ where 'g_m' is the transconductance, 'W' and 'L' are length and width respectively, 'C_{OX}' is the oxide thickness and 'V_{DS}' is the drain source voltage. The transconductance is the maximum which is obtained from the ID-VG curves for all the devices under consideration and is measured by $\frac{\Delta ID}{\Delta VG}$.

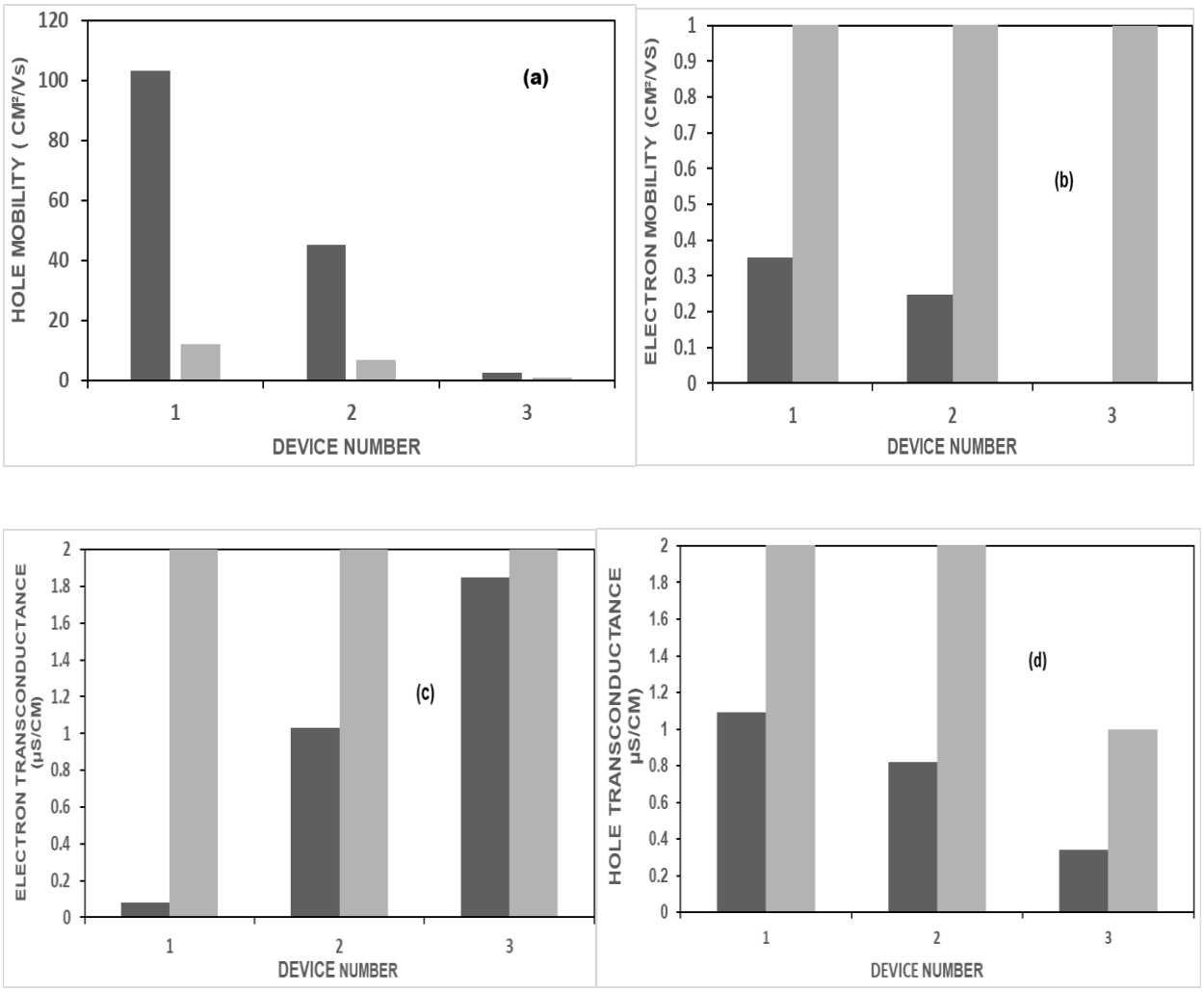


Fig. 28:- Hole mobility for top-gated GFETS of 11x12 µm, 11x7 µm, 11x1 µm dimensions fabricated at RIT SMFL (a). Electron mobility for top-gated GFETS of 11x12 µm, 11x7 µm, 11x1 µm dimensions fabricated at RIT SMFL (b). Hole transconductance of 11x12 µm, 11x7 µm, 11x1 µm dimensions fabricated at RIT SMFL (c). Electron transconductance of 10x11 µm, 10x10 µm, 10x5 µm dimensions fabricated at RIT SMFL (d).

As manifested quite clearly in the above plots in Fig. 28 the channel length of the devices of 11x12 µm, 11x7 µm and 11x1 µm is directly proportional to the electron and hole mobilities. It was seen that the dimensions of 10x11 µm, 10x10 µm and 10x5 µm exhibited no such feature. On the other hand, the hole transconductance was seen to be directly proportional to the channel

length for the 11x12 µm, 11x7 µm and 11x1 µm devices whereas the characteristic was not visible for the 10x10 µm and 10x5 µm ones and the electron transconductance was inversely proportional to channel length for the 10x11 µm, 10x10 µm and 10x5 µm variants and not for the 11x12 µm, 11x7 µm and 11x1 µm ones. So, as a whole it can be inferred that the 11x12 µm, 11x7 µm and 11x1 µm are much more effective in terms of their electron and hole mobilities and hole transconductance than the 10x11 µm, 10x10 µm and 10x5 µm ones. But as far as their Dirac Points and electron transconductances are concerned the 10x11 µm, 10x10 µm and 10x5 µm show much better performance compared to the 11x12 µm, 11x7 µm and 11x1 µm one with a far steeper slope although the 11x12 µm variant showed the highest hole mobility of 103 cm^2/Vs as manifested in Fig. 28. As far as the transconductance is concerned it is true that the 10x11 µm, 10x10 µm and 10x5 µm shows better performance than the other variants in terms of the electrons, not the holes, where again the set of 11x12 µm, 11x7 µm and 11x1 µm dominates. As a summary one can deduce that the decrease in channel width along with the length will be an improvement in terms of transconductance as well as mobility for all the variants. Hence in terms of RF performance these transistors are unstable to give a good value of the f_{max} and as mentioned earlier in discussion of the ID-VG curves did not yield results in frequency performance.

4.2 Application of Polyethylene Imine (PEI) and Dirac Point Shift

As has been discussed in the above sections that the back-gated as well as the top-gated transistors has been proved to be having very poor transfer characteristics in terms of electron mobility as well as the transconductances it is quite evident that the balance of electrons and holes are very much needed for RF performance and to choose a good bias point for the frequency measurements. Also, in this context it is noteworthy that the shifting of the Dirac Point

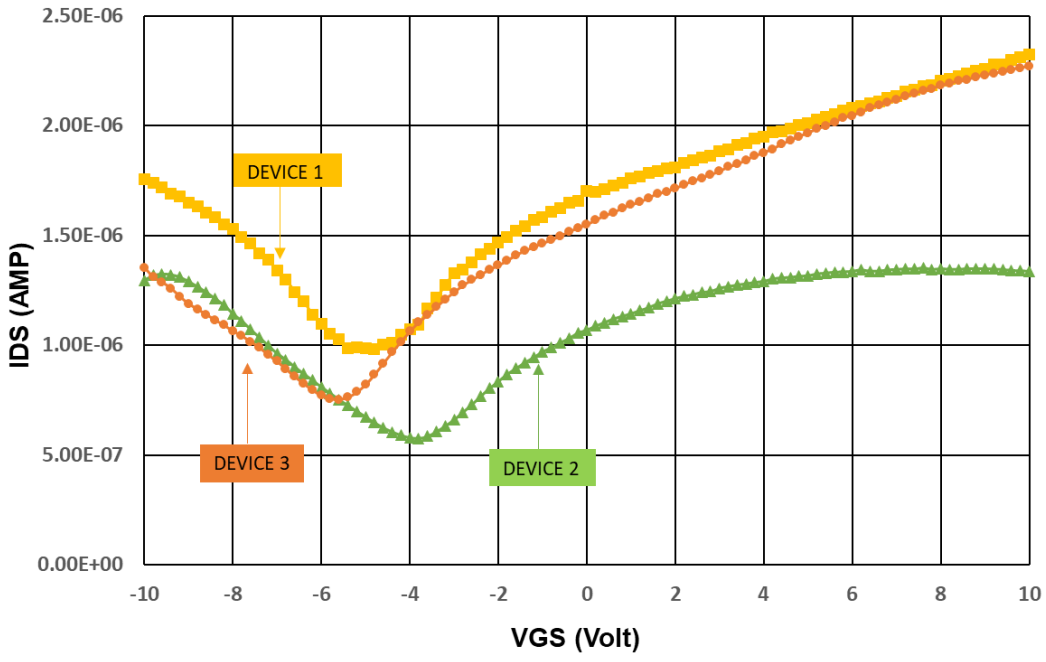
is also needed to the negative voltages in order to facilitate good values for the transconductances. Hence, a n-type doping in the channel region is required for the devices to be performing all the functions discussed above.

Polyethylene Imine (PEI) is a polymer containing an amine group. It is used as a complementary molecular dopant for Graphene previously having shown results for carbon nanotubes [46-47]. The compound produces doping effects which reduce the work function of Graphene considerably. This results in the shifting of the Dirac Point to the left, this is to say that it moves towards its ideal required value of 0 V. Being a complementary dopant PEI is amine rich and reduces the conductance of electrons or holes but not both. It finds its uses for n type doping not only in GFETs but carbon nanotubes as well [43]. In our case, the conduction of electrons have been suppressed and a balance between them has been created as will be shown in the later sections. There are also other dopants such as Hydrogen Silsesquioxane (HSQ) used by Kevin et al. [45] for its properties of both p and n type doping. It showed both dual characteristics as expected and the Dirac Point shifted towards the negative and positive by a large margin of 50 V. Here, HSQ was treated for 3 mins and then baked at 180 °C to give a n- doping effect which results in a shift of -50 V. As for the PEI an experiment done by Zhang et al.[44] in which a regular interval of 3,6,9 minutes in PEI vapor after spin coating and keeping for 10 days was followed. There have been other methods to shift the Dirac Point which have been discussed in the earlier sections.

Hence, the application of the PEI for our top-gated variety is expected to cause a shift in the Dirac Point by making the channel n-doped by the donation of electrons and also supposed to make a rise in electron mobility which was till now absent in our case.

I.Initial PEI Treatment of the Top-Gated GFETS

We have applied the branched variant of the PEI 16% by weight by soaking three chips with all the dimensions of the top-gated devices for 3 hours in an ethanol solution. After that the chips were annealed in forming gas and/or Hydrogen for 10 minutes, rinsed off the excess in ethanol solution again and the chips were dried using a Nitrogen gun. ID-VG tests were then conducted on all of the varieties. The chips were kept in ambient air for 30 hours and then tested by a DC parameter analyzer keeping the V_{DS} value of 0.01 V as before for the Non-PEI chips and all the PEI coated chips were subjected to a sweep from -10V to +10V for the V_{gs}. The Dirac Points which were to date showing a minimum value of 2.8V - 8.20 V for the top-gated variants had now shifted to the left as was proved before for back-gated variants by [43-44][46-47]. This indicated a dominance in the electrons which was absent before the application of the PEI. The 10x10 µm variant with a gate oxide capacitance of 5.78 E-07 was tested for all the three chips.



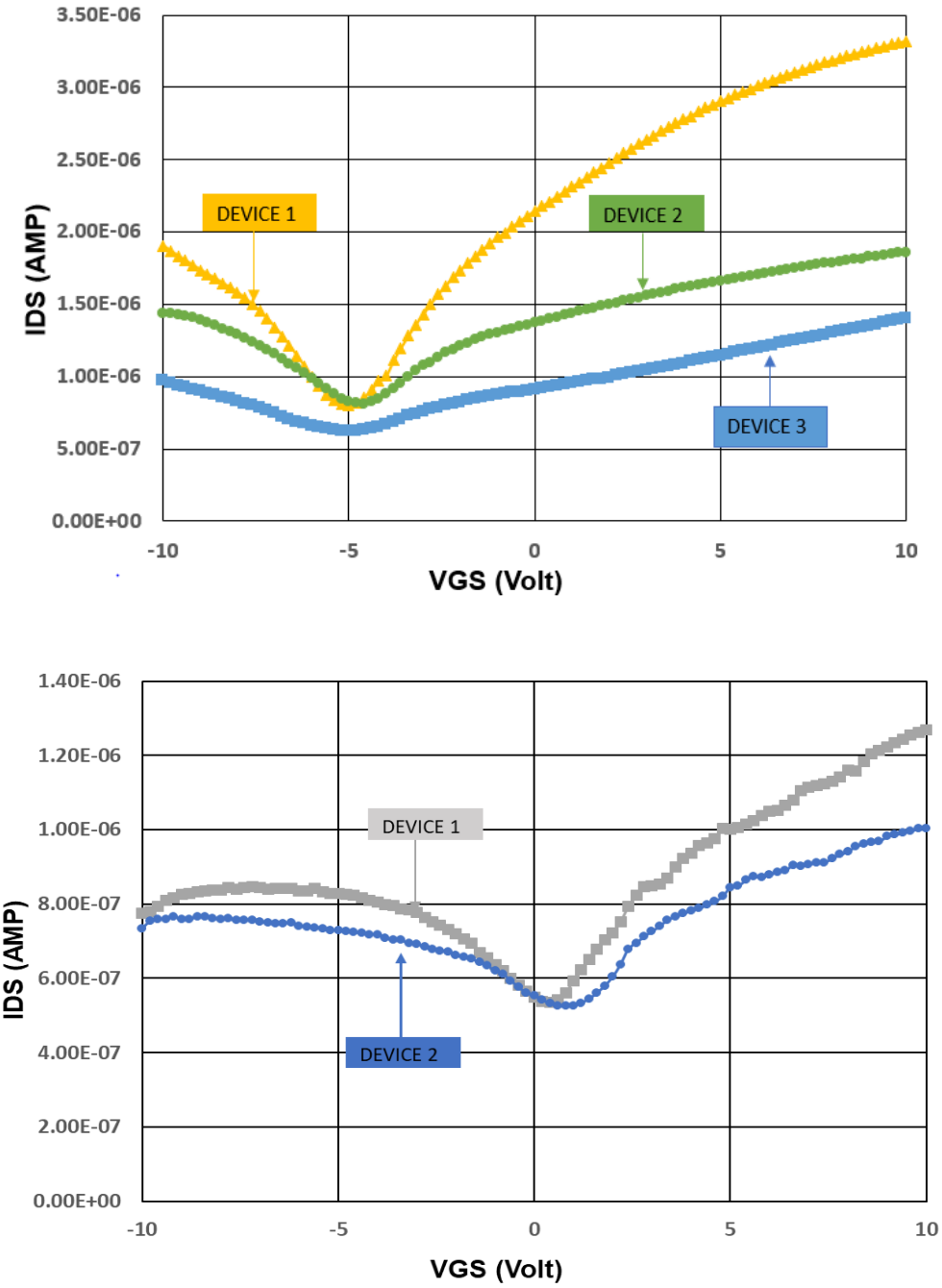
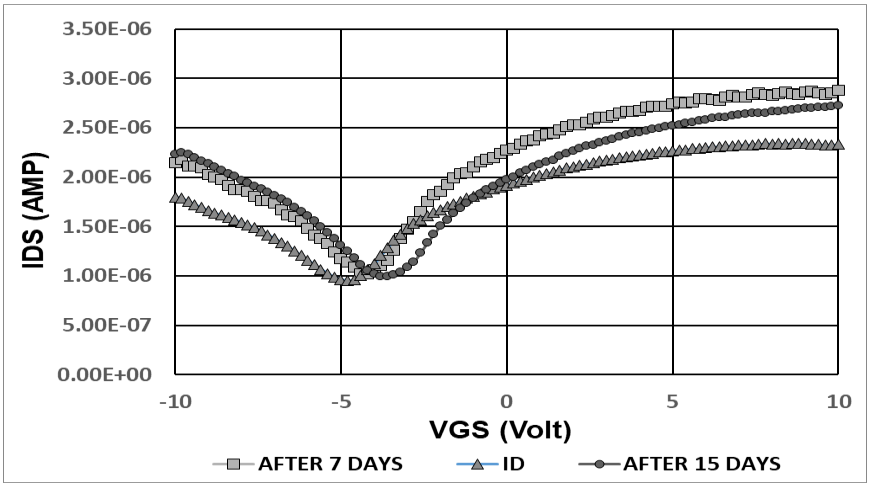
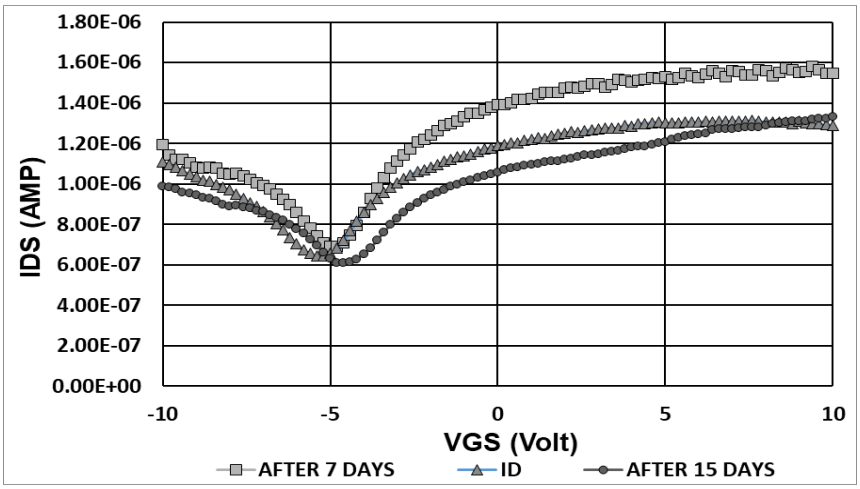


Fig. 29 :- Chip 1 showing three varieties of devices of 10x10 µm in dimension with a Dirac Point shift to a minimum of -5.6V and a maximum of -3.6V (top) Chip 2 showing three varieties of devices of 10x10 µm in dimension with a Dirac Pint shift to a maximum of -4.4V to a minimum of -5V (center) Chip 3 showing two varieties of devices of 10x10 µm in dimension with a Dirac Point shift to a maximum of 1V to a minimum of 0V (bottom).

We attribute this shift of the Dirac Point and shift in the Fermi level to the n-type doping nature of the PEI. This theory is in accordance with the findings of Farmer, et al. and Yan, et al.[43,48] who established the fact that the amine-rich PEI has lone pairs of electrons which are effective electron donors, and the application of a positive gate voltage pulls these electron carriers into the Graphene layer by the means of the downward electric field generated. The sudden rise in electron density also results in high values of the conductance. The flatness of the curve in Device 3 (center) of Fig. 29 indicates that as the negative gate voltage increases there is a subsequent rise in the number of holes which are pulled into the PEI layer and trapped by the amine groups there [48]. It is interesting to note however that one of our devices (Device 1) in Fig. 29 (bottom) has reached the ideal Dirac Point of 0V and Device 2 (bottom) is very close to 0V or at 600 mV. The 0V Dirac Point has been earlier reported to be formed due to the application of 72 nm of Al_2O_3 for a back-gated structure and [27] or by Yan et al. for a 300 nm SiO_2 back gated structure with a dimension of 5x5 μm with 30 nm Pt as source and drain electrodes [48]. The hole mobility was observed to be higher than the electron mobility for all of the devices and variants under consideration. It is safe to assume here that the screening effect of the PEI to screen the charged impurities greatly reduces the Coulombic scattering and hence a steady rise in mobility can be observed [49]. However, it is to be noted that there was always a perfect balance of the electrons and the holes which was absent so far in our experiments. For most of the devices the hole mobility was double that of the electron mobility. The shifting of the Dirac Point to ideal 0V is indeed the perfect condition required for bias point selection in RF measurements.

II. Observation of PEI Soaked Devices after 7 & 15 Days





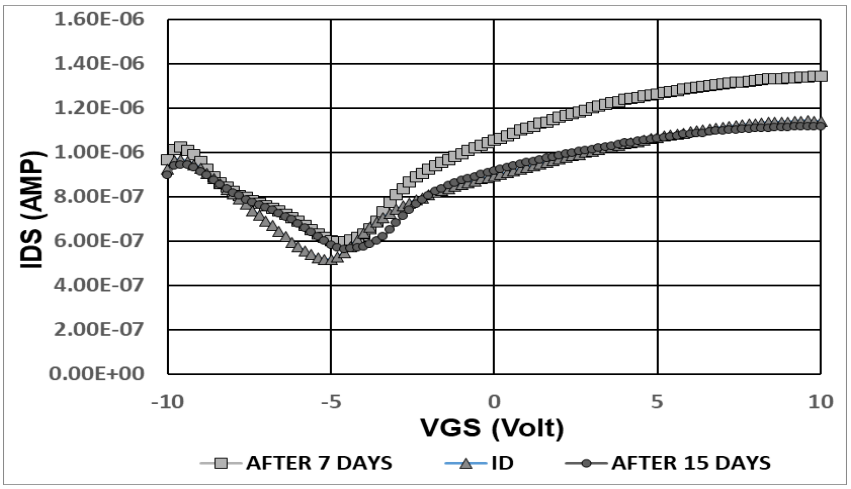


Fig. 30:- Device 1 (top), Device 2 (center) and Device 3 (bottom) show almost no change in Dirac Point after 7 & 15 days of ambient air treatment.

Devices 1, 2 and 3 were exposed to ambient air and kept under observation for 7 days and after that period of time the Dirac Point were observed to be very close to each other without much shift, that is 200 mV, 400 mV and 600 mV respectively. The Dirac Point changes 400 mV for Device 1 and changed 600 mV for Device 2 and 400 mV for Device 3 after 15 days in ambient air. It was observed however that the shift was happening towards the right of the original position (indicated in yellow for all the three plots of Fig. 30). This happens because the GFETS when exposed to ambient air absorbs water, oxygen etc. which results in the shift towards the positive direction [44]. It was observed after 7 days that the electron and hole mobilities for the devices in all of the three chips under observation showed a two-fold or a threefold increment in their values. That is to say a uniform increase of 1.5 times their initial value for both of them. Corresponding transconductances have also risen 1.2-1.5 times from their initial values. The maximum values of transconductance reached for electrons and holes after 7 days are 3.7 μS/cm and 5.58 μS/cm respectively and the electron and hole mobilities were 64 cm^2/Vs and 96 cm^2/Vs respectively.

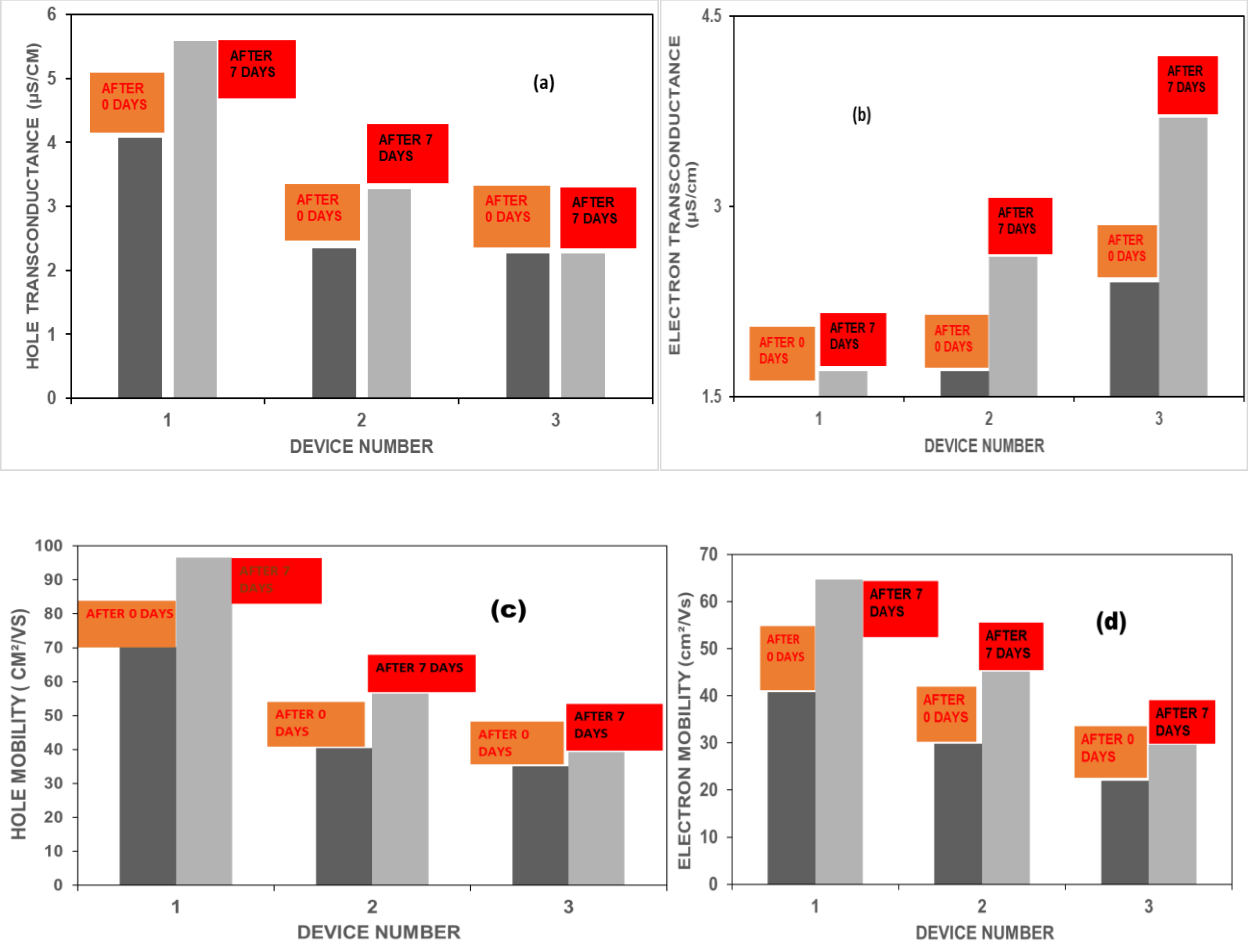


Fig. 31 :- Maximum electron transconductance of all three devices show uniform rise in transconductance after 7 days (a) maximum hole transconductance of all devices show non-uniform rise in transconductance after 7 days (b). Maximum hole mobility showing a non-uniform rise after 7 days (c). Maximum electron mobility showing a uniform rise after 7 days (d).

This uniform rise in both the electron and hole transconductances states the reason why the Dirac Point has not shifted much for all of the devices as if any one of them would have been imbalanced then it would have shifted to the left or to the right accordingly. The balance between the transconductances has prevented that from happening. The little shift which has occurred is towards the right which indicates that the devices have absorbed more H^- ions from the atmosphere.

The electron transconductance had increased for the devices after 15 days to about twice the value they had reached after 7 days while the hole transconductances had decreased to half of their values reached after 7 days. As far as the mobilities were concerned, both the electron and hole mobilities had decreased by 1.5 times of the value reached after 7 days. This uniform decrement is also another reason why the Dirac Point has not shifted much in the position observed after 7 days. The small right shift observed after 15 days from 7 days is also again attributed to the dominance of electron mobility over the holes which causes it to shift.

The maximum value for transconductances of electrons and holes reached after 15 days are 3.4 µS/cm and 4.72 µS/cm respectively. The electron and hole mobilities are 57 cm^2/Vs and 81 $cm^2/Vs,$ respectively, as shown in Fig. 30.

CHAPTER V. Hysteresis analysis for PEI treated and Non- PEI Treated samples

The works of Yan, et.al has proved in the past that the application of the PEI on the GFETS makes them act like an electron and a hole reservoir which can be modulated by external gate voltage and further suggested that varying the thickness of the films the unipolar and ambipolar n type GFETs can be achieved [48]. Feng, et al. further continued the theory of modulating the Dirac Point over a given range of voltage heavily depending on the concentration of the PEI layer being coated on the GFET chips with 300 nm $Si0_2$ [49]. Woo, et al. demonstrated large hysteresis behaviours with a positive Dirac Point about 150V [77]. Xu, et al. showed large hysteresis behaviours as well for GFETs made on 300 nm SiO_2 same as Feng, et al. but also stated that the hysteresis behaviours ceased upon subject to vacuum annealing [78]. Interestingly studies by Sabri, et al. for GFETs made with a parylene (a hydrophobic polymer) layer atop the oxidized layer of SiO_2 has reduced the hysteresis behaviours due to its hydrophobic nature and stated to be less effective that oxide gated devices [79]. To investigate further into the screening function of the PEI and the hysteresis behaviours of the GFETs with applied V_{gs} we have delved into studying them with a set of two experiments. The first one varied V_{gs} applied on the gate for both the PEI soaked chips and the non PEI soaked chips and the second one applied V_{gs} for a particular time on the gate and then made a sweep to observe the hysteresis behaviour of the field-effect devices.

5.1 Experiments done with a constant Frequency and a D.C Offset

I. Non-PEI sample

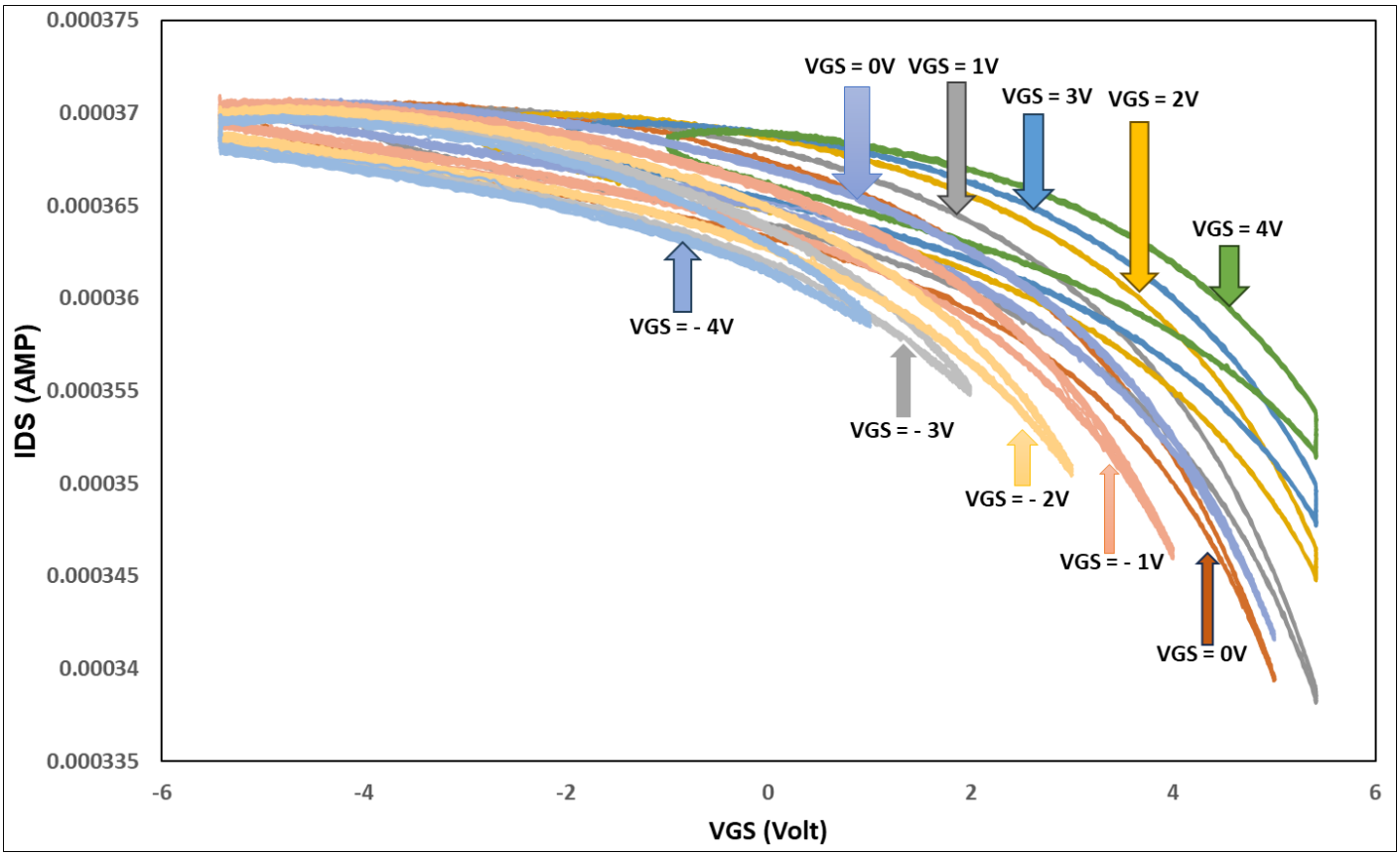


Fig. 32 :- Range of 9 different values of V_{GS} is applied on the gate of a GFET of dimension length = 10 µm and gap= 0.5 µm.(10x0.5µm)

In the first experiment we have applied variable D.C offset sources as shown in Fig. 32 ranging from -4V to +4V to obtain the hysteresis behaviour for the top-gated GFETS of 10 x 0.5 µm dimension of a single device. The drain current remains almost the same in the forward and reverse sweeps of the hysteresis while the shift of the ID-VG hysteresis is not much observed for any given D.C offset value at all. This is to ascertain the fact that the hysteresis loop has not

changed with the applied voltage values. The sweeping range of the voltage being restricted from -6V to 6V the curves have not been obtained to be complete, but it is quite evident that the valley of Dirac Point will be very much visible for all the values of the D.C offset applied with the values +5V to +7V with both forward and backward sweeps applied. The maximum swing which was performed is from +4V to 0V in terms of the D.C offset applied for which the Dirac Point shifted about 2V. This further proves the fact that the absence of a screening effect that the PEI offers from the dipoles of the amine groups present in it on the device. This indicates that with the application of a positive or a negative voltage on the gate the channel becomes n-doped continuously and shifts towards the right. Therefore, it is quite inconclusive here to obtain the tunability of the transport behaviours of the GFET and the correct assessment of the ambipolar nature of the device. Similar to the experiment conducted by Feng, et al. in our devices the ID-VG curves without the PEI have exhibited the same nature. The forward and backward sweeps giving a positive shift of the ID-VG hysteresis was observed in many cases for GFETS with SiO_2 as well.

This right shift can be attributed to the reason that when a positive D.C offset is added to the gate the electrons are attracted by the already present positive charges on it and hence the shift in the Dirac Point happens towards the right. But when we apply a negative D.C offset on the gate due to the absence of the PEI coating the hole or positive charges are not trapped into any layer and are repelled by the already present positive charges on the gate and hence the Dirac Point keeps shifting again towards the right and the trap charges adding a dominant role in doing so.

The Dirac Point steady shift is also explained by the above reasons as a more negative voltage is more number of holes or positive charges and a more negative voltage is more number of electrons or negative charges. Hence, the variation shown in Fig. 32 is the increment of 1V from

-4V to +4V. This characteristic is independent of the gate oxide as this was earlier shown in the works of [50,51,52] the pulsing frequency for the whole hysteresis was kept at 1 KHz and we get to see that the I-V curve could not keep up with the supplied frequency and so the absence of the hysteresis loop was seen. More experiments done with changing the frequency of pulsing will be discussed in later sections.

Hence, in order to better understand the hysteric behaviour of the GFETs a PEI applied chip was taken under observation and tested in the same conditions. The V_{ds} value was kept at +2V for all the measurements and a 120 Ω resistor was connected between the drain and the DC power supply of 3V in order to calculate the value of the drain current by Ohm's Law.

II. PEI sample

The dimension of the transistor under test was kept the same as in the case for the Non-PEI sample. The sweep was started from -2V and done in increments of 1V till 4V with the exception of that from -2V to -4V it was done at an interval of 1V and after that it was tuned to -1V. In contrast to the Non-PEI samples here the PEI coating traps the electrons when a positive D.C offset is applied making the channel p-doped and the opposite that is trap the holes when a negative D.C offset is applied making the channel more n-doped. Apart from this charge trapping the process of capacitive coupling also dominates which is what happens to the curves thus shown in Fig. 33, which can be explained for the forward hysteresis and the backward hysteresis by the capacitive coupling.

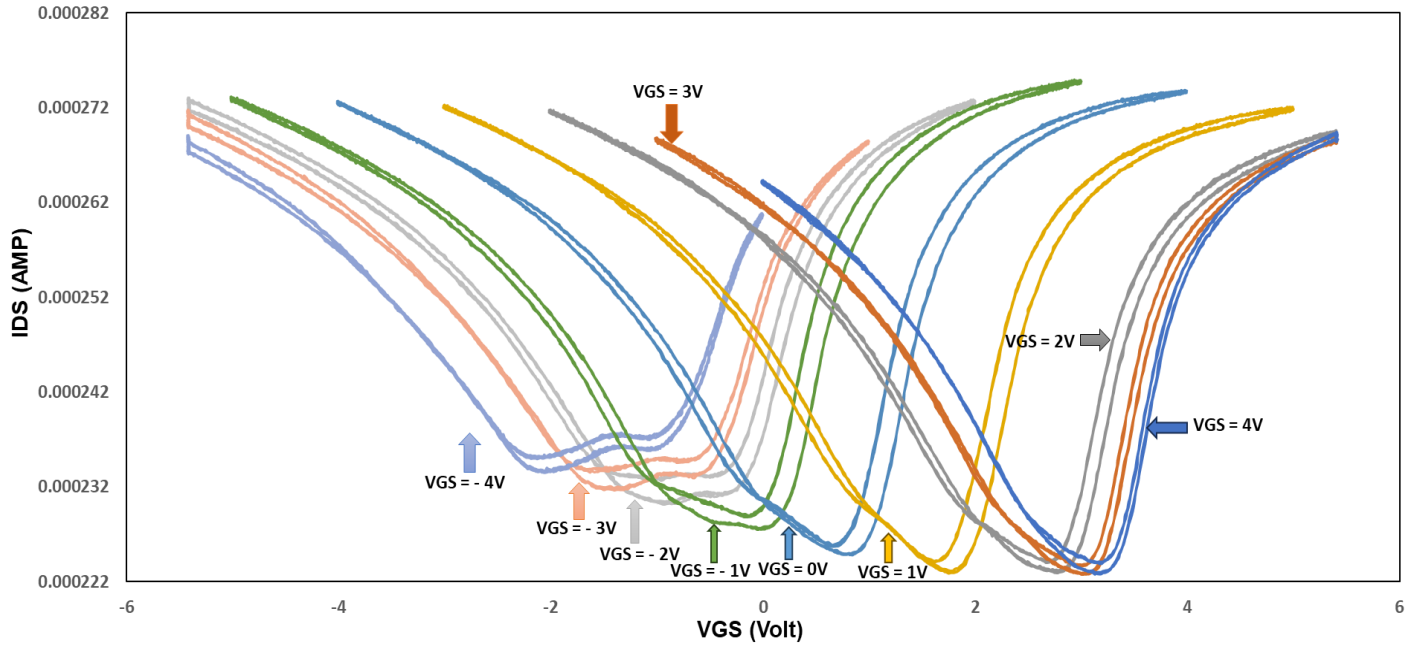


Fig. 33:- Series of 9 curves which demonstrate the hysteresis behaviour of the PEI coated chips under a constant V_{gs} source.

The capacitive coupling is the phenomenon in which the charged ions alter the electrostatic potential around the Graphene layer and pull more opposite charges onto the Graphene from the contacts which are in our case Ni/Au. So, comprehensively in the negative gate voltages applied the negative charges due to coupling drift towards the Graphene layer and induce the holes in the Graphene layer making it p-doped and hence shifting the Dirac Point in the forward or positive direction [49]. The capacitive coupling as mentioned before adds to this phenomenon by adding more positive charges. Again, when a positive gate voltage is applied then the positive charges approach the Graphene layer and due to coupling again renders the channel n-doped causing the Dirac Point to shift towards the left or in a backward or negative direction [49]. The capacitive coupling again plays a role in the shift of the Dirac Point. The hysteresis loop is minimal for the forward or the backward drift because the frequency was 1 KHz which was applied same as with the Non-PEI samples. Another interesting feature observed here was that the value of the drain

current steadily decreases as the value of the D.C offset increases from -3V to +4V. This might be occurring as a result of the interaction between the EDL gating and the oxide gating, that is to say between the aluminum oxide gate and the Graphene layer. It is to be noted here for an applied D.C offset of -4V a prominent double dip in Dirac Point is observed. This is caused by the mismatch of the Fermi level in p-doped and n-doped Graphene due to the applied D.C offset. When a negative D.C offset is applied the value of the drain current is determined by the metal contact region because the Fermi level lies close to the Dirac Point on the left but when a positive D.C offset is applied the value of the drain current is controlled by the channel region as the Fermi Level lies close to the Dirac Point on the right [44]. Hence, with the increasing of the D.C offset values we can observe the double dip slowly decreasing and finally disappearing as the value of the drain current becomes totally controlled by the channel region. This also affirms the fact that the electron mobility is much higher than what it was -4V D.C offset value as explicitly visible in Fig. 33.

Explaining the hysteresis of the backward sweep a bit more, the switching of the amine dipoles of the PEI helps to enhance the transport properties of Graphene [49]. In order to explore more into the hysteresis behaviours of the Non-PEI and the PEI samples we decided to observe the behavior for a variable D.C offset source. The V_{ds} value was kept at +2V for the PEI samples as well and as for the Non-PEI sample a 120 Ω resistor was connected between the drain and DC.

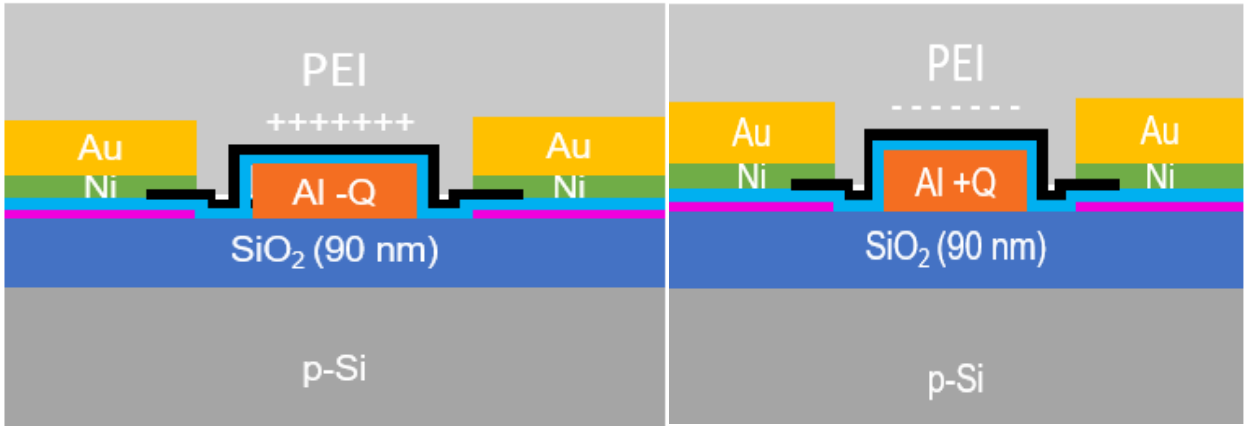


Fig. 34 :- Cross sectional image of PEI coated GFETS showing nature of applied D.C offset on them. Black Layer is the Graphene layer.

5.2 Experiments done without a constant Frequency and an externally applied Gate Voltage

I. Non-PEI sample

Considering time to be an important factor in the supply of the V_{gs} we decided to keep the source on for a considerable time on the gate, then switching it off. After that a sweep was taken to observe the hysteresis behaviours of the GFETS of 10 µm x12 µm with 1 µm gap in dimension. The purpose of the experiment was to ascertain the supply of the positive charges or holes or negative charges or electrons on the gate. The reaction of the Non-PEI and PEI samples to it was to be observed on the basis of accumulation for a particular time to alter the hysteresis behaviours and understand and compare between the constant and variable sources of V_{gs} supplied. Also, we wanted to see how much the drain current extended to, estimate the electron and hole concentration and what was the specific value of the Dirac Point which was not visible for the constant V_{gs} experiment before.

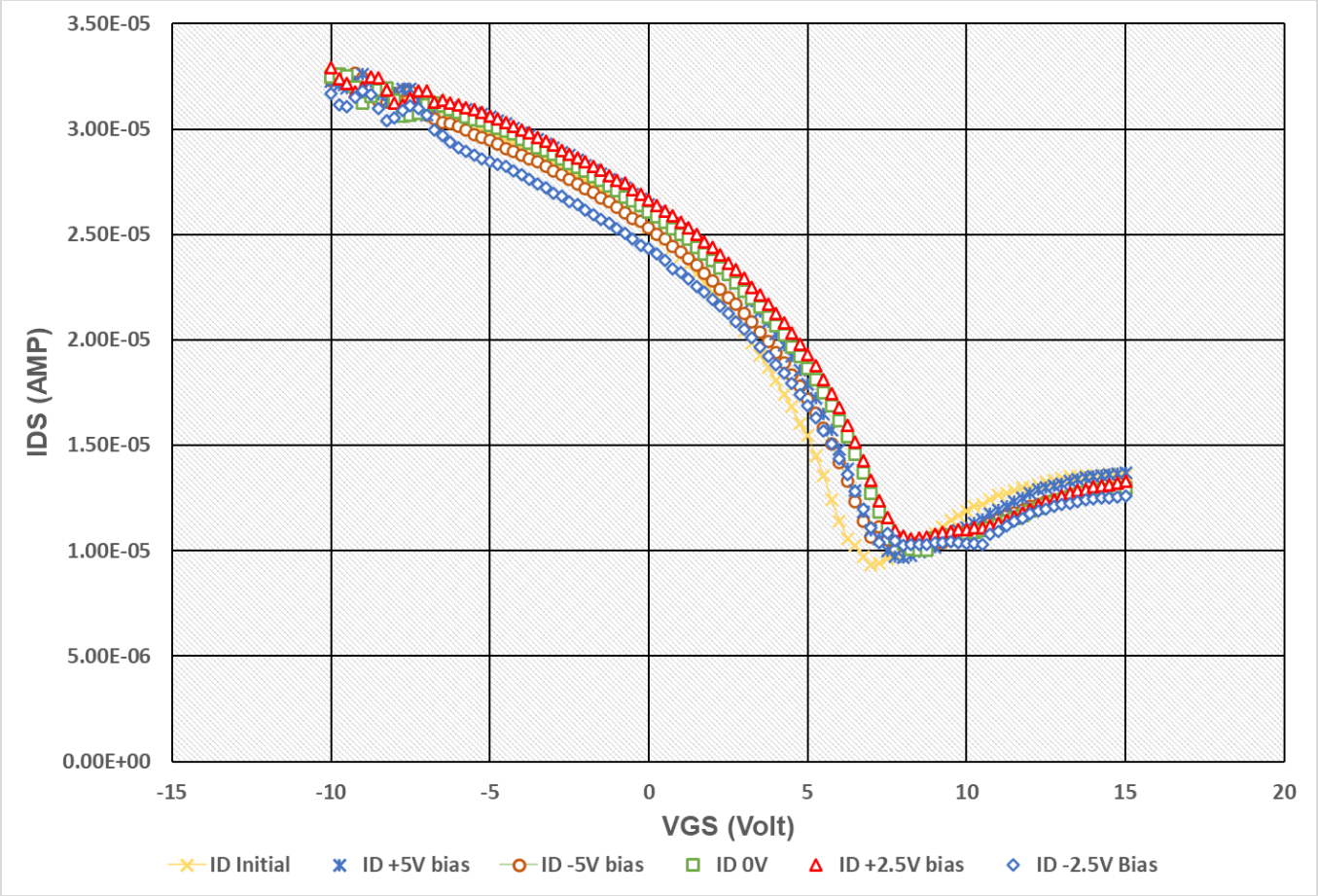


Fig. 35 :- Under no applied frequency and a variable Vgs source of one minute for three values the ID-VG curves as obtained showing a minimal shift in the Dirac Point.

Clearly being manifested from the above image the Dirac Point has not shifted much with the application of a V_{gs} source for one minute for all the values applied on the gate. This implies to the fact that irrespective of the value of the bias or the positive or negative nature of it the charge traps in the Graphene layer were still playing a dominant role in the positive shift of the Dirac Point. The variation was done in a swing from +5V to -5V each being held at for a minute. This was done due to the fact as we wanted to observe if the instantaneous nature of charge change will cause the Dirac Point to shift or not. This is the reason why the steady increaments or decrements in voltages was not followed and for the values of 0, -2.5 +2.5V the same was

observed, the total shift in the Dirac Point being about 3V in the forward direction and nothing more. The electron concentration was being more than the hole concentration all the time and the valley of the Dirac Point flattened out slowly after +5V as is shown in Fig. 35. As we did not see any remarkable change or sign of improvement from the constantly applied V_{gs} values we did not proceed with the backward hysteresis sweep following the same set of V_{gs} values. The V_{ds} value for the variable gate voltage experiments was kept at the same +2V to observe variations under same parameteres.

II. PEI sample

Being apprehensive about the hysteresis behaviours of the PEI coated GFETS being better than the Non-PEI ones we decided to carry out a series of 11 experimental variations on the same applying the hysteresis as a series of forward and reverse sweeps to watch the swing of the Dirac Point. The sweeps were all conducted for a range of -10V to +15V and for one minute supply of V_{gs} of +2.5V, -2.5V, 5V and 0V. In all of the four above mentioned experiments conducted on the variant we have observed that the Dirac Point has not shifted much as was seen in the case for the Non-PEI variant chip but the little variation which is seen has been observed for an increment in the value of the V_{gs}. Hence, it was quite logical to keep increasing the V_{gs} to a considerable value to observe a change in the Dirac Point as well as to increase the supply of the V_{gs} to around 5, 10 and 15 minutes for the next set of seven experiments performed on the variant with an externally supplied gate voltage. One has been already demonstrated in Fig. 36 done with a 5 minute forward sweep of the V_{gs} which has caused the maximum shift in the Dirac Point.

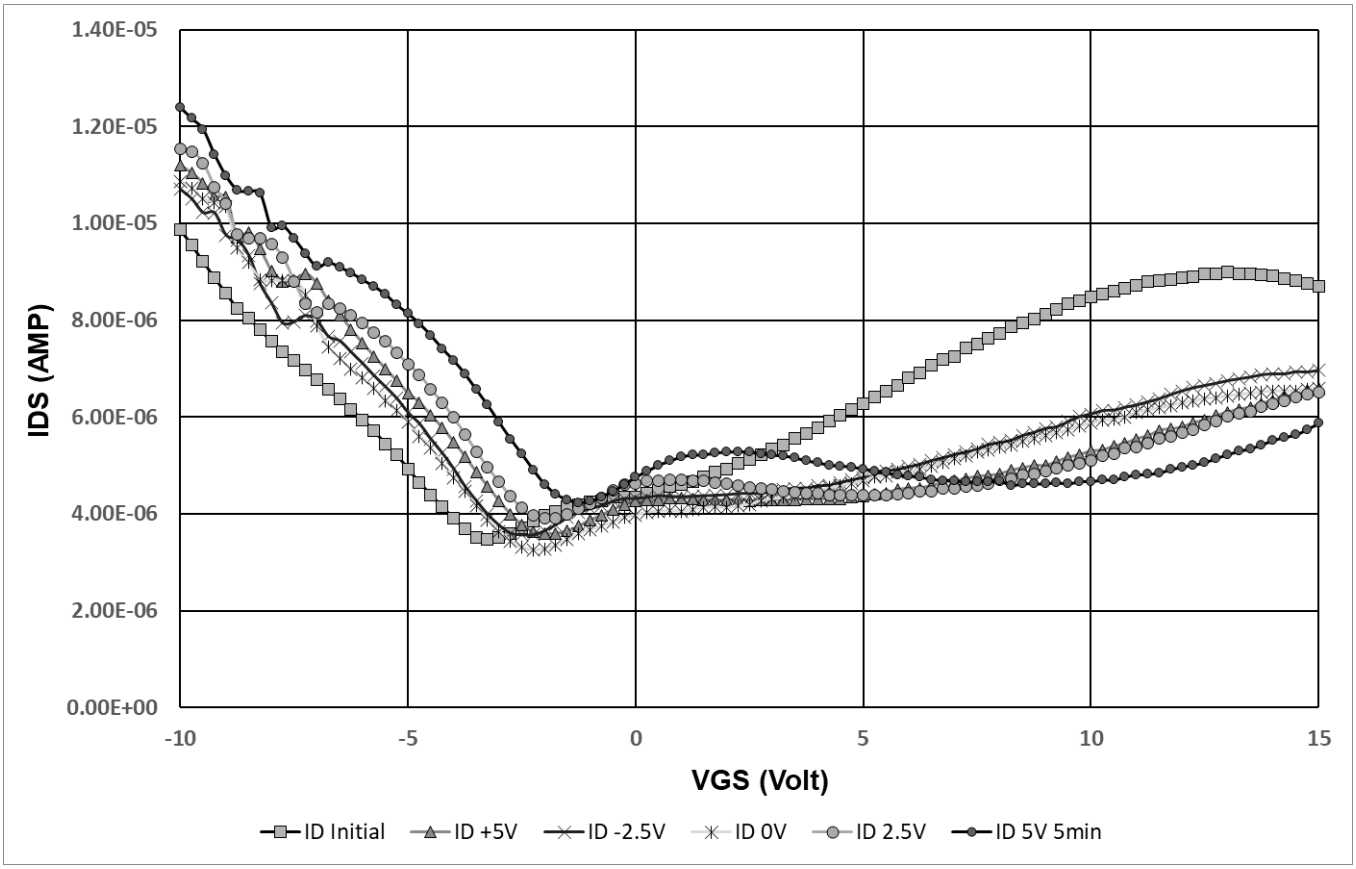


Fig. 36 :- A set of 5 experiments performed with forward sweeps on the PEI variant of 10 µm x12 µm with a gap of 0.5 µm with a variation of Dirac Point better than the Non-PEI variant.

The next set of seven experiments started directly after the 5 minute forward sweep took place just as in the last mentioned experiment. That is, we took a reverse sweep by supplying a V_{gs} of 5V for 5 minutes and switching the supply off as with every case. Doing such we observed the Dirac Point to have swung to a value of around 6.75 V. A total difference of 7.75 V was seen between them. This pointed to the fact that a reverse sweep is beneficial for the PEI coated chip to have a swing in the Dirac Point and that the gathered holes or negative charges was causing it to shift by the mechanisms mentioned earlier in this document. However to ascertain the fact whether it was only the reverse sweep which was causing it to be so we increased the time of supply for the V_{gs} to be around 10 minutes. This time the position of the Dirac Point remained

the same as before. To further the theory of time being a factor for the swing in terms of supply of V_{gs} we increased the value to 15 minutes. This time the Dirac Point did shift a little but the change was negligible. Hence, it was confirmed that the time of supply for the V_{gs} was not a factor in the shift of the Dirac Point and what mattered was the direction of the shift. It is to be noted that for all the sweeps the range of them all was maintained to be from +15V to -10V. A last set of 3 experiments were performed changing the sweeping range and not direction from +10V to -10V keeping the value of the V_{gs} steadily decreasing from 5V then 2V and finally at 0V for all three of them with the time kept for supply of V_{gs} restricted to 5 minutes and no more. The Dirac Point shifted for around 1.75 V with a 5V reverse sweep for -10V to +10V range at a supply time of 5 minutes of V_{gs}. The value of the Dirac Point steadily decreases with the decrease in the value of the V_{gs} that is supplied for the same time, voltage sweeping range and direction. The remaining two experiments were done that way with V_{gs} values of +2V and 0V as shown in Fig. 36. This proves that for a reverse sweep within a fixed range the V_{gs} and Dirac Point value are directly proportional.

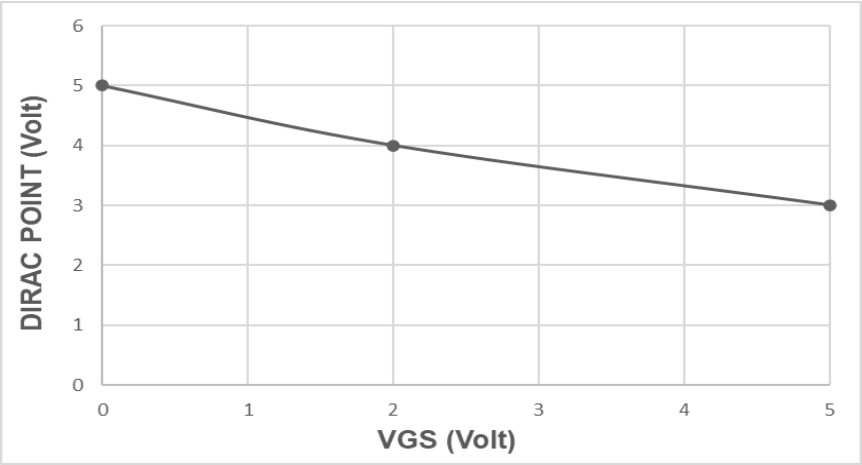


Fig. 37:- A steadily decreasing Dirac Point for a steady decrease in V_{gs} from 5V To 0V values for PEI coated GFETS.

Hence from all of the above as mentioned before time of supply of the gate voltage is irrelevant for the hysteresis behaviour and the shift in the Dirac Point. The range and the value of the V_{gs} are the factors which bring about significant changes to both the above. The V_{ds} value was same as for all the above experiments and at the same +2V.

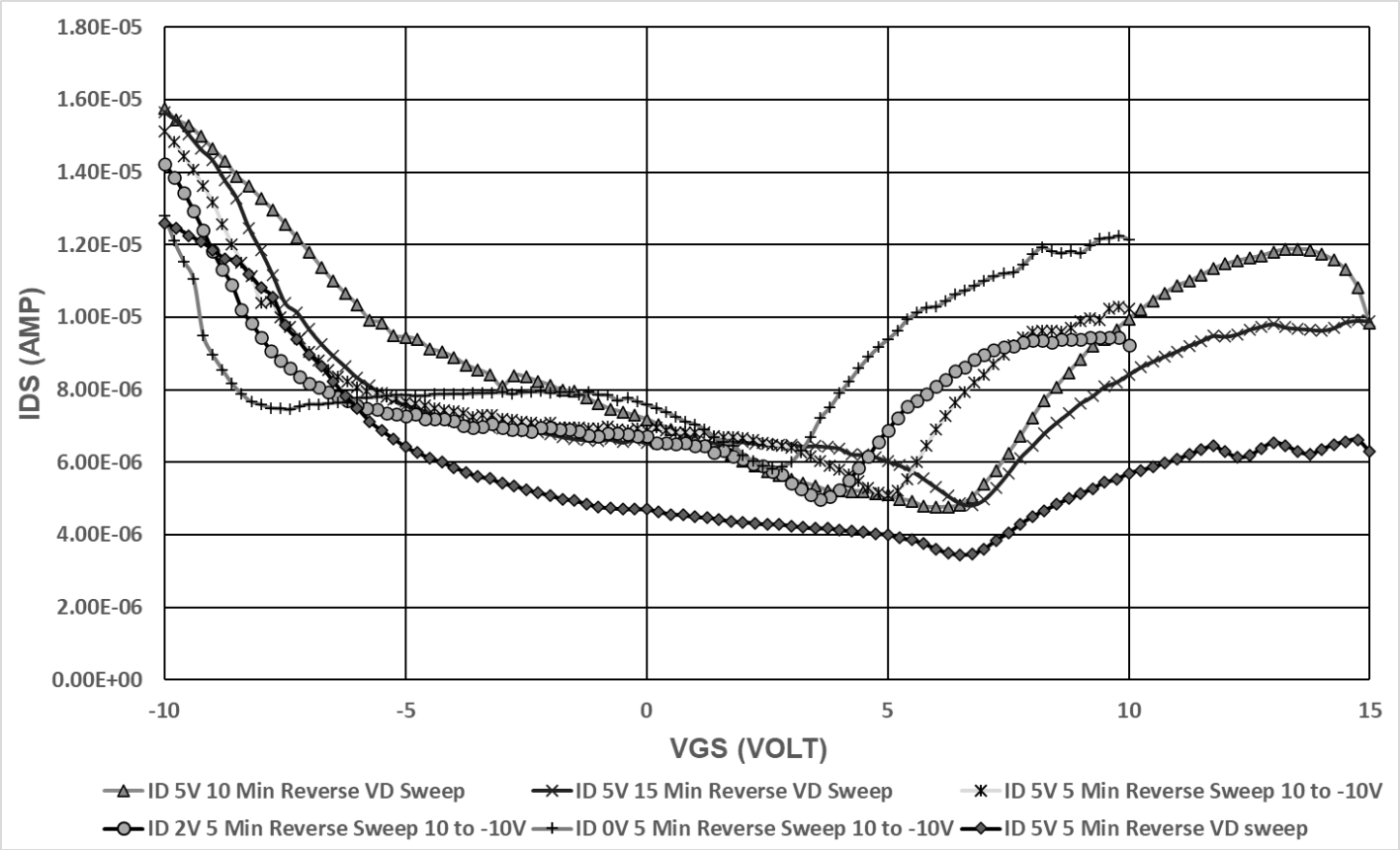


Fig. 38:- A set of 6 experiments performed by reverse sweep with different ranges on the PEI coated GFETs.

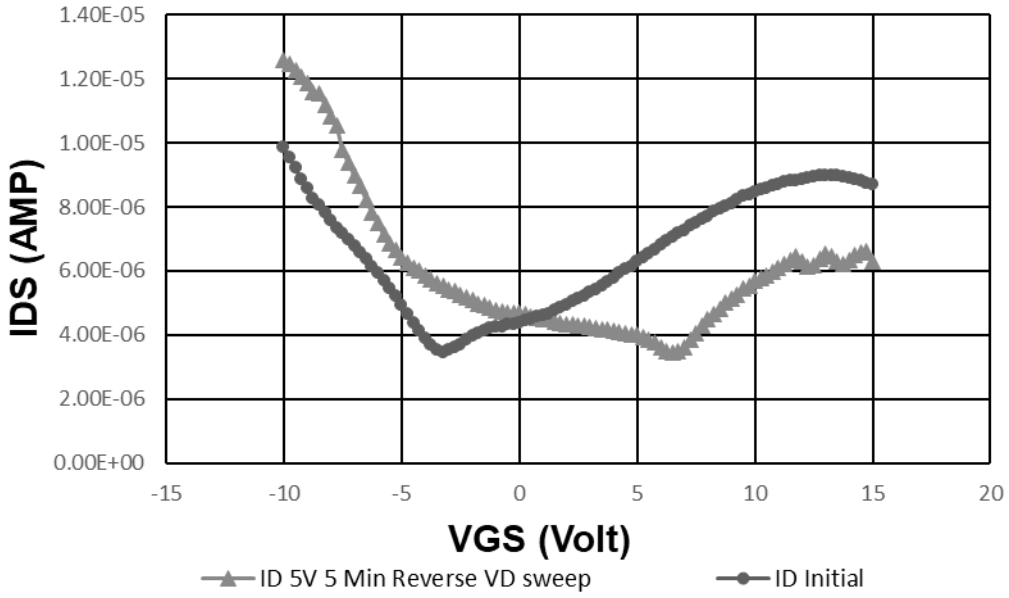


Fig. 39 :- Maximum hysteresis seen in PEI coated GFETs a swing of 10V from the initial value for a applied gate voltage of 5V. The difference between forward and reverse sweeps of -10 to +15V and +15 to -10V is shown in Fig. and has a value of 8V.

The mechanism for all the swings is as explained in the earlier sections but what is most striking is the mechanism of capacitive coupling acting so very prominently for the experiments with variable V_{gs} than the constant values. This can be explained by the fact that of the charges being supplied to the gate the negative or the positive charges are getting trapped in the PEI layer making the channel n-doped or p-doped respectively. This phenomenon happens for a certain period of time and stopped later on. But in the case of a constant supplied V_{gs} the PEI layer reaches a point of saturation of its own where it cannot trap any more charges hence the shift of the Dirac Point is not much visible and the capacitive coupling is also absent in it. The shift occurs only for a certain amount of fixed charges and then stops in the way. Regardless of the channel being n doped or p doped and irrespective of the type of charges approaching the Graphene channel this logic holds good. This reason is also valid for the fact that even with the

steady increments in time values of 5 minutes it does not make a difference as the saturation point for the PEI layer has already been reached. The exact amount of charges and the time of supply of that is however a matter of future investigation. This is further confirming the fact established by Feng, et al.[49] that the concentration of the PEI enhances the backward hysteresis shift of the GFETS. Therefore, it might be the case that the effects of a higher supply time for the V_{gs} that is more than 5 minutes might work more for the hysteresis shift or voltage swing with the increase in the concentration of the PEI from 16% to about 50% or more. This is because the concentration of the PEI being increased thickens the layer which now becomes more susceptible for trapping the charges. Hence the higher time of supply might give different hysteresis results. This theory can be investigated later on in other experiments. Also, rinsing off the excess PEI might not be a good method as that will make the coating more non-uniform and hence its charge trapping properties will not be profound for all the devices on a single chip.

Hence, it can be evaluated that the ions here have a good value of velocity for such a swing to take place. But it also remains as a fact to be investigated whether for a lower value of pulse frequency the hysteresis behaviour remained constant or not as the variable V_{gs} values experiment was done without applying a frequency to it.

5.3 Different variations of experiment done on PEI coated GFETS to understand Hysteresis behaviour

I. Variable Frequency

Previously we were applying a frequency of 1 KHz as mentioned before but then we switched to apply a frequencies of 10 mHz, 100 mHz, 1 Hz, 10 Hz, 100 Hz and 1 KHz as is shown in Fig. 40. We have obseverved that lower the pulse frequency the more prominent is the hysteresis loop

which has been forming.

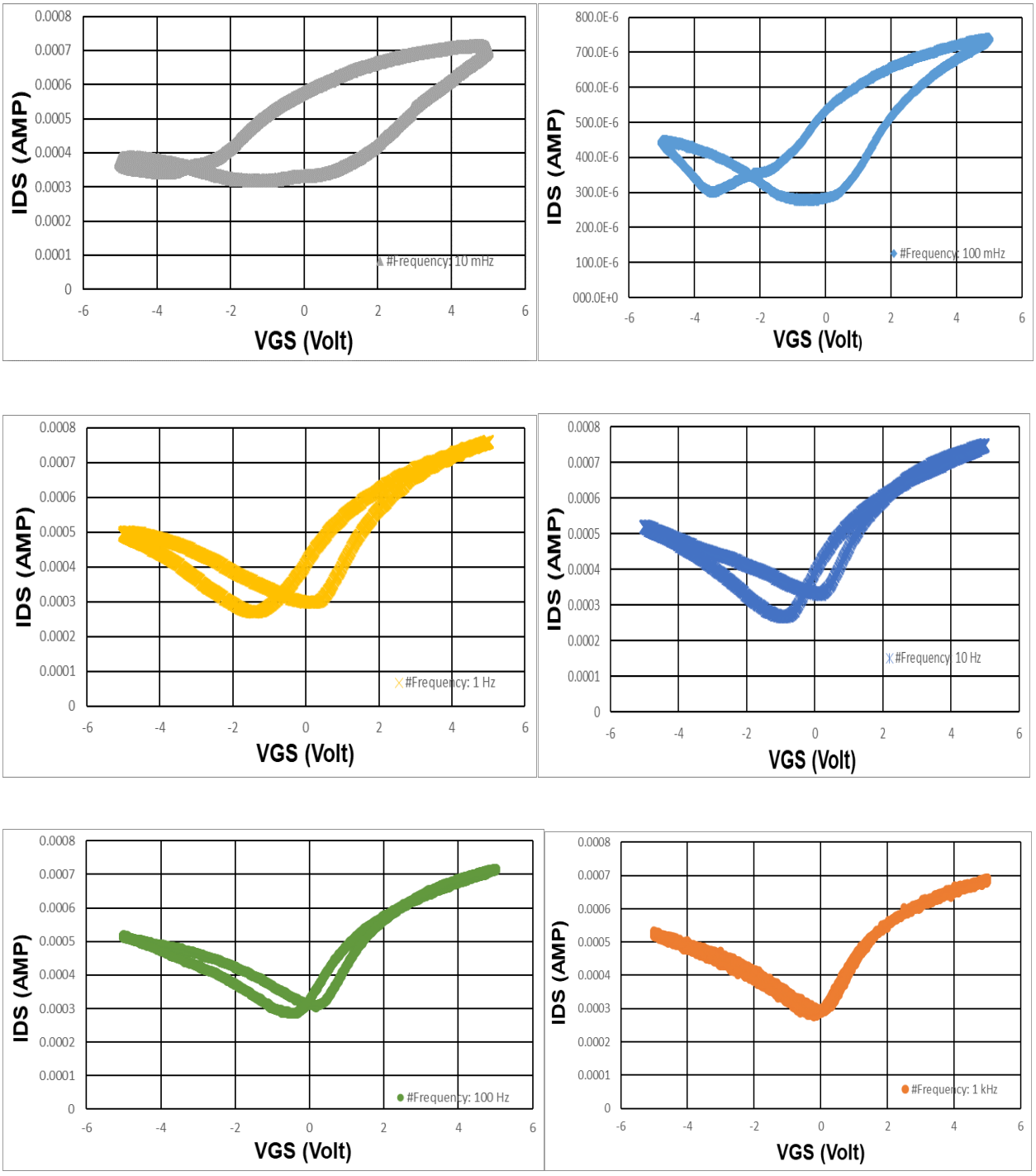


Fig. 40 :- Six hysteresis plots for frequency 10 mHz (light grey), 100 mHz (light blue), 1 Hz (yellow), 10 Hz (deep blue), 100 Hz (green) and 1 KHz (orange).

The variation of the frequency causes the disappearance of the loop as shown in Fig. 40 at a constant V_{gs}. The time period of the respective frequencies are 100 seconds, 20 seconds, 1 second, 100 milliseconds, 10 milliseconds, 1 milliseconds respectively for frequencies of 10 mHz, 100 mHz, 1 Hz, 10 Hz, 100 Hz and 1 KHz respectively. This disappearance of the loop at higher frequencies can be attributed to the fact that the ID-VG curves are incapable of keeping up with the input pulse frequency. A 125 Ω resistor was connected this time for drain current calculations and the V_{ds} remaining at +2V. The time period here indicates the time required to complete one complete hysteresis loop.

The point of the above experiment being conducted was to measure the hysteresis speed of the PEI coated GFETS. From the time extracted it can be asserted very well here that the ions in the PEI have a considerable amount of speed which causes the swing of the ID-VG curve from the positive to the negative. It is to be noted here that the V_{gs} applied here is positive so it was quite imperative to see whether the speed as well as the swing of the ID-VG curve changed with the change in applied V_{gs}. If that happened then what was the time which was required to do so.

II. Variable Bias Voltage

The bias was changed to a variation of -1V, +1V, 0V, +3V, -3V keeping the frequency constant at 1 KHz and the resistance value the same as before for the drain current calculations. The frequency remained constant at 1 KHz and the time period also was constant for all the experiments and the V_{ds} remaining at +2V.

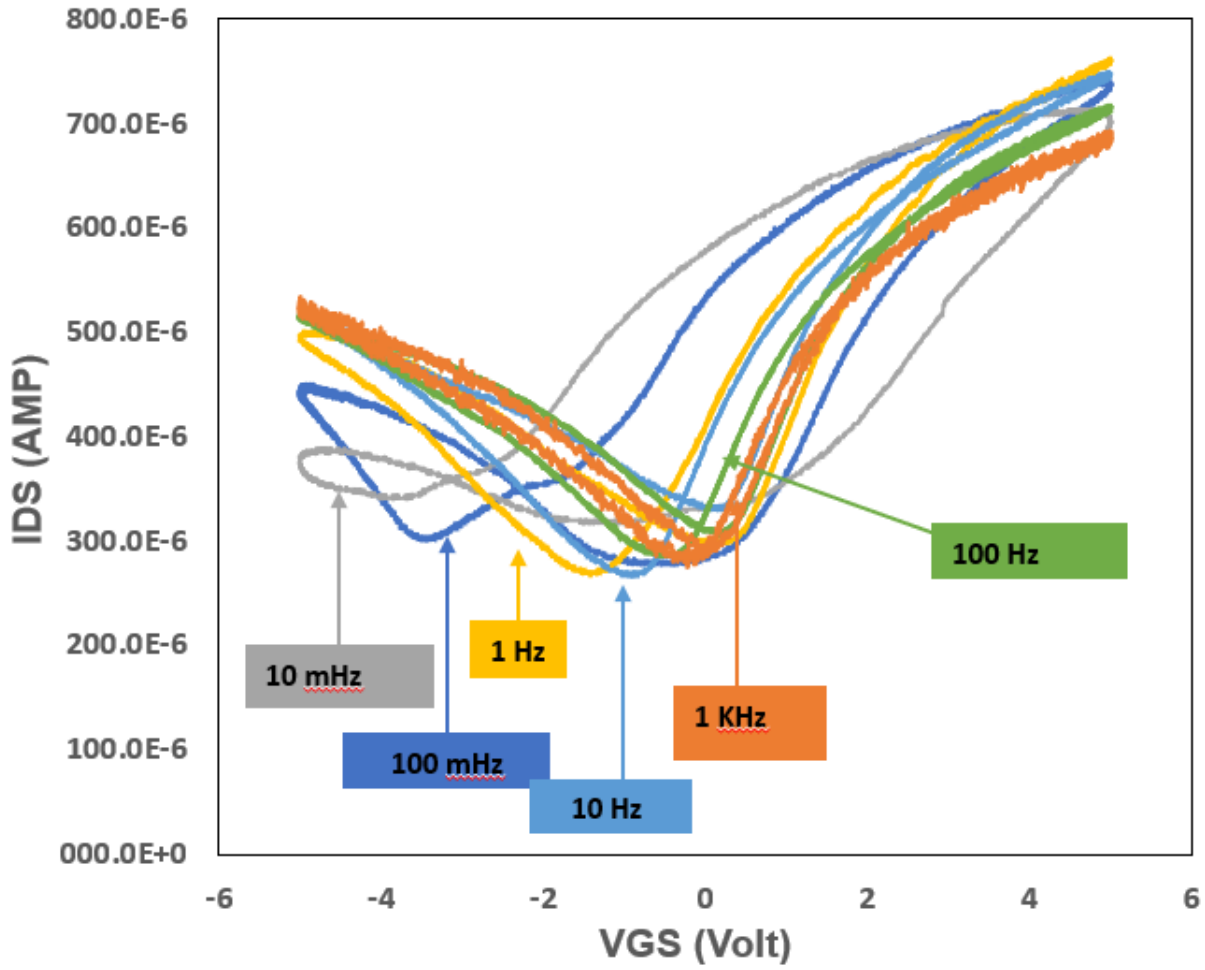


Fig. 41:- Hysteresis behaviour with different V_{gs} applied indicating a large swing in the ID-VG curve.

Not much change in the hysteresis behavior is obtained with the change in the offset as is shown in Fig. 41. The results were more or less the same with the experiments mentioned in the earlier sections done on the PEI. The speed of the ions in this case can be said to be an increment from the earlier experiments as the Dirac Point moves closer to the applied V_{gs}.

These hysteresis behaviours so obtained here are subject to further investigation taking into account and consideration the memory window that they provide. This is because these GFETs then can be attributed to having the properties of Non-Volatile memory devices.

Chapter VI. Frequency Response (f_{max}) of Non PEI and PEI GFETS

6.1 Without Normalization

I.NON-PEI

So far the frequency response from the RIT fabricated GFETS were limited to a negative gain and more importantly a lot of distortions or noise was seen in the output channel. In order to obtain better results from them measurements were again done for a different lot of chips with the dimensions of 10x0.5 µm, 5x0.5 µm, parallel 0.5 µm, 10x1 µm and 5x1 µm. We have measured three different transistors of the 10x0.5 µm variant, two different transistors of the 5x0.5 µm variant, a parallel variant of 0.5 µm dimension and two variants of the 10x1 µm and another one of 5x1 µm dimension. The uniformity of gain was not found for any of the Non-PEI chips with a range lying between 0.02 and 0.14 dB but it was still somewhat better than the other lot of chips which were tested before. This time the minimal noise was also observed for both of the channels especially the output channel. It might be a point to note here that earlier in Chapter III while examining the Graphenea chip we had observed some striking characteristics in the f_{max} Bode plots. A particular large “kink” was observed for all the variants of transistors referenced, this was independent of any temperature or generation of external free carriers as such. In the following section the same observation was noticed for the Non-PEI GFETs made at RIT SMFL but a lot lesser in magnitude which will be analyzed and studied to understand the frequency characteristics.

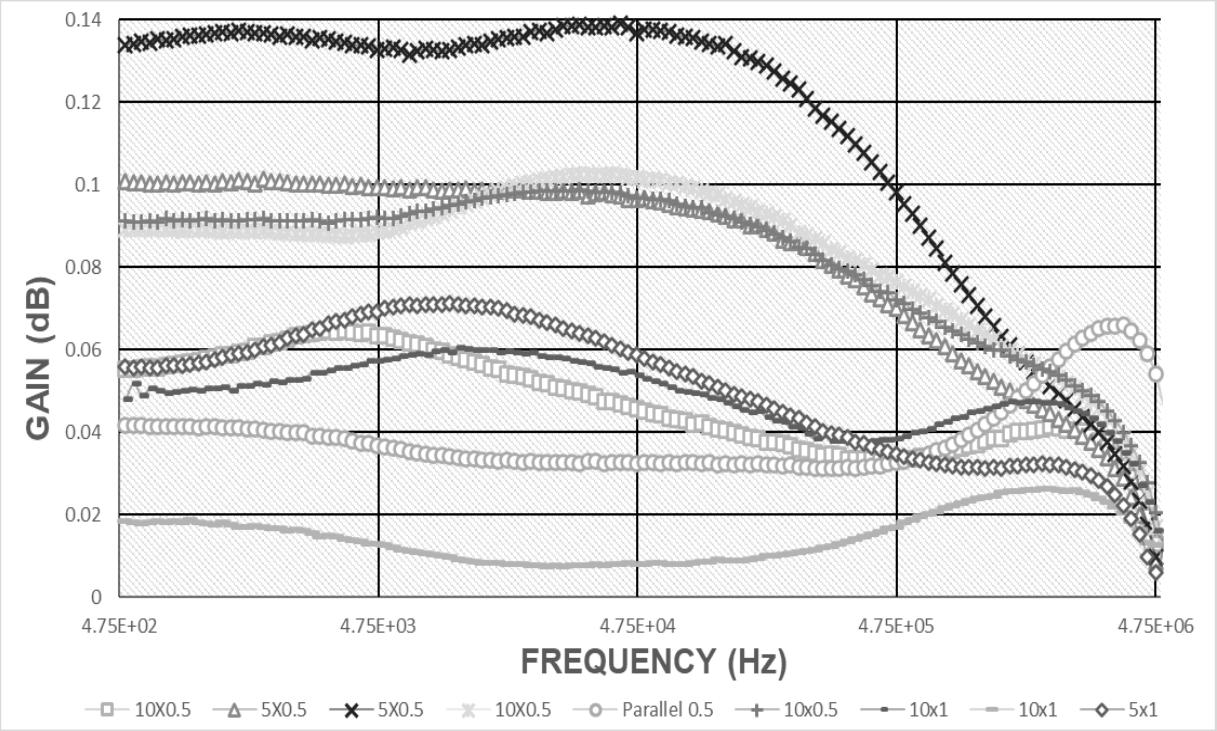


Fig. 42:- f_{max} response for 9 variants of the Non-PEI transistors measured with a minimal gain and a f_{max} value of 5 MHz.

It was seen that all the variants with different gain values had almost the same value of the f_{max} which was 5 MHz. Only the parallel and the 10x1 µm variant of the transistors exhibited a somewhat different characteristic as shown in Fig. 42. This was almost similar to what we had observed earlier for the Graphenea chips of a gain steadily rising and falling off. The only difference was that the ones tested earlier were of the back-gated variant and these ones are all the top-gated variants as mentioned above. All the transistors were tested with a 12 kΩ resistor and a positive voltage supply of 5V with the ground being kept at -1V. This gives a voltage drop of 6V across the resistor. The D.C offset was kept at a constant value for all of the variants, the amplitude being kept at 200 mV. The offset was kept negative to investigate the GFETS for their n-type behavior in terms of the RF response. The circuit of the amplifier was the same as before obeying the small signal model. It was quite evident that the minimal gain shown here was non-

conclusive enough hence the test was done with the same conditions for the PEI coated GFETS.

II. PEI

For the PEI variant we chose to observe and measure four variants of same dimension with variable DC offsets. Two transistors were kept at an offset of -4V and the rest of the two were kept at an offset of 0V and 2V, respectively. The amplitude for all the transistors was kept uniformly at 600 mV that is a three-time increment for the Non-PEI variant. The voltage drop across the resistor was the same as before.

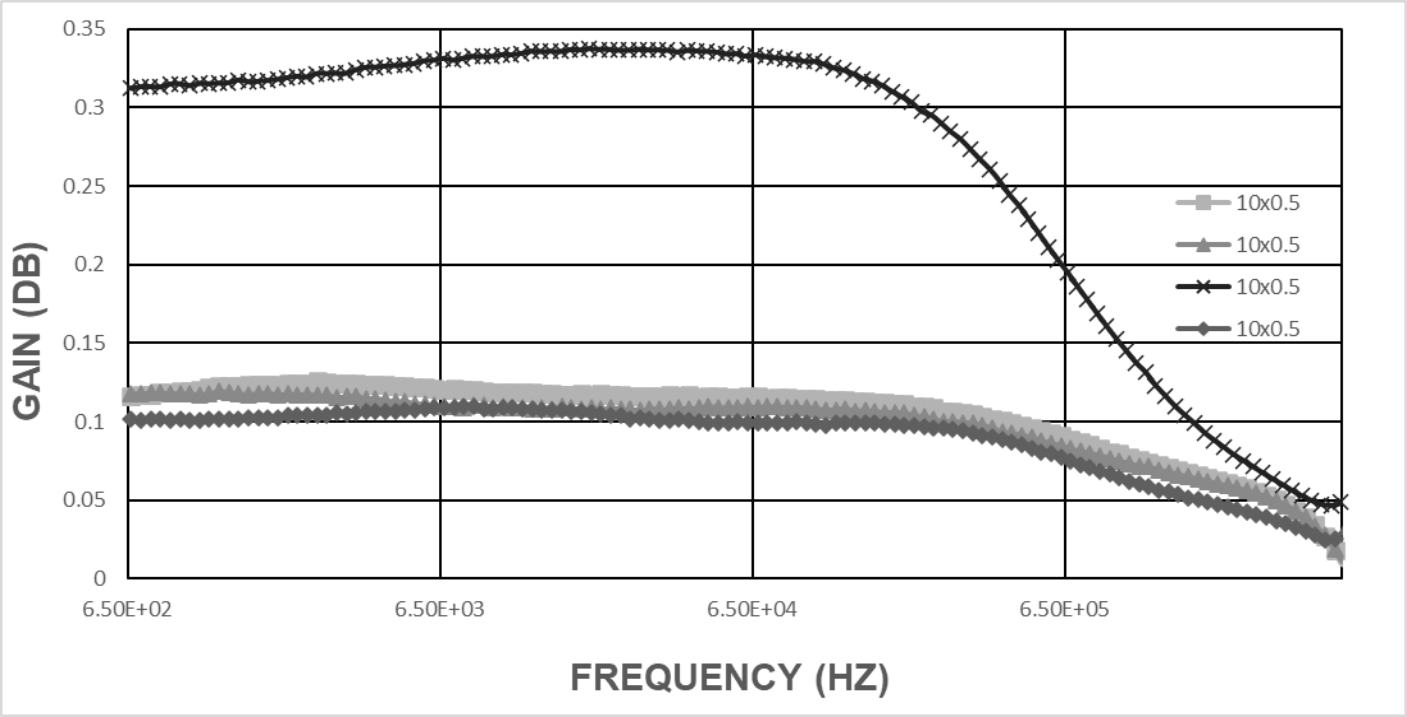


Fig. 43:- PEI coated GFETs showing more than double highest gain for a set variant of 10x0.5 µm variant.

Although the PEI variants had a similar value in terms of the f_{max}, they exhibited almost double value of maximum gain reached as is shown in Fig. 43. Although the electron donation from a lone pair in the PEI cannot be confirmed by seeing the plot in Fig. 43, it can definitely be inferred here that the improved transconductance and mobility have a role to play in the nature of

the gain vs frequency curves. This is because the curves for the PEI do not demonstrate any presence of a “kink” at the onset of the curve as was seen in the Non- PEI ones. As a matter of fact, it can be affirmatively stated here that the transistors do not undergo a frequent rise and fall in transconductance or have a variation in the mobility values along the length of the channel. The ID-VG curve analysis shown earlier can be taken as a background explanation in that regard. The balance of electrons and holes can be taken also as a reason for the perfect slope of the plots as shown above. However as seen there is an anomaly here which is for the plot shown in yellow in the Fig. 42. which is basically a “kink” appearing at the onset and can be attributed to minority carrier injection from the drain of the transistors [53]. The detailed discussion is given in the next section.

To understand both the Non-PEI and PEI variants better the normalization of the curves needed to be done which could then bring the gain for all the transistors be equal to ‘1’ and hence a better comparison between the two variants in terms of frequencies could be confirmed.

6.2 Normalization of the Transistor variants

I. Non-PEI

With the normalization being carried out we see that the gain curve shows a lot of variations as it reduces to 0 dB. This was seen as very much similar to the characterization being done for the commercial Graphenea chips in the initial experiments. In the works of Ramamoorthy, et al. and Meric, et al. [53,54] a typical “kink” formation was reported in the current voltage characteristics [53] and ID-VD curves [54]. The reasoning is given to be minority carrier injection which is electrons for the Non-PEI variant as was stated in the earlier section. Explaining this further we can say that as the gain is defined as the ratio of the drain voltage and the gate source voltage this

minority carrier injection can be explained as a case where there is a significant voltage drop in the channel. This occurs because there is a variation in the carrier concentration of the channel with the application of the drain source voltage V_{ds}. Hence, in the ID-VD characteristics we get to see that there is difference of voltage across the channel especially in the "kink" formed region. When $V_{ds} = V_{ds}$(kink) a particular voltage which is required for the "kink" to be formed, there is a certain pinch off region forming in the channel due to the absence of carrier density. This "pinch off" makes the current in the channel to be opposed to the applied V_{ds} and so the "kink" is formed [54]. With increasing drain bias (V_{ds}) this "kink" moves from source to the drain. The voltage across the majority carriers that is holes remains fixed while the drop across the minority carriers that is electrons increases with $V_{ds} > V_{ds}$(kink) and an electron channel forms at the drain [54]. If the value of the V_{ds} is very high these devices become weakly coupled to the gate and show characteristics similar to punch-through of the silicon MOSFETS.[54] Hence, this variation and reduction in the value of the V_{ds} is also seen for the gain in the Gain Vs Frequency curve in Fig. 44. The gain is subsequently diminished and ineffective for frequency determination. This variation can be said to happen due to the reduction in the channel length. As the channel length decreases, we can observe that the "kink" in the curves slowly starts to diminish irrespective of the length of the gap. As gain is defined as the product of the transconductance and the resistance applied the increasing value of transconductance is making the "kink" disappear slowly. The variations of two 10x1 µm and a single 5x1 µm transistor shows such characteristics as shown in Fig. 43. Although the "kink" for the 5x1 µm one still remains, the plateau of that flattens out much more compared to the others.

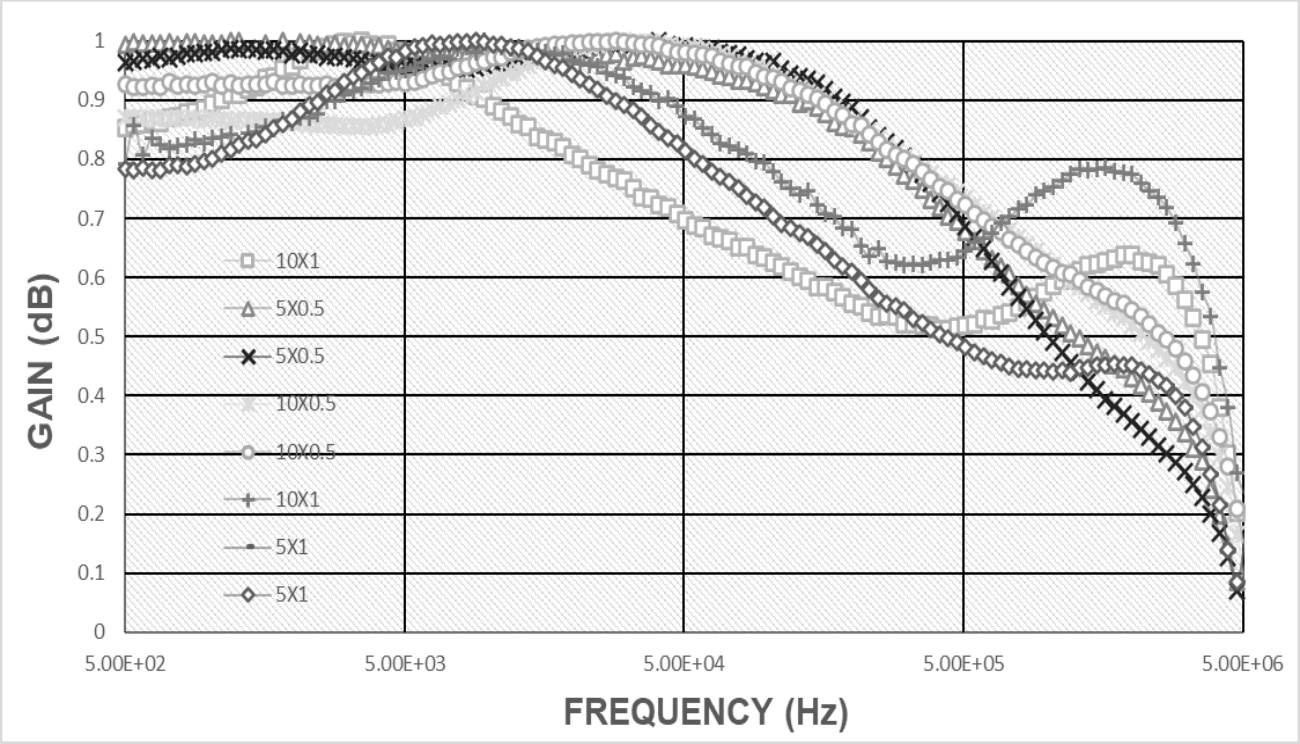


Fig. 44 :- 8 transistors of four separate dimensions each being measured for response of the f_{max}.

It might be interesting to discuss the other transistors under observation specifically the 5x0.5 µm variant and also the 10x0.5 µm do not show the formation of the "kink" compared to others so it can then be deduced that a perfect balance between the channel length and the gap is required to avoid the formation of the "kink" as we have noticed that comparison between a variant with a larger channel length and a gap length of 1 µm and a one with a lower channel length with the same gap length induces the "kink" as seen in Fig. 44. So reducing both the channel length and the gap length will reduce the plateau of the "kink" significantly which as mentioned earlier can be said is related to the mobility and the transconductance. To verify the occurrence of the "kink" formation we measured the PEI variants as well and normalized them to get a good idea of the f_{max} value.

II. PEI

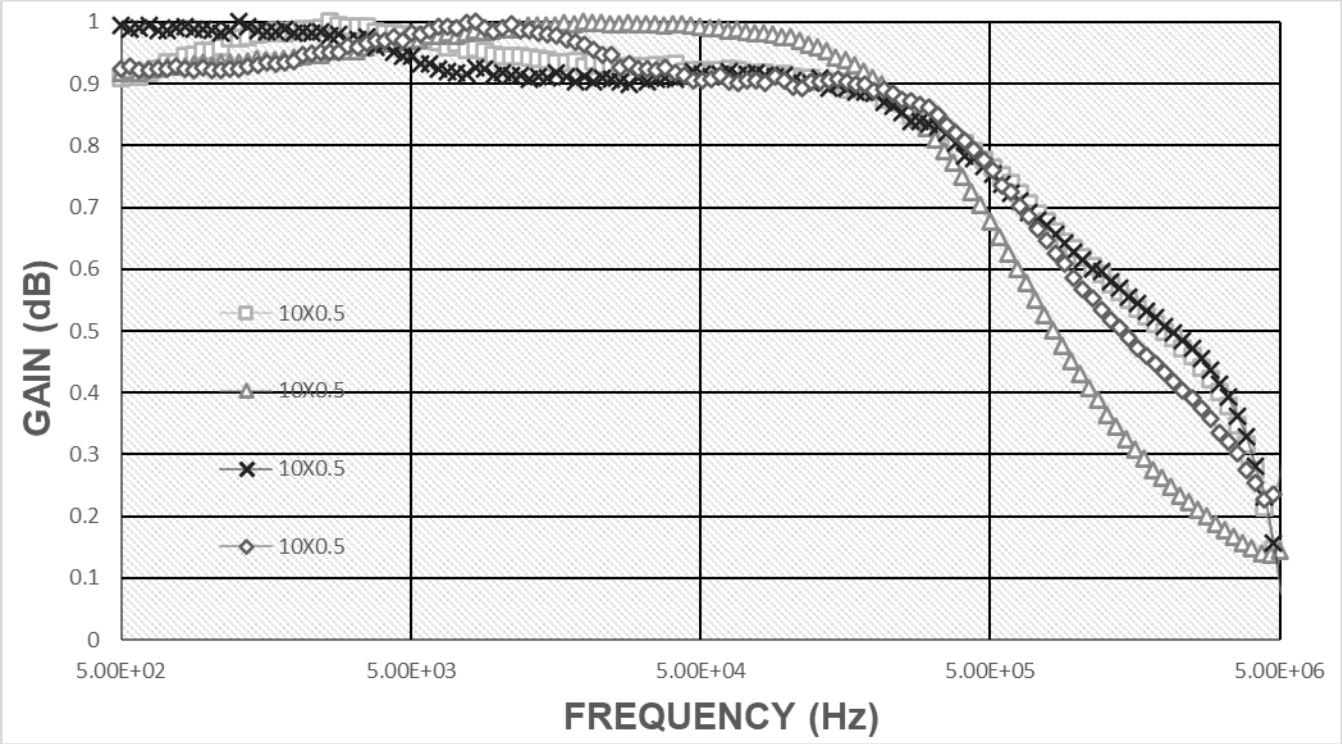


Fig. 45:- Four separate transistors of the same dimension done to estimate the value of f_{max}.

Realizing that the length of the gap is certainly a determining factor in the formation of a "kink" we tested four different transistors of the same dimension and as seen in Fig. 45 there is little to no formation of the "kink" and hence it can be estimated that the PEI samples and its balance of electrons and holes as was specified earlier can be held responsible for no formation of the structure and that there is little to no injection of minority carriers from the drain end due to the balance created. Conclusions can also be made in this regard that the length of the gap is indeed crucial for the determination of the value of the f_{max}. That is to say the difference between the channel length and the gap between the source and drain has to be determined very carefully on

order to have a good RF performance. But, this can be said about the PEI coated chips and not definitively said about the Non-PEI chips as the deficiency of electrons as shown in the ID-VG characteristics earlier has an important role which cannot be mitigated with the length of the channel or the length of the gap in question. It might be logical to question the bias point here but then again that can be traced back to the point of the mobility of the transistors such that the increase and decrease of the bias point has no effect on the gain curve. But conclusively again it might be noted that both the variants have a f_{max} value of 5 MHz which is striking, but if one attempts to observe and compare Figures. 43 and 44 a bit closely it might be observed that the point where the slope starts to fall off from the midband or usable frequency range is higher in the case of the PEI than that of the Non-PEI variant. A 50% drop in gain is noticed for almost all the variants under test.

Hence, RF performance of the transistors optimizable up to 5 MHz has been figuratively shown but a lot of research and experiments are further needed in the goal of getting a positive gain without normalization.

CHAPTER VII. Fabrication process flow of Top-gated & Back Gated Transistors at RIT SMFL

I.Top-gated Transistors

Step 1 :- Standard RCA Clean method was employed for cleaning the wafers which involved taking three p-type Si wafers and dipping them in a solution of water (4500 ml), ammonium hydroxide (300 ml), hydrogen peroxide (900 ml) at 75 °C for 10 minutes followed by DI rinse for 5 minutes, then water and hydrofluoric acid dip for 50 secs and 1 min respectively. DI water rinse was done for 5 minutes. For high particulate matter removal instead of ammonium hydroxide, hydrochloric acid of same quantity as ammonium hydroxide is used along with water and hydrogen peroxide of the same quantity at the same temperature and time. The reason for the second cleaning is because at the first one the organic particles are removed from the wafers but not the metallic particles. Hence, the second clean removes all the metallic particles to create a clean wafer surface, also providing an additional protective layer on the wafer which protects the wafer from further contamination.

Step 2 :- The alignment mark lithography follows the RCA Clean which mainly involves making the alignment marks on the wafer for the next etching step done on the wafer.

Step 3:- The alignment mark so made were etched by Trion Phantom III RIE and SF_6 by LAM 490 etching tool to make them prominent.

Step 4:- Repeat of RCA clean was done to remove remaining organic and metallic residues.

Step 5 :- In order to make the quality of the oxide to be very good dry oxidation was used to grow 90 nm of SiO_2 at 1000 °C on the bare Si wafer with the alignment marks after the etching.

Step 6 :- Lithography is done to do the gate lift off for the formation of the aluminum gate at the next step. This is done by exposing the active area.

Step 7:- Aluminum deposition is done by a CVC Thermal Evaporator over the wafer by evaporation method with 100nm in thickness.

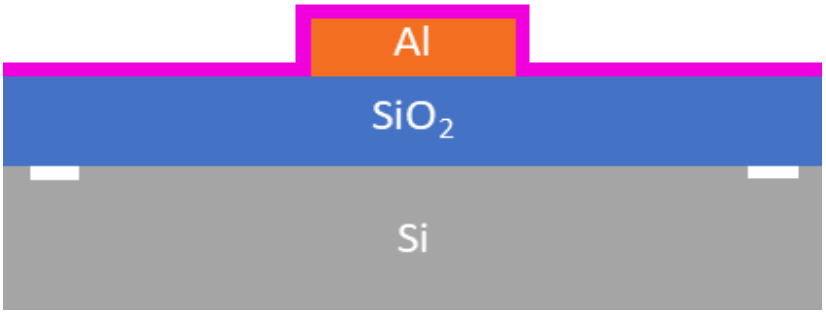


Fig. 46 :- A bare P-Type Si wafer (grey) with 90 nm of dry oxide growth of SiO_2 on it (blue), with the aluminum gate (orange), TEOS deposition is done on top of aluminum gate (pink).

Step 8 :- Deposited aluminum is then subjected to lift off by acetone. Patterning is done before this step as an intermediary one so as to not make the acetone lift off the entire aluminum and leave it over the gate.

Step 9 :- PECVD TEOS deposition of 45 nm in thickness is done over the wafer. The temperature maintained was 390°C and pressure was kept to a bare minimum.

Step 10 :- Lithography is repeated the second time in which the active area is opened up for the process in Trion Phantom III RIE with CF_4, CHF_3 and oxygen. This etches the TEOS and renders the wafer ready for the ALD process.

Step 11:- Atomic Layer Deposition (ALD) is done now by Ultratech S200 G2 Savannah tool to

deposit a thin film of layer 15 nm in thickness. The reason behind opting for ALD is because of the thin oxide layer grown, otherwise normal CVD method would have been chosen.

Step 12 :- The wafer is subjected to hydrogen plasma treatment at 20 sccm pressure and at room temperature for 90 seconds at a bare minimum pressure to passivate the dangling bonds which was not much effective at the end and we still had some bonds there.

Step 13 :- The most important step in the fabrication of the GFETS is the transfer of the Graphene onto the wafer by the assistance of Polymethyl Methacrylate (PMMA). This is done by spin coating the PMMA on the Graphene on a copper foil where copper foil serves as the host substrate. The entire Graphene, PMMA and the copper foil is now placed in an etchant which is water, ammonium hydroxide and hydrochloric acid in the ratio of 20:1:1 to remove the host substrate copper for several hours and acetone is used to wash the PMMA off. The Graphene is scooped out and transferred on top of the SiO_2/Si.

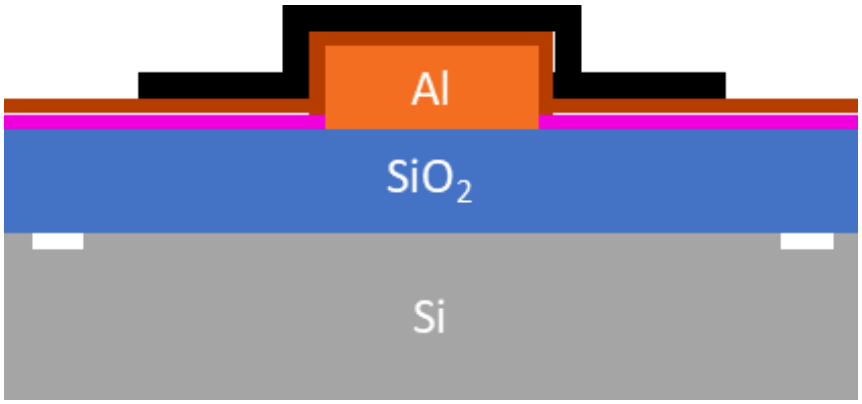


Fig. 47:- TEOS on top of aluminum gate has been etched and by ALD Al_2O_3 has been deposited (brown). Graphene (black) has been tranferred by PMMA on top of Al_2O_3 layer.

Step 14 :- Third level lithography follows the PMMA-assisted transfer process in which

patterning of the Graphene takes place. This is done by exposing the Graphene and further etching the Graphene over the active areas.

Step 15 :- The fourth level lithography is done by exposing and lift off of the TEOS over the source/drain regions.

Step 16 :- Source drain metal evaporation is done after the fourth level lithography which is first the nickel and then the gold is evaporated onto the wafer. The composition of the two metals being (10/100) nm followed by a lift off once more to develop the schematic as shown below.

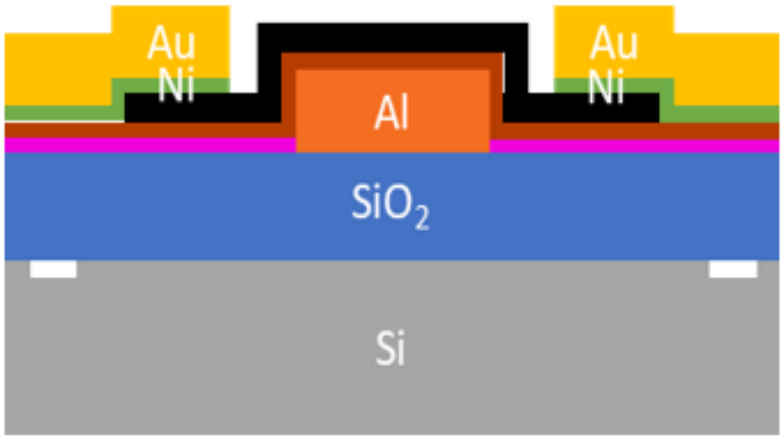


Fig. 48:- Source drain contacts (Ni/Au) (yellow/green) have been put on top of the source drain regions.

Step 17 :- The fifth level of lithography is followed by this to expose the contact vias as the source/drain regions are covered by the gate dielectric that is, Al_2O_3. This etches the gate dielectric from the source drain regions in a Plasmatherm ICP etcher and Trion Phantom III.

Step 18 :- The contact cuts are etched before wafer sawing with the Phantom III RIE at a pressure of 130 mTorr, 200W power, by gases of CF_4, CHF_3, O_2 at a flow rate of 60 sccm, 60

sccm and 8 sccm respectively.

Step 19 :- Wafer sawing is done using with a layer of photoresist on it which was coated after the etching step.

Step 20 :- The photoresist is stripped off the individual chips obtained after sawing.

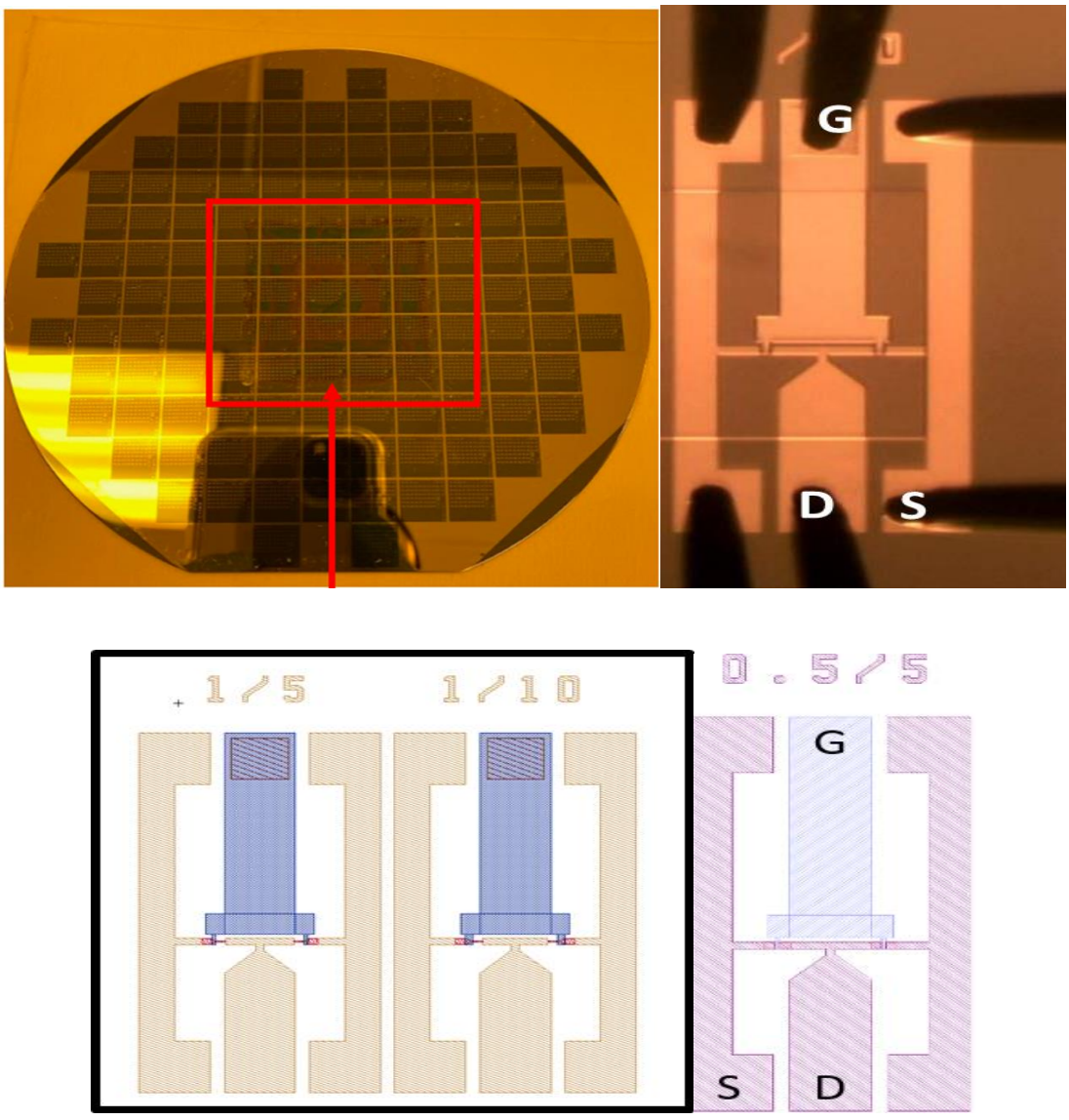


Fig. 49:- Complete fabricated wafer of RIT SMFL where the larger square box indicates the Graphene area which is

2 inches x 2 inches. This means that the Graphene concentration is the highest in that area (top left). A typical GFET fabricated at RIT SMFL with a dimension of 10 µm gate length and 1 µm spacing from source to drain. The striations source, gate and drain are because of the regions being covered by TEOS before lithography (top right). A pictoral image of top-gated GFETS with 5x1 µm dimension and another with 10x1 µm dimension (bottom left). Another variant with 5x0.5 µm in diameter with the source, drain and gate indicated for the transistor on the left and it follows the same for the one on the right. (bottom left).

It is a very interesting feature that all the top-gated variants are designed to have a funnel like channel for the variation in the input and output capacitance. An enlarged view of the channels is shown in Fig. 49 below.

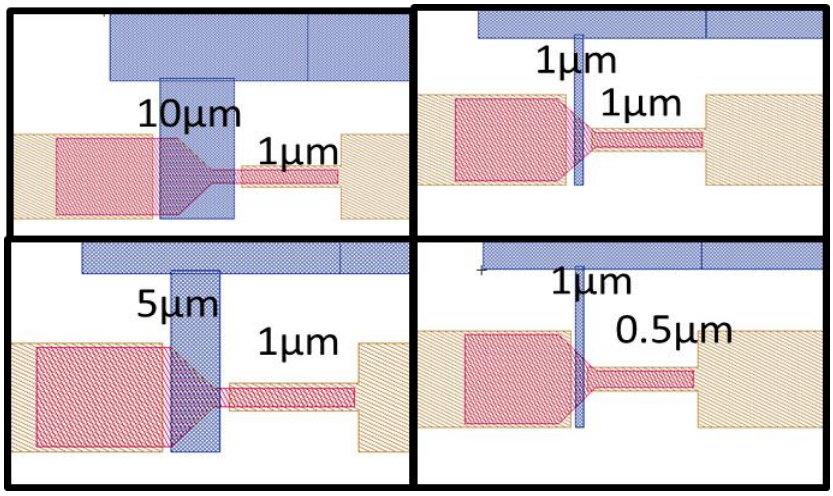


Fig. 50:- Channel schematic of all the variants of the transistors fabricated at RIT SMFL.

II. Back Gated Transistors

Step 1:- Standard RCA Clean procedure was followed on p-type Si wafers same as the case with the top-gated GFETS.

Step 2 :- First level lithography to make the alignment marks was done.

Step 3 :- The alignment mark was again made on bare Si wafer and were etched by Trion

Phantom III RIE and SF_6 by LAM 490 etching tool to make them more prominent as in the case for the top gated variant.

Step 4 :- Coating the wafer with photoresist and baking them on a hot plate, same as was done with the top-gated GFETS.

Step 5:- The coated photoresist was stripped by acetone.

Step 6 :- RCA clean was done once more to remove the residual resist from the wafer.

Step 7 :- Dry oxide growth of 90 nm was carried out on the Si wafer.

Step 8 :- Second level lithography was followed after the previous step this time exposing the active areas.

Step 9:- Reactive Ion Etch (RIE) was carried out by Trion Phantom III for 60 seconds to etch the oxide.

Step 10:- Coating and baking of photoresist was again done and the resist was stripped off by acetone as mentioned in the previous steps.

Step 11:- The most important step same as in the case of the top-gated GFETS here as well the Graphene was transferred onto the wafer by the PMMA transfer process mentioned earlier.

Step 12:- Transferred Graphene was then patterned along with the gate oxide over the channel region by means of second level of lithography.

Fig. 51:- Schematic of a top-gated GFET showing Graphene (black) layer being deposited under the S/D electrodes Ni/Au (yellow/orange). The SiO_2 layer is patterned by lithography.

Step 13:- Etching of the Graphene MESA is done after the patterning.

Step 14:- The wafer is again coated with a photoresist, only this time it is a negative lift-off resist (Future X NR9G 1500 PY) to assist in the source drain metal lift-off in the following steps.

Step 15:- The coated photoresist is now stripped by acetone once more.

Step 16:- Nickel and then Gold (Au) is evaporated onto the wafer to form the metals for the source and drain electrodes of 5 nm of Nickel and 95 nm for Gold (Au).

Step 17 :- Lift-off process in again done to create the source/drain electrodes and removing the rest of the metal from the other areas on the wafer.

It is to be noted that the source/drain metal contacts's composition is different than what was done for the top-gated variants. As these are the back-gated variants hence we used SiO_2 as the back gate and not Al_2O_3 as was the case for the top-gated ones. However, it was the case that a future lot with the same process flow was fabricated as well where the back gate was SiO_2 with aluminum as the gate metal of 200nm thickness was fabricated by metal gate evaporation in a

Bell Jar with the source/drain contacts being Titanium and Gold (Au) in the composition of (5/95) nm. Al_2O_3 was oxidized from the deposited aluminum and formed as a second back gate with the gate metal aluminum on top of it. This was the reason why ALD was not used for the deposition as the layer was thicker and had the purpose of being oxidized further. As mentioned earlier, TiO_2 due to its instability reasons cannot be used as a gate oxide as well as in the source/drain contacts as seen in that lot of wafers. The thickness of the SiO_2 was 300nm in that lot due to the purpose of having larger gate voltage sweep through the gate dielectric.

Fig. 52:- Schematic of a dual back gated fabricated at RIT SMFL with source/drain metal contacts (Au/Ti) (95/5)nm with 200 nm of aluminum and 300 nm of SiO_2.

CONCLUSIONS

In order to estimate the performance of the graphene transistors it was very much important to estimate the characteristic behaviors of the PMOS and the NMOS transistors as to see how the response of these were in terms of f_{max}. This was because a transistor with saturation needed to be estimated first (PMOS and NMOS) and then compared to estimate the characteristics of the GFETs without any saturation. This was all done due to the estimation of the bias point so very much crucial for the RF applications as has been highlighted by the author in the thesis. In order to have a good RF performance from a field effect device the ID-VG characteristics needed to be understood in detail by which the mobility, transconductance could be estimated. That has been done quite extensively with a multitude of chips and variants of transistors with different channel lengths in order to understand them better. The author has in this thesis underlined the effect of capacitance as the main hindrance for RF performance and also emphasize the effect of the quantum capacitance which can prove to be the impediment in RF measurements done for the GFETs made in the near future.

The application of the Poly Ethylene Imine (PEI) in the experiments and tests carried out in the work has been the most crucial characteristic which has altered the Dirac Point position and shifted it to the negative voltages which was not achievable by different methods of dielectric thickness change etc. The balance of the electrons and the holes hence done by this further enhances the

RF performance chances, although great results of the mobility increase has not yet been achieved but can be achieved in future with better preparation methods with the PEI such as spin coating, increasing the concentration of it by weight etc. The hysteresis behavior of the PEI

coated GFETS done with a variety of experiments has proved that with a thin dielectric and under a particular offset the voltage swing is quite remarkable. This most striking feature which the author has illuminated lays the foundation for a future theory that graphene as a 2D material if coated by a polymer can be used in a field effect transistor on a Si or a SIC based substrate for its usage in non volatile memory cells. In order to prove the theory with the PEI another set of experiments and analysis need to be carried out to make this assumption be solidified and hence proved.

In the matter for the RF performance mobility enhancemnent with the PEI is at the moment the best solution. Other than that effective channel length alterations, better quality of graphene and reduction of contact resistances by means of better transfer process of the graphene will be helping the research group achieve a high value in the cut off frequency (f_t) as well as the maximum oscillation frequency (f_{max}).

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