

Development of Automated Alignment Methodology on the Canon I-line Stepper

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Abstract -- Lithography is one of the most crucial processes that is used in modern integrated circuit (IC) fabrication. Level to level alignment and overlay measurements are key factors within lithographic processes. A stepper with an automated level to level alignment system can significantly improve wafer throughput and therefore increase profit for a company. There are many factors that can either enhance or hinder a tool's ability to align one level on top of another. For the past couple of years, RIT has had a Canon FPA 2000 i1 I-line stepper in their possession and the automated alignment system has never been utilized, until now. The data that proves this particular tool can and will align levels automatically is shown throughout. Some of the issues that arose throughout the study will also be discussed.

1. INTRODUCTION

One of the most critical areas of any integrated circuit (IC) production facility is microlithography. Within microlithography, there are two very important factors. These two factors are alignment and overlay measurement. Alignment is defined as "the process of determining the position, orientation, and distortion of the patterns already on the wafer and then placing them in the correct relation to the projected image"[1]. "Overlay" can be defined as "how accurately each successive patterned layer is matched to the previous layers" [1]. Both of these steps are usually carried out by optical means. As our technology improves to smaller and smaller critical dimensions (CDs) our tools will have to change and we may not be using optical exposure tools anymore. This implies that our alignment systems will also have to change with the new technology. Also, as our CDs have gotten smaller, so has overlay budget. Overlay was typically measured on an optical microscope. Now with our smaller overlay tolerances, the overlay will be measured on Scanning Electron Microscopes (SEMs). Current CDs are being measured in this way.

There are two main types of alignment that are currently being used. Both are types of alignment on optical exposure tools can be done using alignment

sensors. The first, "global" alignment, is probably more utilized throughout industry than the second, "field-by-field." This is because the global alignment procedure is much quicker than the "field-by-field" approach. Global alignment does not locate all the fields on the wafer. Also, the global alignment uses a "best overall fit" approach, which makes it less sensitive to noise. The "field-by-field" approach will collect data from one field at a time to align only that field. This makes the alignment sensitive to the optomechanical stability of the tool.

The alignment process itself can be broken down into two steps; course, alignment and fine alignment. During the coarse alignment process, the alignment mark must be within several hundred microns in order for the alignment sensor to "capture" the alignment target. The wafer will then be adjusted so that the alignment is within a few microns. This is enough to move the wafer into the range of the fine alignment system. The alignment sensor will then tell the tool to adjust the position of the wafer so that the alignment is less than a micron.

When overlay measurement is discussed, one must understand that we are measuring the difference in position, orientation, and distortion between two consecutive levels of an IC. There are two types of overlay that are typically measured. The first is "tool-to-itself" overlay. This implies that the two levels that are being measured were both exposed on the same tool. The other type of overlay that is measured is called "tool-to-tool" overlay, which is a comparison of two consecutive layers exposed on different tools. There are many structures that can be used to measure overlay. The two most common types are the "box-in-box" structures and the "diamond-in-diamond" structures.

At RIT the Canon I-line Fine Pattern Aligner system has the ability to align one layer on top of another layer. Since the tool has been turned over to RIT, neither the students nor the faculty have actually gotten the system to work properly. However, Advanced Vision Technologies (AVT) has shown that it is possible. The only issue is that confidence in the tool has never been established. This is one of the key issues that must be addressed. Also, it was shown that the overlay capabilities of the tool are less than 1 μm . This result also needs to be verified and reproduced.

One of the reasons that RIT has not been able to use the tool with the automatic alignment system running is because there are very few RIT reticles with the Canon alignment marks on them. This is another issue that must be addressed in order to get the RIT processes running smoothly on the tool.

There is a second issue that has caused some trouble with the alignment system. This is the lamp intensity. The current lamp is degraded to a point where the alignment system cannot work properly. All the key issues that hinder the ability to align properly must be addressed prior to the start of the investigation.

2. PROCEDURE

For the purpose of conducting this experiment, the following procedure was followed. The Canon stepper is only capable of processing 6 inch wafers, so these were obtained. To start, a thermal oxide was grown on the surface of the silicon substrate. This oxide was approximately 500 Å thick. This was done using recipe 250 on the Bruce Furnace. To check the uniformity across the wafer and also wafer-to-wafer uniformity, 3 wafers were measure at 5 different locations on the surface.

Using the coat recipe on the SSI 6 inch wafer track, the wafers were coated with approximately 1 µm of OiR 620 I-line resist. As part of this standard process, there is a dehydration bake and vapor prime of hexamethyldisilazane (HMDS) at 125° C and a pre bake at 90° C.

After the first coat of resist, the exposure is done. This is done using the first level alignment reticle from Advanced Vision Technologies (AVT). The energy used for the exposure was 150 mJ/cm². The focus setting was kept at 0 µm throughout the study.

After the exposure, the image must be developed. The development process is also a standard procedure on the SSI wafer track. It consists of a post bake at 110° C. After the MF CD-26 developer is dispersed and the wafer is then rinsed with deionized water, the wafer moves into another oven for the hard bake at 120° C.

Now the image must be transferred from the resist to the oxide. This is done using the FACOXIDE recipe on the Drytek Quad in the RIT Fab. This recipe utilizes standard SF₆ and CHF₃ chemistry. The SF₆ flows into the chamber at a rate of 20 sccm. The CHF₃ flows into the chamber at a rate of 40 sccm. The power used during the etch process is 250 W. The pressure was set to 270 mTorr. The total etch time per wafer was approximately 2 minutes and 15 seconds. The etch rate using this recipe is approximately 250 Å per minute. Therefore this time allowed for a slight over etch.

Now that there is a permanent first level image etched into the SiO₂, the second level process can begin. To start the second level process, the OiR 620 resist must

be coated onto the surface of the wafer. This is done using the same coat recipe used before on the SSI wafer track.

With the second coating of resist spread onto the wafer, the second level exposure can begin. This was done using the second level reticle from AVT. This second level exposure utilizes the automated alignment system on the Canon. Once again the exposure energy that was used was 150 mJ/cm².

Now that the resist has been exposed for the second time, it must be developed again. Once again this was done using the develop line on the SSI wafer track. Now that the image can be seen in the resist, the level-to-level overlay can be measured. This was done on an optical microscope using the 1 µm verniers. The overlay was then tabulated.

3. RESULTS

The tabulated data was taken from a sample of 9 wafers. A total of 84 measurement points in X and in Y were taken from the 9 wafers. From the first 3 wafers a total of 60 data points were collected. This shows that there were a total of 20 measurements per wafer. This was done to achieve an idea of the uniformity across the wafer. The next 24 measurements came from the remaining 6 wafers. These measurements consisted of 4 sites per wafer, which were taken at the corner die. The corner die correspond to sites 1, 5, 16, and 20 depicted in the wafer map shown below (figure 1). This is the minimum needed to see any wafer rotation. The averages of the data collected are displayed in table 1 shown below.

	X (µm)	Y (µm)
AVG	1.79	0
STD	0.42	0

Table 1: Average of X and Y overlay data

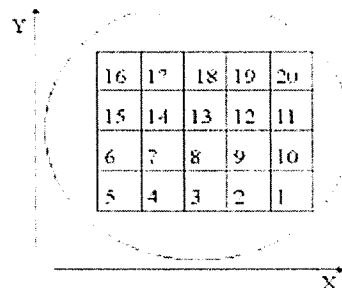


Fig 1: wafer map

4. DISCUSSION

The data shown earlier provides evidence of the usefulness of the automated alignment system. When all the pieces to the puzzle fit, the tool is capable of aligning one level on top of another. The data illustrates some kind of offset in the X direction of about +1.8 μm . There seems to be no offset in the Y direction. The X offset could possibly be corrected by "writing" an X offset by -1.8 μm .

There are some other issues that must be taken care of. First, Canon alignment marks must be etched into the reticle. If this is not done prior to processing, there is no chance of alignment. The alignment system will have nothing to align to.

Next, the stepper job must be written so that the stepper is told to align the reticle to the wafer. The stepper job must also have the pattern recognition tolerances set to a reasonable level. If the tolerances are set too high, the tool will not recognize the pattern if there is any small change in the pattern. This will take care of any distortion of the pattern by the etch process. If the tolerances are set too low, any pattern on the wafer may look like the Canon alignment mark. That is why it is crucial to set this tolerance at a reasonable level.

Finally, another tool parameter that must be paid attention to is the lamp intensity. The lamp can play a major role in the ability of the tool to align both the reticle to the column and also the reticle to the wafer. Once the intensity degrades to low, the tool will have trouble aligning the reticle to the column. The reticle will then have to be aligned manually. However, a person will never align the reticle as well as the tool can. This is a major contributor to the overlay error that can be seen. Also, the intensity of the lamp can hinder the ability of the tool to recognize the alignment mark that is needed to align the reticle to the wafer. If this is the case, the tool must be "helped" along using some manual commands. This is actually a semi-automatic alignment process. But it does prove that the tool can utilize this automated alignment system.

5. CONCLUSIONS

It has been proven that the Canon FPA 2000 i1 can utilize the automated alignment system that is built into it. In order to use this feature, all the pieces must come together. The lamp intensity must be adequate, the etched image must have minimal distortion and the stepper job and reticle must be set up right.

From the data that was collected, it can be seen that the overlay error is repeatable. In the X direction, most of the measurements that were taken showed an overlay of + 2 μm . All the measurements in the Y direction were 0 μm . This says that the tool is capable of less than 1 μm overlay error. In order to get the actual overlay capabilities of the tool, RIT needs a new overlay measurement system. With a box-in-box structure, the

overlay can be measured right on the Canon. It is possible to see less than 1 μm overlay with a new vernier system as well. AVT has already created an overlay measurement system that can determine overlay error of less than 1 μm . It is necessary for RIT to do this as well. As the RIT products become more advanced, the overlay tolerances will be more strict, just as it has for industry.

6. REFERENCES

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7. ACKNOWLEDGEMENTS

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