Copper Interconnect Development At RIT

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Abstract—Aluminum is the current metal of choice for metallization in the IC industry. However, serious electromigration problems, and inferior thermal stability limit its performance and reliability. Copper is an attractive alternative having higher electrical conductivity and improved electromigration performance compared to Aluminum. However, Cu is a fast diffuser in Si, SiO2, and interlevel dielectrics (ILD). To eliminate this issue, a layer of diffusion barrier (DB) material which is conducting, chemically passive with Copper, has good adhesion properties with Cu and ILD and has high thermal stability is required.

Damascene process for Cu was utilized to pattern the wafers in this study. Ta, TaN, Ti and TiN were used as barrier layers. The DB were deposited using pulsed DC sputtering (Ta and Ti) and reactive sputtering (TaN and TiN). A seed layer of Cu was deposited in the same sputtering tool. The wafers were electroplated with Cu and polished using CMP. They were then analyzed using SEM and a high-resolution optical microscope. No electrical tests were conducted at this stage due to lack of multilevel masks.

INTRODUCTION

With the advancement in microelectronics field, properties of thin films and their processing, especially in the field of metal interconnects have gained more interest and demand within the past few years. A high performance interconnect is urgently needed to quench the demands dictated by Moore's Law.

Cu has an intrinsically higher electrical conductivity compared to Aluminum. As a result there will be a gain in virtually all the chips that will utilize Cu interconnect. This alone is a big motivation for transferring to Cu interconnect technology.

A. Issues in Metallization

1. RC Delay [1]

The carrier transient time across the length of the channel decreases with the device dimension reduction. These carrier charges capacitatively couple with the ILD, leading to RC delay. For a MOS circuit, the RC delay is defined in terms of the circuit response, which is given by:

$$V_{out} = 1 - e^{-\frac{t}{RC}}$$

where, V_{out} is input voltage of the circuit, t is the time, R is the total resistance of circuit, C is the total capacitance of the circuit. RC time constant can be determined by the following equation:

$$RC = \rho L^{2\varepsilon}{}_{ILD} / t_M / t_{ILD}$$

where, ρ, t_M, L, ε_{ILD}, and t_{ILD}, respectively are – the resistivity, thickness, length of interconnection, and interlevel dielectric permittivity and thickness.

With the increase in chip speeds, RC time delay becomes a bigger issue than ever before.

2. Electromigration [1]

Electromigration occurs when a conductor is subjected to high current densities at opening conditions where atomic diffusion is high, leading to a mass transport association with atomic flux divergence. The enhance and directional mobility of atoms are caused by (a) the direction influence of the electric field on the ionized atoms and (b) the collision of electrons with atoms, leading to a momentum transfer and atom movement. The atomic flux due to electromigration in the single crystal or large-grained crystal, where the grain-boundary contribution to atomic diffusion can be neglected, is given by as:

$$J_{atoms} = NDZ * qj / (\rho kT)$$

Where N, D, Z*, q, j, ρ, k, and T are atomic density, atomic diffusivity, effective charge on the moving ions, electron charge, current density, electrical conductivity, Boltzmann's constant, and temperature in degree Kelvin respectively. Electromigration can lead to break in interconnections and functional failure of the integrated circuits at large.

B. Copper Metallization

Aluminum has been the most commonly used material for metallization. It has a relatively low electrical resistivity, it has halide compounds with a relatively high pressure which are suitable for reactive ion etching (RIE), It can for am protective oxide film that can withstand various thermal processes and has good adhesion to oxide.

With the reduction in feature sizes, planarization of Al occurs via high temperature process. This places a stringent demand on the integrity of the barrier to prevent junction spiking caused by Al/Si interdiffusion. For metallization of VLSI circuits, Al has a major drawback – electromigration. For ultra-large scale integration (ULSI), the electrical resistivities of Al and its alloys are not low enough. As the circuit geometry shrinks, Al and its alloys will need to be replaced by other interconnect materials.

Copper offers low resistivity (1.7 μΩcm) compared to Aluminum (2.7 μΩcm). Cu also offers ease of deposition, and a higher melting point than Al. Cu also has electromigration orders of magnitude lower than Aluminum.

Even though Copper offers many advantages, it is has its own sets of issues.

Cu diffuses rapidly in Si and acts as an electron trap. Three acceptor levels in the middle of the Si band gap at 0.24 eV, 0.37 eV and 0.52 eV with respect to valence edge are formed. These levels provide a mechanism for excess minority carrier recombination with excess majority carriers. This in turn induces a generation-recombination leakage current in p-n junctions and degrades the performance of the transistors leading to a reduction in the current gain.

Copper forms the silicide Cu_3Si by reacting with the substrate at temperature less than 200 °C. After the formation of the Cu_3Si phase, the underlying Silicon in that Cu_3Si/Si structure is readily oxidized even at room temperature, resulting in rapid growth of a layer of SiO2.

Unlike Aluminum, Copper is readily oxidized to form Cu_2O and CuO phase at low temperature and no self-protective oxide layer is formed to prevent Cu from further oxidation. CuO and Cu_2O degrade the electrical and mechanical properties of Copper. The lack of self-passivation layer makes Copper thin film susceptible to oxidation during processing.

Copper layer exhibit poor adhesion on both oxide and polymer substrate. In general, interfacial adhesion is strongly related to the bonding, surface morphology and stress relaxation at the Cu/substrate interface.

The aforementioned Copper issues can be reduced or completely eradicated with the use of diffusion barriers, passivation layers and adhesion promoters.

In this study the effort to understand diffusion barriers and their adhesion properties were the key focus of attention at RIT. CMP and step coverage were the other aspects that were looked at as well.

EXPERIMENTAL

The procedure had 5 primary steps, namely:

i. Oxide Growth
ii. Pattern Formation and Oxide Trenching
iii. Barrier/Seed Layer Deposition
iv. Electroplating of Copper
v. Chemical Mechanical Planarization (CMP) of Cu

Oxide Growth

Four-inch p-type bare Si wafers were used to grow the initial oxide. At RIT a horizontal Bruce Furnace is utilized to grow thick wet oxide.

Following furnace conditions were used to grow a ~10,000 Å of SiO_2.

Move	Time	Temperature
Boat in	00.0 min	25 °C
Push In	12.0 min	800 °C
Stabilize	15.0 min	800 °C
Ramp to 1100 °C	30.0 min	1100 °C
O_2 Flood	05.0 min	1100 °C
Soak	3-hr 30.0 min	1100 °C
N_2 Purge	05.0 min	1100 °C
Ramp Down	55.0 min	25 °C
Pull Out	15.0 min	25 °C

Pattern Formation and Oxide Trenching

MIT Cu-damascene test mask was used for this purpose. This mask includes lines and spaces and boxes ranging from 1μm – 30 μm in size.

A GCA stepper was utilized to transfer the pattern from the mask onto the wafer. Standard RIT photo-steps were used to coat, expose and develop the photoresist.

The wafers were then subjected to a HF dip for 5 minutes. This process trenched the oxide in the areas where the substrate was exposed after the photoresist development.

The wafers were then placed in an O_2 plasma Asher to remove the unexposed photoresist remaining on the wafers.

Barrier/Seed Layer Deposition

A CVC601 sputter tool was used for deposition purposes in this study. This tool has the ability to handle 4 different substrates up to 8" in size. Depending upon the target placement and utilization within the tool, it was at

times possible to sputter Cu-seed layer just after the barrier layer deposition.

The various parameters for different barrier layers are given below in Table 1.

	Ta	TaN	Ti	TiN	Cu
Target	8"	8"	4"	4"	4"
Power (W)	1000	1000	650	650	400
Time (min)	25	25	20	20	18
Gas	Ar	Ar,N_2	Ar	Ar,N_2	Ar
Gas Ratio	1	5.5:1	1	5.5:1	1
Pressure (Mt)	5	5.5	5	6	5
~Thickness-Å	1150	1200	1250	1100	1100

Table 1

The gas flow into the chamber was 200 sccm. The best vacuum achieved was 4.2 x 10^{-5} mTorr. Various gas ratios were looked at before coming up with the final Ar:N_2 ratio for the TaN and TiN deposition.

Electroplating of Copper

A ReynoldsTech non-rotational plating cell was used for this purpose. The wafers were sent to ReynoldsTech to be plated since an identical tool at RIT, is currently in the process of being installed.

Figure 1. shows a diagrammatic layout of the specified tool.

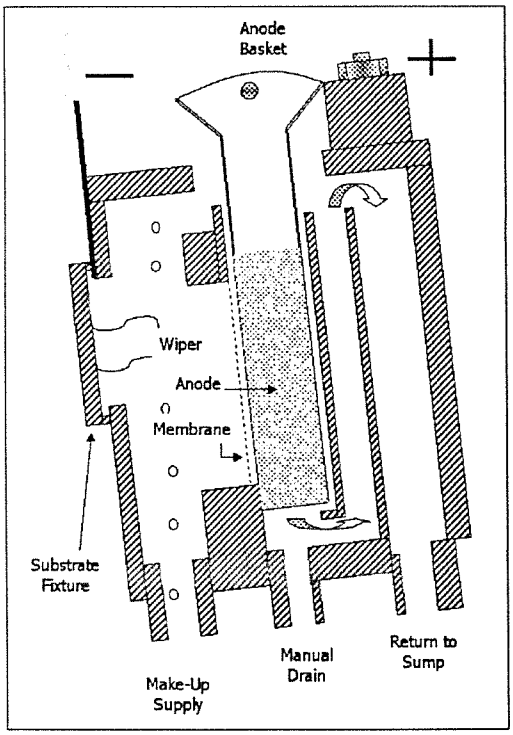

Figure 1

The electroplating parameters that were used during electroplating were:

- Plating Temperature 26.0 °C
- Copper Sulfate conc. 10oz/gal
- Sulfuric acid conc. 25 oz/gal
- Chloride 0 oz/gal

	Current	Voltage	Time
Stage 1	0.2 A	2.5 V	5 min
Stage 2	1.0 A	7.5 V	15 min

Table 2

A ~2 μm thick Copper layer was deposited on top of the seed layer.

Chemical Mechanical Planarization(CMP) of Cu

CMP was done using a Strasbaugh single wafer tool. A Rodel IC 1000/Suba V pad was used to polish the wafers.

The condition were as follows:

Table rpm	48
Carrier rpm	46
Pressure	5 psi
Time	8 min

Alumina based slurry (pH 1.5) was used for this purpose. The composition of the slurry was as follows:

- DI water
- BTA
- H_2O_2
- HNO_3

RESULTS/ANALYSIS

Only adhesion and deposition related parameters were studied in this phase of this work. Due to the lack of instrumentation and dual level masks, a complete electrical and multi-level property investigation of the process could not be conducted. Using a scanning electron microscope (SEM) and a high-resolution optical microscope, the samples were analyzed. Majority of the SEM analysis was done at University of Rochester – Optics Lab. Following were the various substrate images obtained for this study.

The TaN wafer broke prior to the CMP. This resulted in excluding it from post CMP analysis.

On visual inspection the Ta, TaN and Ti wafers show a good film of electroplated Cu. When the wafers were cleaved for X-sectional analysis, the TiN wafer showed extremely high level of peeling.

Most of the analysis was conducted on the Ta barrier layer wafers. This was due to two reasons – firstly, TaN wafer polished properly and secondly, time constraint. If

there was more time available then other wafers would have been analyzed.

In Figure 2 (page 5) 30μm features/20μm spaces (Cu) are seen. The features are oxide islands and the channels are Cu filled. There appears to be slight dishing within the channels and can be seen by looking at the changing gradient of the color. This will later on be confirmed using a profilometer. A similar pattern with wider spacing between the islands can be seen in Figures 3 & 4 (20μm feature/30μm spacing).

The reverse situation where the islands (boxes) are Cu and the spacing between them are oxide, can be seen in Figure 5 (page 5). There appears to be minimal dishing. This could be attributed to smaller size for the feature.

Figure 6 shows 10μm lines and spaces. They appear to be very well defined and filled on optical observation. The next image, Figure 7, shows even thinner lines (5μm) and they too appear to be in excellent condition. Even further level of gap filling and feature resolution was observable. In Figure 8, 9μm lines and 1μm spaces were resolved, filled and polished.

A case of underpolish can be seen in Figure 9 that was observed after CMP in and around the center of the wafer.

Figure 10 (page 6) shows the X-sectional SEM image of this Ta barrier layer wafer. As can be observed from this image, there appears to be no peel of any sorts and a good adhesion between the substrate and Cu. T (1) relates well with the visual inspection upon cleavi wafer, where TiN wafer had Cu peel off and Ta, TaN did not show any kind of Copper peeling.

Figure 11 (page 6) shows the flip side of the above situation. This was a TiN wafer. The Cu appears to have been lifted completely off. There seems to be no adhesion between the substrate and Copper.

The electrical properties were not looked at in this study.

CONCLUSION

This study was conducted to look at the feasibility of understanding and maybe in the future developing of Copper interconnect layer at RIT. The results obtained showed Ta and TaN as a promising barrier and adhesion promoter layer. The deposition was perfect after a few runs. There appears to be no peeling in the case of Ta. Ti also showed a good adhesion and polishing properties. TiN proved to be the worst and showed no adhesion to Cu. The feasibility of seed layer deposition at RIT was proved and showed promise since it acted as an excellent growth layer for Cu during electroplating which resulted in the filling of all the lines and features on the wafer.

Without the electrical tests it is extremely hard to determine if the various aspects of the process fit well together or not. This can understood only after a better understanding of the electrical properties of the different layers and levels.

FUTURE WORK

The need to further develop and understand the Copper interconnect process at RIT will require the following:

- Better analysis (SEM's)
- Electrical testing
- Optimization of deposition parameters (barrier and seed layer)
- Tool startup (Electroplating, CMP)
- Multilevel mask for damascene process
- Investigation of low-k dielectrics
- More information and support from the industry

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REFERENCES

[1] Shyam P. Murarka, Material Science and Engineering, R19, No. 3-4, May 1997.
[2] J. Guttmann, Thin Solidm Films, p 236, 1993.
[3] www.chip.ibm.com/news/ IBM Homepage 2000.
[4] R. Powell, A. Harrus, R. Hill, Raising the IC speed limit by the use of Cu interconnects procd. 1999.
[5] S. Wolf and R.N. Tauber, "Silicon Processing for VLSI Era, Vol. 1-Proicess Technology", Lattice Press, CA, p. 242-246, 1986.
[6] X.W. Lin, Dipu Pramanik, Solid State Technology, p 63 October 1998.
[7] www.electrochem.org Journal of Electrochemical Society Homepage 2000.
[8] W. Quin, Diffusion Barriers, PSU, 1998.

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Ashish Kushwaha, originally from Kanpur, India, received B.S in Microelectronic Engineering from Rochester Institute of Technology in 2000. He attained co-op work experience at Xerox Corp., National Semiconductor and Fairchild Semiconductor.

He is joining National Semiconductor Corporation as a CMP Process engineer starting June 2000.

Image Appendix

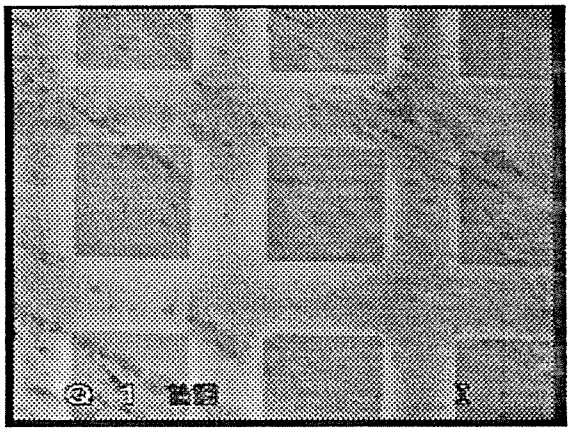

Figure 2

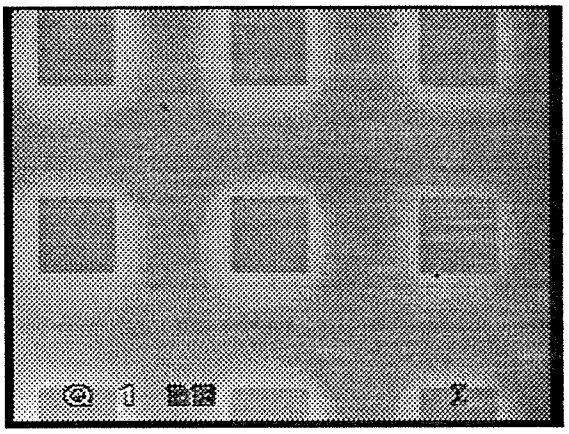

Figure 3

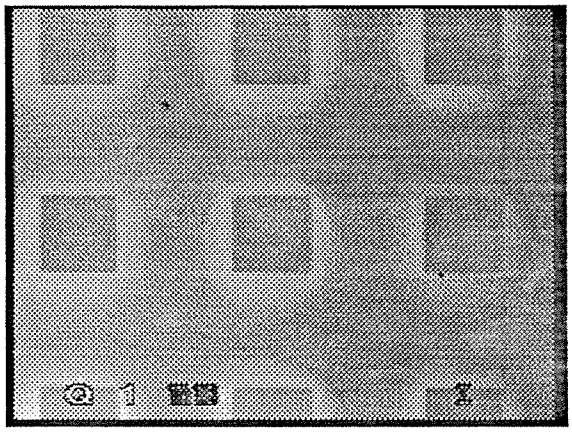

Figure 4

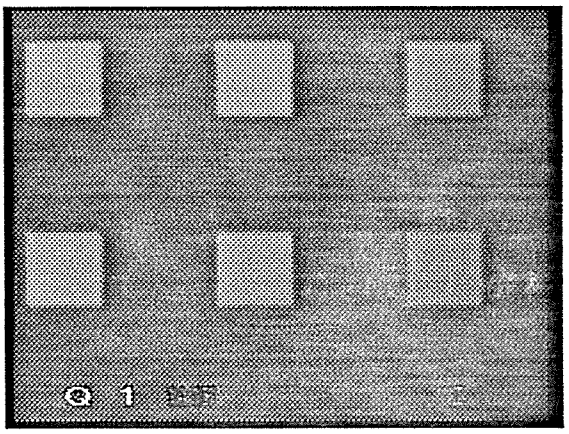

Figure 5

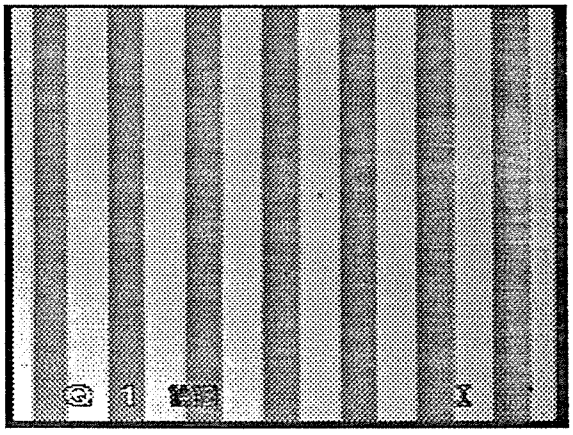

Figure 6

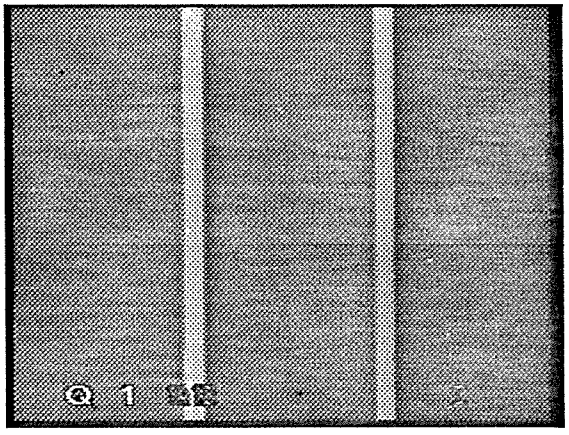

Figure 7

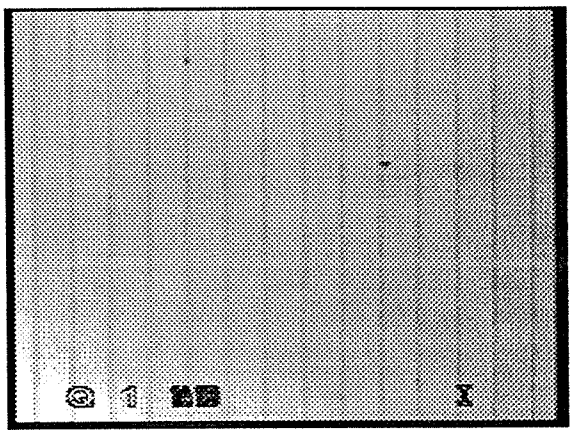

Figure 8

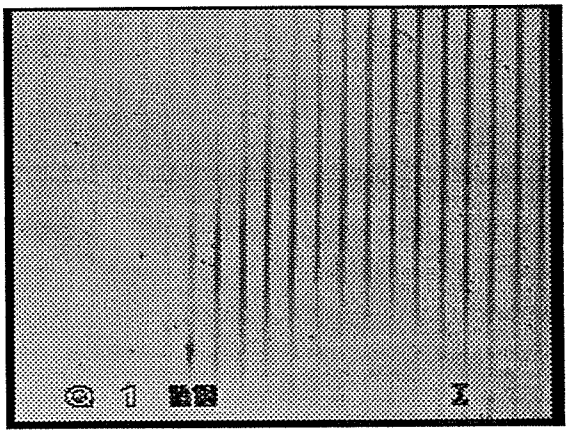

Figure 9

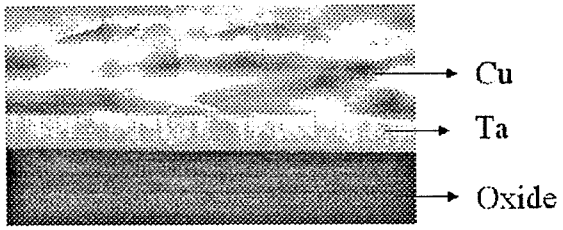

Figure 10

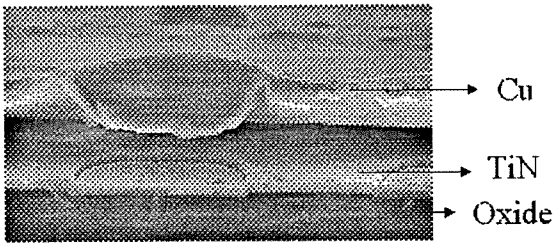

Figure 11