Investigation of Silicon Etching Effects for Monolithic Integration of MEMS with CMOS

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Abstract– Monolithic integration of CMOS and MEMS is quickly proving to be a viable asset to current complex structures. However, synthesis of these technologies has proven to have multiple processing obstacles. Depending on the method used to create these devices, the hurdles include the effects of silicon etching and high temperature processing. For this experiment, previously processed CMOS wafers were obtained and a trench was etched into the silicon. "Family of curves" plots of the working CMOS wafers were taken before and after processing to study any changes in I_D. Results have shown that the processing of this integration will effect the family of curve plots, however this was not concluded as a result of a small sample size.

1. INTRODUCTION

Complementary Metal Oxide Semiconductors (CMOS) transistors are playing a dominant role in today's society ranging from basic to complex structures. With the processing ideas behind CMOS transistors, a new idea about shrinking macro-mechanical devices was created, known as MicroElectroMechanical Systems (MEMS), including such devices as electro-motors, actuators, shutters, and more. As the demand for complex semiconductor devices increases, there is a need to integrate MEMS with driving, controlling, and signal processing CMOS electronics.

This integration promises to improve the performance of micromechanical devices as well as the cost of manufacturing, packaging and instrumenting these devices by combining the micromechanical devices with an electronic sub-system in the same manufacturing and packaging process.[1] Performance of devices will be better by reducing impedance's when testing MEMS sensor structures by having the system analysis in close proximity. Today's systems have the MEMS device in their own package and subsequently are running wires to machines, such as Rochester Institute of Technology's *HP4145 Analyzer* used in the Microelectronic Engineering department. For example, in the case of transducers which convert mechanical forces to capacitance energy, it is important to keep the distance from the transducer to the analyzing electronics as small as possible. This reduces stray capacitances and noise due to considerably deteriorating circuit performance.

In order to integrate these technologies, three different methods have been developed including CMOS first, MEMS first, and interleaving. The CMOS first method was developed by Berkeley researchers, and is used extensively with *Texas Instruments* for manufacturing of their Digital micro-Mirror Devices (DMD). With this method, the aluminum metallization of CMOS is replaced with tungsten so that the circuitry can withstand the following MEMS processing. However this method has some processing challenges when processing the MEMS. One such problem is it requires high temperature processing to dope and relieve mechanical stress in the polysilicon layers. The MEMS first approach, developed by *Sandia National Laboratories*, is a flexible, modular manufacturing process for the monolithic integration. Using this method, a trench is first etched into the silicon to a certain depth. Micromechanical structures are placed into the trench and thereafter filled with a sacrificial layer of low-temperature oxide (LTO). The LTO is then planarized so that the electronics are placed onto the wafer without the worry of destroying the MEMS structures, or thin photoresist stresses from the rough topography. The interleaving method, used by *Analog Devices* for their accelerometers, allows for processing of both the CMOS and MEMS throughout the entire course of manufacturing. The only major drawback to this is the rough topography from the micromechanical devices, which can ultimately cause larger critical dimensions for the circuitry.

This experiment will combine ideas from the MEMS first method with the CMOS first method. Working CMOS wafers will be used and a trench will be wet etched into the silicon wafer after a protective layer of silicon nitride is deposited onto the surface. Wet etch solution of potassium hydroxide (KOH) was used for a couple of reasons. First is that KOH etching is a well-established technology dating back to the early 1960's. Secondly, it is orientation dependent; and for this case, the etch will be anisotropic. Thirdly, the non-etched regions can easily be protected by Si_3N_4, which is also a well-established technology at Rochester Institute of Technology.

This type of work offers numerous advantages to RIT's microelectronic program. One such advantage will allow for student designed micromachines to be electrically

tested, which historically has proven to be problematic due to poor electrical connections. Furthermore, the availability of PMOS, CMOS, and bipolar processes at RIT would allow the MEMS designer a great deal of flexibility because a technology could be selected that easily presents appropriate impedance's to the micromachined devices.[2]

2. PROCESS FLOW

The first part of this experiment was to acquire and test completed CMOS wafers. To do this, a box of 15 finished RIT CMOS Gate Array wafers were found and electrically tested. This first test was used to determine which wafers still work. This information will also be used to compare and contrast the wafers when processing in completed. Figure 1. is a wafer map that refers to the die location of the tested transistors.

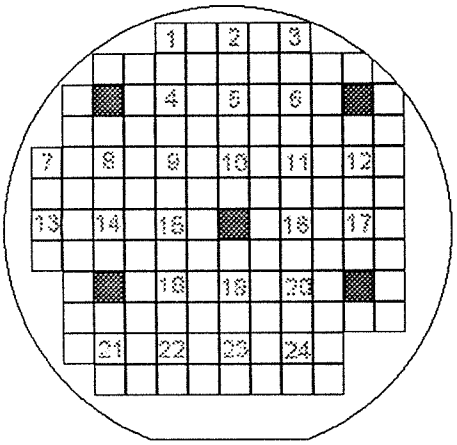


Figure 1. Wafer map showing the locations of the electrical testing (numbered die). The colored blank areas refer to regions of thickness measurements. The rest are gate array dies.

The next step in the process is to perform an aluminum etch on the entire substrate. It is desired to have all the aluminum removed as a result of future high temperature processing. After this, a quick RCA clean is to be accomplished before a silicon nitride deposition. However, this RCA clean will not have a HF dip. The purpose of this clean is to remove any particulates on the surface that may have been left on the substrate after the aluminum etch. Therefore, the HPM, APM, and spin rinser will suffice. It has been determined in previous experiments that a deposition thickness of 1000Å will satisfy the requirements for later processing.

Photolithography is the next step in the process. This step will be used to act as a mask when etching the silicon nitride. However, a hand made reticle is used for this processing using black tape to block the hν light. Referring to figure 1, the areas that are exposed are the die that are neither numbered or colored. Alignment is not critical in this stage for this experiment.

A quick plasma silicon nitride etch using SF_6 gas is performed next using RIT's GEC Plasma Cell. This machines etches silicon nitride at a rate of 1500Å/minute. However, since the desired thickness is 1000Å, the etch time should be a third less. Following the plasma etch, a wet etch in hydrofluoric acid is rendered to remove any oxide in the etched region followed by an ash to remove the photoresist.

Now, a quick silicon etch in KOH is performed. The reason that a quick etch is done is that only a small trench depth is desired. This depth should not be too deep because future MEMS processing will be done in this area and a deep trench will cause unwanted stress on thin films, such as photoresist. After the etch, the wafers are to be cleaned in DI-water and finally spin rinse dried. This is to ensure that the wafers are properly cleaned and will not continue etching the wafer. Figure 2. shows the wafer after the silicon etch.

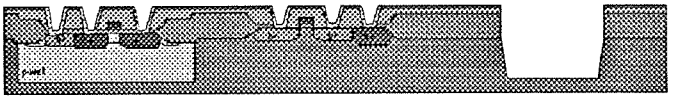


Figure 2. Theoretical look at a cross section of a die after the KOH etches. Visible are the oxide and nitride layers used in masking the non-etched regions.

Next, the second photolithography level is done for contact cut lithography. This step is used to create open regions for the aluminum to come in contact with the active area of the transistor. However, the major difference between this lithography step and the previous is that a larger amount of photoresist is used to prevent streaking. As a result of not filling in the etched silicon region, the holes must be filled with photoresist, or the thin resist will streak and cause highly non-uniform coatings.

Another silicon nitride etch is done to create the contact holes to the active area region. As with the previous nitride step, the etch time will be short. Again, after the etch, a quick HF etch is done to remove any native oxide that may be on the substrate.

An aluminum sputter deposition is next using RIT's CVC601 sputterer. A low base pressure is desired to achieve a high level of uniformity on the substrate. To help attain the low pressure at a faster rate, a preheat of the system is to be done. The expected thickness of the aluminum after the deposition is 5000Å.

The final photolithographic step is now performed to pattern the aluminum and create contact pads. As with the second photolithographic level, a large amount of photoresist is used to prevent any streaking. The wafers are then put into a wet phosphoric acid to etch the aluminum at 50°C for two minutes. Plasma etching is not needed here because the dimensions are so large. The

resist is then ashed off so that a sinter can be performed. A sinter is the step that creates good ohmic contact of the aluminum to the transistor. Sintering is performed in RIT's Bruce Furnace at 450°C for 30 minutes.

Finally, all of the wafers are electrically tested again to determine whether this process will effect the transistors. Results are compared to the original figures and an analysis is completed. Figure 3. shows a cross sectional view of the wafer after processing in complete.

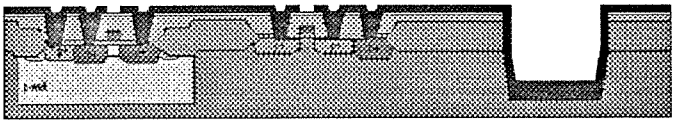


Figure 3. Cross sectional view of the wafer after all processing is complete.

3. EXPERIMENTAL PROCEDURE

Of the 15 wafers originally obtained, only 5 of them were working. Additionally, of the 5 that were working, one wafer broke while trying to remove an identifying sticker. In addition to the four remaining wafers, 2 more were used for experimentation or measurements, along with 3 dummy wafers.

Preliminary research was performed on the first aluminum etch to determine the length of time. Originally, the phosphoric bath was heated to 50°C, where the wafers would etch for 2 minutes. After a preliminary investigation, 2minutes of etch time was not enough since not all of the aluminum was removed. Most of the aluminum was removed, however a strange pattern was discovered which showed that the aluminum was etching faster near the edge of the wafer. This indicated that it is possible that the aluminum is thicker in the center of the wafer and didn't receive a uniform deposition, when originally processed. It was then determined that a higher temperature bath of 70°C would remove the aluminum faster, without ruining the devices. This was concluded to be true after another test wafer was etched for 45 seconds.

Following a standard RCA clean, a nitride deposition was performed using the ASM 6" LPCVD. The furnace was heated to 800°C with a deposition pressure of 360mTorr. Two separate gases were used during the deposition, NH_3 and SiH_2Cl_2. A new bottle of dichlorosilane was used in this experiment and was discovered that the concentration was about half of normal processing at RIT. To compensate, a longer deposition time of 35 minutes was calculated to achieve the target thickness of 1000Å. However, the deposition rate was faster than anticipated and an average thickness of 1250Å per minute was found.

All photolithography steps were hand coated and developed. Each step began with a 250°C dehydration bake for 2 minutes to insure that there was no water on the surface for promoting resist adhesion. Next, the photoresist, Shipley 812, was applied to the substrates and spun at 4500rpm for 60 seconds. A 90°C soft bake was done on the wafers for 60 seconds. Next, the wafers were exposed using the GCA 6700 g-line stepper for 0.4 seconds. A post-exposure bake was performed at 120°C for 60 seconds. The wafers were then developed in CD-26 developer. A final hard bake was performed at a temperature of 125°C for 60 seconds.

A nitride etch was done using the GEC Plasma Cell using SF_6 gas. An etch time of 1 minute was used as a result of the increased thickness as compared to the desired. As indicated earlier, the etch rate of this machine is 1500Å per minute and the thickness of the nitride was 1250Å. The over etch was felt to be okay, and would be used to make sure that all nitride was removed in the desired areas. This was the condition for both the etching steps.

The HF etch step was determined to be a long etch. Preliminary investigation found that the thickness of the underlying oxide to be approximately 7500Å. It was then determined that an etch of 25 minutes in length should clear all areas. Nanospec readings confirmed that this time was enough.

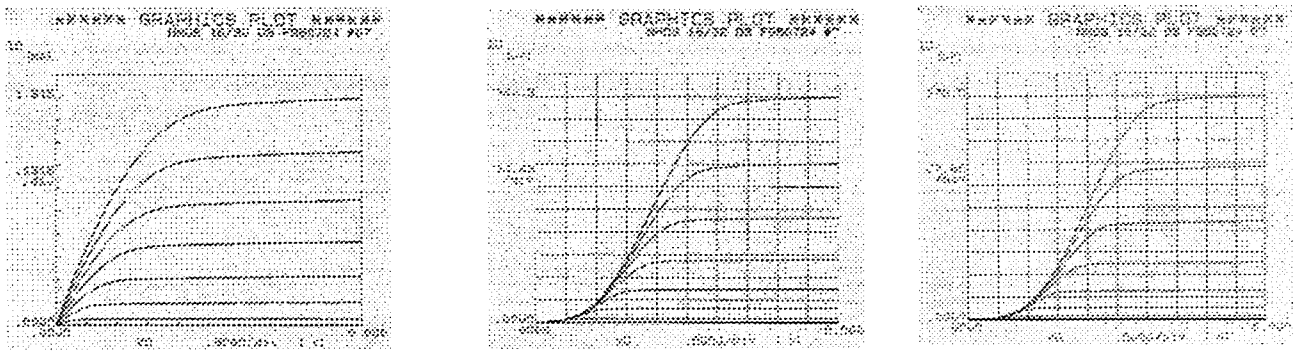
The silicon etch in KOH was performed at a temperature of 70°C. Preliminary investigations found that a 10 second etch would produce a depth of ~2μm. This depth will be too shallow since most micromechanical structures are larger than this. Therefore, etch times of 30 and 60 seconds were investigated. After the etch, the wafers were cleaned in DI-water and spin rinsed clean.

Sputter deposition was done using the CVC601 in the RIT Microelectronic facilities. The conditions for the sputter deposition are listed below in table 1.

Condition	Value
Base Pressure	3.60E-05
DC Watts	2000
Gas	Ar
Sputter Pressure (mTorr)	4.6
Preheat Temp. (degrees C)	300
Preheat Time (min)	20
Deposition Time (min)	20
Expected Thickness (Ang)	5000

Table 1. Sputter conditions.

The actual thickness of the deposited aluminum was found to be 6800Å.



(a) (b) (c)

Figure 4. Family of Curve plots after electrical testing: (a) Before processing (b) After first sinter (c) After second sinter

The second aluminum etch was performed using the standard recipe of 50°C, however this time the etch time was found to be 105 seconds. This is believed to be a result of changing the phosphoric acid, causing a change in the concentration.

Finally, the wafers were sintered using the Bruce Furnace at a temperature of 450°C for 30 minutes. A standard recipe set up by RIT was used in this experiment without any deviations. After the sinter, wafers were again tested and compared to the original results.

4. RESULTS AND ANALYSIS

Electrical testing had proven to show that MEMS processing after CMOS processing does effect the performance of the transistors. Refer to figure 4, which shows the results of die #7 of a wafer that received a 60-second silicon etch. The graphs in figure 4 are representative of all the working transistors. When comparing the results of the original to the post processing, the first thing that was noticed was that the I_D value decreased by a 3x factor. It is believed that this is a result of the nitride deposition, since it was done at a temperature of 800°C under vacuum for 35minutes. It is theorized that this temperature caused the dopants to diffuse further into the silicon, causing extra resistance. In accordance to Ohm's law,

$$I = V/R$$

the current will decrease as a result of the increasing resistance, while the voltage remains constant. The second thing that was noticed was that the Early voltage (V_A) had decreased after processing. For the transistor listed above, the V_A changed from –25.4 volts before processing to –54.0 volts after processing. The third thing that was noticed was that the barrier layer had changed causing the turn-on voltage (V_T) to increase. It is believed that this was caused by a poor sinter, causing poor ohmic contact. Therefore, an additional sinter was perform and tested again. Figure 4-c shows the results after the second sinter. It is noticed that there wasn't much of a change in the electrical performance, and it appears that the second sinter had no affect on the barrier layer. It could be concluded that this was not a result of a poor sinter but of something else, however additional testing should be done to confirm this.

Figure 5 shows an NMOS transistor after the experiment. The small squares within the larger squares represent the nitride contact cut, while the larger squares represent the original contact cut. The difference in size is a result of the nitride receiving a plasma etch, while the original cut was done with a wet etch. Also, closer inspection shows that there was some alignment problems with this experiment. Figure 6 shows the result of the etched silicon hole after sputter deposition of aluminum. The rough topography of the etch is a direct result of the mask that was made with black tape. It should be noted that the pattern is part of the gate array device.

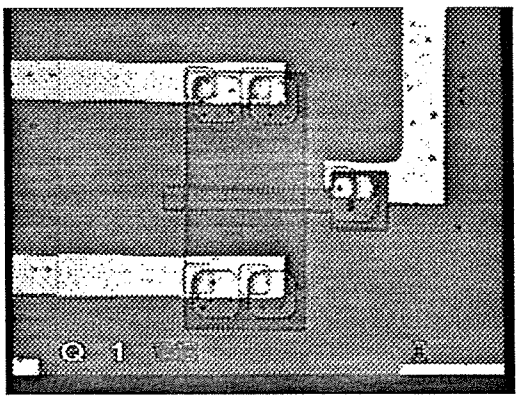


Figure 5. NMOS transistor after all processing.

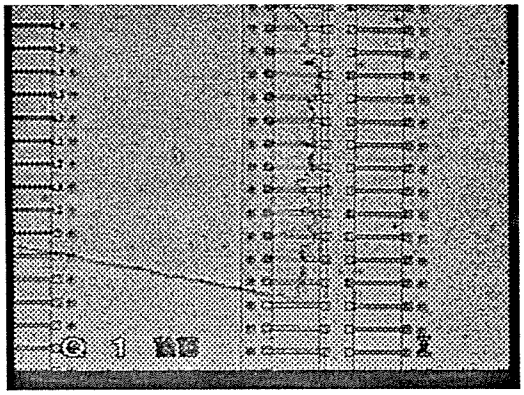


Figure 6. Etch region in the silicon to be used for MEMS processing.

5. CONCLUSION

This experiment is the first of many to come since RIT is trying to ramp up their efforts in the integration of MEMS with CMOS. These preliminary results show that a lot of effort and consideration are needed if the CMOS first method is to be implemented into practice. Despite the resulting outcome of the transistor performance, more experiments need to be conducted to verify the validity. Additionally, further experiments should also consider using the MEMS first approach and then compare the results.

REFERENCES

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