RIT Process and Device Simulation with Microtec

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Abstract– Microtec, a diffusion-drift model simulator by Siborg Systems, Inc., was used to simulate RIT's process for a 2-micron NFET (Long Channel), a scaled-down NFET (Short Channel), and our new advanced CMOS Process NFET. The accuracy of the simulator was tested with voltage threshold curves, sub-threshold characteristic tests, potential distribution plots, doping profiles, and oxide growth measurements. Microtec proved to be able to easily model RIT's device performance and process characteristics with only a small amount of modification.

1. INTRODUCTION

The purpose of the experiment is to investigate the performance of the Microtec Simulation tool from Syborg systems to verify the 2μm NFET process developed and manufactured at RIT. Initial investigation was difficult due to some of the limitations of the tool, but once a workaround was discovered work progressed quite well. The majority of the problems centered on the fact that Microtec will only simulate one oxide growth per section of the device. This made it very difficult to accurately model the process because even the implants are done through a screening oxide to achieve the proper profile and projected range. It was determined that the best method to model the devices was to break them up into three individual regions. The first region was the channel region which had the gate oxide growth on it and was not subjected to the V_T adjust implant. The second and third regions where very similar. The only difference is the drain is oriented around the x=2.5μm and the source is oriented around x=0μm. Both the drain and the source regions were simulated with the Kooi oxide growth and then implanted with the V_T Adjust implant.

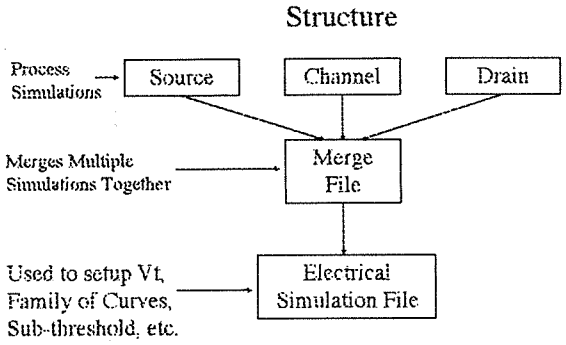

Figure 1

These three sections were combined as illustrated in Figure 1. The second step is the merge file, which combines all three of the process simulations. The third and final step defines the parameters in order to perform the electrical simulations.

2. Oxide Growth Measurements

Microtec doesn't calculate the oxide grown at the surface of the silicon. The value for the oxide grown was, instead, calculated by the amount of silicon consumed at the surface divided by 0.44. Figure 2 below illustrates the amount of oxide grown and the bird's beak.

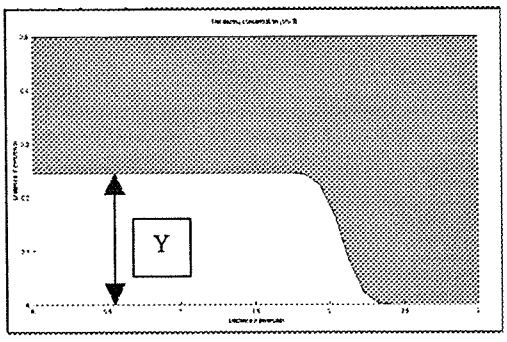

Figure 2

Simulation showed a wet oxide growth result for the Filed Oxide of 11102Å compared to a target of 10000Å. For the Kooi oxide the result was 1061Å versus a target of 1000Å. The dry oxide growth of the gate oxide showed a very similar trend in the results with 536Å in simulation against a target of 500Å.

3. RIT "FACTORY NFET"

The process details for the RIT "Factory NFET" can be found in reference [1]. The gate oxide thickness was 532Å as indicated in part 2.

A. Doping Profiles

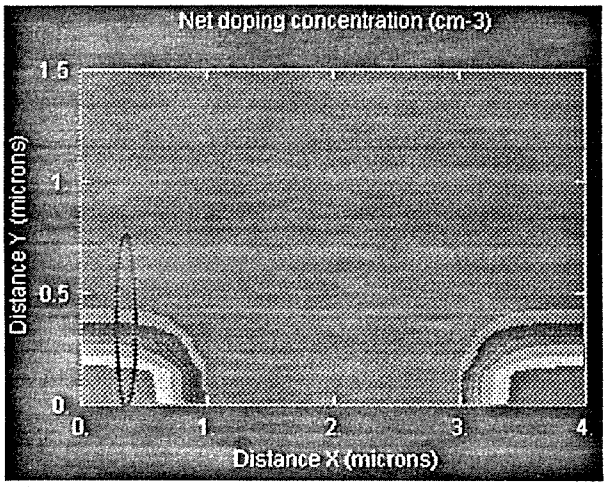

Figure 3

Figure 3 shows the net doping concentration as a contour plot for the x (across the device) and y (into the substrate). The differences in color represent a decade of change in the Doping concentration. It is clear from this contour plot that the Channel length of the device is about 2μm. This device for purposes of easy reference will be referred to as the RIT "Factory NFET" from now on.

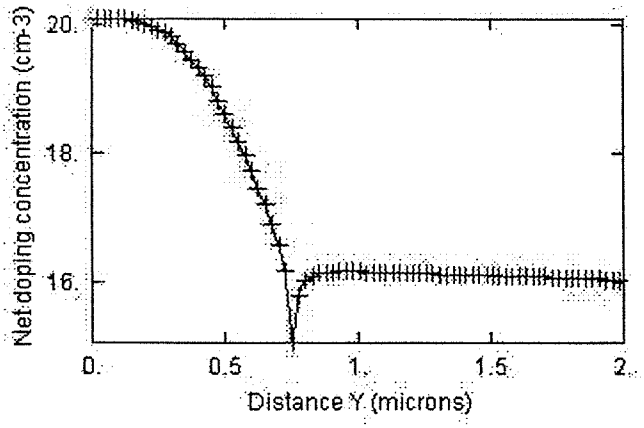

Figure 4

Figure 4 is a 1-D profile of Net Doping concentration versus Distance into the substrate at the point where the ellipse is in Figure 3. This plot was taken after the drain/source implant for the device and it clearly shows the drop in doping at approximately .75μm from the silicon surface and then a return to the substrate concentration of 10^{16} ions per cm^3.

B. Voltage-Threshold Calculation

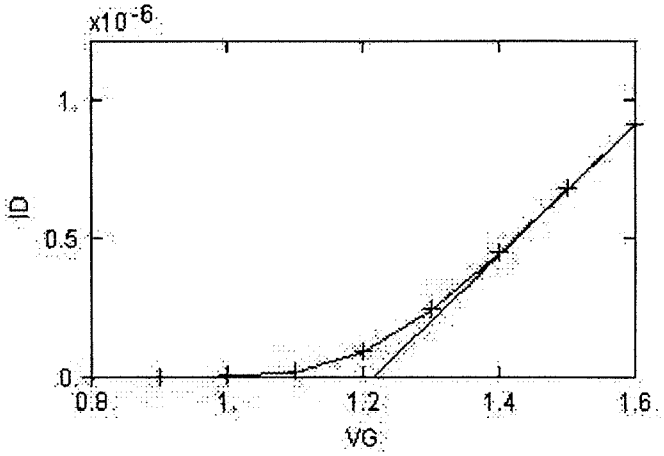

Figure 5

The threshold voltage was calculated by extrapolating a line tangent to the linear portion of the drain current vs. gate voltage and recording its intersection with the Vg axis, as illustrated in Figure 5. The simulated V_T for the RIT "Factory NFET" was 1.22V versus a target of 1V. The most likely reason for the discrepancy was the amount of oxide charge was estimated below that of the devices created in our Factory.

C. Family of Curves

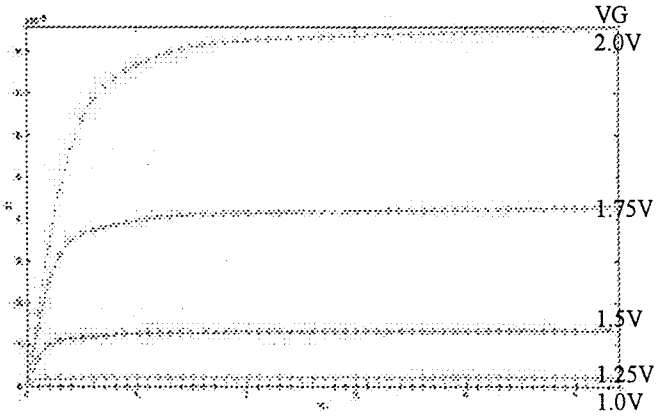

Figure 6

The "family of curves" in Figure 6 illustrates the long channel behavior of the device. The early voltage was measured to be greater than |200V|. The graph was obtained by applying a fixed voltage to the gate (indicated

by the Vg column to the right of the graph) and then ramping the voltage from 0 to 5V on the drain while measuring the current on the drain.

D. Sub-Threshold Characteristics

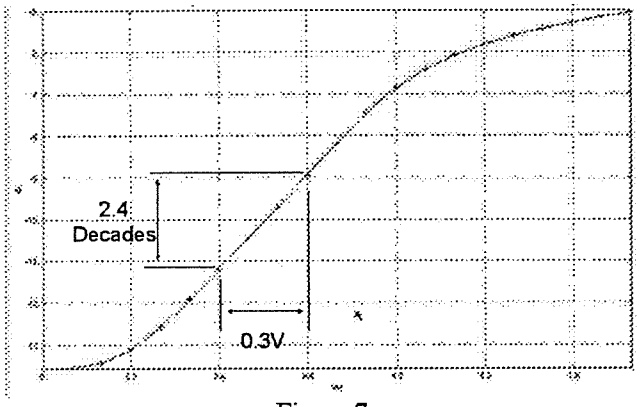

Figure 7

The sub-threshold swing in Figure 7 was modeled to be about 125mV/dec. An ideal device would be about 100mV/decade. The off-state leakage current was estimated at 10^{-14} A/μm. This estimation does not take into account reverse bias junction leakage for the device, which would dominate with the gate voltage near 0 volts.

4. SCALED-DOWN NFET

A. Doping Profiles

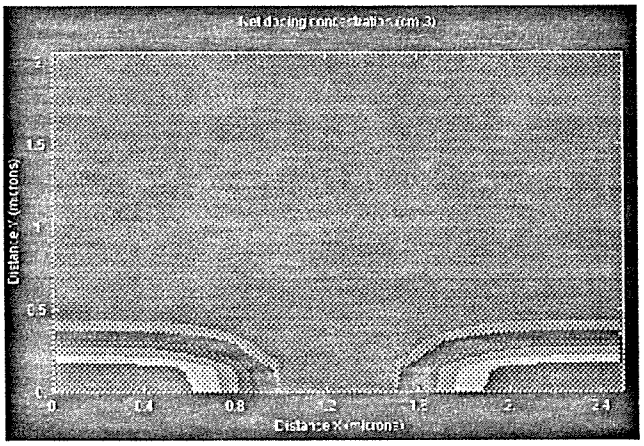

Figure 8

The laterally scaled NFET has a channel length of 0.5μm as illustrated in Figure 8, but is otherwise identical to the RIT "Factory NFET". The junction depth remained .75 μm and the oxide thickness was 532Å. The design of this experiment was to test the hypothesis that a scaled-down device would not perform adequately. In order to produce working devices at 0.8-0.5μm, there would be a need to design a new process.

B. Voltage Threshold Calculation

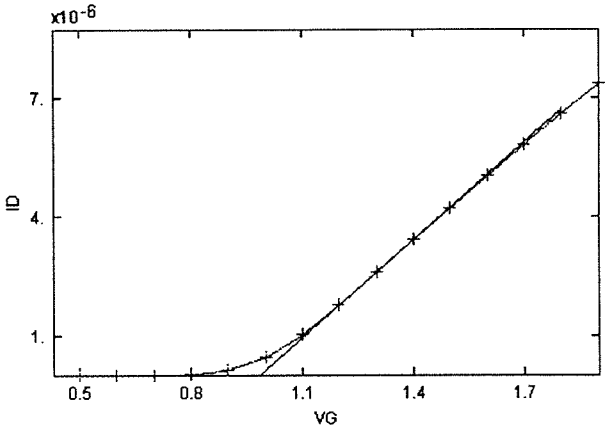

Figure 9

The threshold voltage for the scaled-down NFET was calculated in the same manner as was used for the RIT "Factory NFET". The value was 0.97V as can be seen in Figure 9. The most likely reason for the reduction of the threshold voltage from that value of the RIT "Factory NFET", was due to V_T Roll off.

C. Family of Curves

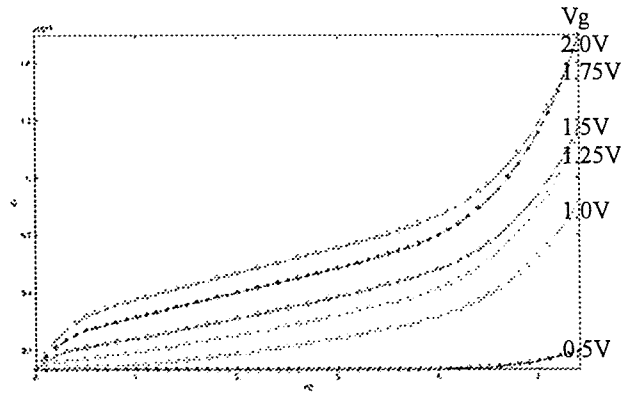

Figure 10

The family of curves in Figure 10 shows a much worse state of affairs. The extreme slop of the curves is due to channel length modulation and the Early voltage was extrapolated to be |2.1V|.

D. Sub-threshold Characteristics

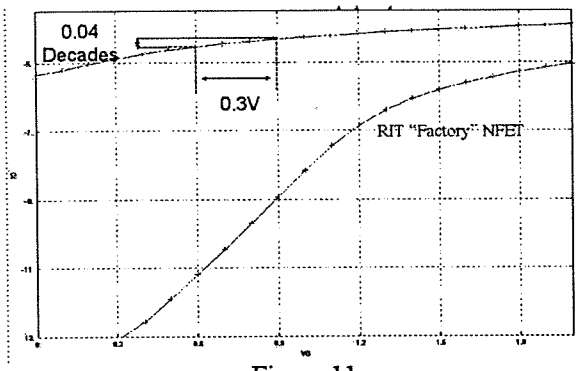

Figure 11

In Figure 11 it is clearly evident that the scaled-down device has serious problems. The RIT "Factory NFET" is included for comparison purposes. The Sub-threshold swing of the scaled-down NFET was calculated to be approximately 7.5V/decade. The off-state current was simulated at 10^{-6} Amp per μm. Again it is important to note that this calculation doesn't take into account reverse bias junction current, but it offers a significant contrast to the Long channel device.

5. RIT's SUB μm CMOS

A. Device Structure

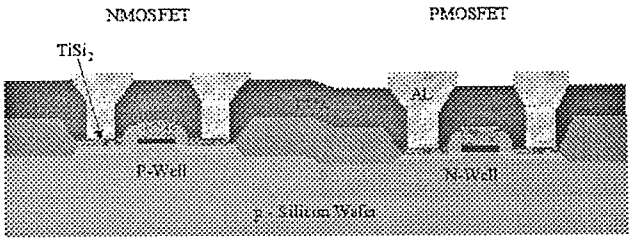

Figure 12

From the results of the Scaled-down NFET it is clear that a new process needs to be designed for RIT to produce working devices with channel lengths of 0.8-0.5μm. Extensive credit needs to go to Suraj Bhaskaran for the figures and results in this section. Figure 11 illustrates a 2D cross section of this newly designed NFET and PFET. Some of the features of this new process include a Dual well, LDD structures, 150Å Gate oxide, Titanium Salicide contacts, 14 Thermal steps, 7 implants (but no V_T Adjust implant).

B. Voltage Threshold Calculation

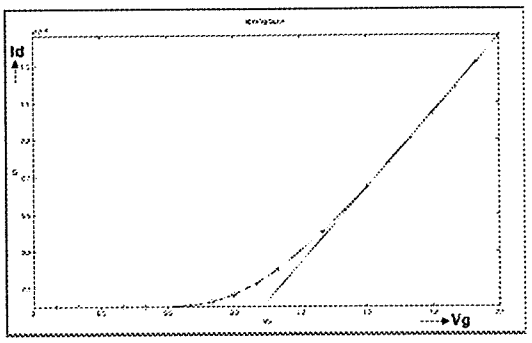

Figure 13

The threshold voltage for the RIT Sub μm CMOS was calculated in the same manner as was used for the RIT "Factory NFET". The value was 1.02V as can be seen in Figure 13 versus a target of 1V.

C. Family of Curves

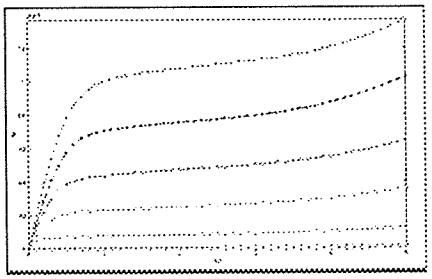

Figure 14

The family of curves in Figure 14 indicates a much better performing structure than the scaled-down NFET. Channel length modulation is still present in the device but has been reduced yielding an Early Voltage of approximately |20V|.

D. Sub-threshold Characteristics

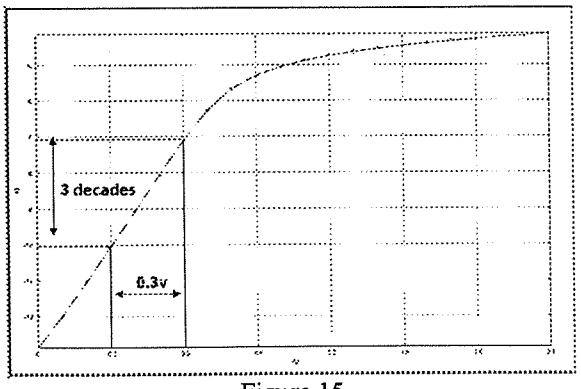

Figure 15

Figure 15 illustrates the improved sub-threshold swing of approximately 100mV/decade. This combined with the off-state leakage current of about 10^{-14} A/μm, illustrates the benefits of the new process that was designed for devices of this size.

6. CONCLUSION

Microtec is a very capable simulator that correctly reflected the results consistent with the RIT fabrication plant. In order to move from the original 2um NFET to a 0.8um-0.5um NFET simulation verified it is necessary to design a new process. The new Microtec release due this summer will allow for even more accurate process and device simulations.

REFERENCES

[1] MESA Process Description of RIT 2μm NFET, Unpublished.
[2] Syborg Systems Inc., Microtec Manual. http://www.syborg.ca, 1998.
[3] Bhaskaran, Suraj, "RIT's Sub μm CMOS Process," Unpublished.

ACKNOWLEDGMENTS

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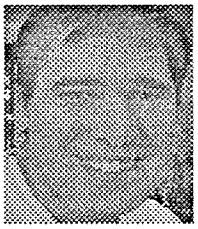

Charles R. Overbeck, originally from Leabnon, OH received B.S in Microelectronic Engineering from Rochester Institute of Technology in 2000. He attained co-op work experience at National Semiconductor and VLSI Technology. He is joining Apple Computer, Inc as a Design-For-Test Engineer starting July 2000.