

Cobalt Silicide Formation and Patterning Technology

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Abstract— The goal of this investigation was to develop a cobalt silicide formation process as a stepping stone to investigate a novel patterning technique known as, LOCOSI (LOCal Oxidation of Silicide). Cobalt silicide films were formed by sputter depositing cobalt onto silicon wafers then annealed at temperatures varying from 750 - 1000°C using two methods. The first method was a conventional anneal using a horizontal furnace using a forming gas ambient. The second method was a RTA (Rapid Thermal Anneal) using a nitrogen ambient. The RTA process for silicidation provided essentially a continuous film with minimal cracking, whereas the furnace anneals resulted in non-continuous cobalt silicide films. The patterning of the films, which requires a patterned oxidation mask similar to the LOCOS (LOCal Oxidation of Silicon) process, was unsuccessful.

1. INTRODUCTION

Cobalt silicide has been used in industry to form self-aligned low resistance source/drain and gate contacts. New applications of cobalt silicide include fabrication of ultra-short Schottky-Tunneling MOSFETs and MSM (metal-semiconductor-metal) photodetectors. Fabrication of these devices requires nanometer scale patterning of cobalt silicide film. Unfortunately, conventional patterning techniques require high-end lithography equipment for the small dimensions and a dry etch process. Using a novel patterning technique, known as LOCOSI (LOCal Oxidation of Silicide), cobalt silicide films can be patterned using low-end lithography equipment.

As cobalt was new to RIT the deposition and silicidation processes needed to be developed before any patterning could take place. This development work sets the groundwork for future optimization and for studies of other cobalt/cobalt silicide applications.

2. THEORY

A. Cobalt

Cobalt is a group VIII, near noble metal with the following material properties.

Table 1: Selected Properties of Cobalt

Property	Value
Atomic Number	27
Atomic Mass	54.938
Reflectivity	67%
Melting Point	1495°C
Resistivity	6 $\mu\Omega$ cm

B. Cobalt Silicide

Cobalt reacts with silicon to form cobalt silicide, which has a resistivity ranging from 18-20 $\mu\Omega$ cm. While many combinations are possible, the stoichiometry of interest is cobalt disilicide, CoSi_2 because silicon-rich silicides are more stable than metal-rich silicides. Figure 1 below shows the how the heats of formation rises as the silicon content increases but levels off after silicide becomes silicon-rich. [1]

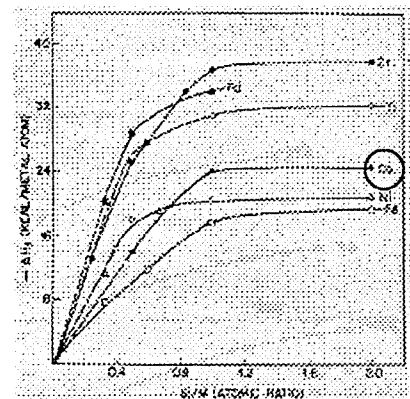


Figure 1: Heat of formation per metal atom of silicides as a function of metal to silicon ratio [1]

The phase of the silicide is temperature dependent. According to literature, at temperatures from 300-600°C mostly CoSi and Co₂Si with some CoSi₂ are formed. At temperatures above 600°C only is formed CoSi₂. Also at temperatures ranging from 200-600°C, cobalt is the dominant diffuser. At higher temperatures silicon gradually becomes the dominant diffuser. These concepts are important when siliciding by annealing cobalt films on silicon substrates. [1]

Cobalt silicide is a tensile film, which can result in film cracking. The magnitude of stress varies with the phase of the silicide, substrate doping, and temperature. As the CoSi₂ phase about to form silicon diffuses through the grain boundaries of the silicide and metal films resulting in compressive stress. Once the phase forms a volume contraction takes place resulting in tensile stress in the film. Once the film has cooled the end result is a tensile film. The silicon doping concentration works to slow the silicidation process thus shifting the temperatures at which the different phases form. [2]

The thermal stability of the cobalt silicide varies with the dopant species in the substrate and whether the substrate is poly or monocrystalline silicon. Silicides on polysilicon substrates typically are more sensitive to thermal processing, however this phenomenon still occurs with silicide on monocrystalline silicon. The degradation of the silicide at temperatures over 800°C occurs because of silicon precipitation in the silicide film. As discussed earlier, at higher temperatures silicon becomes a dominant diffuser. The result is a breakup in the continuity of the silicide film. [3]

C. LOCOSI (Local Oxidation of Silicide)

The LOCOSI process is similar to the well-known LOCOS process used to selectively grow the isolation oxide in CMOS technology. However, the purpose and functionality of these two processes is different. Both processes use a Si₃N₄/SiO₂ oxidation mask to selectively grow an oxide. The purpose of LOCOSI is to pattern the silicide layer under the oxidation mask.

Below is a breakdown of the mechanism, which leads to separation in the film (Figure 2).

- 1) Oxidizing ambient diffuses through oxide and disassociates the silicide.
- 2) The free silicon reacts with the oxidant to form silicon dioxide.
- 3) The free cobalt diffuses through the silicide to the silicide/substrate interface where it reacts with silicon to form silicide.
- 4) Near the edge of the oxidizing mask the stress of the nitride forces the diffusing cobalt to drift away from that edge. This causes a gap to form at the mask edge.

In the LOCOSI process the stress of the nitride film is desired unlike in the LOCOS process.

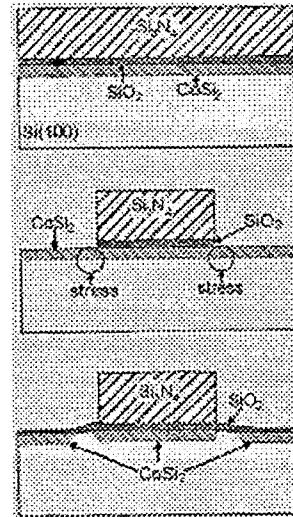


Figure 2: Cross-sections showing the functionality of the LOCOSI process.

Figure 3 below illustrates why the oxidation process forms SiO₂ on the surface rather than a cobalt oxide. [4]

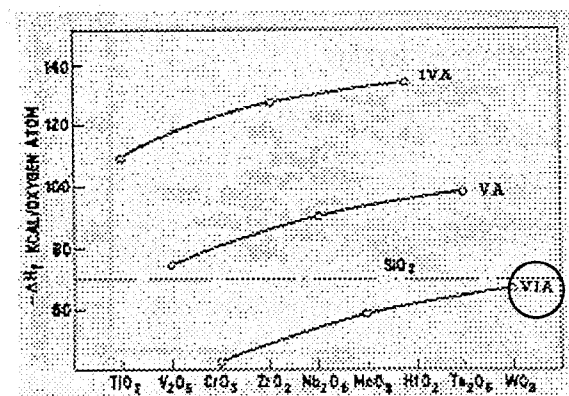


Figure 3: Heats of formation per oxygen atom of various oxides. Also shown is the heats of formation for SiO₂. Cobalt oxides behave like the group VIA elements. [1]

According to literature cobalt oxides behave like the oxides of VIA element oxides. As can be seen in figure 3 it is more favorable for SiO₂ to form than a cobalt oxide. Once the cobalt is dissociated it diffuses through the silicide since it is not favorable for the cobalt to form a metal rich silicide. (Figure 1)

LOCOSI experiments found in literature used epitaxial CoSi₂ deposited by MBE (Molecular Beam Epitaxy). The oxidation mask is then aligned parallel to <110> directions of the silicide to obtain a clean separation. However, it is

mentioned process works for polycrystalline cobalt silicide. [4, 5]

3. EXPERIMENTAL

A. Furnace Anneal

The initial step before cobalt can be deposited on the wafers was a preclean. This was done by immersing the wafers for 10 min in a $\text{H}_2\text{SO}_4/\text{H}_2\text{O}_2$ solution for 10 min. This was followed by a 5 min rinse and a 10 sec HF dip to remove any native/chemical oxide.

The wafers were then pulsed DC sputtered using a CVC 601 sputterer at the following setpoints.

Table 2: Sputtering setpoints for Co deposition

Parameter	Setpoint
Power	500 W (4" Co target)
Base Pressure	~2 E -5 Torr
Argon Pressure	5 mTorr
Pre Sputter Time	5 min
Sputter Time	5 min

The deposited film was about 800 to 1000Å thick. Readings were performed on an Alphastep, which was uncalibrated after being serviced so readings may not be accurate.

The average resistivity of the Co film on Si was 88 $\mu\Omega$ cm, which is about 15 times greater than the literature quoted value of 6 $\mu\Omega$ cm. This could be do to oxygen incorporation into the film during sputtering.

This first batch of wafers were then annealed in a Bruce 6" horizontal furnace at 800°C, 900°C and 1000°C. The basic recipe for the anneal is listed below in Table 3.

Table 3: Basic Furnace Anneal Recipe

Step	Time	Gas
Push in 800°C	12 min	N ₂
Stabilize at 800°C	15 min	N ₂
Ramp up to Soak Temp	20-30 min	N ₂
Soak at Soak Temp	30 min	H ₂ /N ₂
Ramp down to 800°C	30-40 min	N ₂
Pull at 800°C	15 min	N ₂

After the wafers were annealed they were placed in a selective etch to remove unreacted cobalt if any. This was done in a 35 sec dip in $\text{H}_2\text{SO}_4/\text{H}_2\text{O}_2$ at 125°C. The wafers were all hazy and gray before the etch with divots missing in the films. Afterwards it appeared as if the material at

the edges of the wafer etched away and the gray streaks remained on the wafer along with the divots (figure 4). Attempts at resistivity measurements gave odd results with varying amounts of current with no voltage reading or reading that resembled the bare silicon measurements.

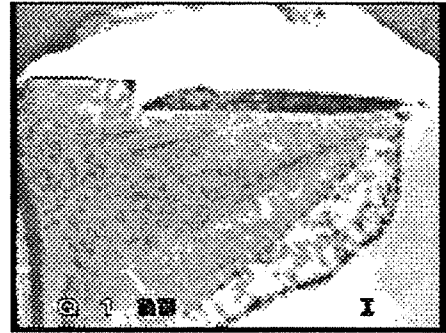


Figure 4: Divot in film after silicidation in furnace.

After inspection of the films under an optical microscope it was discovered that the films were not continuous (Figures 5-7).

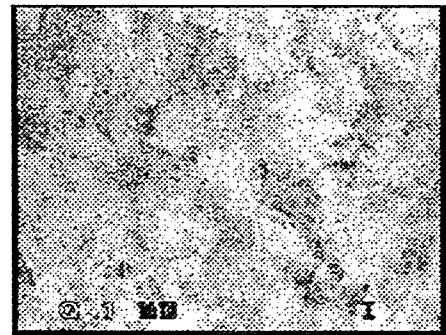


Figure 5: Silicidation in furnace at 800°C

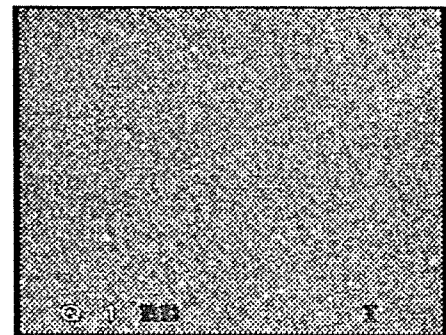


Figure 6: Silicidation in furnace at 900°C

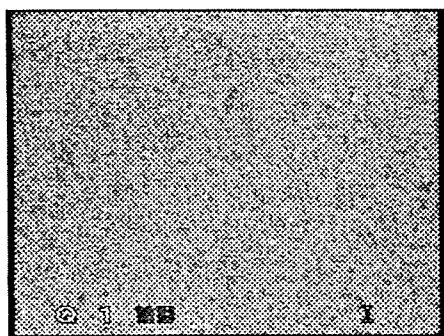


Figure 7: Silicidation in furnace at 1000°C

Although the silicide films were not continuous the wafers were still oxidized to see the effect. The oxidation was performed in a Bruce 6" horizontal furnace using the following recipe.

Table 4: Recipe for thermal oxidation of cobalt silicide.

Step	Time	Gas
Push in 800°C	12 min	N ₂
Stabilize at 800°C	15 min	N ₂
Ramp up to 900°C	20-30 min	N ₂
Soak at 900°C	10 min	H ₂ O
Ramp down to 800°C	30-40 min	N ₂
Pull at 800°C	15 min	N ₂

Figure 8 shows the result after oxidizing a wafer annealed at 800°C. The oxidation process made the non-continuous film worse.

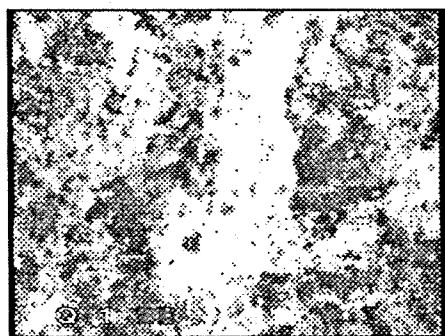


Figure 8: Wet oxidation of wafer silicided at 800°C in furnace.

B. RTP Anneal

Since the furnace anneals gave a poor film a rapid thermal anneal process was developed. Once again the initial step before cobalt was deposited was a preclean. The clean procedure was changed in case the cause for the

divots in the films produced in the furnace was due to poor adhesion. During this trial a full RCA clean was performed followed by a 10 sec HF dip to remove any native/chemical oxide.

The wafers were then pulsed DC sputtered using a CVC 601 sputterer at the following setpoints. The only difference was the lower base pressure.

Table 5: Sputtering setpoints for Co deposition

Parameter	Setpoint
Power	500 W (4" Co target)
Base Pressure	~8.6 E -6 Torr
Argon Pressure	5 mTorr
Pre Sputter Time	5 min
Sputter Time	5 min

Once a gain the deposited film was about 800 to 1000 Å thick. The average resistivity of the Co film on Si was, 48 μΩ cm. This is an improvement over the wafer which were used for the furnace anneal runs which gave 88 μΩ cm. The wafer for this run were heavily doped p-type (20 Ω cm) whereas the wafer used during the previous runs were moderated doped p-type (40-60 μΩ cm). Also the lower base pressure results in less oxygen incorporation into the cobalt film.

This batch of wafers were annealed in a AG Associates HeatPulse 410 RTP at 750°C, 800°C and 900°C in a nitrogen ambient. When performing anneals in the HeatPulse 410 there is no recipe to run, the time and temp are set and then started. However, a 30 sec delay was used after the wafer was in the chamber before starting the anneal to allow the chamber to fill up with nitrogen. Afterwards the wafer was allowed to cool in the chamber for about a minute before removing it. This is to avoid any potential reactions with the clean room ambient while the wafer is still hot. Figures 9-11 below show the cobalt silicide films formed by RTA.

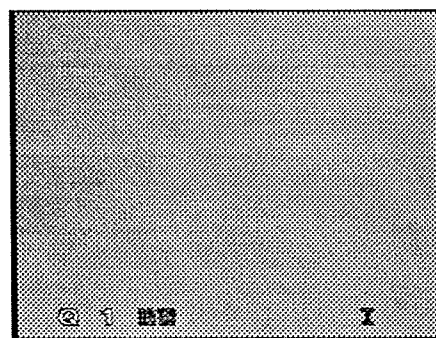


Figure 9: Silicidation in RTP at 750°C for 20 sec.

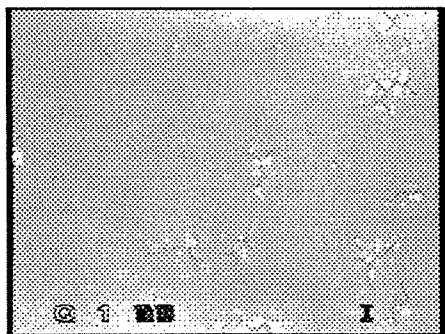


Figure 10: Silicidation in RTP at 800°C for 20 sec.

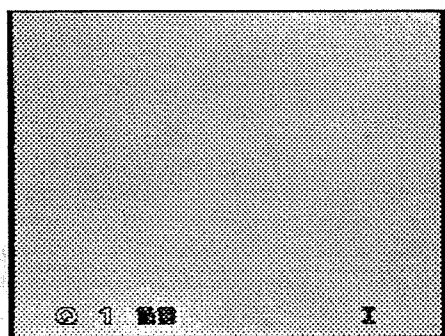


Figure 11: Silicidation in RTP at 900°C for 20 sec.

Notice that the films produced by RTA are continuous with minimal cracking. The wafers annealed at 750°C showed less cracking and flaking of unreacted cobalt. At the higher temperature anneals, 800°C and 900°C, the films showed large areas of flaking cobalt. The majority of the film on the 900°C sample showed film degradation. When the wafers were selectively etched for 35 sec in $\text{H}_2\text{SO}_4/\text{H}_2\text{O}_2$ at 125°C, the degraded film regions and the areas with flaking cobalt were removed. Figures 12-13 below show this film defects.

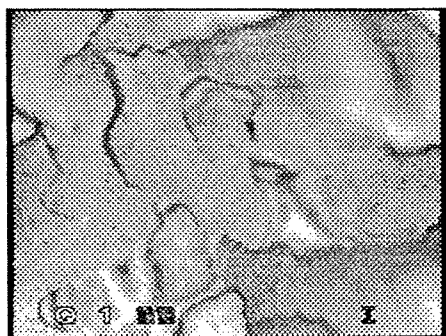


Figure 12: Flaking of cobalt film after anneal at 800°C.

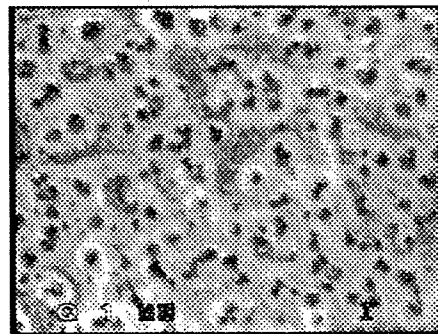


Figure 13: Film degradation after anneal at 900°C.

Table 6 below shows the resistivity results of the RTA silicides on silicon. The measurements were taken in areas where there was no film degradation.

Table 6: Resistivity results for silicidation in RTP

Anneal Temp	Resistivity
750°C	326 $\mu\Omega$ cm
800°C	No reading film was damaged
900°C	16 $\mu\Omega$ cm

C. Patterning

Due to time restrictions a new 800°C sample was not created to replace the one that was damaged. The first step of the patterning process was to build the oxidation mask. The oxide layer was deposited using an LTO process in a 4" LPCVD tube. The process parameters are below.

Table 7: Process parameters of LTO dep.

Parameter	Setting
Temperature	400°C
Base Pressure	60 mTorr
Gasses	40 sccm of Silane
	48 sccm of Oxygen
Dep Time	15 min

The target thickness was 500Å, but the actual thickness was 711Å. Figures 14-15 show the LTO film over the cobalt silicide. The cobalt silicide films look intact which is expected because of the low temperature of the LTO process.

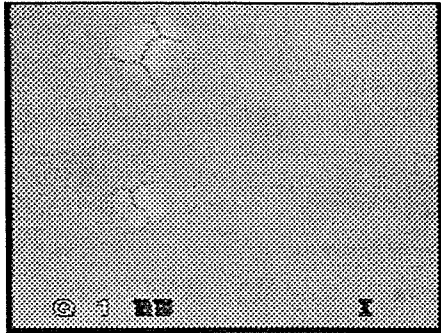


Figure 14: LTO over cobalt silicide film formed at 750°C by RTA

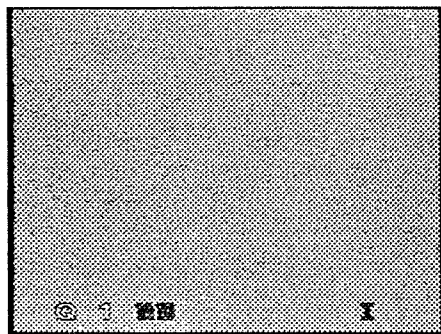


Figure 15: LTO over cobalt silicide film formed at 900°C by RTA

After the LTO deposition the nitride film was deposited in the same CVD tube as the LTO at the following setpoints.

Table 8: Process setpoints for silicon nitride deposition

Parameter	Setting
Temperature	810°C
Base Pressure	60 mTorr
Gas	Dichlorosilane
Dep Time	17 min

The target thickness was 1500Å but the actual thickness was 1349Å. The result is a nitride/oxide thickness ratio of 1.89.

The oxidation mask must be patterned before the actual thermal oxidation takes place. The wafers were coated and exposed using a G-line stepper and capacitor mask, which has large capacitor pads. Afterwards the nitride was etched off using a Drytek Quad. Table 9 gives the process parameters of the nitride etch.

Table 9: Nitride etch process parameters

Parameter	Setting
Pressure	300 mTorr
Forward Power	265 W
Gas	30 sccm of SF ₆
Etch Time	65 sec

This etch process consumes all of the nitride and some of the oxide underneath. Figures 16 – 7 show the films after the etch process.

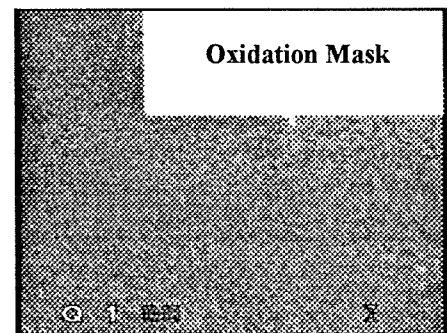


Figure 16: After nitride etch. The exposed cobalt silicide film shows signs of breakup. (silicided at 750°C)

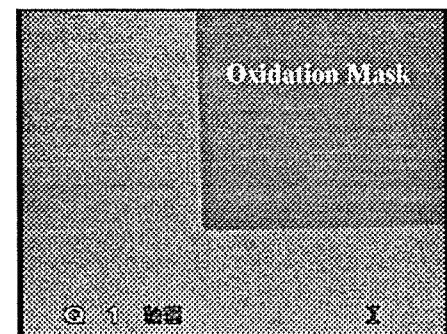


Figure 17: After nitride etch. The exposed cobalt silicide film shows signs of breakup but not as severe as Figure 16. (silicided at 900°C)

Once the nitride is removed the wafers can be thermally oxidized to pattern the cobalt silicide film. The oxidation recipe parameters are the same as described in Table 4. Figures 18-19 show the results after oxidation.

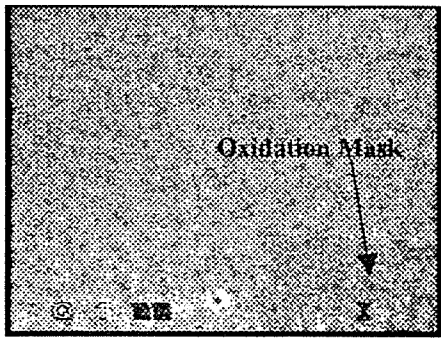


Figure 18: After thermal oxidation. Shows a reaction between the different films. (Silicided at 750°C)

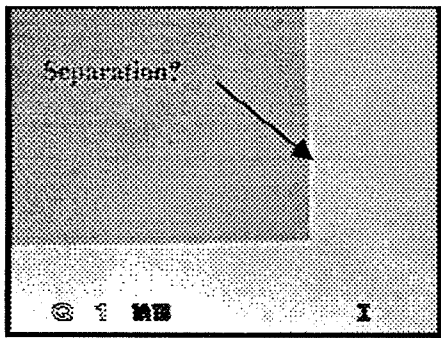


Figure 19: After thermal oxidation. Shows what might be separation. Cobalt silicide film is no longer continuous. (Silicided at 900°C)

While the two wafers shown above were processed in the same run the one which was silicided at 750°C showed a much less thermal stability than the wafer silicided at 900°C.

4. DISCUSSION

The poor results given by the furnace silicidation can be attributed to several reasons. First is the pre clean before the Co deposition, which was not a complete RCA clean as done with the wafers used processed in the RTP. If the wafers were not clean enough the poor adhesion would explain the divots in the silicide film.

Another reason is the furnace recipe itself. The recipe dictates that the wafers are push and pulled at 800°C. Although nitrogen is flowing during this the wafers are exposed to the clean room ambient while they are hot. This can cause oxygen incorporation into the film. Also at the high temperatures the silicon tends to diffuse through the metal and precipitate causing the break up of the film.

A slower furnace recipe may be beneficial in controlling the reaction. The wafers could be pushed in at lower temperatures (500°C) then ramped to the desired anneal temperature.

The RTP anneals showed similar issues with film degradation at higher temperatures as the furnace anneals. The other issue with the RTP anneal was the high resistivity (326 $\mu\Omega$ cm) of the 750°C annealed wafer. This along with the reaction seen with the LTO and Nitride films (Figure 18) during patterning indicate that the silicide film did not contain large amounts of cobalt disilicide, which should be more stable and have much lower resistivity like that of the 900°C annealed sample (16 $\mu\Omega$ cm). Although literature states that cobalt disilicide is formed at temperatures above 600°C, this could be explained by the high dopant concentration in the wafer which slow down the process thus requiring higher temperatures to change phase. However this would need to be investigated further.

XRD data for the samples silicided at 750°C and 800°C showed no peaks. Perhaps this means that the films were still amorphous. Figure 20 is a sample from literature showing peaks.

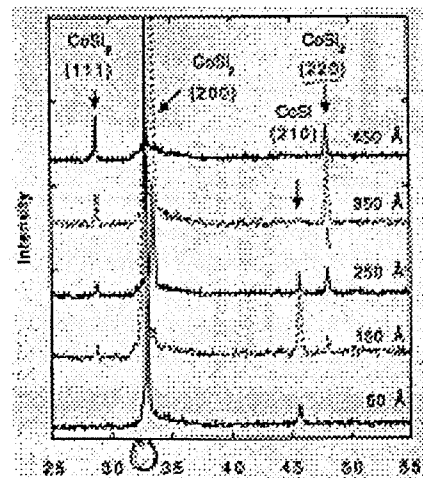


Figure 20: Sample XRD trace showing the peaks corresponding to different phases of cobalt silicide.

The cobalt silicide formed at 900°C showed better thermal stability to the oxidation process and perhaps some separation. Unfortunately, the SEM used to capture an image of the cross-section did not have enough resolution to verify separation.

5. CONCLUSIONS

Of the two silicidation techniques, RTA produced essentially continuous films with minimal cracking. The furnace anneals produced non-continuous films. The flaws in the furnace anneals include the push in at a high temperature of 800°C. This coupled with the long stabilization time may have caused the film degradation. The furnace anneal recipes should be rewritten to start off

at a lower temperature and ramp up once the wafers are in the tube.

Although the RTA films were practically continuous, the HeatPulse 410 does have some thermal non-uniformity which prevent the formation of a uniform cobalt silicide film across the wafer. Another issue is the cracking in the films silicided at temperatures above 750°C. Like the furnace anneals heating the wafer up to such high temperatures quickly causes stress and film degradation issues. It would be beneficial to process the wafers in a 2-step anneal starting with a lower temperature around 500°C and then moving to higher temperatures.

The silicide films produced at 900°C in the RTP proved to be the most stable film and exhibited the lowest resistivity of 16 $\mu\Omega$ cm, which corresponds to literature values for cobalt disilicide films.

The patterning process was not successful. The cobalt silicide films under the oxidation mask broke up into islands after nitride deposition. The wafers, which were silicided at 750°C showed reaction the oxidation mask after the final oxidation step in the LOCOSI process. This however was not observed with the wafer, which was silicided at 900°C.

Some future work that could be done include investigating what effect the pre-deposition clean has on the silicidation and resistivity of cobalt silicide and testing out a piecewise anneal process on both the RTP and furnace to see if a the silicide quality is improved (i.e. thermal stability and continuity). Once a thermally stable and continuous film is achieved then the oxidation mask thickness ratios for the LOCOSI need to be optimized to see observe their effect on the patterning process. Also a rapid thermal oxidation should be investigated for the patterning process.

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