

Development of an Anisotropic, Selective Polycrystalline Silicon Dry Etch Process

Randy Supczak
Microelectronic Engineering
Rochester Institute of Technology
Rochester, NY 14623

Abstract – The development of a polysilicon dry etch process that would result in anisotropic etch profiles as well as high selectivity to photoresist and silicon dioxide has been studied. It was found that decreasing the amount of fluorine (SF_6) in the plasma significantly increased the polysilicon etch rate while only increasing the etch rate of silicon dioxide slightly.

Two optimal processes were found: One that emphasized anisotropy (70% SF_6 flow, 90mTorr pressure, and 200W RF power) and one that emphasized SiO_2 selectivity (70% SF_6 flow, 230mTorr pressure, and 200W RF power).

1. INTRODUCTION

Highly anisotropic etching of silicon is a key process in many applications, such as deep trenches for capacitors, integrated optoelectronics, and integrated sensors. It is also extremely important in the manufacturing of very large scale integrated (VLSI) circuits, specifically in the area of polycrystalline silicon (polysilicon) gate etching. Anisotropic etch profiles are important to ensure that gate lengths are within specification, as well as to facilitate conformal film deposition in subsequent processing.

A. Background

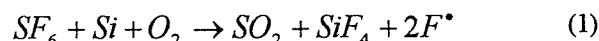
Polysilicon etching is typically performed using a chlorine or bromine chemistry [1]. Both these gases are extremely toxic and corrosive. Their use requires special hardware to prevent corrosion of the processing equipment. Chlorine/bromine etch chemistries also have the disadvantage of etching most masking materials used. This lowers the selectivity to other layers, such as silicon dioxide (SiO_2) and photoresist.

Fluorine-based chemistries, such as SF_6 , offer an alternative to chlorine/bromine. In addition to being less hazardous to the environment, the SF_6 chemistry provides higher silicon etch rates and selectivities than chlorine/bromine chemistries. The major disadvantage of SF_6 is it yields isotropic etch profiles. Cryogenic etching is a means of overcoming this isotropy, as is the addition of O_2 or $\text{C}_2\text{Cl}_3\text{F}_3$ [2]. As reported in [2], the addition of O_2 reduces selectivity to photoresist, and $\text{C}_2\text{Cl}_3\text{F}_3$ is a chlorine containing material.

The development of an anisotropic, selective polysilicon dry etch process was the focus of this experiment. Considerable research has gone into the development of anisotropic, selective dry etch processes for polysilicon using a variety of process conditions [3-5]. Because of the limitations regarding chlorine gas mentioned before, alternatives were sought. Fluorocarbon plasmas were not considered, as they result in polymer formation which can contaminate the process chamber if strict attention is not paid to cleanliness (i.e., O_2 plasma after etch to clean chamber).

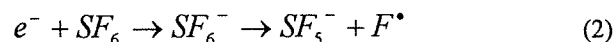
B. Theory

With these considerations in mind, SF_6/O_2 was chosen for the plasma chemistry. As shown in Equation 1, the addition of O_2 to the plasma results in an increase in the F^* concentration, which increases Si etch rate.



Equation 1 shows that O_2 reacts with S and prevents recombination with F^* . Oxygen also combines with Si at the sidewalls to form SiO_2 , thereby passivating the sidewalls and reducing isotropy.

Fluorine is strongly electronegative, and as a result electron attachment ionization can occur in the plasma. This results in the formation of negative ions:



Negative ions assume the role of electrons in the plasma. Because negative ions are more massive than electrons, they oscillate slower under AC excitation. This reduces the conductivity of the plasma, and results in non-uniformity in the plasma. Thus, a SF_6 chemistry can lead to non-uniform etching.

2. EXPERIMENTAL

A. Sample Preparation

All of the etching was carried out in a Drytek Quad 482 parallel plate reactor with an operating frequency of 13.56MHz. A two level factorial experiment was used

where the power (200 – 350W), pressure (90 – 230mTorr), and SF₆ flow (70 – 100%) were varied. Table 1 lists the experimental details of the experiment.

Table 1: Experimental Design

| Run | SF ₆ Flow % | Pressure (mTorr) | Power (Watts) |
|-----|------------------------|------------------|---------------|
| 1 | 100 | 90 | 350 |
| 2 | 70 | 230 | 350 |
| 3 | 85 | 160 | 275 |
| 4 | 100 | 230 | 200 |
| 5 | 70 | 230 | 200 |
| 6 | 100 | 90 | 200 |
| 7 | 85 | 160 | 275 |
| 8 | 70 | 90 | 350 |
| 9 | 85 | 160 | 275 |
| 10 | 70 | 90 | 200 |
| 11 | 100 | 230 | 350 |

Three center point runs (275W, 160mTorr, 85% SF₆ flow) were included to evaluate experimental error.

The starting material was 100mm n-type silicon wafers (100). A 1000Å wet oxide was grown in a 6" horizontal furnace at 900°C for 42 minutes. A 0.6µm polysilicon layer was then deposited in a LPCVD furnace at 610°C for 78 minutes.

In order to simulate the CMOS process used at Rochester Institute of Technology (RIT), the polysilicon was then doped using N250 arsenosilicate spin-on glass. The SOG was spun on at 3500RPM for 30 seconds, followed by a 15 minute pre-bake at 200°C. An arsenic drive-in step followed this at 1000°C for 15 minutes.

The wafers were next coated with 0.98µm of Shipley S-8 photoresist and exposed using a g-line stepper. The reticle used was the RIT CMP test mask, which had various features including dense lines/spaces of varying coverage. The minimum resolvable linewidth in photoresist was 1µm.

Windows were opened through the resist across the wafer to make direct measurements of the polysilicon thickness.

Initial step height measurements were made using a Tencor Alpha-step profilometer. These would be later used to determine polysilicon etch rates and selectivities to SiO₂ and photoresist. Scanning electron microscopy was used to evaluate anisotropy of the individual process runs.

B. Etching Process

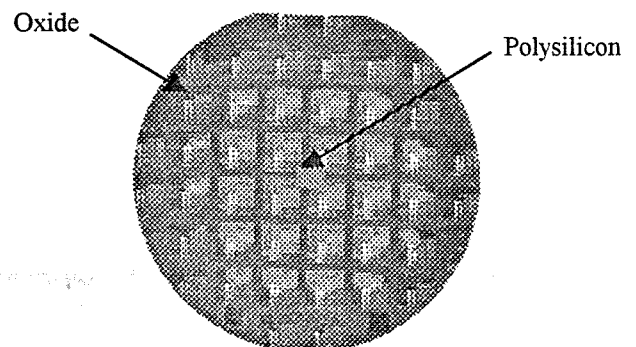
The SF₆ flow was held constant at 40sccm while the O₂ flow rate was varied from 0 – 17sccm. This allowed variation in SF₆ flow from 70-100%. Each wafer was etched for 20 seconds. Polysilicon thickness

measurements were then made using a Nanometrics Nanospec AFT thin film thickness measuring tool. Polysilicon etch rate was calculated from these pre- and post-etch values. Each wafer was then etched, in 15 second increments, until all the polysilicon cleared, exposing the oxide. A 15 second over etch was then performed to determine the selectivity to oxide.

3. RESULTS AND DISCUSSION

The most noticeable result after removing each wafer from the etch tool was the etch non-uniformity across the surface of the wafer. The edges of the wafers etched significantly faster than at the center. This is shown in Figure 1.

Figure 1: Etch non-uniformity across wafer



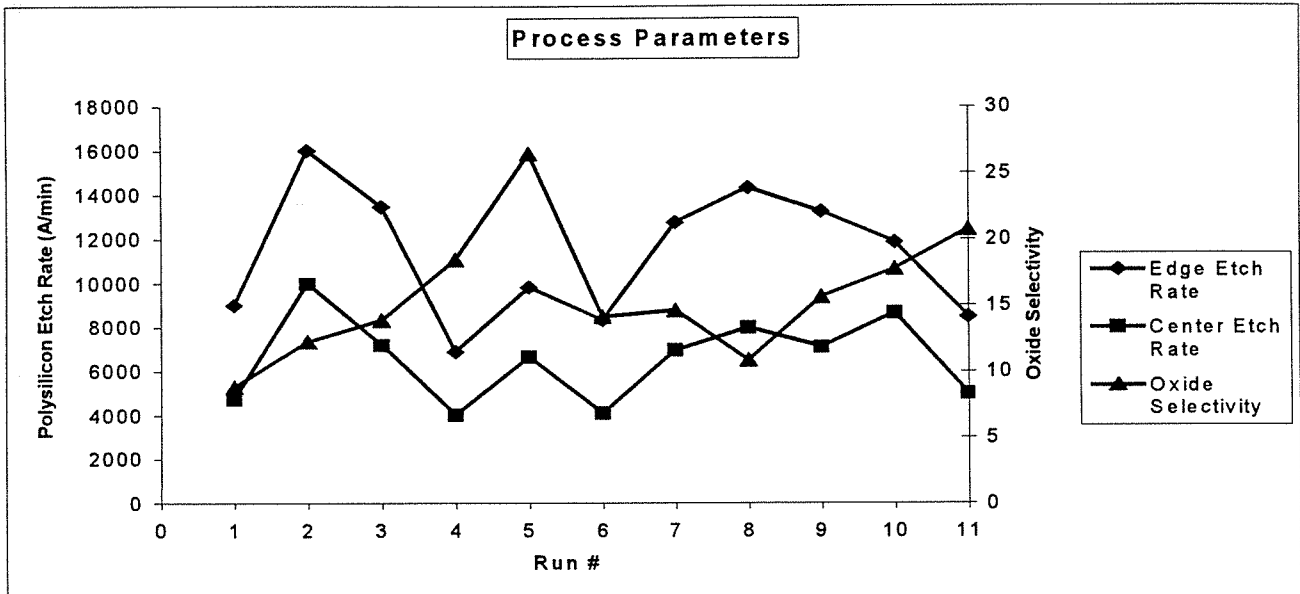
Shown in Figure 2 is a plot of the polysilicon etch rate, both edge and center, and the selectivity to SiO₂. It should be noted that photoresist loss for each experimental run was minimal, and those values are not reported in the results presented.

Figure 2 confirms the etch rate non-uniformity observed in Figure 1. The etch rate at the edges of the wafers was almost twice what it was at the center of the wafers. As mentioned earlier in this paper SF₆ plasmas can be non-uniform due to the formation of negative ions in the plasma. Another possible explanation for this non-uniformity is in the etch tool itself – it is a tool designed for 150mm wafers, and the wafers used in this experiment were 100mm.

From Figure 2 some general trends can be established. With a SF₆ flow of 70% and a pressure of 90mTorr, increasing the power from 200W to 350W caused an increase in edge etch rate of 20%, while the center etch rate decreased by 9%, and the SiO₂ selectivity decreased by 40%. With 70% SF₆ flow and 230mTorr pressure, a power increase from 200W to 350W caused edge etch rate to increase by 133%, center etch rate to increase by 148%, and selectivity to decrease by 34%.

In order to evaluate the anisotropy of each of the etch processes a Philips scanning electron microscope (SEM) was used to view cross sections of the samples. Each

Figure 2: Etch process results



sample was cleaved through the desired features, and then sputter coated with gold at a pressure of 100mTorr for 60 seconds. SEM micrographs are given in Figures 3 – 6.

Not every etch process underwent cross sectioning; only those that yielded relatively high polysilicon etch rates and high SiO_2 selectivities.

Figure 3: 100% SF_6 , 230mTorr, 200W

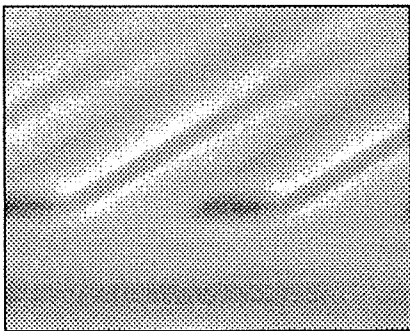


Figure 4: 70% SF_6 , 90mTorr, 350W

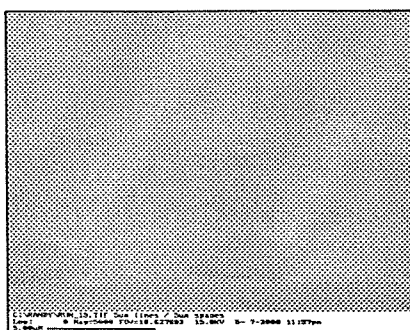


Figure 5: 85% SF_6 , 1600mTorr, 275W

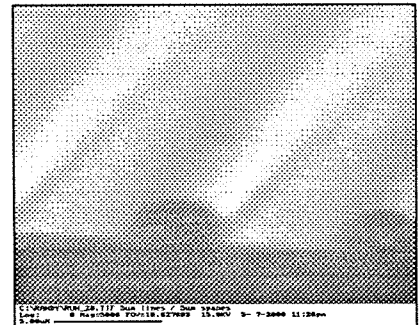
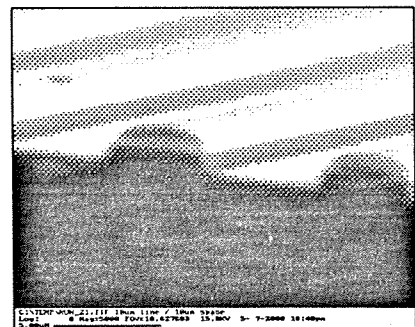


Figure 6: 70% SF_6 , 90mTorr, 200W



Although difficult to tell from the above SEM micrographs, there was significant undercutting of the process shown in Figure 3. There was a significant CD bias due to this undercutting. The same was observed for the process in Figure 4. For the process in Figure 5, no undercutting was observed. However, resist loss at the

edge of the line was significant, resulting in linewidth narrowing.

The process shown in Figure 6 (70% SF₆, 90mTorr pressure, 200W RF power) gave very anisotropic etching. The measured linewidth was 4.5μm for a 5μm line. Resist loss was minimal over the polysilicon line.

4. CONCLUSION

An investigation of polysilicon plasma etching was performed. The goal was to develop a process that had both a high polysilicon etch rate and high selectivity to SiO₂ and photoresist, while at the same time providing anisotropic etch profiles. A single process that met these requirements was not found; instead, two different processes were found.

The process that provided maximum anisotropy (see Fig. 6) used a SF₆ flow of 70%, pressure of 90mTorr, and RF power of 200W. The major drawback of this process was the disparity between center and edge etch rates. A 42 second etch, which would completely clear the polysilicon in the center of the wafer, would result in a 12 second over etch at the edges. This translates to a SiO₂ loss of 125Å.

The process that provided maximum selectivity (see Fig. 2) was run #5 (70% SF₆ flow, 230mTorr, 200W). This resulted in a 108Å SiO₂ loss at the edge of the wafer.

Future work for this experiment includes further study of process parameters around the optimal ones determined in this experiment. Further cross sectioning is needed to understand the anisotropy of the etch processes. Exploration of the etch non-uniformity is critical to developing an anisotropic, selective polysilicon dry etch process.

ACKNOWLEDGMENTS

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Randy E. Supczak, originally from Ware, MA, received the B.S. in Microelectronic Engineering from Rochester Institute of Technology in 2000. He obtained co-op experience from National Semiconductor in the thin films group, and at IBM Microelectronics in the embedded DRAM development group.