Design and Fabrication of Ring Gate Surface Junction Tunneling Devices

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Abstract—Silicon based ring gate surface junction tunneling devices (SJT) were studied due to their promise of incorporating quantum functional devices with integrated circuits. SJT devices of various gate lengths ranging from 1 μm to 50 μm were designed using Mentor Graphics tools, and were fabricated using standard CMOS processes on SIMOX substrates. SIMOX wafers were used to help reduce bulk leakage and enhance the drain impurity profile. SIMOX mesa isolation also significantly reduced the process flow.

1. INTRODUCTION

Recent advances microelectronic technology has reduced device gate lengths to 0.15 μm and below. At these dimensions, effects such as tunneling become significant. Current efforts to reduce these effects usually focus on minor modifications to materials and device structure. The surface junction tunneling device, on the other hand, attempts to utilize tunneling instead of overcoming it.

The silicon based SJT is a three terminal device that operates as a gated tunnel diode. As with other tunneling devices, the SJT exhibits a negative differential resistance (NDR) characteristic curve. Though the SJT differs from these compound semiconductor devices due to its silicon substrate and processing. The advantages over ordinary MOS devices are realized in its high speed and low power consumption.

Similar to a conventional n-channel MOSFET, the SJT employs a source, gate, and drain. The difference lies in the p+ doping of the drain. Applying sufficient positive gate bias will cause the channel to form a p+/n+ tunnel junction that is similar in principle to those studied by L. Esaki. While ordinary Esaki diodes will result in a single NDR curve under positive drain to source biasing, the SJT will result in a family of curves. This is due to the modulation of surface charge density with gate bias. As a result, the gate can control the tunnel current and negative resistance.

2. THEORY AND DESIGN

As mentioned, the SJT is similar in principle to an Esaki junction tunnel diode. Though the formation of the junction is controlled by the gate and can be characterized by ordinary device physics equations, the junction phenomena is identical to that of an Esaki diode.

When p+ and n+ regions are heavily doped to degeneracy, a very abrupt junction is formed and results in depletion layer of 10 nm or less. This depletion layer is the barrier through which the electrons tunnel.

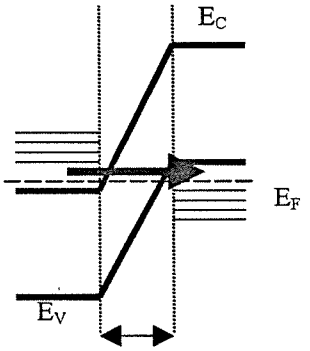


Figure 1: Band diagram for tunneling condition.

Figure 1 shows the band to band tunneling for the device in the forward biased condition. Band to band tunneling will occur as the drain bias is increased from zero volts. This will continue until a drain to source voltage is reached in which tunneling will no longer occur. At this point, termed the peak, the drain current begins to sharply fall off until it reaches a minimum, the valley. In this negative resistance region, the SJT derives its usefulness. Due to the relative ease of varying the drain voltage, the SJT has very fast switching speeds due to the short transit times for electrons across the tunnel barrier. The tunneling current density can be found using the following equation.

$$J_T = J_0 \exp\left\{\frac{-\pi\sqrt{\varepsilon_0}}{2\hbar q^{3/2}}\left(\frac{m^*}{N^*}\right)^{1/2} E_g\right\}$$

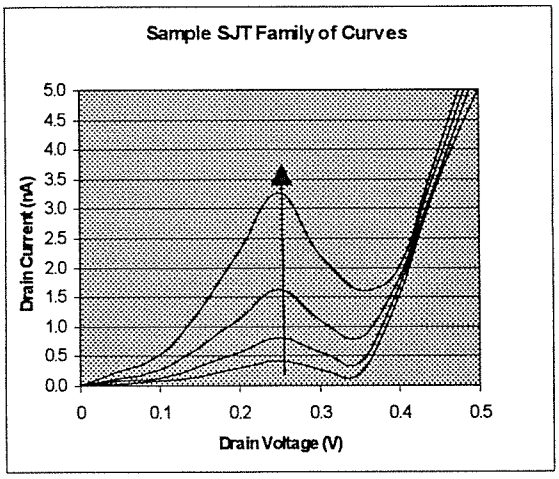


Figure 2: Expected STJ curves.

The ratio of the peak to valley current (PVCR) is controlled by the gate bias. Figure 2 shows how the PVCR is changed with increasing the gate to source voltage. Note that a zero bias is expected to give an ordinary p-n diode curve.

The design of the device is centered on defining the ring gate structure. Koga *et al* found that using a ring gate significantly reduces excess tunneling by eliminating corner [1]. Excess currents are undesirable because they tend to degrade the PVCR. This effect might be severe enough to completely cancel the NDR region. To avoid this possibility, the ring gate is used.

Implementing the combination of p+/n+ implants with the ring structure requires the use of two photolithography steps. After polysilicon is deposited, the outer structure of the ring must be defined. A n+ flood implant dopes the source, but the drain is masked by the poly. The next photo step is a dark field mask that defines the inner diameter of the ring. A p+ implant then creates the drain. These mask levels were designed using Mentor Graphics IC-Station component of Design Manager. The design process was the standard RITCMOS and the design rules were modified versions of the MOSIS rules.

3. FABRICATION

The device was fabricated using SIMOX silicon on insulator substrates. The prime reason for using SOI in this study was to simplify the process flow through the use of silicon mesa isolation. The use of SOI has also been found to enhance the drain impurity profile as well as reduce bulk leakage. The SOI wafers had approximately 300 nm of silicon on top of 350 nm of oxide. The use of the Nanospec and ellipsometer was not possible for measuring film thicknesses on the SOI substrates. The thickness of films was determined using dummy wafers. The process flow and procedure are shown in figure 3 and in the appendix, respectively.

4. RESULTS AND DISCUSSION

Testing of the completed SJT devices initially yielded no observable NDR characteristics or the expected diode curve for zero gate bias. These results were confirmed with more extensive testing. There were a few process issues that might have contributed to this.

The first issue is that there were difficulties with stepper overlay. Since the mask levels were designed from scratch, a stepper job needed to be created to handle the design. This includes the identifying the location of the alignment key. Though this was done, there was difficulty in adjusting for the mechanical error due to stepper. As a result, the misalignment rendered all but the largest devices inoperable.

Another issue is with the LTO deposition and etch. As a result of the inability to measure the thickness of films on the SOI wafer, the thicknesses had to be estimated from the films that were deposited on the dummy wafers. The six inch LPCVD tube using caged boats produced wafer to wafer thicknesses ranging from 3500 A to 5100A. This made it difficult to calculate and LTO deposition rate.

The wafers were etched in the GEC-Cell for 6min each, since a 20% over-etch is acceptable. It is possible that the plasma etched completely through the oxide and then through the silicon layer down to the buried oxide layer. This would account for the nano-amp noise that was experienced. Another related possibility is that the plasma did not completely clear the oxide. In both cases, the metal would be in contact with the oxide which would result in an open circuit.

5. CONCLUSION

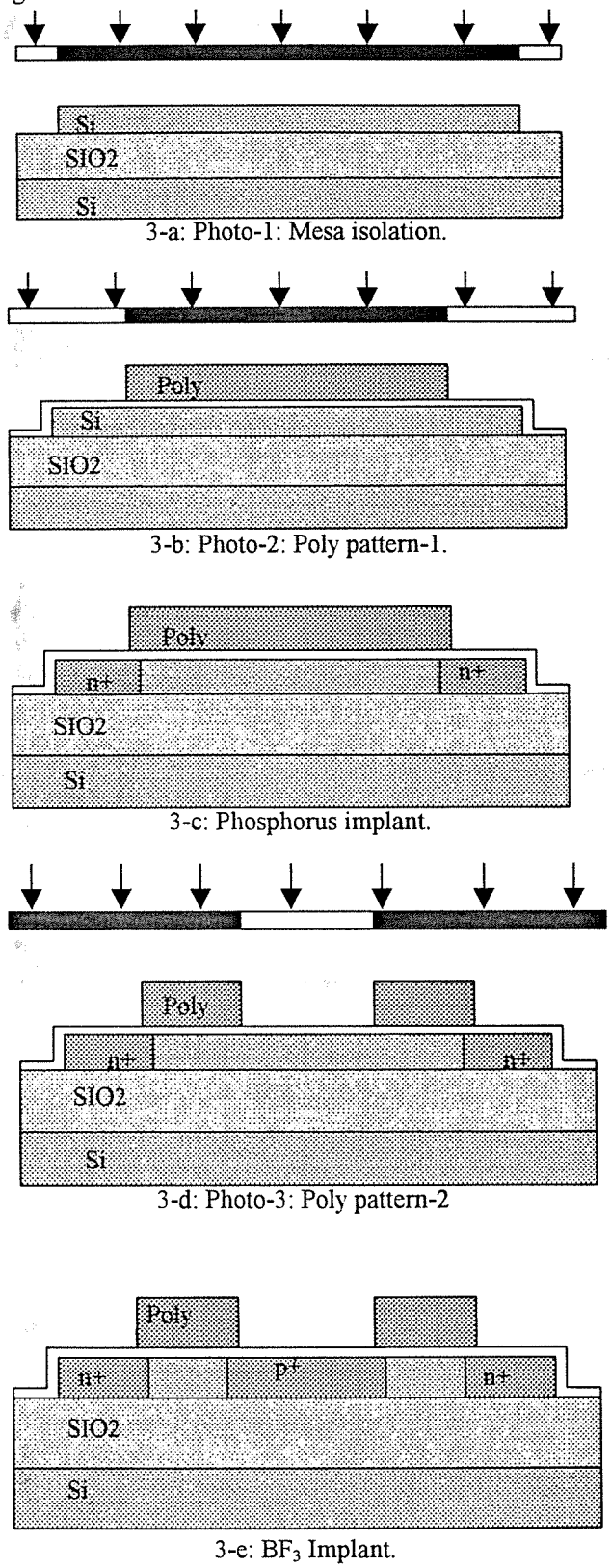
A silicon based quantum functional device, the surface junction tunneling device, was design and fabricated. Though devices displaying negative differential resistance and ordinary p-n junction characteristics were not observed, the desired results might be achieved with further study and modifications and improvements to the existing process. Further might will include modifications and simulations of implant profiles as well as modifying the LTO etch. The use of the new advanced RIT CMOS processes might also be considered

REFERENCES

[1] J. Koga and A. Toriumi, "Three-terminal silicon surface junction tunneling devices for room temperature operation," *IEEE Electron Device Lett.*, vol. 20, pp. 529-531, 1999.

[2] K. Chang, "Parametric and Tunnel Diodes", Prentice-Hall, NJ, pp. 31-48, 1964.

Figure 3: Process cross sections.



3-a: Photo-1: Mesa isolation.

3-b: Photo-2: Poly pattern-1.

3-c: Phosphorus implant.

3-d: Photo-3: Poly pattern-2

3-e: BF_3 Implant.

APPENDIX

A. Experimental Procedure

1. Scribe.
2. 4pt probe.
3. RCA clean.
4. Photo-1: Mesa isolation.
5. Etch Mesa: SF_6+O_2 42:7.5 sccm, 35sec, 400mT, 40W.
6. Ash resist: 45min
7. RCA clean.
8. GOX growth: Dry O_2 soak at 1000C for 25min.
9. Poly Deposition: 70min.
10. Photo-2: Poly pattern-1.
11. Etch Poly: SF_6+O_2 42:7.5 sccm, 45sec, 400mT, 40W.
12. Ash resist: 45min.
13. Implant Phosphorus 100keV and 1E15 dose.
14. Photo-3: Poly pattern-2.
15. Etch Poly: SF_6+O_2 42:7.5 sccm, 45sec, 400mT, 40W.
16. Implant BF_3 150keV and 1E15 dose.
17. Ash resist: 45min.
18. RCA clean.
19. Anneal D/S.
20. LTO deposition: target 5000 A.
21. Photo-4: Contact cuts.
22. Etch Contacts: 6min SF_6+CH_3, 50mT and 270mT.
23. Ash resist: 45min.
24. Pre-Metal clean.
25. Metal Deposition.
26. Photo-: Metal pattern.
27. Etch metal.
28. Ash resist: 45min.
29. Sinter.
30. Test.

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