MOSFETs with Variable Gate Oxide Thickness by Selective Nitrogen Ion Implantation

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Abstract- The incorporation of nitrogen in silicon has been shown to retard the oxidation growth rate. The present study produced aluminum gate PMOSFETs with varied gate oxide thickness on the same chip through selective nitrogen ion implantation. The nitrogen implant dose of $4x10^{14}$ ions/cm^2 at 35 keV prior to gate oxide growth reduced the oxidation rate between 10% and 60% at the oxidation schedules employed. This active area N-implant led to no degradation in electrical parameters such as gate delay, mobility, or subthreshold swing. MOSFETs with different gate oxide thicknesses allow for different threshold voltages on the same chip and increased non-minimum channel length MOSFET reliability.

I. INTRODUCTION

Current trends in industry are leading to system on a chip solutions. These solutions generally require varied devices to perform many different functions. The integration of different voltage bipolar junction transistors has been developed, but MOSFETs have not yet crossed this technological river, as MOSFET threshold voltage is primarily determined by the blanket processed gate oxide thickness and composition.

Gate oxide thickness is generally scaled down with channel length. This gate oxide thickness reduction leads to reliability issues associated with thin oxides. Nitrogen implantation in Si prior to oxidation has been shown to retard oxidation rate in thin oxide regime [1]. Selective nitrogen ion implantation would allow long channel MOSFETs devices to have thicker gate oxides than minimum length transistors on the same chip. This would lead to enhanced chip reliability. Direct thermal incorporation of nitrogen in gate oxide growth steps has been standard practice in industry for some time.

The nitrogen in the SiO_2 film improves dielectric strength, acts as an impurity diffusion inhibitor, and reduces hot-carrier effects in submicron MOSFETs [2]. Previous work examined the kinetics and reliability of N-implanted and Si-implanted SiO_2 gate dielectrics. Data showed increased dielectric strength and decreased thickness uniformity for N-implanted SiO_2 [3]. This study fabricated aluminum gate PMOSFETs with N-implanted gate oxides. The fabricated PMOSFETs have two different gate oxide thicknesses on each wafer. The standard RIT aluminum gate PMOS process was run on n-type wafers with resistivity in the range of 10-30 ohm cm. The standard process involves four photo steps namely Source/Drain, Active, Contact Cut, and Metal. An additional photo step to selectively block the nitrogen implant was introduced prior to gate oxide growth. Nitrogen was implanted at a dose of $4x10^{14}$ ions/cm^2 and at an energy of 35 keV. This energy and dose had been optimized by a previous study [4].

The gate oxide growth process resulted in a thickness differential between masked and unmasked active regions. The standard process grows a 700A thermal SiO_2 gate dielectric. This study grew thermal oxides between 55A and 675A. These results can be seen in Figure 1. Oxides were grown in dry oxygen between 900 and 1050 degrees Celsius for eight to thirty minutes. All oxide growth recipes included a nitrogen anneal ramp down cycle.

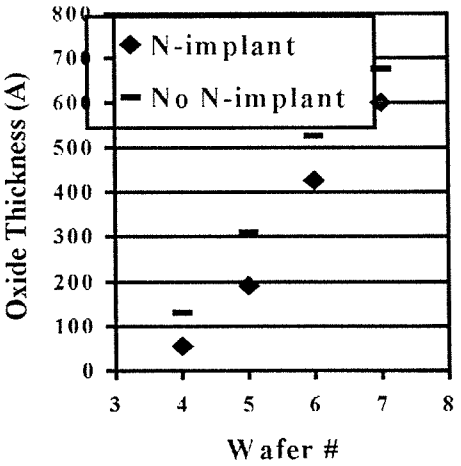

Figure 1. Oxide thickness obtained on un-implanted and N-implanted regions.

Following the gate oxide growth, the PMOS fabrication was completed with identical processing. The

devices were then tested using an HP4145 parameter analyzer.

3. RESULTS AND DISCUSSION

PMOS transistors with different threshold voltage magnitudes and transconductance have been realized on the same chip. The threshold voltage was found by extrapolating the x-intercept of the linear fit to the transfer characteristic- drain current versus gate voltage at a drain-source voltage of – 0.1 V as shown in Figure 2. The figure shows two distinctly different characteristics of the same size PMOS devices fabricated on each wafer

The threshold voltage of a PMOSFET is given by

$$V_t = \phi_{ms} - Q_{ss}/C_{ox} - |2\phi_f + 6\phi_t| - \sqrt{(2q\varepsilon_s N_D|2\phi_f + 6\phi_t|)}/C_{ox} \qquad (1)$$

Where ϕ_{ms} is the metal semiconductor work function difference, Q_{ss} is the oxide charge density in C/cm^2 associated with the SiO_2/Si interface, C_{ox} is the oxide capacitance in F/cm^2, ϕ_f is the Fermi potentials and ϕ_t is thermal potential, N_D is the substrate (channel) doping density. The magnitude of the threshold voltage varies almost linearly with the oxide thickness.

The slope of the threshold voltage versus oxide thickness plot can be written as

$$\text{Slope} = (\sqrt{(2q\varepsilon_S N_D|2\phi_f+6\phi_t|)} + Q_{ss}) / \varepsilon_{OX}$$

and the intercept on the y-axis gives the value of $\phi ms-|2\phi_f + 6\phi_t|$.

The experimentally observed threshold voltages have been plotted with the corresponding gate oxide thickness for un- implanted and nitrogen implanted devices in Figure 3. A fairly good linear fit to the data is obtained for both un-implanted and N-implanted devices. It can be observed that for lower substrate doping and lower oxide charge density, the threshold voltage is insensitive to the change in oxide thickness[3]. The wafers employed in the present study correspond to a doping density of $1.5X10^{14}$ cm^{-3}.

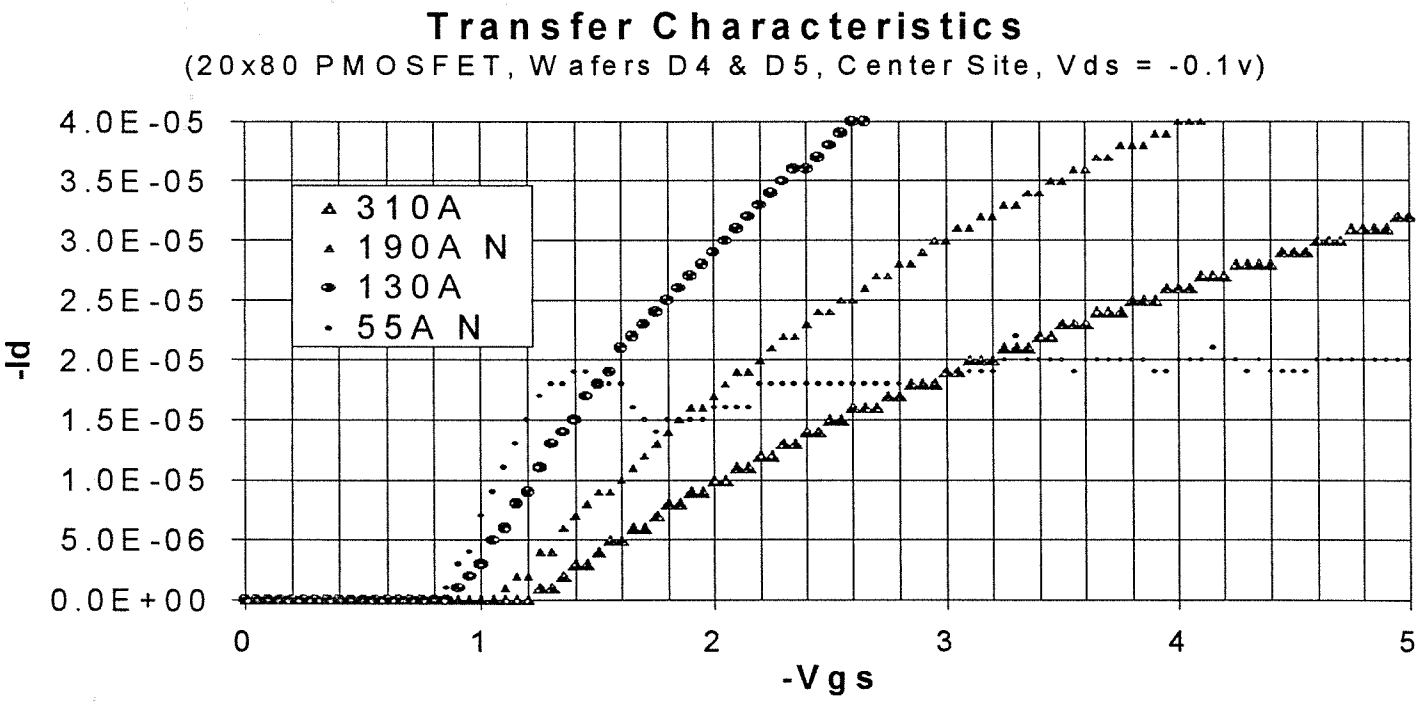

Figure 2. Drain current versus gate voltage for the drain-source voltage of -0.1V for identical size PMOS devices on the same wafer with different oxide thicknesses.

From the calculated data shown in Figure 4, it can be seen that at this doping level, the magnitude of the threshold voltage should be essentially independent of the gate oxide thickness. It is inferred that the slope observed in Figure 3 is primarily due to the presence of appreciable oxide charge density. SUPREM simulations show that the piling up of phosphorus at the SiO_2/Si interface at the substrate doping employed is not expected to a significant effect. Assuming the effect of oxide charges alone, an interface oxide charge density of $4X10^{11}$ q/cm^2 has been estimated.

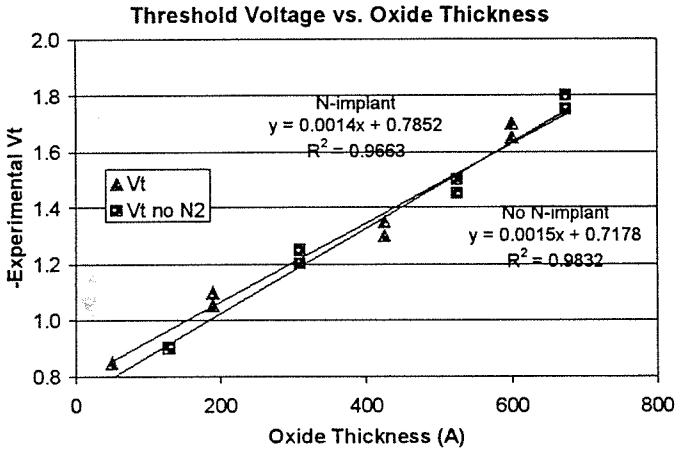

Figure 3. Threshold voltage versus gate oxide thickness

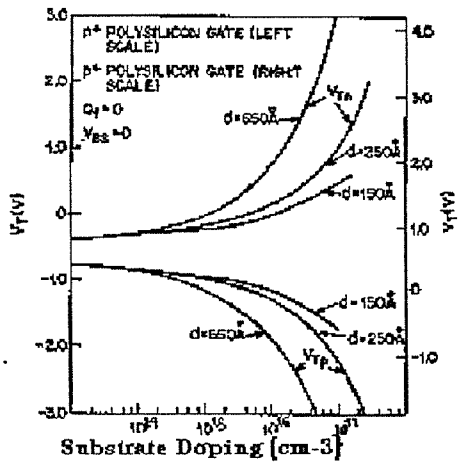

Figure 4. Calculated threshold as a function of substrate doping and oxide thickness (after Sze [3])

Detailed analysis of PMOS electrical characteristics did not resolve nitrogen implant induced variation in hole mobility, subthreshold swing, or gate delay as shown in Figures 5, 6, & 7.

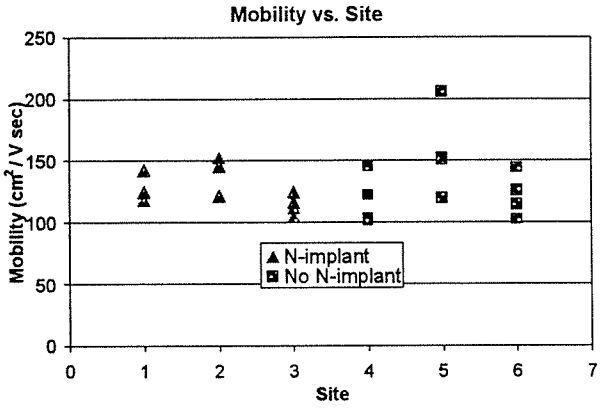

Figure 5. Calculated hole mobility of un-implanted and N-implanted devices

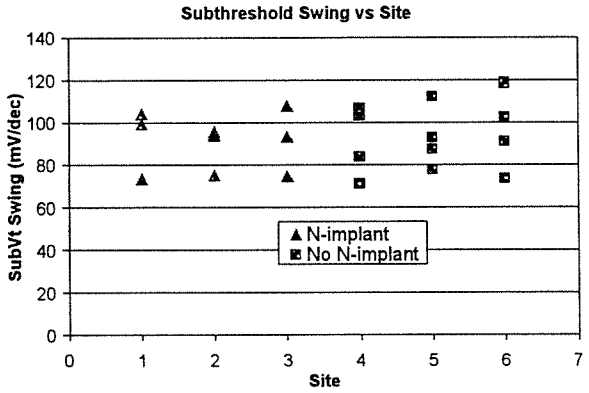

Figure 6. Subthreshold Swing for un-implanted and N-implanted devices.

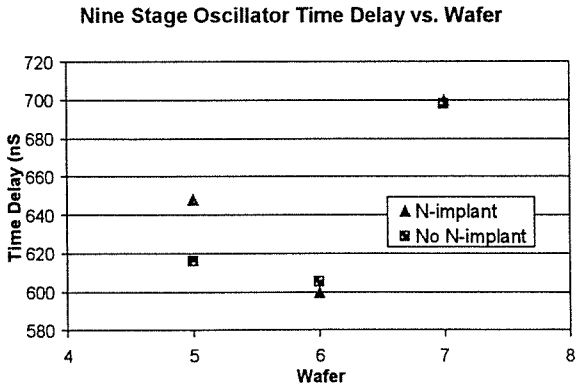

Figure 7. Ring oscillator time delay on both type devices.

4. CONCLUSION

Aluminum gate PMOSFETs with two different gate oxide thicknesses, threshold voltages, and transconductances were fabricated on the same chip. This selective nitrogen implant process gives the IC design team more device flexibility, and enhances non-minimum channel length MOSFET reliability. In addition, the RIT aluminum gate PMOS process has been shown to be effective with a gate oxide thickness down to about 10 nm.

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REFERENCES

1] L. J. Lopez, "Thin Gate Oxides Over Nitrogen Implanted Silicon," 15th Annual Microelectronic Conference, Rochester Institute of Technology, Rochester, NY 1997.

[2] H.R. Huff & C.A. Richter, "Ultrathin SiO_2 and High-K Materials for ULSI Gate Dielectrics," Materials Research Society, vol. 567, pp. 265-270, April 5-8, 1999.

[3] VLSI Technology, 2nd ed., S. M. Sze, McGraw-Hill

[4] S.K. Kurinec, M.A. Jackson, K.C. Capasso, Kent Zhuang and G. Braunstein, Mater. Res. Soc., Vol. 567, p. 299, 1999.