Tantalum Pentoxide Deposition and Applications

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Abstract—A Tantalum Pentoxide deposition by reactive sputtering was optimized on a CVC-601 sputterer and working MOS transistors were made using Tantalum Pentoxide. The target was an 8" pure Tantalum target. The optimization was done over a power range of 700 to 1700W DC and over an Oxygen flow of 15 to 35%. The optimal process from this study was at 1200W and an Oxygen flow of 15% or less. A standard PMOS process was modified to use Tantalum Pentoxide using the gate dielectric. The resulting transistors worked well.

1. INTRODUCTION

Tantalum pentoxide is a material that has received much attention from microelectronics researchers over the past few decades. The regions of interest have been its dielectric properties, its optical properties, and its chemical properties.[1] The high dielectric constant (typically in the range of 20 to 25) makes it desirable for capacitor and gate dielectrics as devices are scaled down to smaller and smaller dimensions. The high refractive index (greater than 2.0) have made it of interest for mirrors, waveguides, and other optical devices and structures. The chemical resistance it displays has seen it being used as etch barriers in various studies. Many different methods and combinations of methods, including thermal oxidization, anodization, chemical vapor deposition, and sputtering, have been used to deposit tantalum pentoxide.[2] The low temperature deposition and the ease of implementation of sputtering have made it the focus of this experiment. More specifically, the DC reactive sputtering of a tantalum target in a partial ambient of oxygen was explored and optimized for dielectric properties.

The optimization was performed on a CVC-601 operating in DC mode with an 8" tantalum target. Initial runs were made to establish a good design space before establishing the design. The design that was chosen was a central composite design (CCD) because it can detect quadratic effects and it has the spreads the design to five levels while maintaining a reasonable amount of runs. The parameters that were varied as factors in the CCD were power and percentage of oxygen flow (as compared to the total flow of argon and oxygen). The responses that were observed were breakdown voltage, leakage current, and dielectric constant. These were tested by making capacitors with the heavily doped p-type silicon substrate, the film, and aluminum. Other responses that were observed were film thickness and refractive index.

In addition to the design of experiments, MOS devices and capacitors for gallium arsenide were planned to be made and tested with the optimized film. For MOS devices, the higher dielectric constant of tantalum pentoxide could allow for smaller effective gate dielectric thicknesses than currently possible with silicon dioxide. An established MOS device process was used up to the gate oxidization. The tantalum pentoxide film was then deposited in place of the gate oxide. The processing continued with the addition of a CHF_3 RIE etch to pattern the contact cuts through the tantalum pentoxide film. The MOS devices were made in conjunction with Dave Rines' senior project. The resulting devices were made on wafers that had received a nitrogen implant on half of the wafer. This could potentially help reduce silicon dioxide formation at the interface between tantalum pentoxide and silicon. Capacitors are used on gallium arsenide substrates to supplement an control optoelectronic devices. For gallium arsenide, the processing temperature is limited because of the outgassing of arsenic. The sputtering of tantalum pentoxide has a low enough temperature to be compatible with gallium arsenide processing.[3] Tantalum pentoxide could reduce the area of the capacitors on these substrates.

2. DEPOSITION OPTIMIZATION PROCESS

The process that was to be used for the deposition was established before any of the DOE runs were done. The process started with 4" heavily doped p-type Silicon substrates. These substrates acted as the bottom electrode for the test capacitors. The Si substrates were dipped in buffered oxide etch (BOE) for 30s, DI rinsed and spin rinse dried (SRD) just before being put into the sputtering chamber. This was done to get rid of any native oxide. The sputterer was pumped down to the low 10^{-5} to high 10^{-6} Torr range. The CVC-601 was operated with a pulsed DC power supply set at the desired power. The heater was

Table 1. DOE settings

Run #	Power (W)	Oxygen flow (%)
1	846	17.9
2	1554	17.9
3	846	32.1
4	1554	32.1
5	700	25.0
6	1700	25.0
7	1200	15.0
8	1200	35.0
9	1200	25.0
10	1200	25.0

turned on during the run to help densify the film.[4] The substrates made a complete revolution around the chamber every 15s. The total gas flow of the Argon and Oxygen was held at 200sccm while the percentage of Oxygen was changed run to run. This equated to pressures of about 6.2mTorr. After everything was set up, a 10 minute presputter was done before the 30minute deposition. After the deposition was complete, the wafers were again dipped in BOE, rinsed, and dried before the Aluminum top electrode layer was sputtered. The a capacitor test mask was used to pattern the capacitors with a standard g-line photolithography process. The Aluminum was etched in heated Aluminum etch. The wafers were then stripped of the resist and SRDed. The backside Aluminum was then sputtered. No sintering step was used because there is evidence that the smaller metallic and semiconductor elements such as Si and Al diffuse into the Ta_2O_5 film and decrease the quality of the film.

3. TESTING

The film thickness and refractive index were measured after deposition with an ellipsometer. The dielectric constant, breakdown voltage, and the leakage current were measured in the test area after the devices were completed. All of the device testing was done on the smallest round capacitors, which were 100,000 microns square in area.

The capacitance of several devices on a wafer were measured on a CV analyzer. The capacitance, the area, and the film thickness were used to find the dielectric constant using the following equation.

$$\varepsilon_r = \frac{C \bullet t}{\varepsilon_0 \bullet A}$$

Where C is the capacitance, t is the film thickness, A is the area, ε_0 is the absolute dielectric permittivity, and ε_r is the relative dielectric permittivity or the dielectric constant.

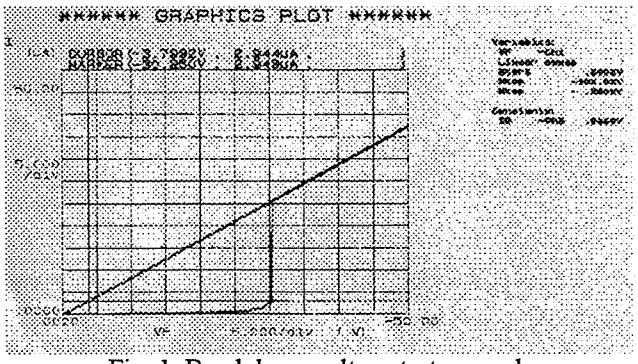

Fig. 1. Breakdown voltage test example

The breakdown voltage was found by using a series resistance with the capacitor. An HP4145 was used to ramp the voltage until the device broke. The resistor line was then appended to find out how much of the voltage at breakdown was handled by the capacitor as seen in Fig.1. The voltage was then divided by the film thickness to get the strength in terms of V/cm.

The leakage current was attempted to be measured in a similar method. The series resistance was left out though. This measurement produced no distinguishable leakage current above the noise in the testing system. The noise was on the order of pF's.

4. DOE RESULTS

The results from the testing are shown in Table 2. The leakage current was left out due to troubles with testing for it. This was a surprise due to the fact that film was expected to be very leaky. The breakdown voltages were higher than were expected, but the dielectric constants were lower than expected. The refractive index was in the expected range.

The results were analyzed with RS/1. From this analysis the peak breakdown voltage should be around

Table 2. DOE Results

Run #	t avg. (m)	ni avg.	ε_r	strength (V/cm)
1	7.74E-08	2.085	1.33E+01	5.49E+06
2	1.50E-07	2.036	1.75E+01	6.65E+06
3	7.20E-08	2.065	1.22E+01	7.08E+06
4	1.29E-07	2.072	1.52E+01	6.98E+06
5	6.26E-08	2.065	1.15E+01	6.43E+06
6	1.65E-07	1.939	1.88E+01	6.07E+06
7	1.16E-07	2.095	1.61E+01	7.83E+06
8	9.67E-08	2.09	1.35E+01	7.06E+06
9	1.03E-07	2.101	1.34E+01	7.79E+06
10	1.07E-07	2.092	1.59E+01	7.24E+06

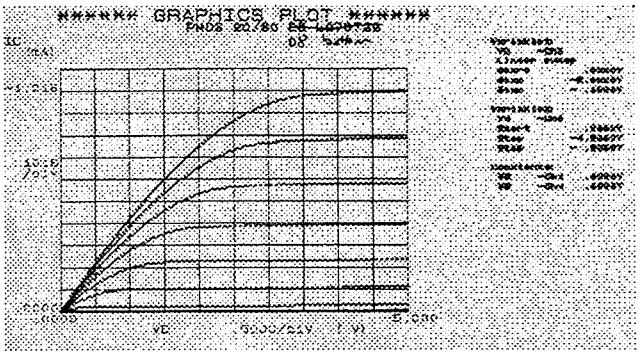

Fig. 2. Family of Curves plot

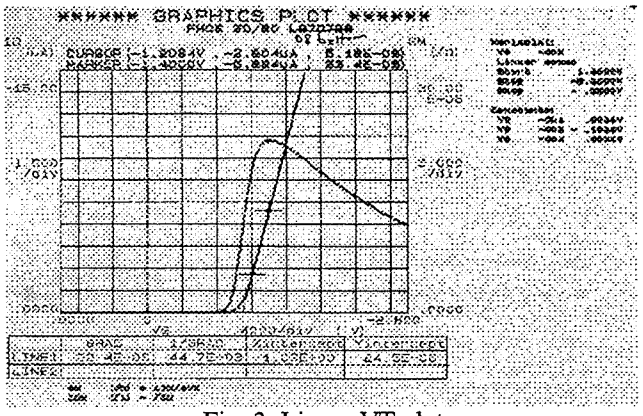

Fig. 3. Linear VT plot

1200W and the peak refractive index should be slightly below that. The analysis also showed the dielectric constant to be increasing with increasing power and decreasing oxygen flow. These both could be due to too much oxygen getting into the film with these settings. From these results the best film parameters would be 1200W and 115% or less flow of Oxygen

5. MOS APPLICATION

For the MOS devices, the film was deposited on wafers that had been implanted with Nitrogen on one half and processed up to the gate oxide step. On one wafer, a 420 Angstrom layer of Ta_2O_5 was deposited at 1200W and 25% Oxygen flow. The film was then annealed at 750C for 5 minutes in dry Oxygen in a furnace tube. The anneal was done to improve the film quality. Another wafer received an additional 80 Angstrom layer of Ta_2O_5 on top of the annealed layer to help prevent possible migration of Al during the sinter step.

Contact cuts were then etched through the Ta_2O_5 (after contact cut photolithography) in a CHF_3 RIE step. The RIE step was developed on a Drytek Quad Etcher from published papers to have a favorable selectivity to resist.[5] The gas flow was 50sccm and the power was 350W. The resulting etch rates were 150

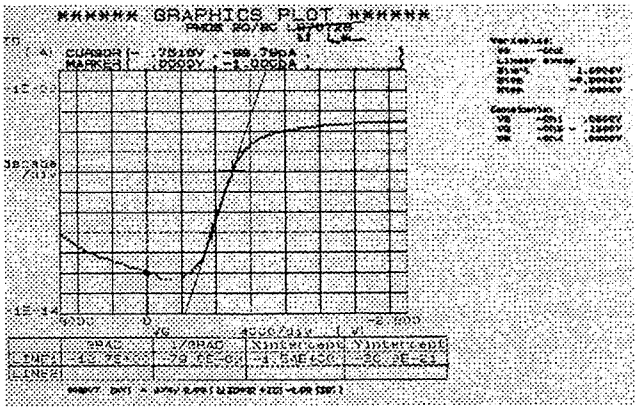

Fig. 4. Linear Subthreshold plot

Angstroms/minute for Ta_2O_5 and 200 Angstroms/minute for Shipley 812 positive resist.

After this step, the processing continued as normal. The resist was removed. The Aluminum was deposited, patterned, and sintered.

The devices were tested using the standard PMOS test setup with a wafer prober and an HP4145. Family of curves, linear VT, and linear subthreshold plots were made for both sides of each wafer. The general results showed higher gains and lower thresholds than the normal process. The nitrogen implanted sides actually had higher thresholds than the non implanted sides. This was opposite to the results that Dave Rines observed in his SiO_2 gate PMOS. A set of plots from the nitrogen implanted side of the wafer with a single layer of Ta_2O_5 can be seen in Fig. 2, 3, and 4. This set of devices was the only one that demonstrated the best subthreshold plot. The rest were mostly noisy at the leakage regime. The characteristics of these particular films were not tested so expected results for threshold could not be accurately calculated.

6. CONCLUSIONS

The development and optimization of the Tantalum Pentoxide deposition process was a success. The base process is now ready to be applied to future research and applications. The basic process is at 1200W and 15% Oxygen flow.

The demonstration of MOS devices with Tantalum Pentoxide as a gate dielectric was also successful. The devices worked well. The GaAs capacitors were not made however.

There is much room for future work with both the process and the applications. For the process, the Oxygen flow could be reduced even more to try to get better films. Other parameters such as pressure could also be varied to find better results. Anneal steps could also investigated as ways of improving the film quality For the MOS applications, thinner films and more exhaustive testing could be done, especially in regards to the nitrogen

implants. The GaAs capacitors could be made and tested. Optical applications and MEMs applications could be looked at as well.

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ACKNOWLEDGMENTS

The author acknowledges Dr. Santosh Kurinec guidance in this work, Dr. Mike Jackson for guidance in the deevice testing, Dave Rines for Nitrogen implanted PMOS wafers, and Rich Battaglia for the maintenance of and assistance with the CVC-601 sputterer.

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