

Silicon Based Light Emission

by

Avalanche Breakdown of Shallow p^+/n^+ Junctions

Peter I. Ritchie
Microelectronic Engineering
Rochester Institute of Technology
Rochester, NY 14623

Abstract—The objective of this study was to develop and demonstrate a technology for producing optical signals on a VLSI chip using only standard silicon processing techniques. The design of the process requires shallow p^+/n^+ junctions to minimize the high absorption inherent in silicon for $\lambda < 850\text{nm}$ and to obtain low reversed biased voltages for avalanche breakdown of the p^+/n^+ -junction due to impact-ionization. The effects of doping and device geometry on the visible luminescence of reverse biased Si p^+/n^+ junction diodes has been investigated. Each diode designed has a unique design incorporating sharp edges that promote high fields that aid the onset of break down. The p^+ -doping was varied while other processing parameters were held constant. All vertical junction diodes had excellent diode characteristics but no light emission was observed. Lateral junction diodes had typical reverse breakdown voltages of between 6 and 7 volts while certain devices of set geometry broke down rather sharply at 4 volts with light emission. Intensity and breakdown characteristics seemed to correlate with magnitude of p^+ dose and device geometry.

I. INTRODUCTION

The use of Silicon light emitting structures promises to be a strong contender in the future as an effective electro-optical source in opto-electronic integrated circuitry. This study is the collaboration between Dr. David V. Kerns of Vanderbilt and RIT. In the past the intensity obtained was typically low with quantum conversion efficiencies of 5×10^{-8} [1,2]. Because of the high absorption coefficient for wavelengths below 850nm it is not surprising that intensity of visible light in this range suffers. This study and others that have preceded it minimize light absorption by optimizing the device design [3]. Here in this study both co-planar controlled and electric field confinement devices were fabricated to assist in increasing quantum conversion efficiencies. On going challenges for integrating these devices into CMOS technology are: (1) increasing the adaptability of device design and fabrication procedures for

standard bipolar or CMOS processes, (2) increasing both the electrical-to-optical power and quantum conversion efficiencies associated with silicon LED's, (3) increasing the lateral uniformity in emissions from LED's surfaces, especially the avalanche-type diodes, and (4) lowering the operating voltages and currents associated with these diodes [4].

II. FABRICATON

The device wafers were n-type (100) silicon with an average resistivity of $5.71\Omega\text{-cm}$. Of the 13 wafers, 10 were allocated for device wafers and 3 were used as control wafers. The 10 wafers were scribed: PR1-10 and the control wafers were scribed: D1-3.

An implant with Phosphorus at a dose of $3 \times 10^{14} \text{ P}_3$ ions/ cm^2 with an energy of 100kev followed n^+ lithography for all wafers. Wafer PR-10 was chosen for a blanket implant of 4 different doses, each occupying one quarter of the wafer surface. Supreme-3 simulations gave junction depths of $x_j = 0.294, 0.325, 0.349$ and $0.370\mu\text{m}$ for the doses: 4,5,6 and $7 \times 10^{15} \text{ BF}_2$ ions/ cm^2 respectively. Actual junction depths for these for doses were: $x_j = 0.345, 0.299, 0.409$ and $0.449\mu\text{m}$ respectively and were obtained using the "groove and stain" technique. Surface concentrations ranged between 1.9×10^{20} to $2.8 \times 10^{20} \text{ BF}_2$ ions/ cm^3 .

During the p^+ implant it was found that the lateral devices received insufficient dopant through a large oxide of about 2600 Å. This necessitated a split in the device wafers so that lateral devices could be recovered. The split consisted of wafers D1, PR-1,3,5 and 7 for continued processing for vertical diodes and was designated "lot-1." Wafers D2, PR-2,4,6 and 8 were called "lot-2" and re-worked by etching the oxide over the p^+ regions for the vertical and lateral structures. These vertical regions experienced a second implant since they originally received p^+ dopant through a masking oxide of about 980 Å designed to help achieve a more shallow junction. While etching the oxide it was found that since BF_2 was present the etch rate decreased

from the normal rate of 900 Å/min. down to 180 Å/min.. Initially the etch was done in a buffered oxide etch (BOE) which after the second p⁺ implant and resist ash was found to be severely over etched. An RIE etch would have been more appropriate for removing this oxide since it is highly an-isotropic. The doses and energy determined in Supreme-3 were: 7×10^{14} , 1×10^{15} , 3×10^{15} and 4×10^{15} BF₂ ions/cm² at an energy of 120keV. For the anneal a wet oxide was used since no oxide was present for contact isolation and was best in this case to keep the implant from being driven in too deep.

Both lots next received contact cut lithography and since BF₂ was present an RIE etch was used. The gases used were: 25 sccm CF₄, 10 sccm CHF₃ and 80 sccm of Argon with power and pressure set at 100 watts and 200 mT respectively. The masking resist was then removed in a Plasma-line asher for 50 minutes then RCA cleaned. An HF dip was included to help reduce residual oxide before sputtering of the alloy Al/Si in the CVC601 sputter tool. The sputter was done in an Argon ambient with a base pressure of 1.4×10^{-5} Torr. A pre-sputter was done before the actual sputter to help reduce any contaminants that might have been present on the Al/Si target. An average aluminum thickness of 0.887µm was measured using the Tencor "alpha step" tool.

Finally photo level four for metal patterning was done. This step was followed by an aluminum etch. The etch time was approximately 1.5 minutes per wafer. A sinter at 450 Celsius in H₂N₂ was done to help improve ohmic contact and the 1% silicon in the aluminum helps to alleviate migration of silicon into the aluminum that can cause spiking and eventual shorting at the junctions. The following page shows the device chip.

III. RESULTS

All testing was performed using an HP4145, probe station and voltage source. Lot 1 was tested for vertical device behavior. All I-V curves were very symmetric with a reverse breakdown voltage (V_{BR}) of 3 volts and forward turn on voltage (V_F) of about 3 volts. These devices emitted no light. Both forward and reverse characteristics were sharp, showing no sign of series resistance.

Lateral devices from lot 2 gave good results. All devices that had an I-V curve also emitted light. Wafers tested from this lot were PR-2,4,6 and 8 with doses: 7×10^{14} , 1×10^{15} , 3×10^{15} , and 4×10^{15} BF₂ ions/cm² respectively. Table 1 shows a summary of light emission observed by dose and device geometry. It is clear from table 1 that in the F-series of devices F5-9 emitted light across all 4 doses tested. This is no surprise since these devices are virtually identical in geometry and are the simplest in design. They are constructed such that the p⁺ material lies in a circular

plain surrounded by an n⁺ ring concentric around the p⁺ material. Under reverse bias light was first seen around the aluminum contact over the n⁺ ring at 7.5 volts and 10mA for the lowest dose and was 6 volts for the highest. The light observed extended through the whole circumference as the current exceeded 20mA at 12 volts regardless of dose. Series resistance in the reverse characteristic was observed to be worst with lower dose. Considerable improvement in the lack of series resistance was observed in the same device at the highest dose of 4×10^{15} BF₂ ions/cm². All devices had a V_F of between 2.5-3 volts with the exception of device D8, which had a V_F of about 1 volt and only functioned on the wafer with the highest dose. Device D8 had very sharp forward and reverse characteristics and its geometry consisted of three rows of sharp zig-zag like p⁺ structures centered across a square n⁺ plain. Devices F1-4 only functioned and emitted light at the highest dose tested with the exception of F3, which also functioned on the third highest dose of 1×10^{15} BF₂ ions/cm². Device F3 is made up of a crescent shape n⁺ region over a circular p⁺ region. When under reverse bias the crescent shape was highly defined by the outline of a bright yellow/orange luminescence. Device F4 also showed bright light defined by its coil like n⁺ structure concentric about a p⁺ circular plain.

The second best series of devices tested that emitted light was the E-series. E5 and E6 emitted light over all doses. Their geometry resembles two sine like patterns superimposed over each other running 180 degrees out of phase, each pattern being of opposite doping. There are three rows in this pattern and when under reverse bias a grid of pin point light is seen through the microscope and is well defined. Again all operating characteristics are the same as that described for the F-series.

All the C-series devices failed to operate and it is not understood why at this time. Their geometry is not unlike that described above for the D-series devices.

The lowest breakdown voltage of less than 5 volts was observed in one device among the B-series. Device B1 is made up of n⁺ wedge shapes placed concentrically over a circular p⁺ plain. Although it had the lowest V_{BR} its light emission was rather weak and the device could not withstand currents above 30mA at 15 volts where as all the other devices could be reversed biased as high as 30 volts at 200mA before failure occurred. See figure 2 and 5 for device B1 and its matching I-V curve. Figures 3 and 4 show a typical device E3 and its I-V curve. Devices like E3 and B1 are good examples of a field confinement type devices. An electric field confinement was created at the p⁺n tips when biased.

Table 1: Light emission observed by dose and device geometry.

* = Breakdown is ≤ 5.0 volts ♦ = Light Observed for Wafer Id. PR-2, Dose = 7×10^{14} BF ₂ ions/cm ² ♥ = Light Observed for Wafer Id. PR-4, Dose = 1×10^{15} BF ₂ ions/cm ² ♦ = Light Observed for Wafer Id. PR-6, Dose = 3×10^{15} BF ₂ ions/cm ² ♦ = Light Observed for Wafer Id. PR-8, Dose = 4×10^{15} BF ₂ ions/cm ² A1.....F9 = Device Types.								
A1	A2	A3	A4	A5	A6	A7	A8	A9
B1 ♦ ♦ ♦	B2 ♦	B3 ♥	B4 ♥ ♦ ♦	B5	B6	B7 ♦	B8	B9 ♦
C1	C2	C3	C4	C5	C6	C7	C8	C9
D1	D2	D3	D4	D5	D6	D7	D8 ♦	D9
E1 ♥	E2	E3 ♥ ♦	E4	E5 ♥ ♦ ♦ ♦	E6 ♥ ♦ ♦ ♦	E7	E8	E9
F1 ♦	F2 ♦	F3 ♥ ♦	F4 ♦	F5 ♥ ♦ ♦ ♦	F6 ♥ ♦ ♦ ♦	F7 ♥ ♦ ♦ ♦	F8 ♥ ♦ ♦ ♦	F9 ♥ ♦ ♦ ♦

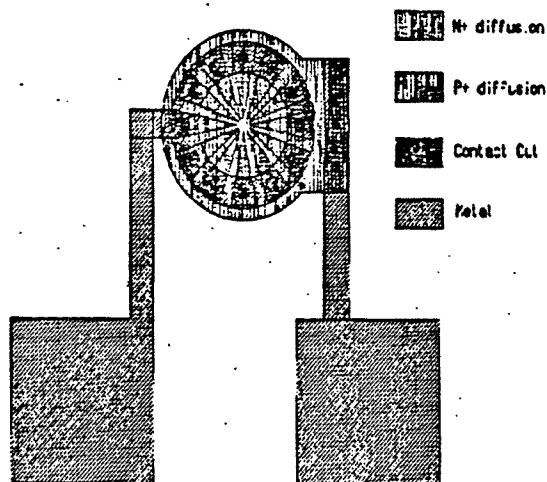


Figure 2 Device B1

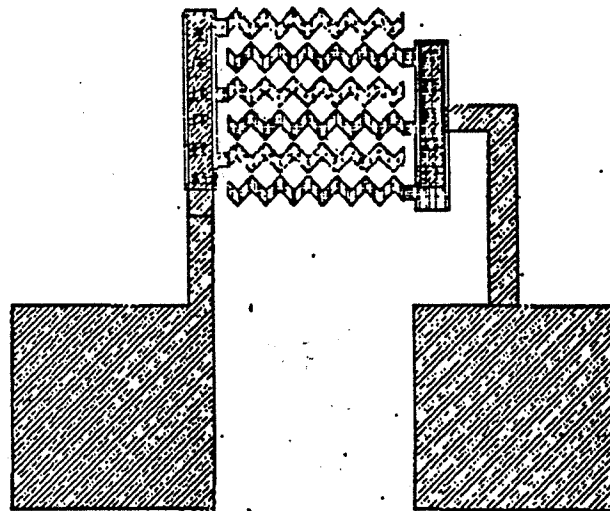


Figure 3: Device E3

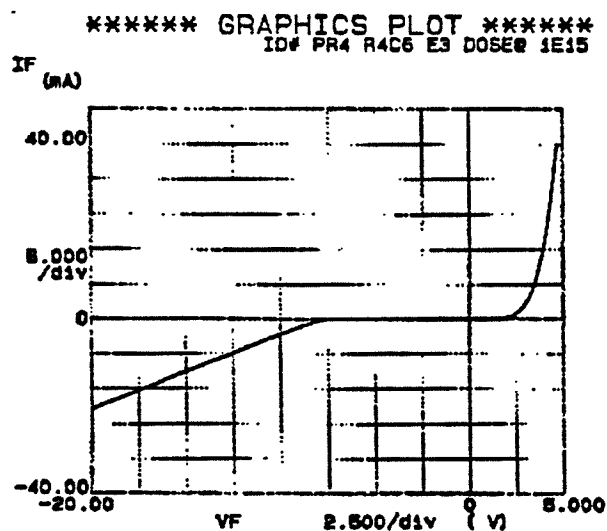


Figure 4: Characteristic curve for device E3

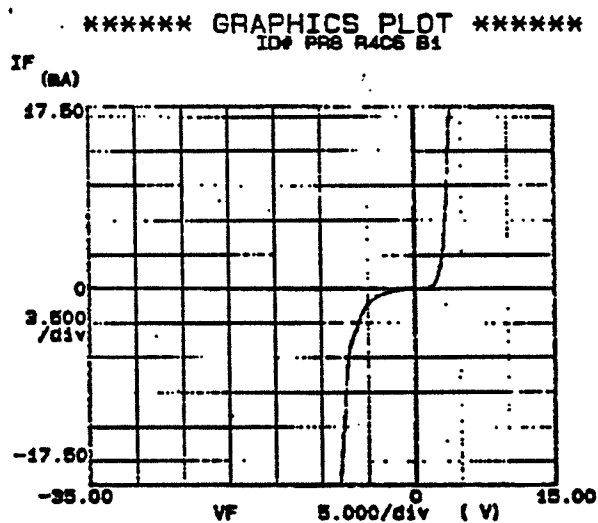
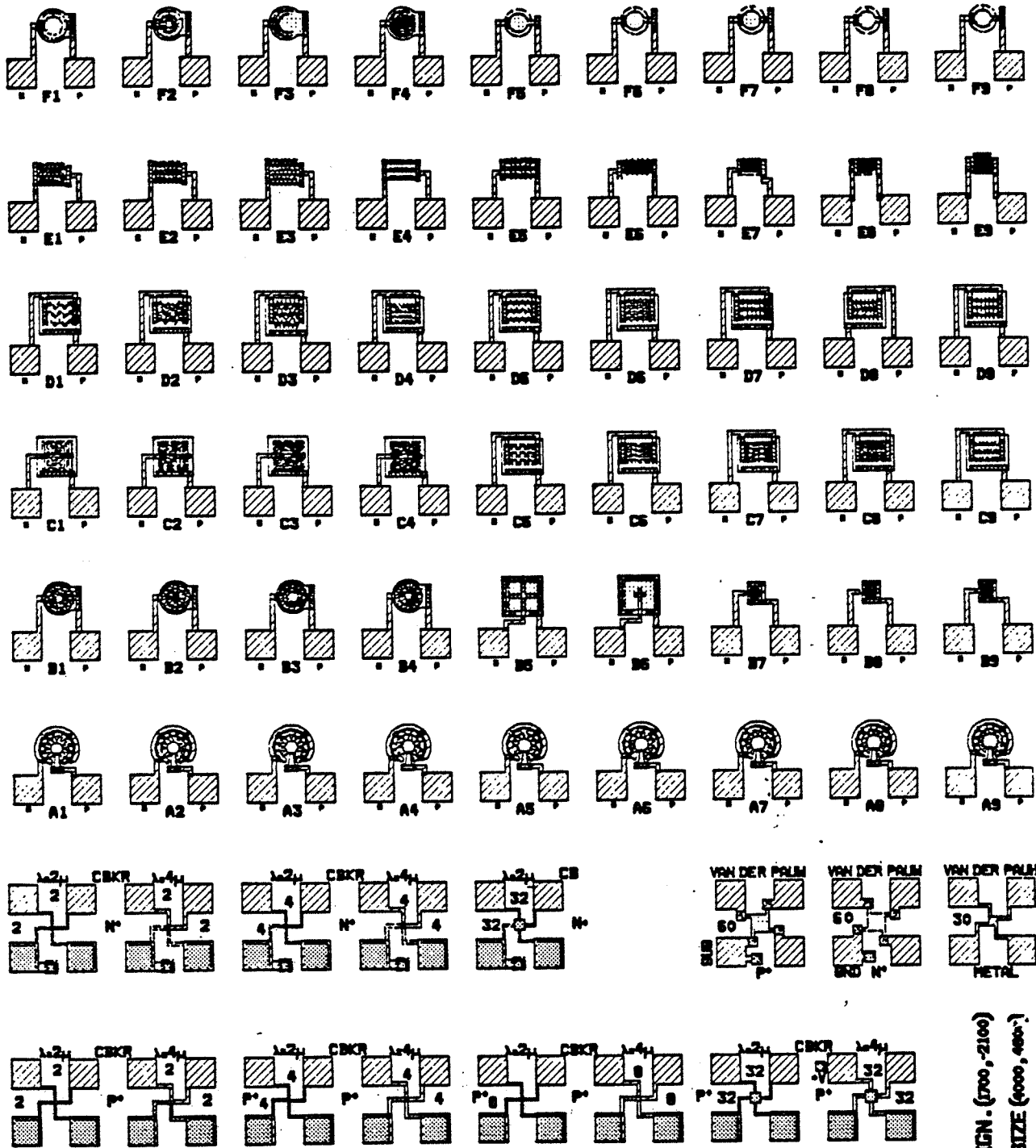
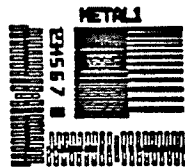
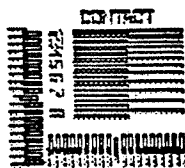
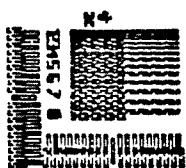


Figure 5: Characteristic curve for device B1



ALIGN - (700, 2100)
SIZE (4000, 4000)



VANDERBILT
UNIVERSITY



P-N AVALANCHE ELECTROLUMINESCENCE



IV. SUMMARY

The objectives of observing light under relatively low reverse bias voltages and low currents was realized. It was found that higher doses most likely are of interest for field confinement type devices. Co-planar surface devices such as in the F and higher E series devices worked over a wider dose range. Geometry is important but process technique and materials is a key factor in achieving devices that can be integrated into the CMOS process. Of principle importance is the quantum efficiency and photonic yield that results from silicon light emitting structures. These parameters are important in that they help to determine the viability of these devices as electro-optical sources to be used in opto-electronic integrated circuitry.

REFERENCES

- [1] P. Van Driehhuizen, "Optocoupler based on the avalanche emission in Silicon", Sensors and Actuators A, 31,229-240, 1992.
- [2] J. Kramer et al, "Light Emitting devices in industrial CMOS technology", Sensors and Actuators A, 37-38, 527-553, 1993.
- [3] Lukas W. Snyman, "Practical Silicon LED's with Standard CMOS technology", Southeast Conference 98 Orlando Florida, 1998.
- [4] Lukas W. Snyman, "Increasing efficiency of Silicon light-emitting diodes in a standard 1.2um CMOS technology", Optical Engineering, 1998.

ACKNOWLEDGMENTS

The author would like to thank Prof. D.V. Kerns, Jr. of Vanderbilt University for his guidance and support. Special thanks are due to George Lungu for chip design and other help. The help and support from all RIT clean room technicians, especially Richard Battaglia and David Yackoff is highly appreciated. The author acknowledges the advice of Dr. Santosh Kurinec for the project, Dr. Karl Hirschman, Dr. Mike Jackson, Dr. Richard Lane, Dr. Lynn Fuller and the staff of Advanced Vision Technologies, Inc. for their valuable input. Finally, the author is grateful to Dr. Renan Turkman for providing mentorship throughout his studies.

Peter I. Ritchie, originally from Rochester, NY, received B.S. in Microelectronic Engineering from Rochester Institute of Technology in 1999. He attained internships at Quantum Corp. and Intel Corp.