Investigation of a Silicon Bulk Etched Incandescent Light Source

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Abstract - An attempt of fabricating an incandescent light source was made at Rochester Institute of Technology. Filament length, width, material and shape as well as encapsulation method were under investigation in the experiment. Due to a design flaw, the devices could not be tested for functionality. This has since been fixed and another attempt will be made to fabricate the devices.

PURPOSE

For many years, methods of producing light from a silicon wafer have been investigated. These methods have included trying to make LED's, using Porous silicon but few have succeeded. With the radical change in thinking brought about with the fabrication of Microelectromechanical devices (MEMs), a new method has been realized. Using a sacrificial oxide layer covered with silicon nitride, a hollow cavity can be created. If a metal or polysilicon line is run through this cavity, then it may be possible to produce an incandescent light source. This source is a way of integrating a light source with standard CMOS processes. This may lead to the advent of optoelectrical circuits at an integrated circuit level. If such devices can be fabricated the speed of circuits may increase dramatically, since the limiting factor would be the speed the light can travel through a medium.

EXPERIMENTAL DESIGN

This experiment investigated the light emission from polysilicon and tungsten lines spanning the cavity. It also investigated the effects of filament length, width, shape, and encapsulation method.

The structure depicted in Figures 1 and 2 were fabricated in the lab at RIT. Figure 1, shows the final cross-section of the encapsulated filament sealed at a pressure of 5mT. The metal lines will be comprised of either silicon or tungsten depending on the run. The length of the filament will be varied at 300, 400 and 500μm while the width is varied at 5 and 10μm. Filaments will also be created that have a 90° bend in them but are identical in every other aspect.

Since the filament is coated with silicon nitride, it may not be necessary to encapsulate the filament with a vacuum. Therefore, a second process flow was investigated which will not enclose the filament inside mini-chamber. The cross-section is depicted in Figure 2.

PROCESS FLOW

The following section will describe the processes which were used to fabricate the devices. All processing was done starting with <100> silicon wafers.

The first step is to grow a 1500Å silicon nitride film. This film will be used to protect the silicon substrate during subsequent processing. It is important that this layer is low in stress so that it will not fracture and crack during later thermal steps. The nitride was grown with the following recipe.

Parameter	Setpoint
Temperature	800°C
Gas(es)	SiH_2Cl_2/NH_3
Flow(s)	60/150sccm
Pressure	430 mT

Table 1 : Nitride CVD process

The nitride is patterned and etched by reactive ion etching chamber using the recipe given in Table 2. The resulting cross section is shown in Figure 3 in the appendix.

Parameter	Setpoint
Power	50 W
Gas(es)	SF_6
Flow(s)	30 sccm
Pressure	300 mT

Table 2 : Nitride etch process

Following the Nitride etch, the first sacrificial oxide layer is grown. This oxide layer should be 1μm thick. This thickness was chosen so that the filament will be free standing. The process used to grow this oxide is shown in Table 3.

Parameter	Setpoint
Push/Pull	800°C
Ramp up	30Min
Soak	1100°C/210Min
Ambient	Wet O_2
Ramp Down	60Min

Table 3 : Sacrificial Oxide process

Following the oxide growth, a second nitride layer is grown on top if it. This nitride layer is deposited under the same conditions as the previous one. This layer is going to be the bottom layer of the protective coating surrounding the filament. Figure 4 show the resulting cross sections.

The next step is to deposit a metal layer to be used as a filament. This experiment used both polysilicon and a titanium/tungsten alloy as the filament. The polysilicon was grown under the following conditions.

Parameter	Setpoint
Temperature	600°C
Gas(es)	SiH_4
Flow(s)	90 sccm
Pressure	350mT

Table 4 : Polysilicon CVD process

The poly should be doped p-type using a spin on dopant. The boron was driven into the poly for 10 min at 1050°C in Wet O_2. The resulting sheet resistance should be approximately50 Ω/square.

The TiW film was deposited at CVC products using the recipe in Table 5. The resulting film thickness was approximately 2000Å and had a sheet resistance of 3Ω/square.

Parameter	Setpoint
Target Power	600 W
Gas(es)	Ar
Flow(s)	70 sccm
Pressure	5mT
Bias Power	0W
Target - Wafer Distance	2.0"

Table 5 : TiW Sputter process

Following the deposition of the metal film, the filament pattern should be etched using the process in Table 6. Both the polysilicon and the TiW films will be etched using the same process.

Parameter	Setpoint
Power	50 W
Gas(es)	SF_6
Flow(s)	42 sccm
Pressure	300 mT

Table 6 : Metal etch process

Following the metal etch process, a third nitride layer is deposited. This layer is repeat of the first two processes and it will act as the top filament protective layer. The cross sections in Figure 5 show the device at this stage of processing.

After the nitride is grown, the wafers are again patterned and the nitride is etched off. This will expose the sacrificial oxide under the filament but will leave the metal filament isolated from the outside world (see Figure 6).

At this point, a 3μm Oxide is grown on the wafer. This is done using a Tetra-ethyl-ortho-silicate(TEOS) process. This layer will act as a top sacrificial layer and will help suspend the filament inside the mini-chamber.(see Figure 7).

After the oxide is grown, the wafer must be patterned and etched. This etch will provide an anchor hole for the nitride cap layer. After the etch is done, a capping nitride layer is deposited. This layer needs to be thick enough to preserve the vacuum integrity of the device. On average, the thickness should be on the order of 2-3μm(See Figure 8).

The capping nitride must then be patterned and etched with holes in which the sacrificial oxide can be etched. Once the holes are etched in the capping nitride, the wafers are placed in a Buffered Oxide Etch(BOE) solution that will remove the sacrificial oxide layers. The etch rate of the BOE is on the order of 1000Å/min so the wafers need to be left in the solution for a few hours so that all of the oxide can be removed. Following the BOE etch the wafers are places in a KOH etch solution. This solution is a 20% by weight solution at 75°C. This solution will etch the silicon substrate in a V shape. This V shape will redirect any light that is emitted down and shine it to the surface (See Figure 9).

The next step is sputter Aluminum. This time the aluminum will be used for two purposes. The obvious reason is to create a good electrical contact to the filament. The second reason is to seal the cavity underneath the capping nitride. When the aluminum seals the cavity, the pressure inside the cavity will be the same as the pressure at which the Aluminum is sputtered (see Figure 10).

Finally the Aluminum should be patterned and etched. The final cross sections are shown in Figure 11. After the Al is etched, the devices can be tested by attaching a power source to either side of the filament.

PROCESSING ISSUES

Quite a few issues were come across while trying to fabricate the device. One of the biggest issues is that the time allowance to fabricate this device was short. The proper attention could not be paid to each of the individual processes. In many cases, the previous work was used as a basis for these processes but there were a few that there had been no previous testing.

For instance, there had been no interest in optimizing a dry etch process for TIW. There had been some work with TIW but it was all for CMP related research. A process was found in some papers and it was utilized at RIT. Wafers were not available at the time to check the process prior to the need for it. This caused an issue in and of itself. When the TIW was etched (to define the filament) there was shadowing around the features. In other words,

the nitride around the edges of the features was etching as well so the features were not as defined as they should be.

In the process of modifying the stepper program, the offsets were changed by 1mm. This made the overlay between levels shift by 2mm. This took several days to pinpoint the problem and correct it. Once the source of the problem was found it was easy to correct but the time table in which to complete the processing grew even tighter.

The final and most crucial issue came when the protective layer was to be etched. The etch was designed to remove approximately 4000Å of nitride. This would have etched the nitride back down to the sacrificial oxide layer. However, when this etch was done the probe contacts were not protected with photoresist. Therefore, the process etched the 1500Å of nitride on top of the filament and then it etched through the metal filament back down to the underlying nitride layer. Due to this process miscalculation, the device could not be manufactured beyond this point since there was no way to test the filament. At the time the mask was designed, the etching chemistry was not known. Therefore, this level was designed improperly.

CONCLUSIONS

Several important things can be learned from this project. First of all, never trust other people to leave your recipes alone. Somehow, the stepper recipe was tampered with which caused a major delay in processing. The fix was simple but the downtime could have seriously impeded the research.

The second lesson learned was that recipes that are proven in other labs do not necessarily transfer to this one exactly. Some monitor wafers should have been coated with TIW along with the device wafers. This would have enabled the process to be optimized prior to the etching of the device wafers. Therefor any harmful side effects resulting from the shadowing would be eliminated.

Finally, the use of an etch stop is extremely important. If an etch stop was used surrounding the metal filament then the etching of the contact pads could have been prevented. There would need to have a slight process modification, which would be to deposit a low temperature oxide (LTO) just prior to the metal for the filament. After the filament is etched then the etch stop should be deposited again. This would prevent the accidental over etching of one film into the next film.

Another way to prevent this from happening would be to correct the mask level so that the probe contacts are protected during the protective layer etch. This is only a band aide because over etching is still a problem at other levels.

All in all, this experiment was troubled from the start. Given the numerous issues with this investigation, it was a great learning tool. Afterall, how many devices are completely fabricated and function properly the first time.

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APPENDIX

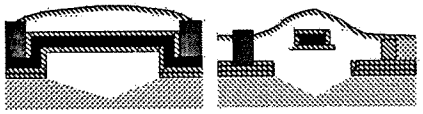


Figure 1 : Final Encapsulated Cross Section

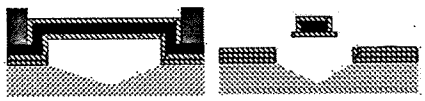


Figure 2 : Final Cross Section Non-Encapsulated

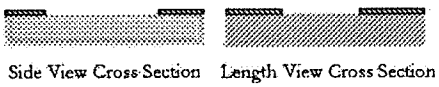


Figure 3 : Cross Section # 1

Figure 4 : Cross Section # 2

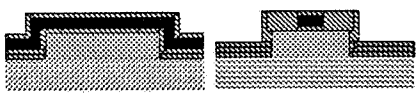
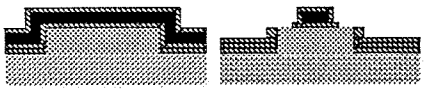
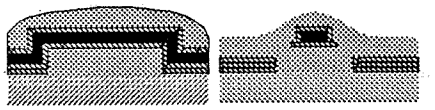


Figure 5 : Cross Section # 3



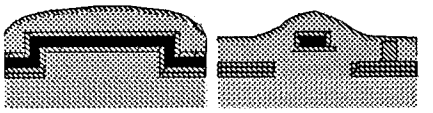
Side View Cross Section Length View Cross Section

Figure 6 : Cross Section # 4



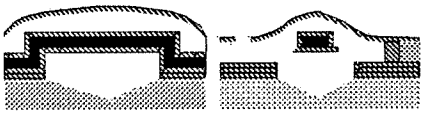
Side View Cross Section Length View Cross Section

Figure 7 : Cross Section # 5



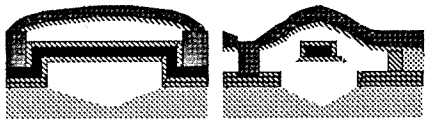
Side View Cross Section Length View Cross Section

Figure 8 : Cross Section # 6



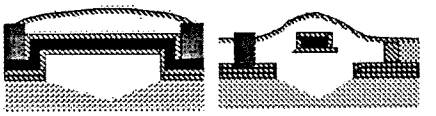
Side View Cross Section Length View Cross Section

Figure 9 : Cross Section # 7



Side View Cross Section Length View Cross Section

Figure 10 : Cross Section # 8



Side View Cross Section Length View Cross Section

Figure 11 : Cross Section # 9

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