Oxide Passivated Nanocrystalline Silicon LED Optimization

Tina M. Wheaton
Microelectronic Engineering
Rochester Institute of Technology
Rochester, NY 14623

Abstract- The objective of this project was to create an optimized, repeatable process for integrated PSi (Porous Silicon) LEDs. Porous Silicon is a light-emitting version of silicon, formed by electrochemical etching in an HF-containing solution. This material becomes stable once passivated with oxygen at high temperatures (900°C) and maintains its light-emitting properties. This study systematically investigated the process effects on electroluminescence (EL) and electrical transport characteristics. The relationship between fabrication conditions and the structural and electronic properties of porous silicon have been subsequently examined. It was discovered that pre-anodization substrate preparation had a dominant influence on the device characteristics. Analysis of the designed experiments (ANOVA) has been used to quantify the influence of factors under study; details of which will be presented.

I. Introduction

With silicon as the dominant semiconductor in the microelectronic industry, the realization of silicon LEDs would greatly enhance the capabilities of integrated optoelectronic systems. Such devices could provide a cost-effective alternative to hybrid technologies for use in display devices and optical interconnects. Silicon, however, is an extremely inefficient light-emitter, and for this reason had not been able to achieve the desired levels of dominance in optical applications. Fortunately, porous silicon, an optically efficient silicon-compatible material has been developed. Porous silicon is a network of nanometer-sized silicon regions surrounded by void space, resulting in a light-emitting material. A porous silicon film is typically prepared by electrochemical anodization of the surface of a silicon wafer.

The fabrication of these devices involves multiple factors that require optimization, each of which have significant effects on electroluminescense (EL) and transport characteristics. The selection of process factors was influenced by background process knowledge of porous silicon materials and the requirements for "working" LEDs (uniform light-emitters, with good transport properties).

II. Theory and Device Fabrication

In order to interpret optical properties of porous silicon, it is necessary to understand why bulk silicon, which is an indirect-bandgap semiconductor, has a low optical efficiency.

Band-edge light emission from a semiconductor involves the excitation of an electron from the filled valence band to the empty conduction band and subsequent recombination of the electron with an empty state (or hole) back in the valence band. Light emission occurs when the recombined energy is given off as a photon. In silicon, this process of photon emission is unfavorable, meaning the laws of physics does not allow it to happen very often.[1] However, if the silicon material is modified from a bulk solid to small crystals of silicon, as in the case of porous silicon, radiative recombination events become much more favorable. Here, electrons, in the conduction band and holes in the valence band are confined spatially by potential barriers, such as nanocrystal surfaces. As a result of the confinement of both these electrons and the holes, the lowest energy optical transition from the valence to the conduction band increases in energy, effectively increasing the bandgap and pushing the emission wavelength into the visible region. The pure quantum confinement model was initially proposed by Canham [2].

Porous silicon is a material formed by electrochemical etching of crystalline silicon using an HF/Ethanol solution. Porosity and PSi thickness are dependent on the variations in the anodization process, and effect the silicon structure size as well as the mechanical stability. [See Figure 1].

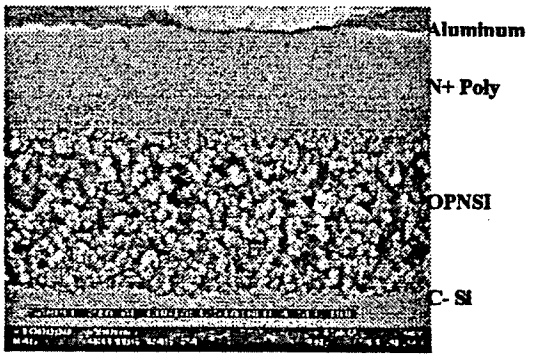


Fig 1: Porous Silicon Cross Section

The basic fabrication process for OPNSi bulk film devices developed at RIT goes as follows:

First, 10 Ω-cm p-type (100) oriented crystalline silicon wafers, with a BF_2+ implanted surface layer, go through a steam oxidation to intentionally induce stacking faults. They are then etched and anodized in a 1:1 HF/Ethanol solution. The current density during anodization was approximately 3.5mA/cm^2. The wafers were anodized for two minutes. Anodization transforms the silicon into a nanoporous layer (porosity ~70%) that is ~.4um thick. The film thickness depends on the anodization time. After anodization, a fifteen minute anneal at 900°C is performed to passivate the porous silicon with oxygen. A polysilicon film is then deposited using LPCVD, and then selectively doped n+ to form the device cathode. Aluminum contacts were then sputtered on the polysilicon and on the backside in order to form an ohmic contact to the substrate for device testing purposes.[3] [See Figure 2 below.]

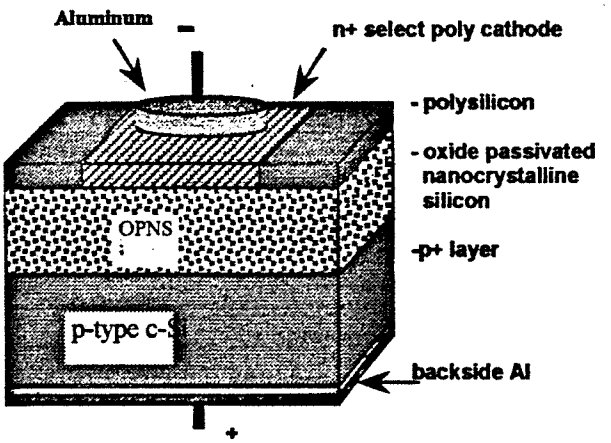


Fig 2: Schematic cross section of porous silicon light-emitting diode, capable of light emission at visible wavelengths.

III. Experiments and Evaluation

Process development for this project included a total of three separate designed experiments. The experiments focused on the relationship between fabrication conditions and the electronic properties of porous silicon. The first experiment investigated the relationship between the amount of pre-anodization surface stress, film thickness, and passivation temperature. The second experiment investigated the amount of lattice damage, surface stress and the anneal method. The third experiment investigated lattice damage and pre-anodization surface stress.

In the first experiment a 900°C steam oxidation time was systematically varied between 2,4, and 6 hours. This was to see if time really played a key role in producing desired stacking faults. The anodization time was varied between 1.5, 2, and 2.5 minutes. This was used to measure importance of film thickness. Lastly, the anneal temperature was varied between 850, 900, and 950°C to measure the degree of passivation. The transport characteristics were not very good, and there was minimal to no light emission on these devices. However, this helped design the second experiment, where implant dose and steam oxidation, as well as Rapid Thermal Process versus furnace anneal were investigated.

The second experiment varied implant dose, steam oxide, and anneals. The implant was 1E14 cm-^{2} vs. 1E15 cm-^{2}. This was used to evaluate how lattice damage effects responses. The steam oxide was varied by whether or not to do a seven hour 900°C steam oxidation or not. This was to evaluate how the degree of surface stress on the wafer effects light emission and transport characteristics. Both the implant dose and the steam oxidation were performed to induce stacking faults on the wafer surface. Finally, the anneal method was varied between RTP and furnace. This was performed to see if RTP was as effective as the furnace in passivating the anodized wafers.

The third experiment was designed with the process information discovered from the second DOE. The implant dose was varied between 1E14 cm-^{2} and 1E15cm-^{2} and the steam oxidation between 900°C and 950°C. The seven-hour steam oxidation was performed on all wafers and the wafers were annealed in the furnace, not the RTP, per DOE #2 results. The strategy for the experiment was to fabricate repeatable devices while optimizing the process.

IV. Results

After analysis of each designed experiment, it was discovered which factors influenced light emission and transport characteristics of the devices.

Each device was tested for light emission, which at this point is purely a visible test for light, and transport characteristics. [See Figure 3].

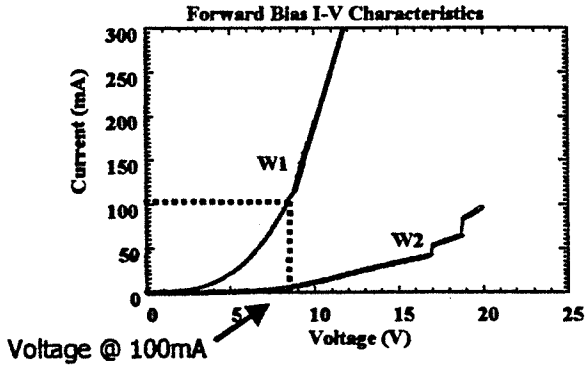
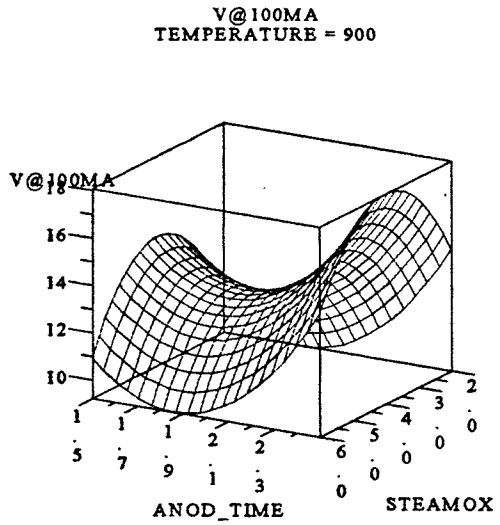


Fig 3: "Good" and "Poor" Transport Characteristics

The desired characteristic curve is described by W1. This has "Good" Transport, this means the device displays small variation in device behavior, and uniform EL over the entire cathode area. W2 represents a typically "Poor" Transport curve, this typically has inconsistent device behavior, and pinpoint EL spots at the aluminum edge. The voltage was measured at 100mA for all devices.

The first experiment, except of one treatment combination, did not have light emission, and several devices had "poor" transport. During the analysis, it was seen that none of the factors had a real impact on the experiment by themselves, and only a transformed quadratic version of the factors impacted the outcome of the experiment. Figure 4 shows the anodization time vs.



voltage, and the steam oxidation vs. the voltage.

Fig 4: Results of DOE #1

The horseshoe effect is a result of the transformed factors, and shows their quadratic behavior. In this experiment only 74% variation is accounted for. This raises the question as to how influential these factors are.

However, from this experiment, and prior porous silicon knowledge, the second experiment was designed. In this experiment, 82% of the variation was accounted for and two wafers emitted substantial (very bright) light. Both of these wafers went through the seven-hour steam oxidation and were annealed in a furnace. Figures 5 and 6 show the single effect relationship of implant dose and steam oxidation on the electrical response (voltage at 100mA). The implant dose is shown to have a linear effect in relationship to the voltage of the device. The steam oxidation shows that the wafers that received a steam oxidation have minimal voltage variation in comparison to the wafers not receiving the steam oxide.

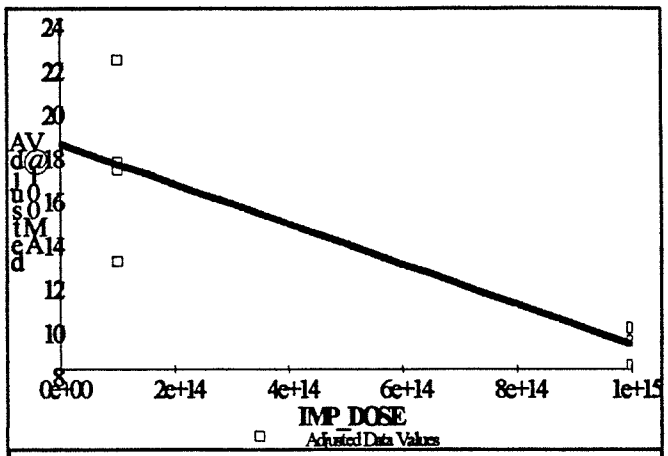


Fig 5: Single Factor Effect, Implant Dose Vs. Voltage @ 100mA

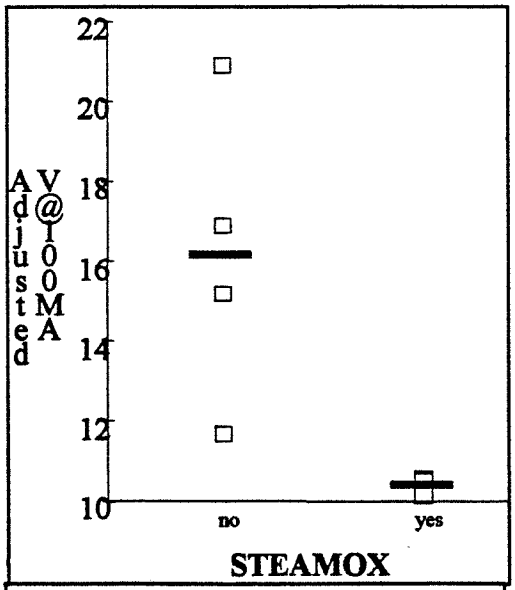


Fig 6: Single Factor Effect, Steam Oxidation Vs. Voltage @ 100mA

Both of these factors influenced the third designed experiment, where it was decided to process all the wafers with the steam oxidation, (varying temp from 900°C to 950°C) and to vary the implant dose between 1E14 cm^{-2} and 1E15 cm^{-2}.

V. Conclusions

An optimized porous silicon LED was not achieved, in the first two designed experiments, however, the third DOE is still being analyzed and current data looks promising. It was discovered that lattice damage from ion implantation and induced stacking faults from the steam oxidation, are both significant influencing process factors in 'good' transport characteristics and EL device behavior. More work still needs to be completed to ensure repeatability and optimization of the process.

VI. Acknowledgements

The author would like to give special thanks to all the help and support from Karl Hirschman and Burcay Gurcan.

Tina M. Wheaton, originally from Fair Haven, NY, received B.S. in Microelectronic Engineering from Rochester Institute of Technology in 1999. She obtained co-op experience at Eastman Kodak and Motorola. She is joining Motorola, Austin, TX, as a Device Engineer in June 1999.

---

[1] R.T.Collins, P.M. Fauchet, and M.A. Tischler, *Physics Today*, **24** (1997)
[2] L.T Canham, *Appl. Physics. Lett.* **57**, 1046 (1990)
[3] K.D.Hirschman, L. Tsybeskov, S.P. Duttagupta and P.M. Fauchet, "Integrating Bipolar Junction Transistors with Silicon-Based Light-Emitting Devices" *Mat. Res. Soc. Symp. Proc.* **453**, 705(1997)