Fabrication and Development Of a Charge Injection Device Imager

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Abstract- As Rochester Institute of Technology (RIT) brings into production i-line capabilities with a new Canon stepper, resolution beyond 2μm will be possible. The present project prepares one of RIT's most novel and successful processes for this transition. The process for a Charge Injection Device Imager (CID) has been entirely developed at RIT through the work and collaboration between the Imaging Science and Microelectronic Engineering Departments. After the initial success in the design and fabrication of 8X8 and 32X32 imager, a more challenging 54X40 process was developed employing 6-micron PMOS technology. The goal of this project is the successful fabrication of an imager that will allow for the capture of real images. All this exclusively fabricated at RIT. This project recalls on the latter design and which transitions the CID process in preparation for 2-micron technology. The device transistors has been tested and characterized and the results are compared to simulated transistor data obtained using SUPREM-IV.

I. INTRODUCTION

Charge Coupled Devices (CCD's) dominate the digital imager industry today. They are found in many different applications such as High Definition TV (HDTV), astronomy , space based imaging [1] and the widely used hand-held video camera. However, there are some low light level imaging and harsh conditions applications where Charge Injection Devices (CID's) provide a distinct advantage over the CCD. Furthermore, Charge Coupled Devices, still present some challenges that are avoided with the use of CID's, such as charge transfer problems, non-random readout, and expensive and complex fabrication techniques since it cannot be integrated with CMOS technology.

The CID approach, on the other hand, has the main advantage of its total compatibility with CMOS fabrication techniques. This makes them cheaper to manufacture and it also allows for electronic components to be integrated in the chip. Other advantages are its avoidance of charge transfer losses, minimized blooming and random non-destructive readout.[2]

This paper reports on the basic CID structure, readout mechanism and process fabrication at RIT.

II. DESCRIPTION

A basic description of how light is collected and stored by the CID follows. Then, figures and an explanation of the readout mechanism of the device, provide an insight of the operation and some of its advantages. Finally noise reduction techniques are taken into consideration when selecting a pixel design.

A. Light Integration and Charge Collection

It is important to understand how light is collected by the device and what considerations are taken when fabricating the structure. The basic element of a CID imager is a MOS capacitor. This operation is portrait in figure 1. Basically, light is collected by bringing a MOS capacitor to a deep depletion state. Photons will enter the Silicon creating electron/hole pairs. Light with short wavelengths will travel a shorter distance, depending on the absorption coefficient of Si, figure 2. Holes created by shorter wavelength light will be directly collected by the potential well. Holes produced by light with longer wavelengths, which absorption coefficient is larger than the depletion length, may or may not be collected in the potential well. It will depend on their characteristic diffusion length. A lightly doped substrate will allow for a lager depletion width, thus a larger sensing area is possible. Charge is integrated on the Si/SiO2 interface of the collection MOS capacitor.[3]

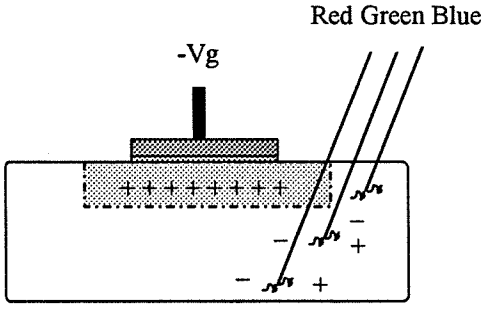

Figure 1. Light Collection and Charge Integration

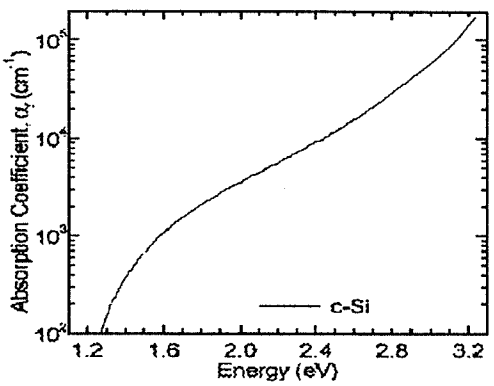

Figure 2. Light Absorption Coefficient of crystalline Si

B. *Pixel Operation*

Figure 3 sequentially represents the basic pixel operation and readout mechanism utilized in this design. Two capacitors are utilized for a random X-Y selection a pixel. Both capacitors are biased to a negative potential but the column or collection capacitor is biased to a larger negative potential, all charge is stored here. Then, the row or sense capacitor is left floating and its potential, which should be near the potential of its source, is read. All the stored charge is then moved to the potential well of the sensing capacitor by biasing the collection capacitor to a lower negative potential. After this transfer operation the potential of the sensing capacitor is read again. The potential difference between these two readouts of the sensing capacitor is proportional to the collected charge. As an advantage this readout technique is not destructive and can be repeated as many times as necessary. This results in a reduction of noise. Finally the charge is cleared by injection into the substrate. Consequently another pixel can be selected and read on a similar way.

C. *Active vs. Passive Pixel Design*

The CID structure allows for two different kinds of pixels, active and passive. A passive pixel uses most of its area for light collection. After storing the collected charge, this is sensed and transfer to the output stage where its amplified and read. The active pixel has a smaller collection area since it includes a pre-amplifier in the pixel are itself. This group of transistors will amplify the sensed charge before its transfer to the output stage. Although the active pixel has a smaller sensing area, the resulting noise reduction of this design makes it advantageous over that of the passive pixel.

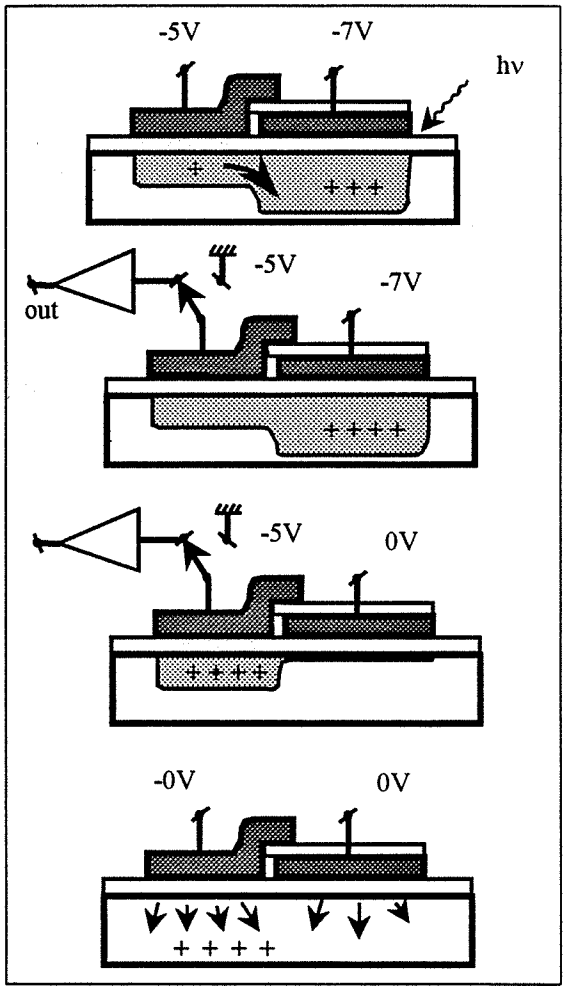

Figure 3. Basic CID operation

III. PROCESSING AT RIT

A 54x40 Active Pixel Charge Injection Device Array (APCID) has been exclusively fabricated at Rochester Institute of Technology (RIT). RIT has a state of the art microelectronic facility which allows for complete in-house processing.

PMOS transistors are utilized. The process flow includes 63 steps such as localized oxidation of Silicon (LOCOS) isolation, 9 photo levels, two levels of poly, 50nm gate oxide and 4-micron minimum dimension.

The starting substrate is a 30-micron lightly n-type doped epitaxial layer over a highly doped p-type Silicon substrate. It starts with LOCOS isolation. Then, and after reconditioning the substrate with a sacrificial KOOI oxide, a high quality 500A of SiO2 is thermally grown as the first dielectric material for the collection capacitor. Polysilicon is then deposited in a LPCVD reactor. This film is then doped using an Ion Implanter to the desired level of conductivity. The second gate is constructed with a slightly thicker dielectric layer, ~600A, of also thermally grown SiO2. Poly 2 is deposited via LPCVD. A highly

resistive Phosphorous implant in perfomed next to act as transistor load. Due to the uncertainty of the characteristics of the Polysilicon deposited a pre-screening implant is necessary to determine the necessary dose. After the pre-screening five different doses were used 1e14/cm2, 2e14/cm2, 3e14/cm2, 4e14/cm2 and 5e15/cm2. The remaining of the polysilicon is doped to a low resistivity level and etched. Then, another series of implants follow. These include a p+ drain/source for the PMOS transistors, a pinning implant to avoid surface inversion in the exposed gate oxide areas and an n+ substrate contact. Finally a thick layer of oxide is deposited via LPCVD and metal contacts and routing are deposited and patterned.

IV. SIMULATION

The preceding process flow was simulated using the software package SUPREM-IV. The resulting structure is presented in figure 4. This allowed for the simulation of the PMOS transistor characteristics as well as obtaining information about the resistance characteristics of our films.

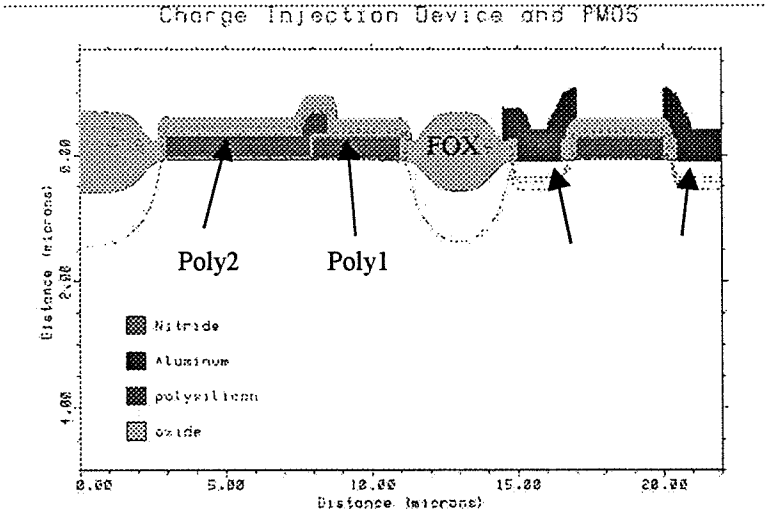

Figure 4. SUPREM-IV simulated structure

The simulation results showed a threshold voltage of the PMOS transistor of –1.2Volts. It was inconclusive on the resistivity values of the polysilicon films since no specific grain boundary properties could be established for the modeling.

V. RESULTS

As it can be seen in figure 5, good PMOS transistors were fabricated. The two sub-threshold curves correspond to transistors fabricated at Poly1 and Poly2 respectively. The difference observed in threshold represents the difference in thickness of about 200A. An excellent gain is observed out of this two curves. Unfortunately, as seen in figure 6, the load resistance tested in the fabricated devices proofed to be too low. Represented here is the device which received the lowest implant dose at the resistor level. The values obtained were too low and prevented the PMOS-transistor-based logic from operating properly.

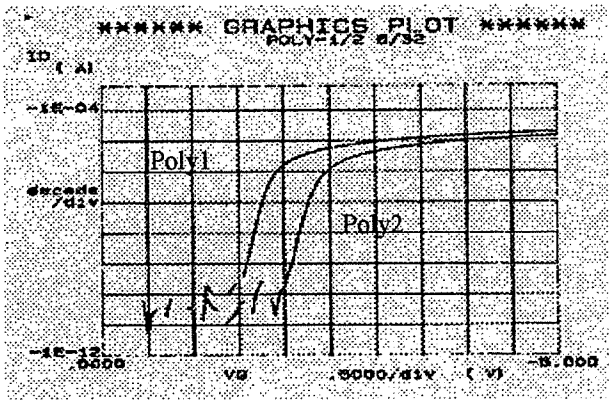

Figure 5. Sub-threshold Plots for Poly1 and Poly2 PMOS

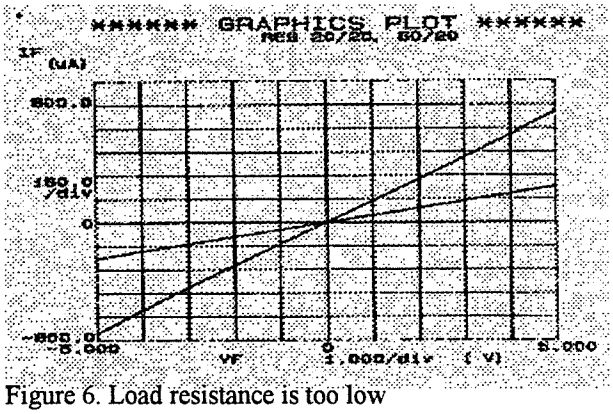

Figure 6. Load resistance is too low

VI. CONCLUSION

An Active Pixel Charge Injection Device has been fabricated at Rochester Institute of Technology. The process flow has proven solid but with room for improvement. A better qualitative characterization of the polysilicon layer is necessary if PMOS transistors are to be used. CMOS utilization could avoid some of these issues.

REFERENCES

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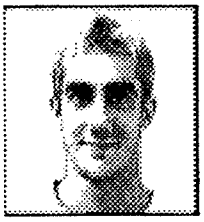

Ivan Puchades, originally from Barcelona, Spain, received his B.S. in Microelectronic Engineering from Rochester Institute of Technology in 1999. He attained co-op work experience at Advanced Vision Technologies and National Semiconductor. He is Semiconductor. He is currently pursuing an M.S. in Electrical Engineering at Rochester Institute of Technology.