8 Bit Analog-to-Digital Converter Design and Simulation

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Abstract- The purpose of this study is to present and characterize an 8 bit AD converter implemented with flash architecture. Flash architecture provides with one of the fastest and easiest ways to convert analog input signals to digital outputs. Analog-to-digital conversion is the process in which a continuously varying analog signal is transformed into a multilevel digital signal.. Analogue electrical waveforms are applied to the converter and are sampled at a fixed rate. Sample values are then expressed as a binary number consisting of 0's and 1's. The resulting digital code can be used to encode digital audio, applications in video and image processing systems. The more bits that are used to represent the amplitude of the original signal, the higher the quality of the output. 8 bit sampling is typically used to encode speech, 16 bit to encode music.

I. INTRODUCTION

A. Flash-Type Converter

Sampling levels for an 8 bit ADC are 256. Sampling frequency should be twice that of the highest frequency in the sampled waveform, if it is to be represented correctly when digitized according to the signal sampling Nyquist theorem.

The input voltage of the ADC can range from 0 to Vref. The voltage reference is used to set the range of conversion of the converter. If the input to the ADC is equal or larger than Vref then the converter will output all ones. For inputs between these two voltage levels, the A/D converter will output binary numbers corresponding to the signal level. Because of the numerous output levels there is inherently noise in the quantized output signal. The key to reducing the effects of the noise is to maximize the input signal level. A good rule of thumb is to keep Vref at least as large as the maximum digital signal.

The most straightforward method to perform Analog to Digital conversion is to compare the sampled analog signal with different levels implementing the Flash AD architecture Fig.1. An 8 bit AD converter was implemented in CMOS, the number of comparators required using simple flash architecture is 2^N –1 comparators, number of transistors 6200. We assigned a full scale input level of 10 V between positive and negative rails for Vcc and Vss supplies to the comparator, the LSB voltage level is 10/255 = 39 mV. The input signal was first sampled by the circuit , the comparator made a decision whether or not the sampled value is greater or smaller that the reference voltages. Each reference level in the series of resistors ladder needs to be one Least Significant Bit apart from each other. The offset of the comparator needs to be less than the least significant bit level of 39 mV. The converter ladder resistance was assigned a value of 2550 Ohms. In CMOS, this offset requirement is difficult to achieve.

Some special circuit techniques are required to reduce the offset of the comparator, which requires large amounts of power because of its fast conversion rate, this limit the family of flash converters to 8 bit or less resolution. The fundamental block of the design for this project is the 32 level sampling output element, the total number of comparators is 255 and total number of resistor is 256.

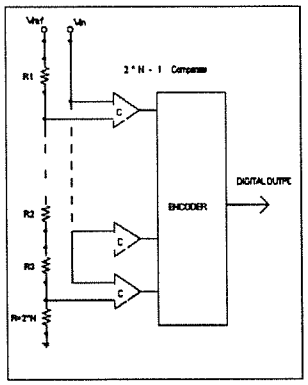
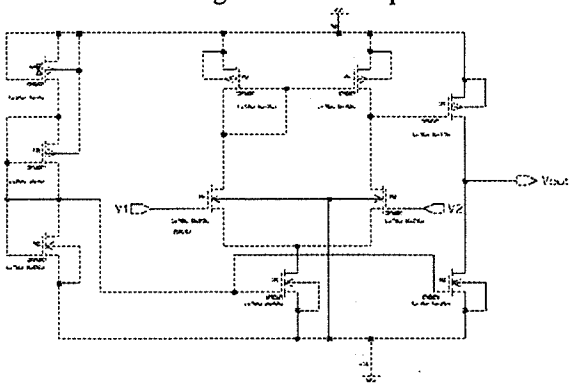


Figure 1. Flash AD architecture

B. The Comparator

The comparator circuit is displayed in Fig. 2, it is implemented in CMOS technology, the transistors

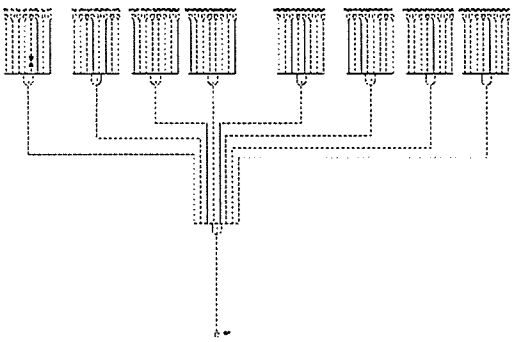
Figure 2. The comparator



geometries are balanced to conduct the same amount of current, taking into account the difference in carriers mobilities between NMOS and PMOS.

B. *The Combinational Logic*

Figure 3. The combinational logic array



The combinational logic array of Fig. 3 geometries have been set up according to the number of inputs N:

$$(W/L)n = N/2\ (W/L)p$$

for NMOS and PMOS transistors. The logic used is NAND to NAND. This logic was selected to save silicon area. For the present case the outputs produced will be inverted. The decoder combinational usual logic is AND to NAND. NAND logic replacing the OR logical output. A set of two trees of NAND gates with 64 inputs each has been used to implement the binary code. The number of input is half the sampling level or two to the power eight, in this case 256/2= 128 inputs.

1. DC *Bias Analysis*

The comparator is biased to make the pull-down network conductive and turn the current mirror transistor, assuming the transistors are working in the saturation regime, we can use the following approximation to obtain the bias voltage,using transistor M8, M9 and M10.

Idsat = kW / L (Vg-Vt)^2 [1]
Isd8 = Isd10 = Isd9

The sum of all potentials from thepositive rail to the negative rail is given by:

20 V = Vsg10 + Vsg9 + Vgs8

20 V = 2 Vsg9 + Vbias

Vbias - 20 / 2 = -Vsg9

The voltage drop at Vgs8 will produce the Vbias needed to turn the current mirror transistor

From equation [1] we obtain:

K W9 / L 9 (Vgs9 - Vt)^2 = k W8 / L8 (Vgs8 - Vt)^2

W9 / L9 [(-Vbias/2 + 20 / 2 - Vt)] ^ 2 = W8/L 8 (Vbias -Vt) ^ 2

[(W9 / L9) / (W8/L8)]^ 0.5 = (Vbias - Vt)/ (-Vbias/2 + 10 + 1)

[(W9 / L9) / (W8/L8)] ^ 0.5 = (-9.6 - 1) / (9.6/ 2 + 10 + 1)
[(W9 / L9) / (W8/L8)] ^ 0.5 = - 0.514

[(W9 / L9) / (W8/L8)] = 0.264

(W8 / L8) = 3.77 (W9 / L9)

This gives an approximate ratio of four to one for the PMOS and NMOS transistors of the Vbias circuit.

2. Differential Pair

The saturation currents for the differential pair transistors and the current load transistors are given by:

Idsat = u W Cox' / 2 L (Vgs - Vt) ^2

Assume Idsat =15 uA

IdsM1 = IdsM2 = IdsM3 = IdsM4 = 7 uA

IdsatM1 = 600 * 30 /20 Cox' / 2 (1.5-1) ^2 = 900 cm^2 / V sec * (1.5 - 1 V)^2 * (6.9E-8 F/cm^2) / 2 = 7.85 uAmps for NMOS transistor

IdsatM3 = 300 * 40 /20 Cox' / 2 (1.6-1) ^2 = 3000 cm^2 / V sec * (1.6 - 1 V)^2 * (6.9E-8 F/cm^2) / 2 = 7.58 uAmps for PMOS transistors.

IdsatM5(current mirror) = 600 * 40 /20 Cox' / 2 (1.6 -1) ^2 = 1200 cm^2 / V sec * (0.6 V)^2 *(6.9E-8 F/cm^2) / 2 = 14.9 uAmps

2. *Output stage*

The output stage calculation of Idsat is done taking into consideration the channel length modulation parameter lambda of 0.02

Idsat = uW Cox' / 2 L (Vg- Vt)^2 (1 + λ Vds) [2], λ channel length modulation lambda = 0.02 and Vout = 0V
Vout near zero so Vds should be ~10 V

From equation [2] we obtain for M7 PMOS transistor:
Idsat = (300) (80/20) * (6.9E-8/2 F/cm^2) *(1.6-1) ^2 * (1 + 0.02 * 10V) = 15.2 uAmps

M6 NMOS transistor Idsat:

Idsat = (600/ 2) (40/20) * (6.9E-8 F/cm^2) * (1.6 - 1) ^2 * (1 + 0.02 * 10V) = 15.3 uAmps

4. Differential amplifier small signal analysis

Gm = W u Cox' / L (Vg – Vt) = 2 Id / (Vg –Vt) ; rds = 1 / (λ Id)

Gm = 2 * [7.5E-6 u Amps / (1.6 – 1)] = 30.24 umho

rds = 1 / (7.5E-6 * 0.02) = 6.66 M

Vo / Vin = 2 * gm * rdsn // rdsp = 2 * 30.24 umho * 6.66 M // 6.66 M = 201.6 (differential pair gain)

M1 and M2 differential pair
M3 and M4 are current source loads

5. Output stage small signal analysis:

Transconductance Gm
Gm = W u Cox' / L (Vg- Vt) = 2 Id / (Vg –Vt) ; rds = 1 / λ Idsat

Gm = 2 (15.07 uAmps) / (1.6 –1) =50.2 u mho

rds = 1 / (lambda Id) = 1 / (0.02 *15.07 uAmps) = 3.31 umho
Output gain = Vout / VM4 = Gm rdsPMOS // rdsCMOS = 50.2 umho * 3.31 M // 3.31 M = 83

6. Differential mode gain

Acm = common mode gain = - Gm rdsPMOS / (1 + 2gm Ro) = - 50.2 E-6 (3.31E6) / (1 + 2 * 50.2E-6 * 1.65 E6) = - 0.99
Avd = differential mode gain = 201.6 * 83 = 16,732.8 or 84.47 dB
CMRR = |Avd/ Acm| = 16565.47 = 20 log16565.47 = 84 dB

CL = Area * Cox' = 80 pF/cm^2

Gain Band Width Product
GBW = gm / 2 pi CL = 99.86 KHz

Slew Rate = Id / CL where CL = CL min (parasitic load capacitance) + CL ' (nominal load capacitance) .The output of an ideal op-amp has the ability to change instantaneously. In a real op-amp the rate of change of the output, expressed in volt/ unit time should never exceed the slew rate value

SR = 15 uAmps / 80 pF = 0.187 V/usec

Table of the comparator parameters

Comparator Specs	
Output Resistance	1.65 Mohm
Avd= 200.1 * 83	16732
Common Mode Gain	-0.99
CMRR = 16732* 0.99	16565
CMRR	84.3 dB
Vcc/Vss	10 V
Gain Bandwidth Product	100 KHz
Slew Rate	0.187 V/usec

III. RESULTS

Figure 4 shows the converter output obtained and presented in this study, the performance of the converter is measured in terms of digital synchronous outputs. Future work will include the improvement of the model and refinement of the A/D circuit.

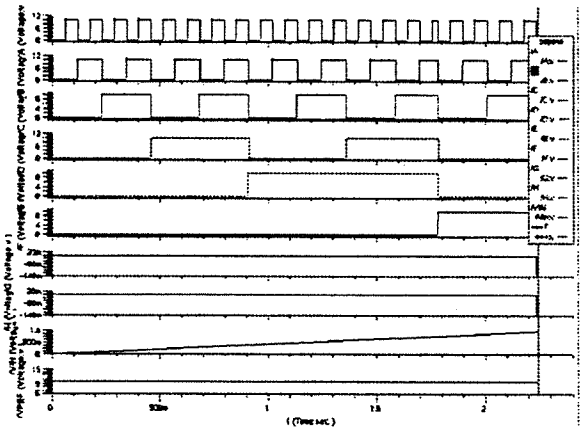


Figure 4. Transient output of the converter.

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