Electrolytic Plating of Copper for Advanced Interconnects

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Abstract- There is great interest in the semiconductor industry to move to copper for advanced interconnect processing. The purpose of this study was to develop an electroplating process so further studies in copper processing can be undertaken at R.I.T. Electroplating was performed using the facilities available at the University of Rochester. This system utilizes a copper sulfate based electrolyte and an 8" wafer holder. In order to use the electroplating tool for four-inch wafers, a fixture was designed. Plating was performed on Si wafers coated with adhesion and seed layer of copper at varying current densities. Plated films were characterized for sheet resistance. A 7% standard deviation in sheet resistance of the electroplated layer has been achieved with this wafer fixture design. This variation can be explained in terms of the electric field distribution in the electrolytic cell. The bulk resistivity for the plated copper was found to be 2.06E-6 Ω·cm. Powder X-ray diffraction analysis showed that the plated films had (110) preferred orientation

I. INTRODUCTION

Interconnect resistance and capacitance has become increasingly important in determining packing density, reliability, and the manufacturing cost of ICs. Copper's low resistivity and excellent thermal conductivity makes it a good a candidate for the next generation conducting material for interconnects in ICs. Copper can also handle higher current densities which allows for smaller line dimensions. Copper also has superior resistance to electromigration compared to aluminum. Lower manufacturing costs can be expected because a dual damascene requires 20-30% less process steps. Due to a higher level of integration per level, fewer levels of metal are needed (about half required compared with aluminum). Some issues that are associated with moving to copper processing include the inability of copper to be patterned using plasma etching due to the lack of volatile halide by-products. This requires the implementation of the dual damascene process which takes a while to develop. Another issue is that copper is a known fast diffuser through Si and $Si0_2$

II. BACKGROUND

A basic copper interconnect process contains three layers that includes a barrier layer, seed layer, and a copper electrofill layer. A typical cross-section is shown in Figure 1. The first layer is the barrier layer. This layer prevents copper from diffusing through oxide and silicon. If the copper diffusion is not blocked, copper atoms can reach the substrate and cause devices to fail. This layer must provide good step coverage during deposition, be a good adhesion layer for copper deposition, and must also be easy to remove during the chemical mechanical polishing (CMP) step. Tantalum deposited by sputtering was used for this layer. Tantalum was chosen because it has excellent step coverage properties and it is a highly reactive with other metals. The second layer of the process is a copper seed layer, which was also deposited by sputtering. This layer offers a low-resistance path for conduction. It also provides a nucleation layer for initiation of the plated copper film growth. The main copper layer was deposited with an electroplating process. The last layer is a Si_3N_4 cap. This layer prevents diffusion of copper between metal levels. It also acts as an etch stop during the dual damascene process.

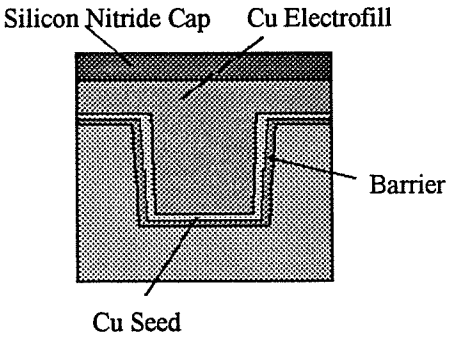


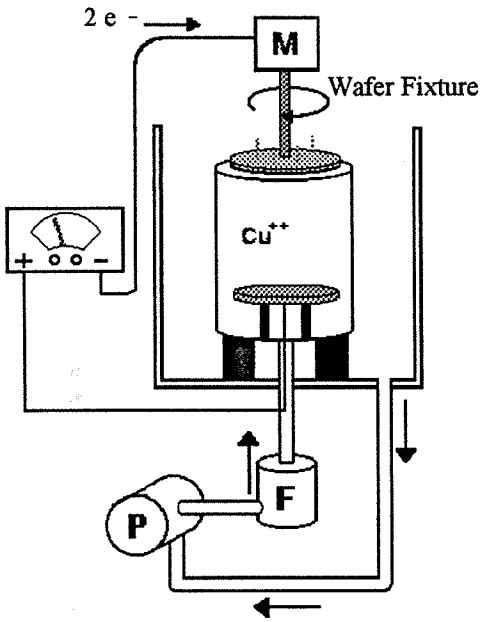
Figure 1: Cross section of a Basic Copper Process

Figure 2 is a cross section of the electroplating tool that was used for this study. The wafer with a seed layer is immersed in a solution containing cupric ions. Electrical contact is made to the seed layer which becomes the cathode in the circuit and the reaction $Cu^{2+}(aq) + 2e- \rightarrow Cu(s)$ occurs. The amount of copper that is deposited can be calculated using Faraday's law. It states that in the

absence of any secondary reactions, the current delivered to a conductive surface during electroplating is directly proportional to the quantity deposited. Using Faraday's law and Faraday's constant the following relationship can be derived to find the theoretical deposited weight:

$$\text{Weight Deposited} = \frac{63.546\text{g/mol} \times (\text{Amps} \times \text{time})}{2 \times 96{,}500}$$

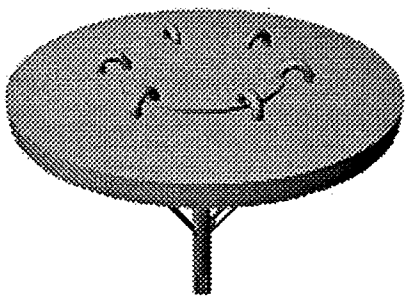
Figure 2: Cross-section of Electroplating Tool



III. EXPERIMENTAL

In order to use the electroplating tool at the University of Rochester a 100-mm wafer fixture was designed and constructed. Figure 3 shows a bottom view of the fixture. A constant current flows from a power supply to a copper rod and gets distributed to six copper clips. The current flows onto the wafer and makes it into a cathode. The clips hold the wafer in place with compression springs. Plating was performed on silicon wafers coated with adhesion and seed layers using varying current densities. Various currents and plating times were tested to obtain a uniform film and to determine a deposition rate.

Figure 3: Bottom View of the 100mm Wafer Fixture

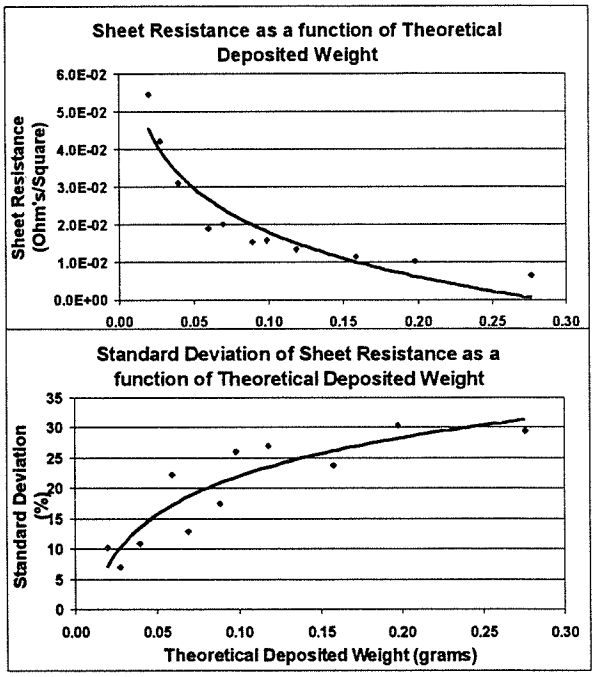


IV. RESULTS

The following is a plot of sheet resistance as a function of the theoretical deposited weight. This plot shows that as the deposited weight is increased the sheet resistance decreases as expected. This was used to verify the wafer fixture is working properly.

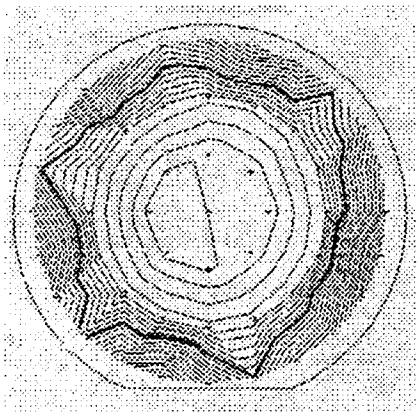
The next plot shows that the standard deviation of the sheet resistance increases as the amount of copper deposited increases.

The following is a sheet resistance contour plot of a wafer plated with 2 amps of current. Higher deposition of copper is visible at the edge of the wafer. This is due to a higher current density existing at the edge of the wafer. The wafer fixture was simulated using a field simulation program called Maxwell. Simulations show that with the current wafer fixture design a higher current density is expected at the edges.

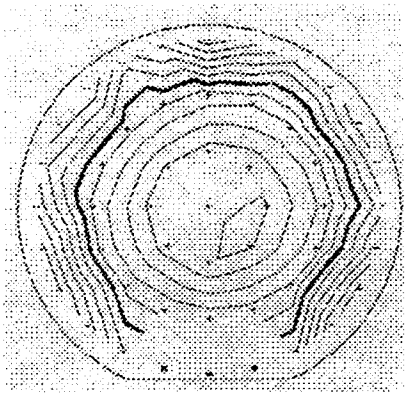


The next sheet resistance contour plot is of a wafer plated with 0.2 amps. When using a low current there are less current density effects. This current yielded a standard deviation of 7%.

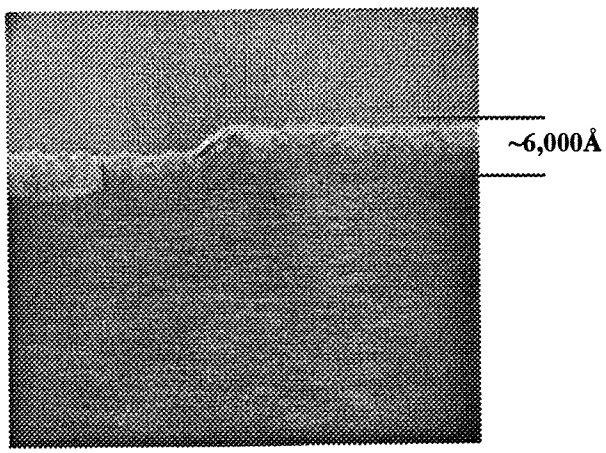
Sheet Resistance Contour Plot (2 Amps)



Sheet Resistance Contour Plot (0.2 Amps)



The following picture is a SEM image. It shows the thickness of the deposited copper to be ~6,000 Angstroms. The sample was plated with 0.2 amps for 10 minutes. This gives a deposition rate of ~600 Angstroms per minute.



Knowing the sheet resistance of the sample and the thickness, the resistivity can be calculated and is found to be 2.07×10^{-6} ohm cm.. The actual resistivity for bulk copper is reported to be 1.6×10^{-6} ohm cm.

X-ray diffraction analysis revealed a stronger peak corresponding to the (220) planes (d = 1.27 A) indicating a (110) preferred orientation of the plated films.

V. CONCLUSION

An electroplating wafer fixture was constructed and a process was characterized for plating 100mm wafers. Plated films were characterized for sheet resistance. A 7% standard deviation in sheet resistance of the electroplated layer has been achieved with this wafer fixture design. Variation can be explained in terms of the electric field distribution in the electrolytic cell. The bulk resistivity for the plated copper was found to be 2.06E-6 Ω·cm. Further studies in copper processing are planned using the optimum plating process that was determined.

VI. ACKNOWLEDGEMENTS

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VII. REFERENCES

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