Integration of SiGe Resonant Interband Tunneling Diodes with RIT CMOS

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Abstract- This study investigates the integration of SiGe resonant interband tunneling diodes (RTD) with a standard silicon p-well CMOS process. It is feasible to build the RTD devices on the MOS source/drain regions if the RTD process did not degrade MOS devices. Besides, some etch selectivity issues need to be addressed. MOS transistors were subjected to the thermal cycling of the molecular beam epitaxial growth process and the rapid thermal anneal used in the fabrication of RTDs prior to contact formation. No destructive effects on the operation of NMOS and PMOS devices were observed. NMOS devices exhibited a positive shift of about 100mV in threshold voltage, while transconductance was reduced by about 5%. PMOS devices exhibited under 5% change in both threshold voltage and transconductance. The CMOS devices were proven to be compatible thermally with the RTD device fabrication process.

INTRODUCTION

Tunnel diodes were first discovered by Leo Esaki in 1958 while studying bipolar transistors.[1] Tunnel devices exhibited multi-valued I-V characteristics as well as negative differential resistance and high-speed transient response. These properties made them very interesting, but due to the lack of a Si-based manufacturing process, they have seen little commercial exposure. To date III-V material systems are the only ones which realize fully integrated tunnel diodes and transistors.[3]

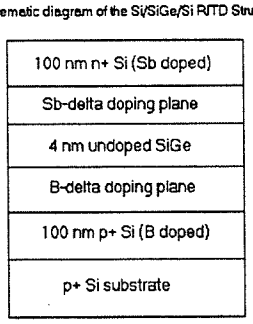

Figure 1: Schematic Diagram of RITD Structure

In the early 1990s Si/SiGe resonant tunneling devices were demonstrated. In the last few years further improvements in the manufacturing of these devices has been made. Peak-to-valley current ratios for these devices have been measured at 1.54 at a peak current density of 3.2 kA/cm^2 [2]. These devices were fabricated using molecular beam epitaxy (MBE) followed by a thermal anneal. This process is compatible with current Si-based CMOS manufacturing, unlike the previously mentioned III-V RTDs.

PROPOSED INTEGRATION

Due to the high sensitivity of the RTD devices to thermal steps it was decided that the fabrication of these RTD devices should occur after the bulk of the CMOS devices were completed, but before metallization. The aluminum used in the wiring of the transistors would not be able to withstand the temperatures that the MBE process uses. While the RTD device mesas were being etched, the CMOS devices would also need some sort of protective layer. With this in mind, the decision was made to present an integration scheme that involved the CMOS wafers being taken right before the contact cut etch step. The wafer would be completely encased by CVD deposited low temperature silicon dioxide (LTO) which should provide adequate protection for the CMOS devices from the RIE step necessary for RTD mesa formation. Also there would be no metal on the wafers.

RIE would be used to open up windows in the LTO for the formation of the RTD mesas. MBE growth would follow, covering the entire wafer with the Si/SiGe/Si stack. It has been noted that over the LTO the Si/SiGe/Si epitaxial stack would not grow as single crystal stack. After the MBE growth a refractory metal etch mask would be deposited and patterned to delineate the areas where the mesas would be. Following this step the contact cuts would be etched, still using the refractory metal mask to protect the RTD devices. After contact-cut etch the refractory metal would be removed as it would be no longer necessary. The final CMOS steps of metallization, photo and sinter would then be performed as usual. A final cross-section can be seen in Figure 1.

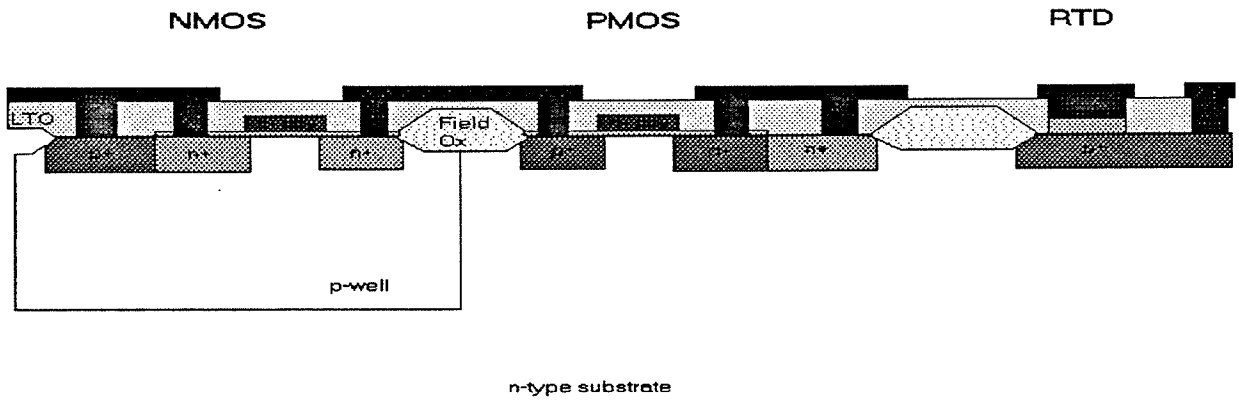

Figure 1: Final Integrated Cross-section

EXPERIMENTAL

A thermal study of the impact of RTD device fabrication was performed on the p-well CMOS process (PW-3) developed at the Microelectronic Fabrication Facility of the Rochester Institute of Technology. A completed CMOS wafer was taken and three NMOS as well as three PMOS devices were tested. The wafer was then stripped of aluminum and RCA cleaned to insure a clean surface for the subsequent steps. The aluminum was removed from the wafer due to the fact that Al would melt and diffuse into the silicon at the temperatures to be used in the subsequent thermal steps. A rapid thermal furnace was used to simulate the RTD growth and anneal processes. The simulation consisted of a 320 °C for 30 minutes, followed by 500 °C for 5 min, and finally 700 °C for 1 minute. All of the thermal steps were performed in a N_2 ambient so that the wafer surface would remain unchanged. After the thermal treatments, Al metal was deposited on the wafer using evaporation. The wafer was patterned using a GCA Mann g-line stepper and wafertrac, and then developed. Finally the wafer was placed in a furnace for 15 minute at 450 °C in H_2/N_2 (5%/95%) ambient for sintering. The same transistors were then re-tested and the results were recorded.

RESULTS

Table 1: Thermal Simulation Results

Site 1	Before	After	Δ
NMOS VT (mV)	427	547	120
NMOS gm (1/Ω)	2.65E-05	2.68E-05	3.00E-07
PMOS VT (mV)	-424	-442	-18
PMOS gm (1/Ω)	9.11E-06	9.16E-06	5.00E-08

Site 2	Before	After	Δ
NMOS VT (mV)	568	670	102
NMOS gm (1/Ω)	2.51E-05	2.40E-05	-1.10E-06
PMOS VT (mV)	-833	-841	-8
PMOS gm (1/Ω)	1.10E-05	1.06E-05	-4.00E-07

Site 3	Before	After	Δ
NMOS VT (mV)	363	467	104
NMOS gm (1/Ω)	2.52E-05	2.30E-05	-2.20E-06
PMOS VT (mV)	-742	-717	25
PMOS gm (1/Ω)	8.13E-06	7.98E-06	-1.50E-07

Table 1 shows the results obtained before and after for the three wafer sites tested. Site one corresponds to the center of the wafer, while site 2 and site 3 correspond to

the right and left sides of the wafer respectively. For the tests the flat was oriented away from the probe operator. The PMOS devices remain largely unchanged, with a few mV shift in V_T and a few % decrease in transconductance. The NMOS devices exhibited about a 100mV shift in V_T and under 10% decrease in transconductance.

CONCLUSION

The thermal simulation on CMOS devices has proved that the RTD device fabrication process is not destructive, and can be integrated with standard Si-based CMOS processes. A small degradation in CMOS performance should be expected, but this can be accounted for in previous CMOS thermal processes, and perhaps the V_T-adjust implant step for NMOS devices.

FUTURE WORK

In the future, a plasma etch chemistry and appropriate etch stop should be investigated. The selectivity of the Si/SiGe/Si to LTO and the barrier metal used should also be investigated. A thermal study on the impact of the sinter step should also be done on the RTD devices. Finally masks and a circuit utilizing integrated CMOS and RTD devices should be created.

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