Plasma Induced Damage to Thin Gate Oxides

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Abstract - Two mechanisms of plasma processing damage to thin gate oxide structures were studied. Thin 17.5 nm oxide on Si substrate structures were studied after direct exposure to a oxygen plasma environment with surface charge analysis and breakdown voltage measurements. A second antenna structure was used to study the charging effects of an oxygen plasma on 17.5 nm gate oxides through breakdown voltage measurements. A correlation was found between duration of plasma exposure and the extent of damage in terms of decreased dielectric strength and changes in oxide charge levels for both experiments.

INTRODUCTION

IC fabrication has become dependent on plasma processes for the anisotropic etching of polysilicon, aluminum, oxide, and polymers/photoresist (ashing). Within a plasma, wafers are exposed to charged particles, in the form of reactive ions and electrons, as well as high energy photons. Both of these have been determined to cause damage to CMOS processes with sub-micron geometries.

CMOS designs are most vulnerable to damage in the area of the thin gate oxides. One source of damage is a result of direct exposure of the gate oxide to the plasma. UV radiation and charged particles in the plasma induce dangling bonds and trapped charges in the oxide in regions which are directly exposed to the plasma ambient [1]. Damage can also result when the gate oxide in not exposed directly to the plasma by a mechanism referred to as "charging". Charging is the condition where gate conductors collect a charge from the plasma which in turn forms electric potentials across the wafer [2,3,4]. If the voltage at the gate is sufficiently high, then the current will discharge through the gate oxide by Fowler-Nordheim tunneling or, at the highest voltage levels, will result in breakdown of the oxide.

Antenna structures have been used in previous studies to investigate the effects of charging [2]. In their simplest form antennas are large metal or polysilicon features on the surface of the wafer which cover a smaller gate region. The charge is then collected over the entire antenna area while discharge is focused through a smaller gate area.

This damage results in several negative effects for CMOS devices including; shifts in threshold voltage [5], increased gate leakage current[3], decreased oxide breakdown voltage[2], and general yield loss. Increased leakage current and oxide breakdown can both be studied with simple capacitor devices which employ antenna ratio structures [6]. Furthermore, if the metal layer completely covers the thin gate oxide, the device will be protected from damage caused by UV radiation and ion bombardment and the effects of charging can be isolated [1,2].

Damage is believed to occur primarily during the over-etch period of plasma processing [2]. For photoresist ashing, this is the time when the metal gates are directly exposed to the plasma. For polysilicon and metal etching, the devices are also most vulnerable during over-etching because at this time the gate structures become isolated from each other.

EXPERIMENTAL DESCRIPTION

Two experiments were designed to test for charging and direct exposure damage using the RIT GEC plasma cell. First the effects of charging were studied by building capacitor like antenna devices (see figure 1a). These devices required two lithography steps to open holes in the field oxide for gate oxide growth and to pattern the Al antennas. A second device which uses only a thin oxide with no field oxide was fabricated to study direct exposure effects (see figure 1b).

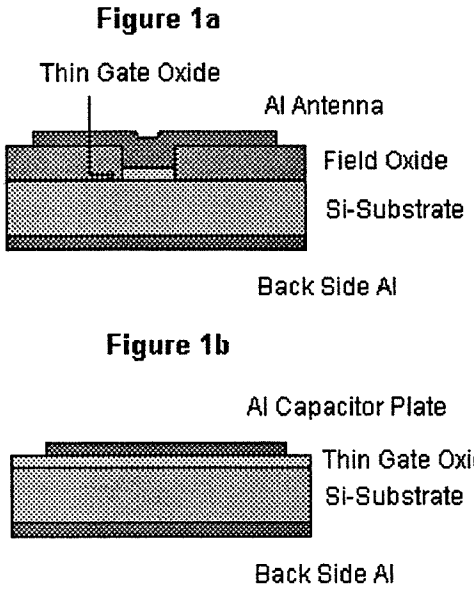

Figure 1. Side view of test structures. (a) Antenna structure used to test for plasma 'charging' damage. (b) Thin oxide structure used in 'direct exposure' damage experiment.

The charging test device was subjected to plasma processing (100 W, 200 mT, 30 sccm O_2) after fabrication was completed. This plasma was not intended to perform any function in device construction, its purpose was to simulate over etching conditions. Breakdown voltage was then measured using an HP4145B parameter analyzer.

The direct exposure test device were subjected to the experimental plasma (40 W, 200 mT, 30 sccm O_2) after the gate oxide growth. Surface charge analysis was performed using a Semitest SCA2500 before and after the plasma. These devices were then returned to processing to add the capacitor plates and back side aluminum. Finally, breakdown voltage was determined using the HP4145B parameter analyzer.

EXPERIMENTAL RESULTS

The antenna structure devices used in the 'charging' experiment were tested for shifts in breakdown voltage shifts. A linear decrease in average Vbd from 25 V at 0 minutes of exposure to 23 V at 20 minutes of exposure was observed as illustrated in figure 2.

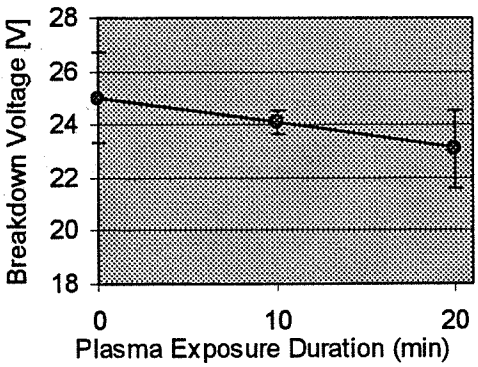

Figure 2. Charging experiment breakdown voltage measurements.

The 'direct exposure' devices were also tested for changes in breakdown voltage. Given the planar structure of these devices, applied voltage can easily be converted into electric field by dividing by the oxide thickness of 17.5 nm. The theoretical maximum for applied field before breakdown for SiO_2 is 10 MV/cm. A histogram of the measured values for devices tested on each wafer for 0 min, 2 min and 20 min plasma exposures is presented in figure 3. A control sample, labeled as 'no plasma' is also listed which yielded at approximately the theoretical maximum. The 0 min sample was placed in the plasma chamber for 10 min with gas flow but no power. A 10 min sample was also prepared but was destroyed during aluminum processing.

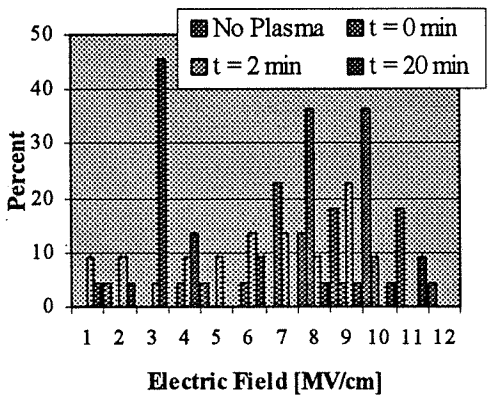

Figure 3. Direct exposure experiment histogram showing percentage of devices tested vs. the applied electric field required to cause breakdown.

A slight decrease in the electric field required to cause breakdown was observed for the 0 min. sample compared to the control sample. This is likely due to particulate contamination from the plasma chamber. However, most devices still tested in the high range (7 to 10 MV/cm). The 2 min. duration exposure sample exhibited a greater

number of failures at low electric fields in the 1 to 5 MV/cm range. Finally, the 20 minute sample showed the greatest number of devices breaking down in the low range.

The direct exposure devices were also measured after plasma processing with the Semitest SCA2500 surface charge analyzer to detect for changes in oxide charge concentrations. The control sample, 0 min., 2 min., and 10 min. plasma exposure duration samples all averaged +3E10 charges/cm^2. The 20 min. exposure duration sample, however, showed shifts toward –4E11 charges/cm^2 in a ringed pattern around the center of the wafer's radius (see figure 4).

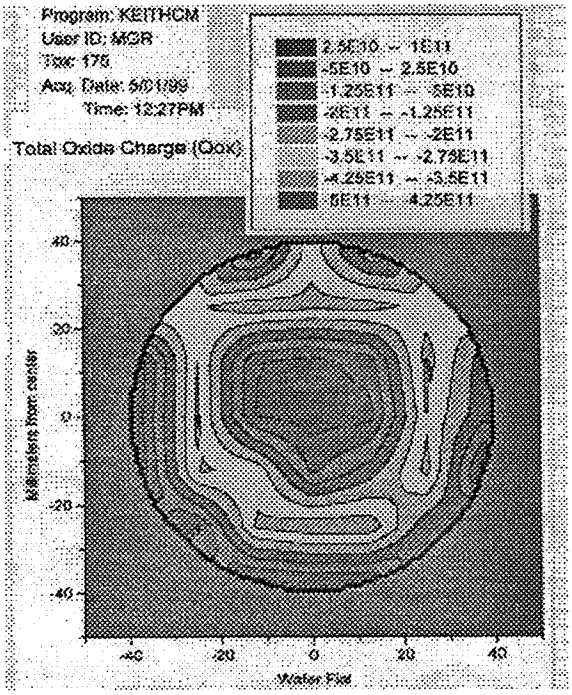

Figure 4. Output from suface charge analyzer for the 20 minutes of direct plasma expsoure sample showing the shift from +2E10 at the center and edges of the wafer to –4E11 in ringed pattern at mid-radius.

This pattern can be explained by the non-uniform electric fields believed to be generated in the plasma system.

CONCLUSION

Plasma damage occurring through a 'charging' mechanism was found to result in a lower breakdown voltages which decreased linearly with increased plasma exposure duration. Plasma damage occurring through a 'direct exposure' mechanism was found to result in both lower breakdown voltages and a shift in oxide charge density for the sample with the greatest plasma exposure duration (20 min). Therefore, plasma processes during CMOS fabrication should be optimized to minimize these negative effects on gate oxides.

ACKNOWLEDGMENTS

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