I-line Exposure Capability for 6 inch Wafers

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Abstract- The RIT Factory is currently in the development phase for a 6 inch sub-micron CMOS process. The addition of the Canon FPA-2000i1 stepper completes the necessary equipment required to perform a 6 inch photo process at RIT. The major focus of this project is to further the 6 inch photo process development, specifically to setup the exposure process for the first two levels (p-well and active) of the RIT test chip.

TV pre-align mark number 2 and auto-align mark 20P-4F were added to all eleven levels of the RIT test chip layout around the originally designed pattern area. The revised well and active designs were fabricated on a single mask, along with the Canon FRA marks. Six files were written and linked to the job files F983TC_WELL and F983TC_ACT, which can be run to perform the well and active exposures respectively. Well exposure is complete and tested; however, the active exposure will not align to the well pattern. This is most likely due to an error in the active level job and related data files.

1. BACKGROUND

The RIT factory currently fabricates P-well CMOS devices on 4" wafers. This process includes 11 photo levels, p-well through metal 2, and generates devices with a minimum gate size of 6 microns. The next generation of integrated circuits at RIT will be sub-micron CMOS devices, which will be fabricated on 6" wafers. This process is currently in the development phase.

Ground work for the 6" photo process has been underway for some time. The 6" coat and develop tracks are online. RIT recently acquired a Canon I-line wafer stepper, which completes the necessary photo equipment required for the future sub-micron CMOS process. Layouts exist for existing 4" CMOS devices and the design tools necessary for their modification are available. In addition, RIT has a fully functional mask fab, which can create reticles for use with the Canon stepper.

The Canon FPA-2000i1 is a 5X reduction stepper for 6" wafers, which exposes at a wavelength of 365 nm. It is capable of printing 0.5 micron features in conventional i-line photo resists and overlaying patterns to within 0.1 micron error. This exposure tool meets all of the requirements for RIT's future sub-micron CMOS process.

2. DESIGN

There are two major methods of alignment for the Canon. These are the TV pre-alignment (TVPA) and the wafer auto-alignment (AA). The TV pre-align is the initial alignment sequence. Two TVPA marks are measured with an optical camera and the wafer stage is adjusted according to the measured locations of these marks. The TVPA mark design implemented was the "TVPA Mark #2 – Canon Standard," which was chosen because it consumed less area than the alternate mark design. Below is a picture of the TVPA mark (Fig. #1) printed with active level photo. The numeral "3" is not part of the actual mark design. It is used to define the level the TVPA mark was printed for. In this situation the active level exposure prints the TVPA mark for level 3 (channel stop).

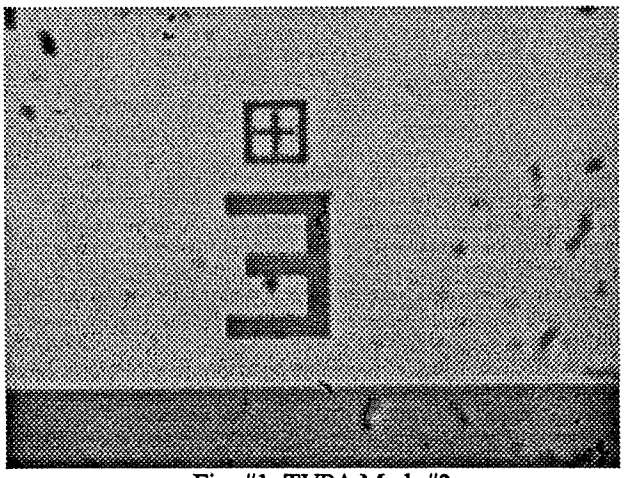

Fig. #1: TVPA Mark #2

The wafer auto-align is the second and final wafer alignment sequence. Four locations are measured on the wafer and two AA marks are measured per location, which account for x and y stage adjustments. AA marks are measured with two HeNe lasers. Shown below in figure #2 is AA mark 20P-4F. This particular mark design is more effectively measured in a degraded or "washed out" pattern. Unfortunately the HeNe laser is currently down; however, the Canon is capable of alignment using only the TV pre-alignment.

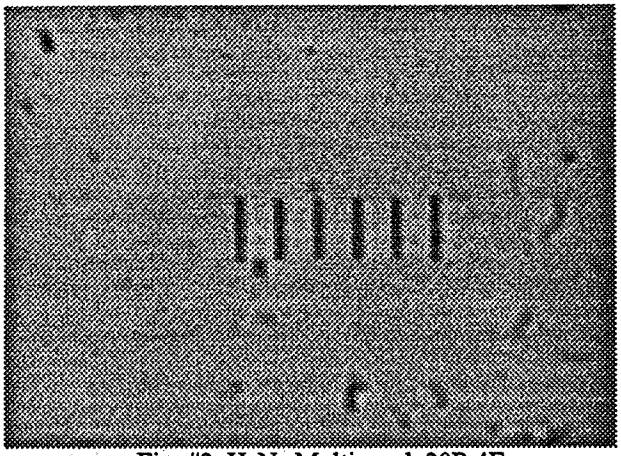

Fig. #2: HeNe Multi-mark 20P-4F

Figures #3 and #4 display the layouts for the p-well and active areas, which are levels one and two respectively. Each level in this 11 level CMOS process will contain it's own set of alignment marks, which are located outside the pattern area. Ideally one would want to always align to the level one pattern to minimize overlay error; however, if this pattern should become degraded to a point where the alignment marks cannot be measured, marks will be needed on the more recently process levels.

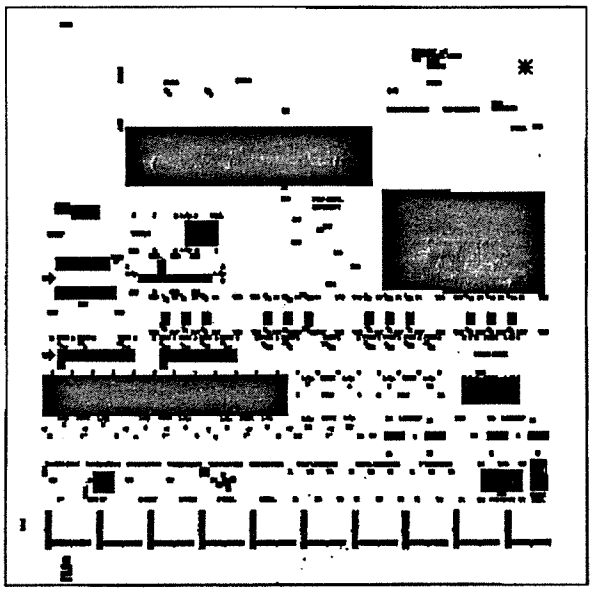

Fig. #3: Well Lvl. (5.7 mm^2 on wafer)

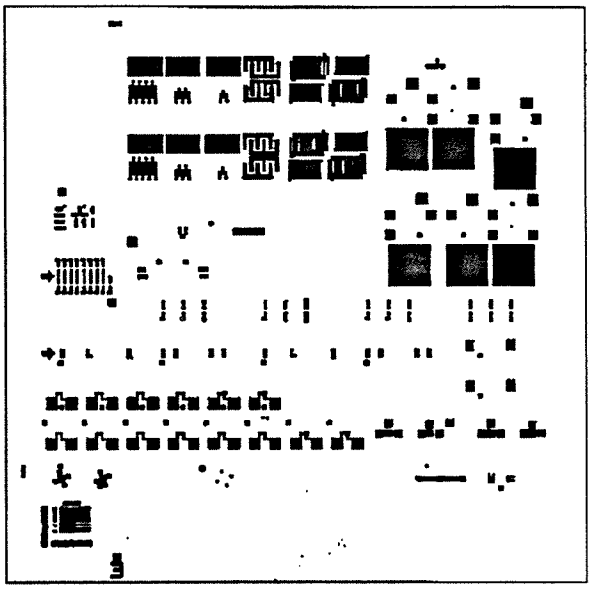

Fig. #4: Active Lvl. (5.7 mm2 on wafer)

The p-well and active patterns for the RIT p-well CMOS test chip can be fabricated on the same reticle. There is space for four separate levels on a single mask. The p-well pattern is dark field and the active pattern is clear field. Fine Reticle Alignment (FRA) marks were inserted outside the pattern area. Refer to figure #5 below for reticle layout.

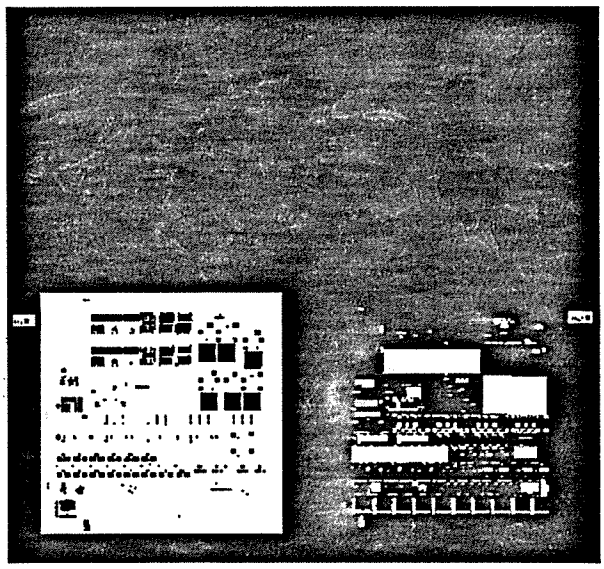

Fig. #5: Test chip P-WELL/ACT Reticle

The job files and the associated data files these jobs are linked to are listed below in figure #6. The process files contain the alignment sequence data. The shot files hold aperture blade settings, shot ordering, and default focus and exposure information. The layout file contains the

shot matrix and the reticle table lists the reticles used and reticle alignment data. The layout and reticle files are common for the entire test chip process.

F983TC_WELL (job file)
PF983TC_WELL (process file)
SF983TC_WELL (shot file)
LF983TC (layout file)
RF983TC (reticle table)

F983TC_ACT (job file)
PF983TC_ACT (process file)
SF983TC_ACT (shot file)

Fig. #6: Level 1 & 2 Exposure Jobs

3. RESULTS

The eleven level layout of the RIT test chip has been modified for use with the Canon. The remaining levels can be fabricated on as few as two reticles if metal 2 is not required.

Level one (p-well) exposure with the Canon is setup. Active level lithography remains incomplete. Useable pattern overlay could not be achieved. This problem is most likely due to an overlooked parameter in one of the job files created for the active level exposure.

The continuation of the 6" photo process at RIT will need to include active level job testing. The remaining test chip levels can be fabricated on 2 reticles and their respective job files need to be written. These files will be very similar to the active level job.

There are some optional repairs for the Canon, which are not required for processing; however, these modifications will improve equipment performance. The FRA lamp is out and if this is replaced the operator will be relieved of having to manually align masks. In addition, the repair of the HeNe laser would reduce overlay error, which is not a large issue for the test chip layout; however, the future sub-micron process will require tighter control of pattern overlay.