Chemical Mechanical Pad Characterization Using Shallow Trench Isolation Structures

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Abstract- In this study the effects of front-side pad composition were examined for a chemical mechanical polishing process. The examination involved evaluation of film removal uniformity across the wafer surface and within each die, dishing effects, and selectivity between silicon nitride and CVD oxides. Trenches were fabricated in the substrate via dry etch, the resultant depth was 1.5 μm. The trench backfill was accomplished with a CVD low temperature oxide. Best results were obtained using a dense single layer polish pad, which exhibited imperceptible dishing and wafer polish uniformity on par with all other combinations.

I. INTRODUCTION

Chemical mechanical polishing has been a recent advancement in processing technology which has allowed device design to consistently decrease the minimum feature size through global wafer planarization. This advancement has also been applied to device isolation structures such and Shallow Trench Isolation (STI). The trenches are used as electrical isolation between adjacent transistors on a wafer. Due to the nature of fabricating these trenches, CMP has dramatically increased the efficiency of such processes.

When attempting to planarize a wafer, careful selection of pad material can be the deciding factor between good planarity and surface smoothing. In general a denser pad material will produce a more planar surface which will allow for a more uniform resist thickness coating at the next lithographic step. A softer pad composition will result in a smoothing of any steps in the wafer surface, creating rounded edges where any steps may have been present. This will also allow for a more uniform resist coat, however, not to the same degree as a planar surface. The nature of a softer pad material allows the polish surface to conform to the features of the wafer topography and also promotes a smoother microscopic finish on the surface. Combining a dense pad on top of a softer conformal pad should yield a globally planar surface while conforming to the features to produce a surface smoothing effect. However, this conformal quality does not come without drawbacks. The conformal nature causes isolated step features to polish more rapidly than densely packed features. In a densely packed areas the features are better able to disperse the pressure from the polishing pad and thereby slow the polish rate.

Within both isolated areas and densely packed feature areas, another phenomenon, called dishing, occurs. Dishing is where a softer material will polish away faster than a harder material, and near the feature edges the conformal pad will round off these edges. The trench area will polish away faster as distances from the polish stop film increase.

Some early concerns for processing an STI process were the ability to completely refill the etched trenches. Early attempts included partial deposits of polysilicon due to non-conformal CVD oxide deposition. More recent methods include TEOS depositions or high-density plasma CVD. Both of which have enhanced conformality and better electrical properties than previous methods.

II. WAFER PROCESSING

Starting with bare silicon wafers, the first step was to grow a 700Å pad oxide. This serves as a stress relief layer between the silicon substrate and silicon nitride layer due to a mismatch of crystal structure size. This also helps to minimize wafer bow, which is induced by the silicon nitride layer. This oxide growth was accomplished in a dry O2 ambient.

The next step was to deposit the silicon nitride layer. This was accomplished in the CVD reactor where the nitride thickness was targeted at 1500Å. The purpose of the silicon nitride is to provide a polish stop layer once the LTO has been polished away in the areas surrounding the trenches.

The final processing step was to backfill the trenches with CVD low temperature oxide. This was accomplished with two back to back runs in the CVD system. In between the two runs, the order of the wafers was reversed to provide a more uniform

deposition across the lot. However, a significantly thick edge profile of oxide was deposited on the wafers. To minimize the polishing effect of the edge profile, the wafers were masked with photoresist in the center and the oxide was partially etched from the outer edges of the wafer.

Upon completion of wafer processing in the fab, the wafers were transferred into the CMP room. There the wafers were split into separate runs, where the two variables were the polishing pressure and the composition of the pad.

III. RESULTS

Extracting results from the wafers proved to be a difficult task. Most of the thickness measurements had to be taken only in areas which had one film on top of the substrate. Both the thermal oxide growth and the nitride depositon resulted in very uniform films with < 100Å deviation across the wafer for nitride, and < 25Å deviation across the wafer for the thermal pad oxide. The LTO deposition, however, was very non-uniform with approximately 3300Å thickness variation across the wafer surface. This made the polishing step very non-uniform as well, with endpoint detection being the most difficult portion of the polish process.

For the wafers that did receive the polish step, and were polished within reasonable time of endpoint, the typical results for wafers polished on the ESM-57 dense pad exhibited a dishing effect which was immeasurable from the SEM pictures. (see figure 1)

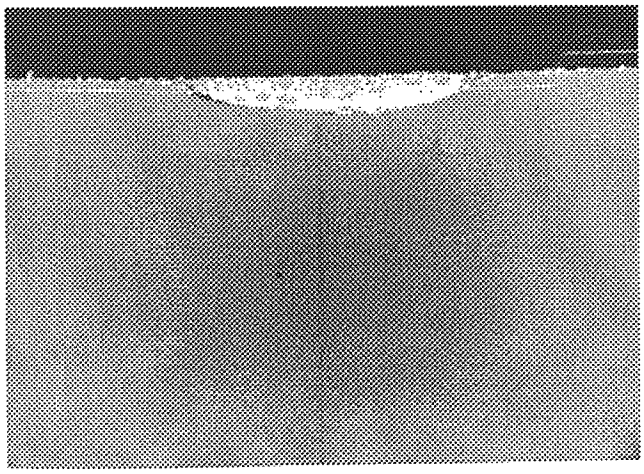

Figure 1. Sem Cross section of polished trench ESM-57 Dense single layer pad. (note immeasurable dishing effect)

As seen in figure 2, the stacked configuration of the IC-1000/SUBA-IV shows slight dishing effects. This dishing was measured to be 2100Å across the 5μm wide trench arrays. This dishing is due to the more conformal properties of the soft base pad.

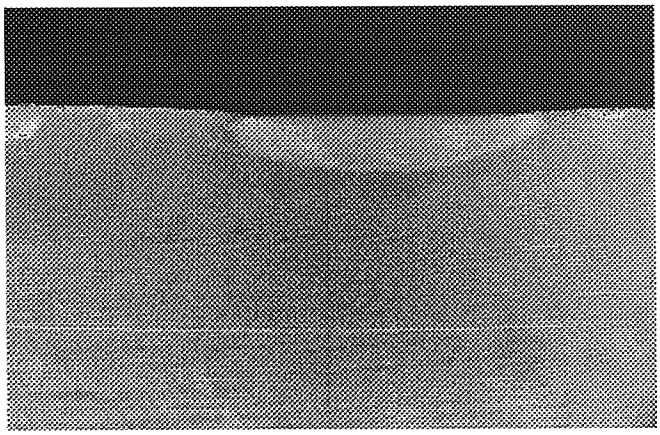

Figure 2. SEM cross section of post polish wafer. IC1000/SUBA-IV stacked pad. Visible dishing effects approx 2000Å across 5μm trench.

Both SEM pictures included are from wafers which were polished @ 5PSI pressure on the pad. For the dense pad, no change was observed for dishing at higher pressures. No additional SEMs were available for the stacked pad.

Other data collected for the pad configurations was the polish rates for both oxide and nitride. These results are compiled into figure 3. As the pad pressure increases, the polish rate also increases. The rates do not increase linearly, but exhibit a slower increase in polish rate with increasing pressure.

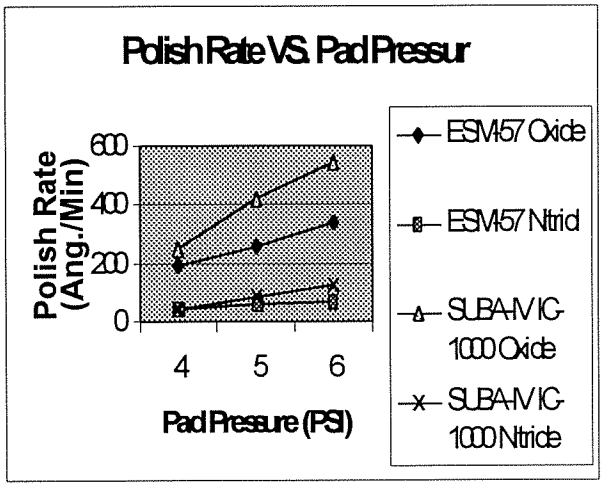

Figure 3 Polish rate for oxide and Silicon nitride films, pad dependant

IV. CONCLUSION

A dense pad will provide a more planar surface when polishing wafers. However, the stacked pad configuration provides smoother transitions between edge profiles of features on the wafer surface. Dishing effects were minimal on both pads, with the more dense pad exhibiting better performance. For better results, a better method of polish endpoint detection needs to be implemented, further work on thermal endpoint detection would yield more consistent results in the future.

Due to the better conformality of the stacked pad configuration, it would be the better choice for polishing. Especially in a case where a thick film deposition is needed (such as STI) the stacked pad will planarize the surface faster and allow for smoother transitions between step heights.

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