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Variable Gain Amplifier with Digital Control

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VARIABLE GAIN AMPLIFIER WITH DIGITAL CONTROL

by

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Approved by:

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Dedication

I dedicate this work to my family and friends, for all of their endless love, support and encouragement through out my career at Rochester Institute of Technology.

Declaration

I hereby declare that except where specific reference is made to the work of others, that all content of this Graduate Paper are original and have not been submitted in whole or in part for consideration for any other degree or qualification in this, or any other University. This Graduate Project is the result of my own work and includes nothing which is the outcome of work done in collaboration, except where specifically indicated in the text.

Diksha Singh

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I would like to thank my advisor, professor and mentor, Mark A. Indovina for his endless support, guidance, feedback, and encouragement which helped in the successful completion of my graduate research and studies.

Abstract

The design of CMOS variable gain amplifier (VGA) with digital control is presented in this project. The first stage of VGA is a two-stage op-amp connected in a voltage follower configuration with a series of resistors and transmission gates at the output followed by the second stage which consists of a two stage Op-amp in parallel with a series of transmission gates and resistors which is used to control the gain of the circuit. The two-stage op amp is designed using gm/Id methodology. The gain of this two-stage op amp is 80.34 dB, phase margin is 94.58º, input common mode range (ICMR) range is from $-893.21\ mV$ to $894.22\ mV$, output swing is from $-888.34\ mV$ to $872.13\ mV$. The gain of the variable gain amplifier ranges from -28.99 dB to 28.62 dB with power consumption of $6.80989512e^{-11}W$. The simulation is performed using Cadence Virtuoso in 45nm technology with a supply voltage range of $+900\ mV$ to $-900\ mV$.

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Chapter 1

Introduction

The Automatic Gain Control (AGC) circuit maintains a constant output signal amplitude after amplification regardless of fluctuation of levels of the input signal. The AGC circuits are used in many applications. Few of the applications namely are disk drives, bio-medical devices like the hearing aids, sensitive microphone pre-amplifiers, regulators and so on The constant amplitude of the signal is achieved at the output by providing stronger amplification for the weak signals and weaker amplification for the stronger signals and thus maintaining a constant amplitude at the output. The variable gain amplifier (VGA) is the indispensable part of the Automatic Gain Control circuit. The amplitude of the output is varied by controlling the gain of the amplifier. The gain of the amplifier can be controlled by either an analog signal or by a digital signal. In general, the voltage gain amplifiers exhibits exponential gain characteristics to portray a wide dynamic range.

In the past, the amplifiers in the VGA was designed based on the exponential I-V characteristics of the BJT. With the evolution of the MOSFET's, the amplifiers could be designed using two methods. The first method is to use the MOSFET in the sub-threshold conditions which gives an exponential relation like that of the BJT's. The second method is to obtain the

relative exponential function with the MOSFET's in the saturation region. In this project we use the MOSFET based operational amplifier along with the transmission gate switches and resistors to design a VGA.

1.1 Project Goals

The primary intent of this project is to design a VGA that could subsequently be used in an Automatic Gain Control circuit. Shown below is a summary of the leading project goals:

- To understand the working of the VGA.
- To design the operational amplifier to build the VGA and design the top-level circuit for varying the gain of the circuit.
- To simulate the circuit for its effective in operation and understand the results.
- To design the layout of the sub circuits and integrate them at the top level layout and get a LVS/DRC clean layout.

1.2 Contributions

The significant contributions to the projected are listed below.:

1. Designing the operational amplifier to meet the required specifications of closed loop gain, phase margin, Common mode gain, Common mode rejection ratio, Input common mode range, output voltage swing.
2. Designing the transmission gate switches to pass to reject the input based on the input signals.

3. Designing the VGA to vary the gain from -28dB to +28dB.

4. Designing the layout considering the process variations to match the schematic.

1.3 Organization

The structure of the project is as follows:

- Chapter 2: This chapter discusses about the design methodology using references to journals/articles wherever required.

- Chapter 3: This chapter explains about the different sub-circuits necessary to build the VGA and the top level integration of the sub-blocks to design the VGA.

- Chapter 4: The chapter goes into the test bench setup for simulation of the various sub-blocks of the VGA and finally discusses about the simulation for the top level circuit design where the sub-blocks are integrated to design the VGA.

- Chapter 5: This chapter explains in depth analysis about the results obtained in the simulation.

- Chapter 6: This chapter explains about layout of the various sub-blocks of the VGA and the integration of the top level layout of the VGA design.

- Chapter 7: This chapter outlines the conclusion of the study and possible ways of extending it.

Chapter 2

Design Methodology

2.1 Variable Gain Amplifier

One of the methods of realizing a Variable gain amplifier is using a two stage operational amplifier with class AB amplifier at the output stage and controlling the output impedance to vary the gain of the VGA. The two stage operational amplifier can be designed using the the gm/Id analogy to design the sizes of the transistors. In this operational amplifier, the first stage is a differential amplifier which is non-tailed followed by a second stage class AB amplifier which has miller compensation. The gain of the amplifier can be varied by controlling the output resistance of the second stage of the operational amplifier. Fig.2.1 shows the operational amplifier designed for acting as the voltage gain amplifier by controlling the output impedance. The special features of this operational amplifier circuit is that it is a non-tailed configuration with symmetrical structure, it is highly insensitive to common mode variations and has a high output voltage swing, the input pair is cross-coupled bulk driven pairs which is truly differential. The majority of the gain is achieved in the second stage of the circuit. The gain of the circuit is controlled by giving a gain control voltage to the gate of the PMOS of

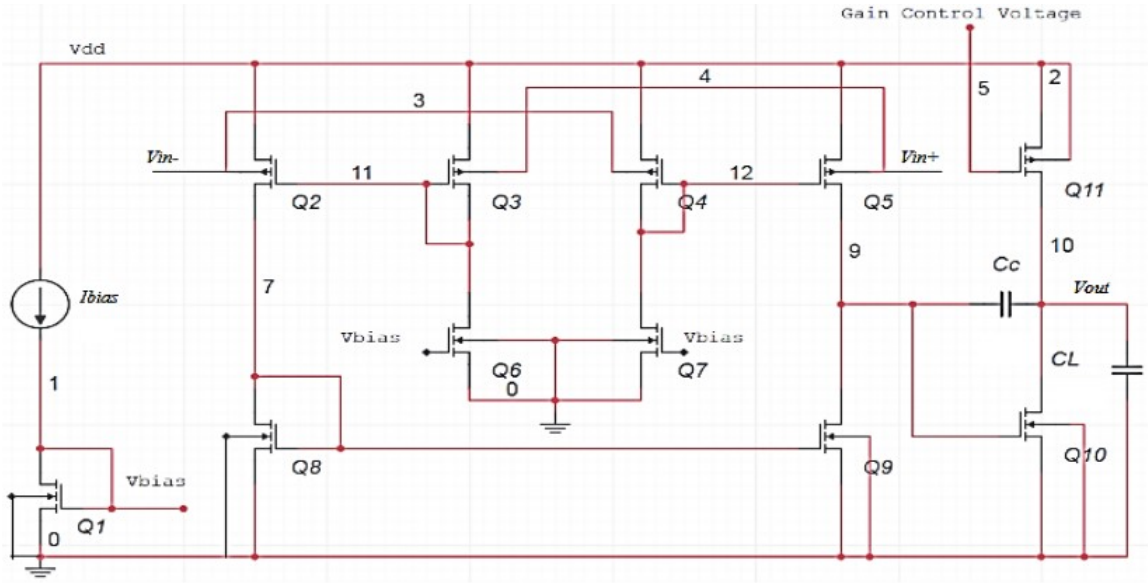


Figure 2.1: Op Amp Circuit Diagram [1]

the second stage of the amplifier. This voltage given to the gate of the PMOS transistor in turn controls the value of the output impedance of the operational amplifier. This control of the output impedance of the circuit controls the gain of the amplifier. The major dis-advantage of this proposed variable gain amplifier is that it has limitations with respect to the gain and the gain bandwidth product.

2.2 Variable Gain Amplifier using CCII

The second-generation current conveyor (CCII) is a useful building block that is used in a wide range of high-frequency current mode applications to implement analog signal processing circuits and systems such as amplifiers, oscillators, filters, and nonlinear circuits. CCII is a three-terminal device, and it is characterized by port relation, expressed by a matrix as shown

in equation 2.1.

$$\begin{bmatrix} i_y \\ v_x \\ i_z \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ 1 & 0 & 0 \\ 0 & \pm 1 & 0 \end{bmatrix} \begin{bmatrix} v_y \\ i_x \\ v_z \end{bmatrix} \tag{2.1}$$

It is stated that a voltage is applied to terminal Y, an equal potential will appear on terminal X. (i.e. $v_x = v_y$) An input current i_x being forced into terminal X will end in an equal amount of current conveyed to output terminal Z. Potential at X being set by Y is independent of the current being forced at X. Port X can be used as voltage output or as a current input port. Therefore, this current conveyor is often used to process both voltage and current signals.

CCII is used to overcome the drawbacks of the first-generation current conveyor (CCI). CCII offers high input impedance at voltage input port Y which results in avoiding the loading effect. There are two ways to implement the CCII in CMOS. The first is class A topology and the second is class AB topology. Class AB provides better bandwidth, stable voltage/current gain, and bidirectional current output. Due to this reason, CCII is designed using class-AB topology.

The second-generation current conveyors (CCII) exhibit high linearity, wide dynamic range, and high performance under low power operation. It also exhibits high current following actions over the wide bandwidth. But due to high impedance at current node X, the voltage following action is bad. To overcome the high impedance, there are multiple methods. The first method is the constant potential technique and the disadvantage is that it requires class A amplifier. The second method is the current feedback technique and the disadvantage of this is the PMOS and NMOS pair have to be matched. The third method is the voltage feedback based on op amp architecture which can be realized using class-AB CCII architecture. Because of this feedback configuration, the impedance at the current input node is made small by increasing the open-loop gain of the voltage amplifier in the feedback loop configuration

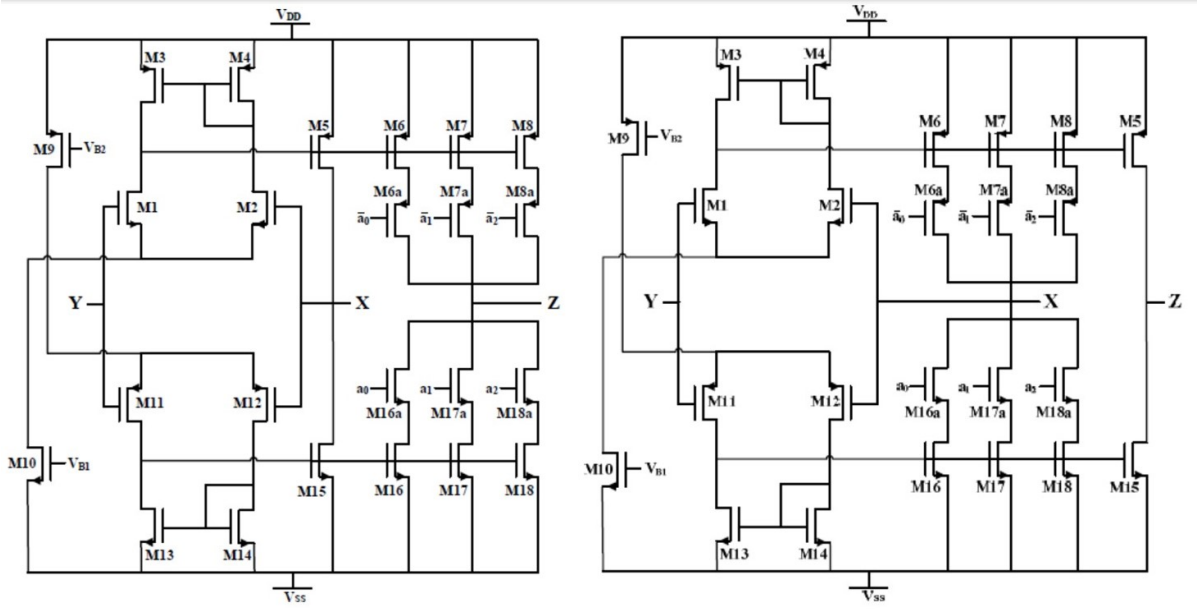


Figure 2.2: CMOS realization of the DPCCII block with (gain K) and (gain K^{-1}) [2]

which results in less bandwidth because of gain-bandwidth limitations. Fig.2.2 shows the design of Variable gain amplifier of two stages using CCII. In this circuit topology, the VGA is based on two digitally programmable second generation current conveyors (DPCII). This first digitally programmable CCII is used to provide gain greater and equal to one (*gain K*). The second DPCII gives a gain of less and equal to ONE (*gain* K^{-1}).The CCII circuits uses transistor arrays and MOS switches for gain via a n-bit code-word.

2.3 Improved Dynamic Range VGA

The third different topology of the variable gain amplifier consists of two stage operational amplifier, transmission switches and resistors. In this design, the first stage is a two stage operational amplifier which is connected in unity gain feedback configuration. The second stage uses a resistor string ladder with operational amplifier. The second stage of this topology contributes to the maximum gain of the variable gain amplifier. The operational amplifier

for this topology consists of a differential stage as the first stage followed by the class AB amplifier as the second stage. The class AB amplifier is selected for the second stage because of high output voltage swing. The resistor ladder values are chosen based on the exponential functions of R, $e^{-1.68}R$ and $e^{+1.68}R$. The transmission switches control the selection of the resistor ladders and that controls the gain of the variable gain amplifier. The advantage of using this Variable Gain amplifier is that it is immune to input common mode signals, high output voltage swing and has high gain. The variable gain amplifier circuit topology has been described in detail in this project.

Chapter 3

Circuit Description

The designed CMOS Variable Gain Amplifier (VGA) is composed of two inverting stages. The first stage of VGA is an inverting amplifier with an input and feedback resistor forming a voltage divider network. The second stage is also an inverting amplifier with different combinations of switches and resistors at the negative input and output terminal.

In this circuit, the first stage of VGA is in unity gain configuration due to which the voltage gain of the 1st stage is always 1. However, the 2nd stage of VGA decides the overall gain in this circuit. The total gain of the circuit varies its gain depending on the digitally controlled voltage given by the different combinations of switches and resistors values. This circuit provides gain selection in gradual increments. There are multiple ways that this circuit can be designed, having certain components in the circuit remaining the same. The simplest circuit is having a toggle switch connected between the feedback resistor which provides different gain settings. With the multiple switches and resistors setting, each switch can turn on a particular resistor which in turn controls the gain of the amplifier. The block diagram of VGA is shown in Figure 3.1.

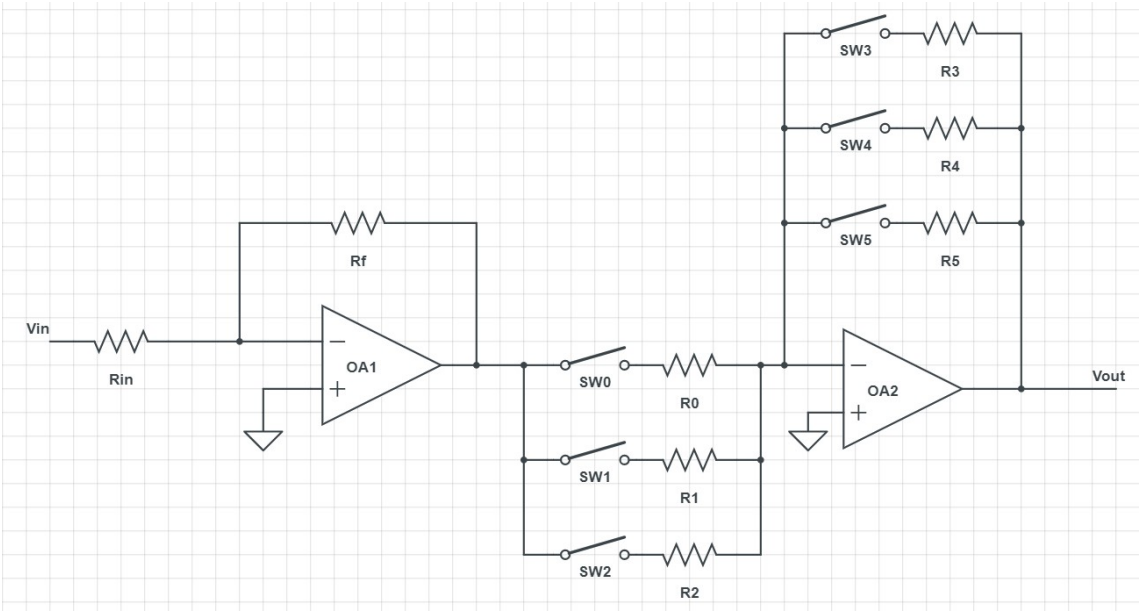


Figure 3.1: VGA - Block Diagram [3]

3.1 Inverting Amplifier

The inverting amplifier is an amplifier in which there is a feedback signal from the output connecting to the input to have a closed loop configuration. In the Inverting amplifier the voltage between both the inputs stay at the same potential and they do not vary because of a concept called the virtual ground. The concept of virtual ground is that the feedback and the input are at the same potential at the negative input and the the positive input is tied to ground. Due to this concept of virtual ground, the potential of both the positive and negative terminals stay at the same voltage.

In the inverting amplifiers there is no current at the input terminals thought in the real world there is always some minute current flowing into these terminals. The output of the inverting amplifier is at a 180° phase shift with respect to its input. This means that when the input is negative, the output is positive and when the input is positive the output is negative. In the

inverting amplifier the input in connected to the negative terminal of the op-amp through a resistor. The output of the op-amp is given as feedback to the negative terminal through a resistor which stabilizes the circuit. The necessity of adding the input resistor is to separate the input signal from the feedback signal. The Fig. 3.2 shows the inverting amplifier configuration.

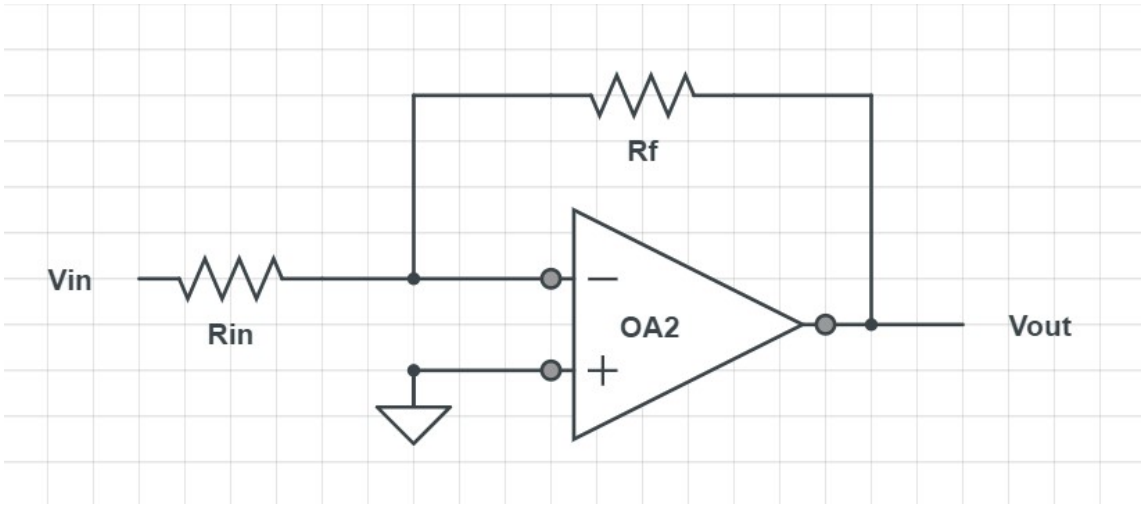


Figure 3.2: Inverting Amplifier - Block Diagram

The gain equation of the inverting amplifier is given by,

$$A_v = -\frac{R_f}{R_{in}} \tag{3.1}$$

The gain equation of the inverting amplifier has a negative sign, and this negative sign indicates that the output is negative or has an inversion of 180° in phase.

3.2 Inverter

The inverter is a circuit which changes the polarity of the input signal. There are so many ways to design an inverter. The design of the inverter used in this project consists of a PMOS and

NMOS in which the drains are connected together to give the output. The input is tied to the gate of the transistors. The source and the body of the PMOS is connected to the VDD and the source and the body of the NMOS is connected to the VSS. If the voltage at the input is low, the NMOS is turned off and the PMOS is turned on and this allows the electron flow through the gate of the PMOS transistor and thus giving out high voltage. Similarly if the voltage at the input is high, the NMOS is turned ON and PMOS is turned off and this stops the flow of electrons and thus the voltage at the output remains low. This concept produces an output that inverts the input signal.

The major advantages of the CMOS inverter is that the power dissipation is very low except for that of the power dissipated due to leakage currents, the voltage characteristic curve is relatively very sharp, the noise is very low and this in turn rejects unnecessary frequency spikes. The CMOS logic inverter diagram is shown in Figure 3.3.

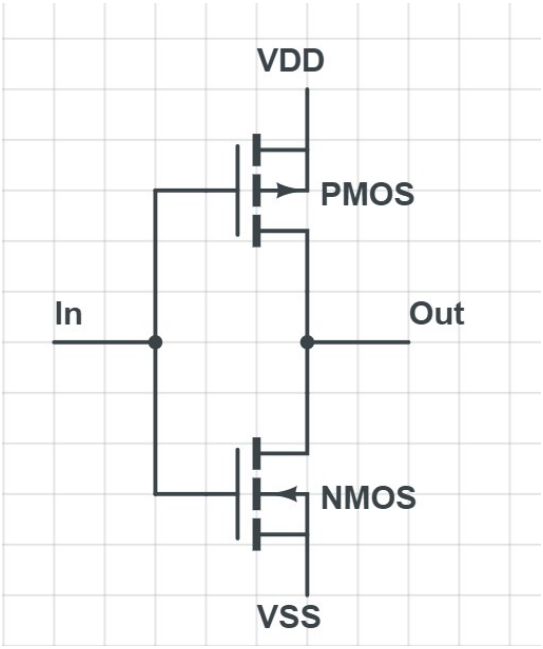


Figure 3.3: CMOS Logic Inverter - Block Diagram

3.3 Transmission Gate Switch

The transmission gate switch consists of a transmission gate and an inverter In the transmission gate the drains of the PMOS and NMOS are connected together and act as the output. The sources of the PMOS and the NMOS are connected together and this acts as the input signal. The control signal (V_c) is given to the gate of the NMOS. The input control signal is flipped using an inverter before feeding to the input of the gate of the PMOS transistor. The body of the PMOS is connected to the VDD and the body of the NMOS is connected to the ground of the circuit.

The basic concept of working of the transmission gate is that the PMOS does not pass 0 but strong 1 and NMOS does not pass 1 but strong 0. In the transmission gate, this concept works simultaneously.When the control signal is 0, the gate of the NMOS is low and the gate of the PMOS is high and this in turn does not turn ON the transistors and thus the input is not passed on to the output irrespective what voltage is given as input. When the control signal is 1, the gate of the NMOS is high and the gate of the PMOS is low and in turn turn ON both the transistors and conduction of the transmission gate occurs and thus the input is passed on to the output. The major applications of the transmission gate switches are in the multiplexers, logic circuits, electronic switches. The Figure 3.4 shows the circuit of the transmission gate switches.

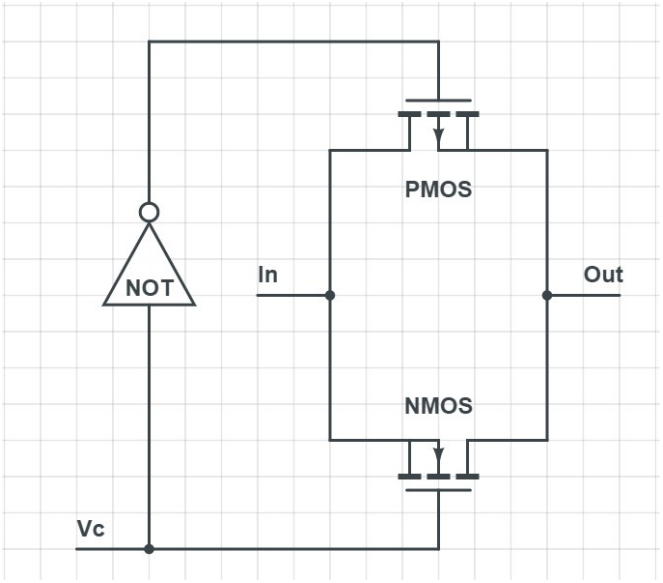


Figure 3.4: Transmission Gate Switches - Block Diagram

3.4 Two Stage Operational Amplifier (Class AB Output Stage)

Operational Amplifiers are one of the most useful electronic circuits. The operational amplifier is a circuit that amplifies the difference in the inputs and gives an output that is multiple times larger than the input voltage difference. Op-amps are used in a wide variety of applications. The ideal operational amplifier has infinite bandwidth, zero output impedance, zero noise, infinite open-loop gain, infinite input impedance, zero offset voltage. In the real world, it is impossible to obtain the ideal op-amp due to technological restrictions. The Op-amp designed in this paper is a two-stage op-amp with a PMOS differential input pair and single-ended output and it is designed using $\frac{gm}{I_d}$ methodology in 45nm technology.

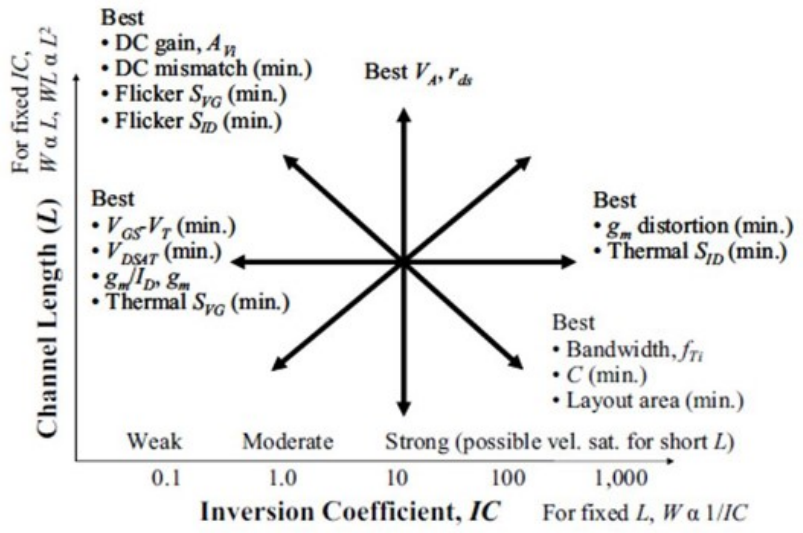
The $\frac{gm}{I_d}$ [6, 7] method considers the ratio between transconductance over dc drain current and the normalized drain current is used as a design tool to calculate the width of the transistor. This method helps to find the operating region of the MOSFET. The convenient approxima-

tions of weak, moderate, and strong inversion are 20,10, and 5. Figure 3.5 shows the trade-offs and optimization in Analog CMOS design [8].

In weak inversion ($IC < 0.1$), when the $\frac{gm}{I_d}$ ratio is large. The drain current (I_d) starts to decrease with an increase of channel length modulation (L) which results in large device sizes and layout area (WL, W), high transconductance (gm), high intrinsic gain (A_v), low bandwidth (ft), low V_{dsat}, $V_{gs} - V_t$, and minimum DC mismatch, flicker noise, and thermal noise voltage.

In moderate inversion ($0.1 < IC < 10$), Channel length modulation (L) is moderately short which results in moderately small device sizes and layout area (WL, W), moderately high transconductance (gm), intrinsic gain ($gm * r_{ds}$) and bandwidth (ft), moderately low V_{dsat}, $V_{gs} - V_t$, and better V_a and r_{ds}. It is a good compromise in terms of speed, gain, and power consumption.

In strong inversion ($IC > 10$), Channel length modulation (L) is short which results in small device sizes and layout area (WL, W), low transconductance (gm), intrinsic gain ($gm * r_{ds}$), and high bandwidth (ft), V_{dsat}, $V_{gs} - V_t$, and minimum gm distortion and thermal noise current. In strong inversion ($IC > 10$), Channel length modulation (L) is short which results in small device sizes and layout area (WL, W), low transconductance (gm), intrinsic gain ($gm * r_{ds}$), and high bandwidth (ft), V_{dsat}, $V_{gs} - V_t$, and minimum gm distortion and thermal noise current.



Weak Inversion	**Moderate Inversion**	**Strong Inversion**
IC < 0.1	0.1 < IC < 10	IC > 10
Device Size (W, WL) - Large	**Device Size (W, WL)** - Moderately Small	**Device Size (W, WL)** - Small
Bandwidth (ft) - Low	**Bandwidth (ft)**- Moderately High	**Bandwidth (ft)** - High
g_m/I_d - High	g_m/I_d– Moderately High	g_m/I_d- Low
g_m - High	g_m - Moderately High	g_m - Low
V_{DSAT} , $V_{GS} - V_T$ - Low	V_{DSAT} , $V_{GS} - V_T$ - Moderately low	V_{DSAT} , $V_{GS} - V_T$ - High
Channel Length (L) – Large	**Channel Length (L)** – Moderately Short	**Channel Length (L)** - Short
Layout Area – Large	**Layout Area** – Moderately Small	**Layout Area** – Small
Intrinsic Gain - High	**Intrinsic Gain** – Moderately High	**Intrinsic Gain** - Low
DC mismatch Flicker Noise Thermal Noise (Voltage) Minimum	**Better** V_A and r_{ds}	**gm distortion Thermal Noise (Current)** Minimum
-	Good for power-efficient and low voltage design	Difficult for power-efficient and low voltage design

Figure 3.5: Trade-offs and Optimization in Analog CMOS Design [4]

The designed CMOS op-amp consists of three blocks, differential input stage, second gain stage, and bias string (current mirror). Figure 3.6 shows the block level representation of two-stage op-amp with miller compensation.

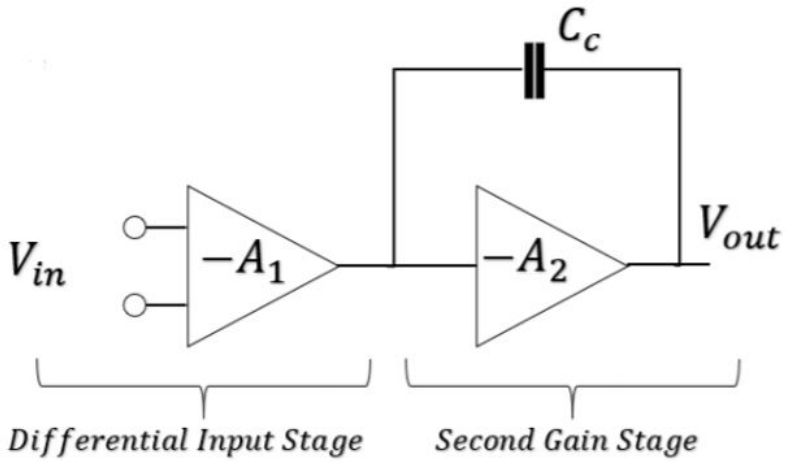


Figure 3.6: Two Stage Op-amp - Block Diagram

3.4.1 Differential Input Stage

In an op-amp, the differential input stage amplifies the difference between two input signals and also eliminates the common-mode input voltage applied to the input stage. The gain of an amplifier can be increased by either increasing the number of gain stages or the transconductance of the input differential pair and second gain stage. The differential input gain stage consists of M1, M2, M3, and M4 of the op-amp where M1 and M2 are the PMOS differential input pair which allows better ICMR closer to the lower voltage rail of ground (GND) and M3 and M4 are current mirrors active load which gives a very large output resistance. Current in the transistor M1 and M3 is mirrored to transistor M2 and M4. The two important output resistance which contribute to the gain of the first stage are that of input transistor and active load transistors. The gain of this stage is given by the product of transconductance of the transistor M2 and the parallel output resistance of M2 and M4.

$$A_{v1} = g_{m2}\left(r_{o2}||r_{o4}\right) \tag{3.2}$$

3.4.2 Class AB output stage

The second gain stage is in the configuration of a class AB [9] where M7 and M8 provide additional gain in the amplifier. Output from the drain of M2 is fed as an input to the gate of M8 which amplifies the output of the first stage. Similar to the first stage, M7 is an active load that serves as the resistance of M8. The gain of the second stage is given in equation 3.3.

$$A_{v2} = g_{m7}\left(r_{o7}||r_{o8}\right) \tag{3.3}$$

The overall gain of the circuit can be calculated as shown in equation 3.4.

$$A_v = A_{v1} * A_{v2} \tag{3.4}$$

3.4.3 Current mirror (bias String)

The biasing of the transistor is achieved by M5 and M6 where it sources a certain amount of current based on their Vgs which is controlled by the bias string. M1 and M2 are biased by the current mirror (M5 and M6), in which the reference current is the dc bias of 10μA. Transistor M8 is biased by the active load M7.

3.4.4 Miller Compensation

In the CMOS op-amp, the miller compensation capacitor is connected between the input and output of the second stage. It is a technique that is used to increase phase margin for better stability in the system. It also helps to eliminate the right-hand pole (RHP) which occurs due to the introduction of zeros in the system. The compensation capacitance can be calculated as

shown in equation 3.5 where the capacitance load is 10pF.

$$C_c = 0.22 * C_L \tag{3.5}$$

Figure 3.7 shows the schematic of a two-stage op-amp (class AB output stage) with miller capacitance.

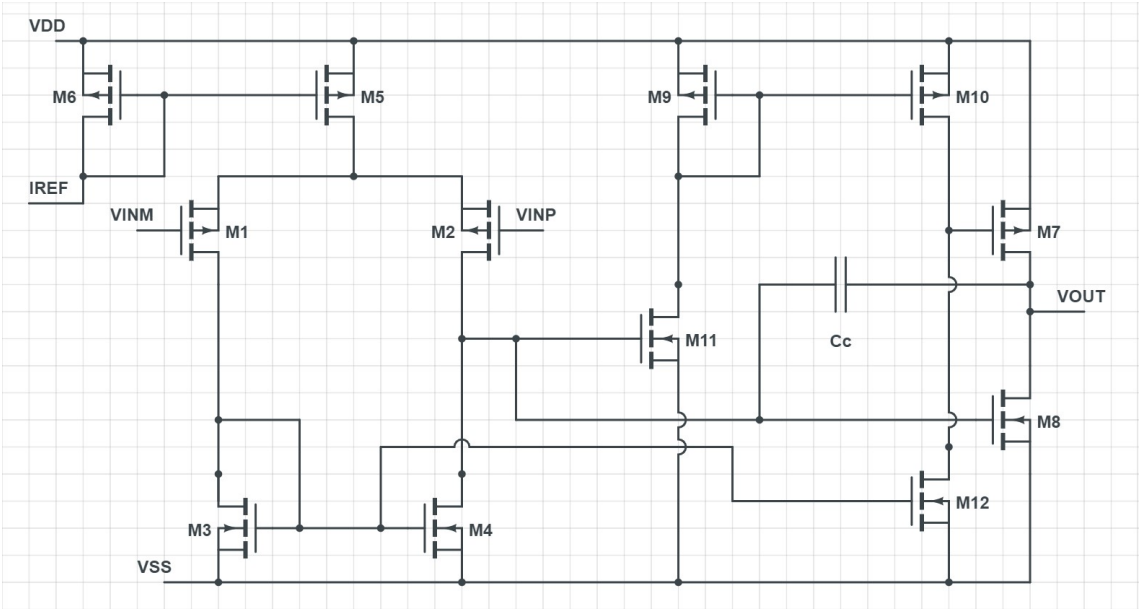


Figure 3.7: Two Stage Op-amp (class AB output stage) [5]

3.4.5 Common Mode Rejection Ratio (CMRR)

CMRR is the acronym of Common Mode Rejection Ratio. It is the ability of the amplifier to discard the common mode voltage at the input. In an amplifier the input signal with the same potential should be fed only to one input or both the inputs with different polarities. Unwanted signals like noise add up to the input of the amplifier and this common mode helps in eliminating such noise added to the inputs. In general the common mode of the differential

pair should be very very small. The differential gain should be very high compared to the common mode gain for a good differential amplifier.In ideal cases, the CMRR is expected to be infinite for an amplifier which is realistically not achievable in the real world. This is the exact reason why operational amplifiers are expected to have as high CMRR as possible.The measurement is made at the output to determine the common-mode gain (A_{cm}) which is then subtracted from the differential gain (A_d) in dB as shown in equation 3.6.

$$CMRR = A_d - (-A_{cm}) \tag{3.6}$$

3.4.6 ICMR

ICMR is the acronym of Input Common Mode Range. The ICMR is defined always relative to the supply voltages. This term describes the common mode signal range for the normal operation of the operational amplifier. Once the value of the common mode crosses the input common mode range, the output is non linear and becomes distorted. So it is always necessary to have the common mode voltage within the input common mode range. In PMOS differential input pair, the ICMR value is closer to the lower rail or ground. In NMOS differential input pair, the ICMR value is closer to the upper rail or the VDD.

3.4.7 Output Voltage Swing

Output Voltage swing is the maximum voltage that can be obtained for the output between the positive and the negative supply without clipping the signal while performing the intended operation of an operational amplifier. This output voltage swing varies based on the supply voltage and the output load impedance.The value of output voltage swing determines whether the amplifier is working as a source or a sink.

Chapter 4

Simulation

The chapter discusses the schematic and testbench setup of all the VGA components. The results of these simulations are discussed in the next chapter.

4.1 Inverter

The CMOS inverter circuit is designed by specifying the length and width of the PMOS and NMOS transistors. The length and width of these transistors are 180nm and 320nm as shown in Fig.4.1 Following the device instantiation, the connection is made through the wire, and also the pins are created for input, output, VDD, and VSS. The transient simulation is ran for 200n by setting up the stimuli for the input, VDD, and VSS. The VDD is set for 900 mV and the VSS is set for -900 mV. The input for the inverter is a square waveform with pulse width of 20ns and time period of 40ns ranging between 900 mV and -900 mV.

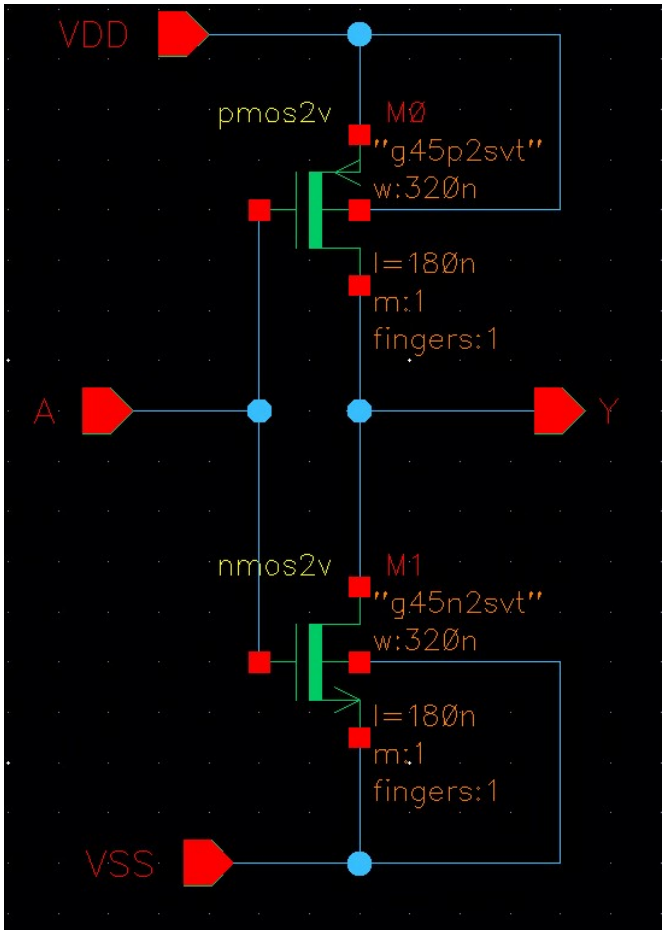


Figure 4.1: CMOS Inverter - Schematic

4.2 Transmission Gate Switch

The circuit of the Transmission Gate Switch consists of CMOS design. The devices are instantiated by specifying the length and width of the PMOS and NMOS transistors. The length and width of these transistors are 180nm and 320nm The Fig.4.2shows the captured results through histograms. shown in Fig.4.3.

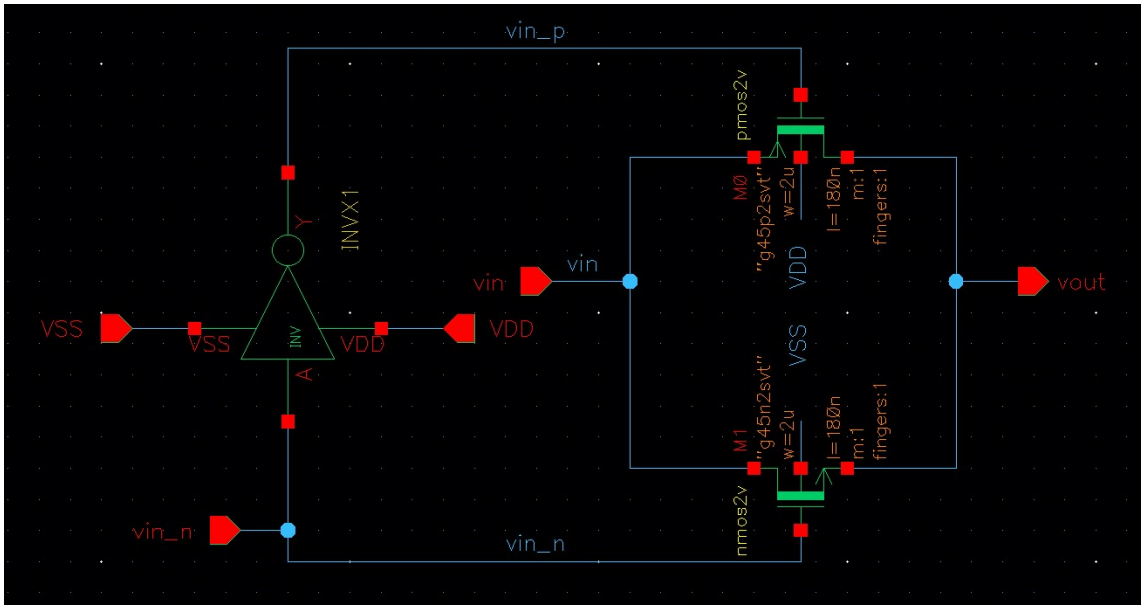


Figure 4.2: Transmission Gate Switch - Schematic

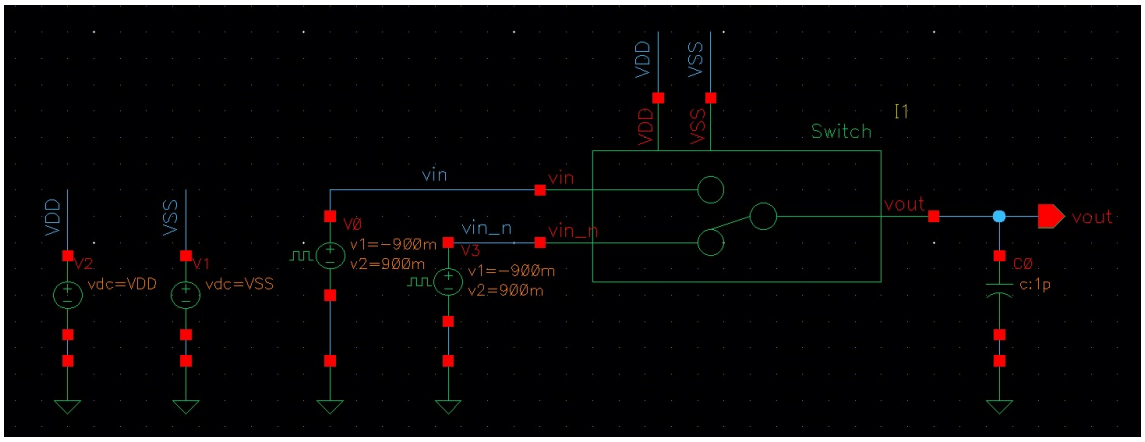


Figure 4.3: Transmission Gate Switch - Testbench

4.3 Two Stage Operational Amplifier (Class AB Output Stage)

The two stage op-amp circuit with Class AB output stage is designed as shown in the Fig.4.5 This Op-amp has PMOS differential input pair with PMOS current mirror and NMOS load. Class AB output stage is used to get high gain and high output swing.The testbench setup for the two stage operational amplifier is shown in the Fig. .4.4. The VDD is set at 900mV , VSS at -900 mV, IREF is set at 10 µA, sine waves with a frequency of 100 kHz and 10 kHz with amplitude voltage of 5 mV is provided as inputs to the op-amp. The sizes of transistors are summarized in Table.4.1. The length and width of the transistors are kept constant with only varying the multiplier of the devices. This is done so that the layout is uniform and the devices can abutted without any Design Rule Check errors.

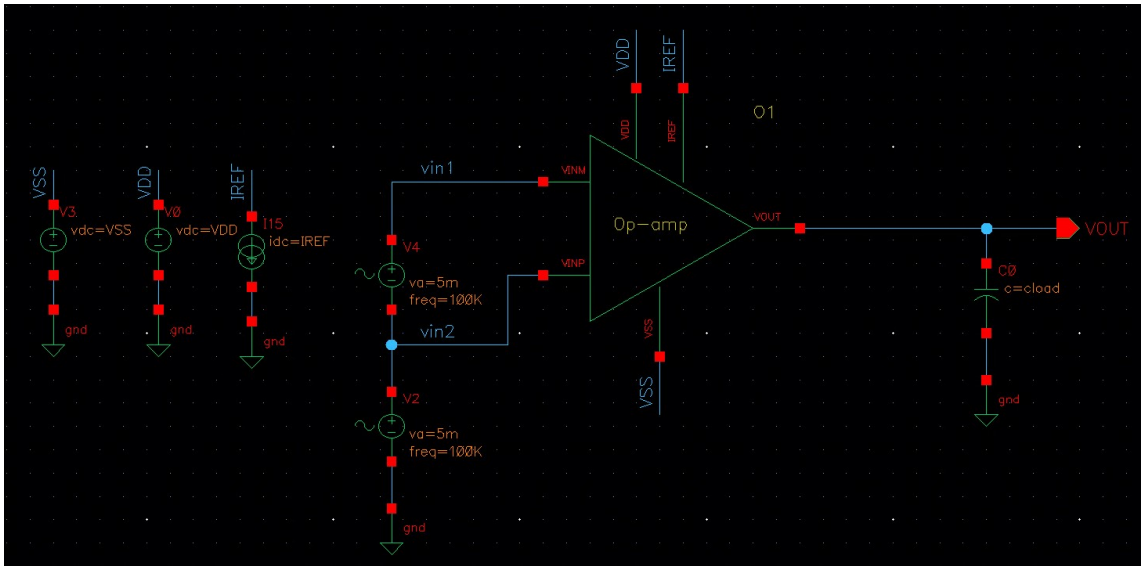


Figure 4.4: Two Stage Opamp - Testbench

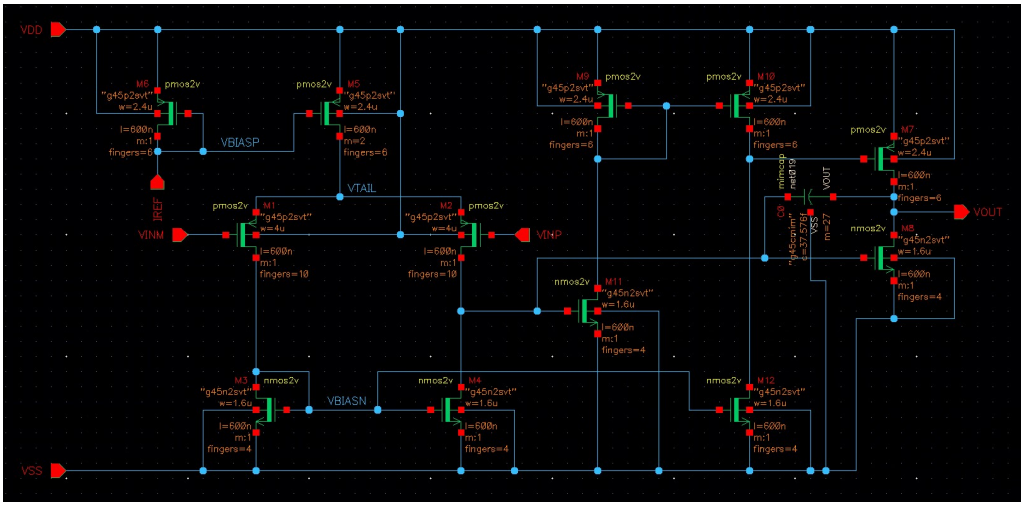


Figure 4.5: Two Stage Op-amp - Schematic

Table 4.1: Transistor Sizing

Transistor	Multiplier	Length	Width	Fingers
M1	1	600nm	400nm	10
M2	1	600nm	400nm	10
M3	1	600nm	400nm	4
M4	1	600nm	400nm	4
M5	2	600nm	400nm	6
M6	1	600nm	400nm	6
M7	1	600nm	400nm	6
M8	1	600nm	400nm	4
M9	1	600nm	400nm	6
M10	1	600nm	400nm	6
M11	1	600nm	400nm	4
M12	1	600nm	400nm	4

4.3.1 CMRR

Fig.4.6 show the testbench and result for CMRR(Common Mode Rejection Ratio). The configuration of the test bench is supplying both inputs with the common-mode DC voltage of 0 V with an AC peak to peak voltage of 1.8V, VDD at 900 mV, Vss at -900 mV, IREF at 10 µA with a capacitive load of 10 pF.

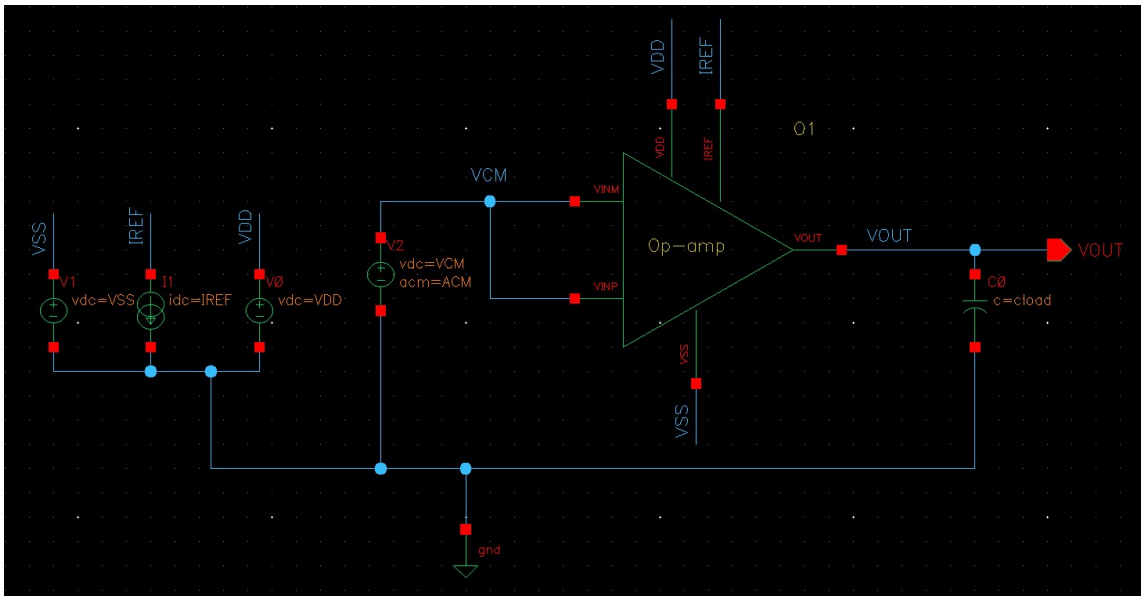


Figure 4.6: CMRR - Testbench

4.3.2 ICMR

Fig.4.7 show the testbench and simulation result of the input common-mode range (ICMR). For simulating the ICMR, the op-amp is set-up in unity gain feedback configuration with the positive input provided with a DC voltage of 0 V and AC magnitude of 5 mV, VDD at 900 mV, VSS at -900 mV, IREF at 10 µA and a capacitive load of 10 pF.

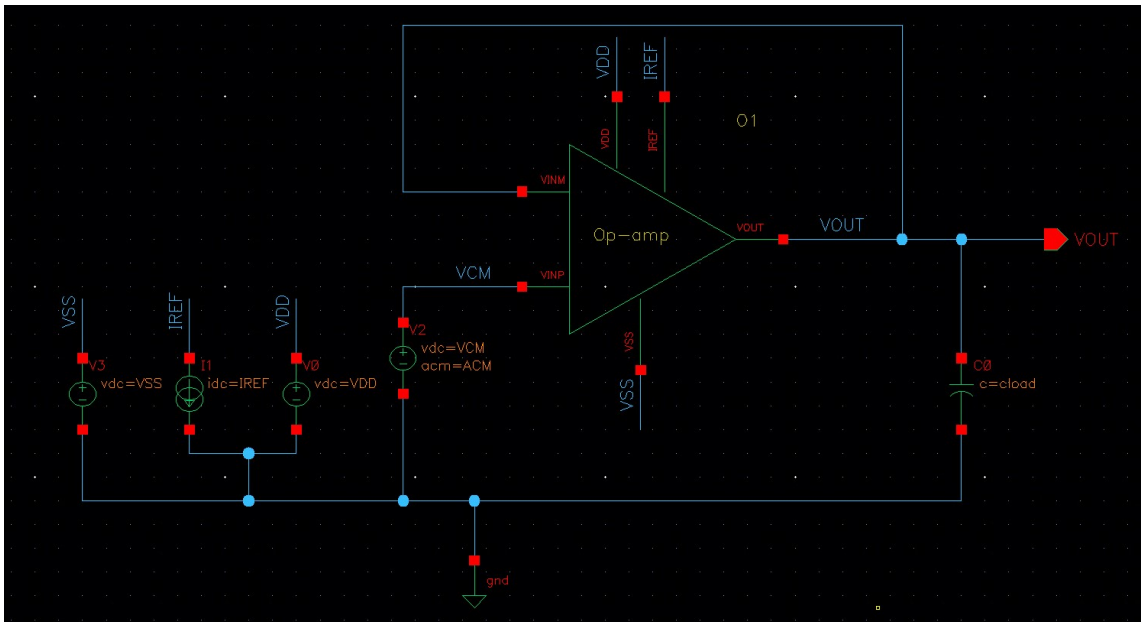


Figure 4.7: ICMR - Testbench

4.3.3 Output Voltage Swing

Fig.4.8 shows the testbench of output voltage swing. In the output swing test-bench the inputs of the op-amp are provided with sinusoidal signals with frequency of 10 kHz and 100 kHz with an amplitude of 5 mV. The supply voltage is set at 900 mV and -900 mV with the input reference current of 10 µA, capacitive load of 10 pF.

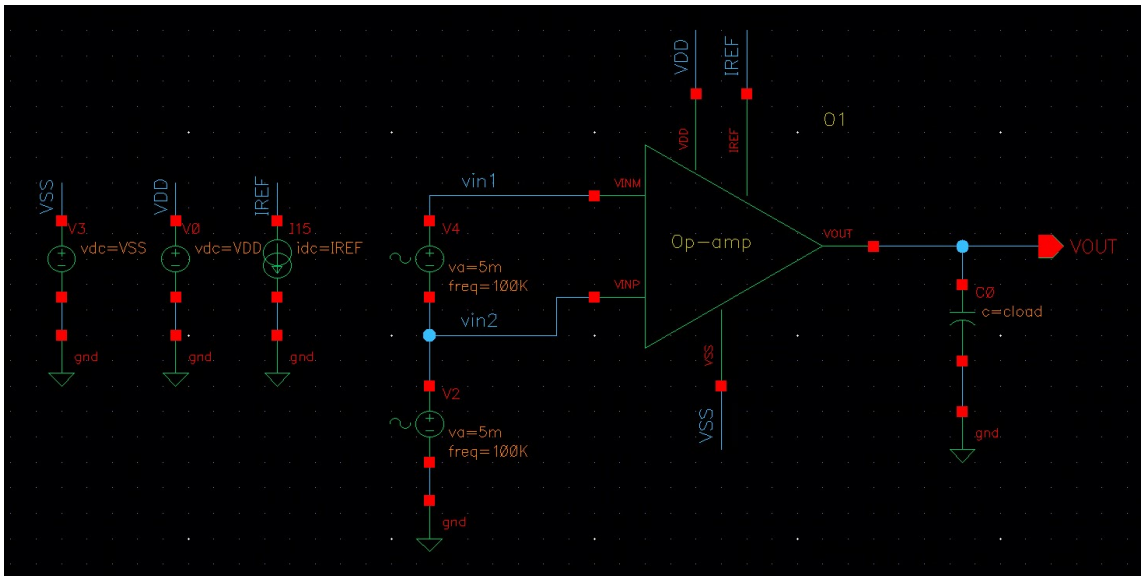


Figure 4.8: Output Swing - Testbench

4.4 VGA

The Fig 4.10 shows the circuit of the VGA.The VGA circuit is designed instantiating the operation amplifiers, transmission gate switches and the resistors. The resistors used in the VGA is made of poly resistors. Poly resistors are chosen for this circuit because poly is highly resistive in nature. The Fig 4.9 shows the the testbench setup for the Variable Gain Amplifier. In the testbench the supply voltages are set at 900 mV and -900 mV, input reference current is set at 10 µA with a capacitive load of 10 pF. The VGA inputs are setup based on the concept

of virtual ground. The positive terminal of the VGA is set to ground and the negative terminal is given a sine wave of 100 kHz with an amplitude of 5 mV. The switches S0, S1, S2, S3 ,S4, S5 are controlled by using a dc voltage of 900 mV and -900 mV. Whenever the switches are to be turned ON, they are supplied with a voltage of 900 mV and whenever the switches are to be turned off they are provided with a voltage of -900 mV.

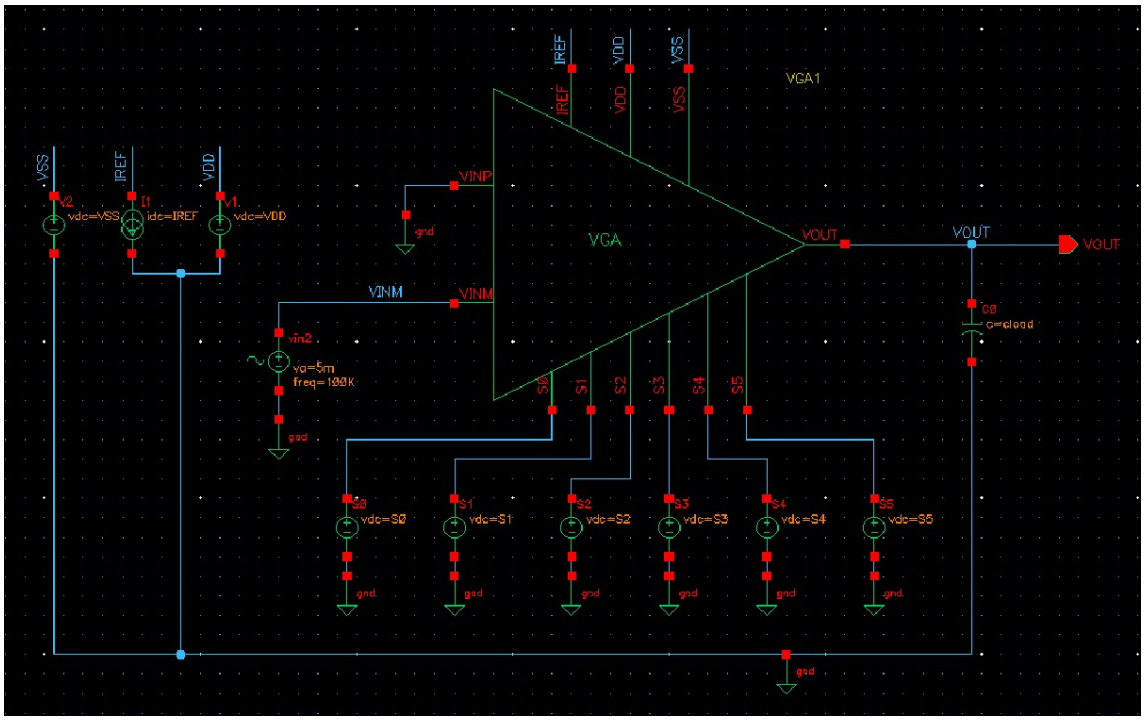


Figure 4.9: VGA - Testbench

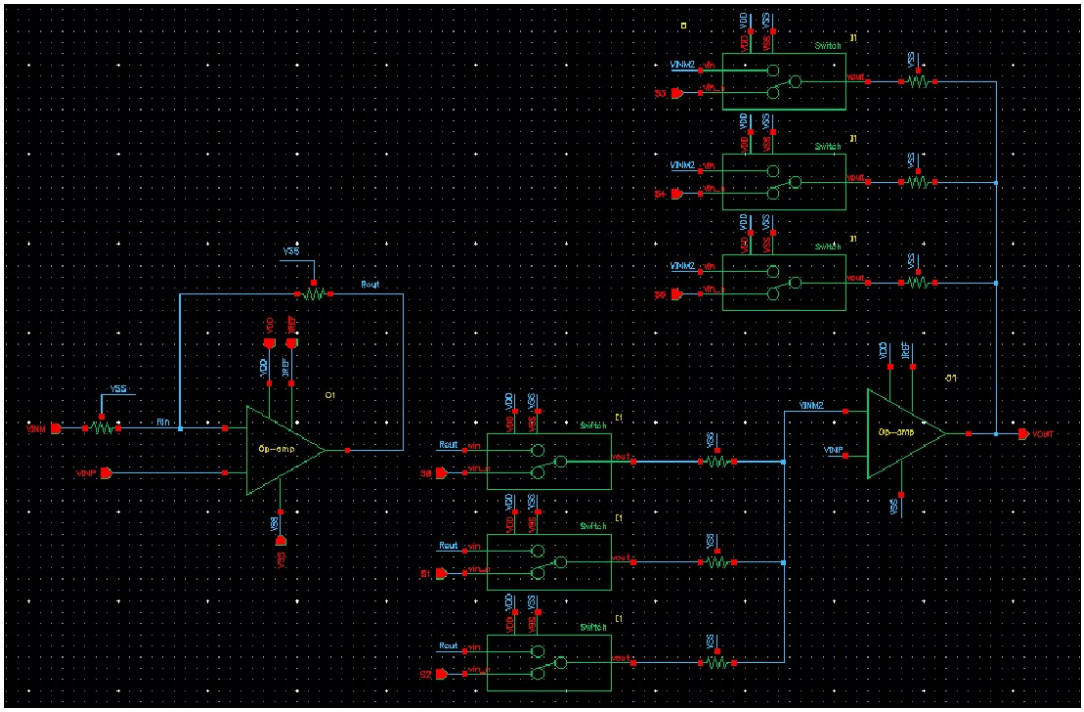


Figure 4.10: VGA - Schematic

The poly resistor values are mentioned in below Table.4.2.

Table 4.2: Poly Resistors

Resistor	Value
R_{in}	1K
R_f	1K
R0	18.6K
R1	100K
R2	536K
R3	18.6K
R4	100K
R5	536K

4.5 Total Current and Power

The testbench for the measurement of the current is shown in the Fig.4.11. The output is connected across with a resistor of 500 Ω. The current that flows across the resistor is measured and that provides the total current of the circuit. The total power of the circuit is calculated by multiplying the output voltage with the current across the resistor.

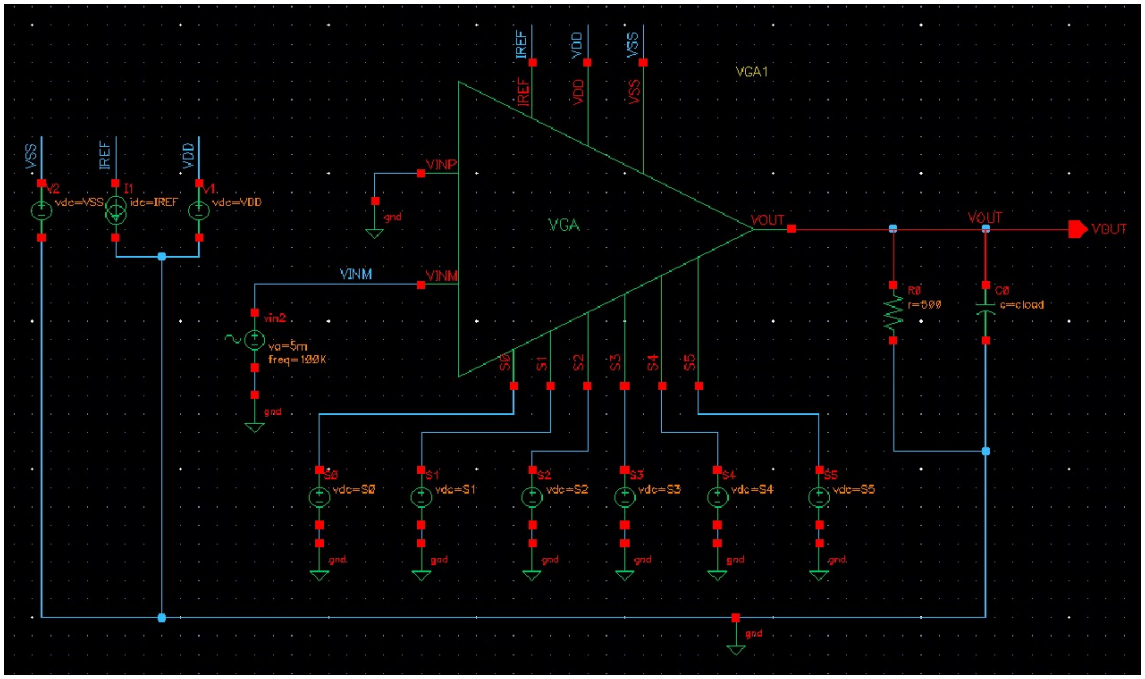


Figure 4.11: Total Current - Testbench

Chapter 5

Results and Discussion

The results of the simulations and analyses of the results is provided in this chapter. The chapter discusses the simulation results of all VGA components.

5.1 Inverter

The red waveform in the graph represents the input and the green waveform represents the output. The result of a CMOS inverter simulation waveform can be found in Fig.5.1. In the results it is seen that the input is inverted and given as output which is what is the expected result of the inverter.

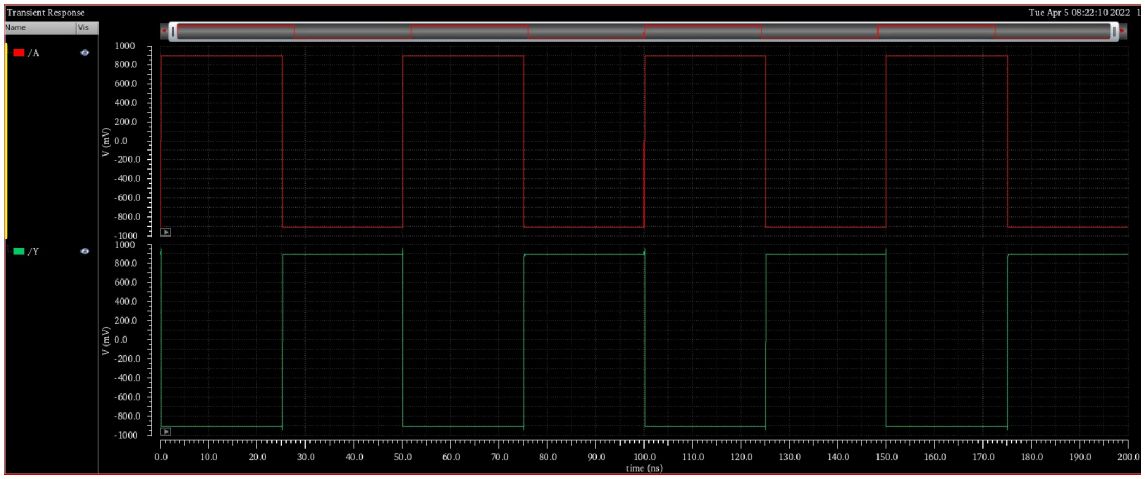


Figure 5.1: Inverter Simulation Waveform

5.2 Transmission Gate Switch

The Transmission gate switch circuit is simulated for the transient simulation with stimuli for VDD, VSS, vin and vin_n. The vin is the input that needs to be passed on to the output. The vin_n controls if the switches or turned ON or OFF. When the vin_n is high, the vin_p is always low and vice versa. When vin_n is high, the NMOS in the switch is turned ON and vin_p is low, PMOS in the switch is turned OFF and it passes the input signal to the output. If the vin_n is low, the NMOS is turned OFF and vin_p is high, PMOS in the switch is turned ON, the input signal does not pass to the output. Fig.5.2 shows the output waveform of the transmission gate switch.

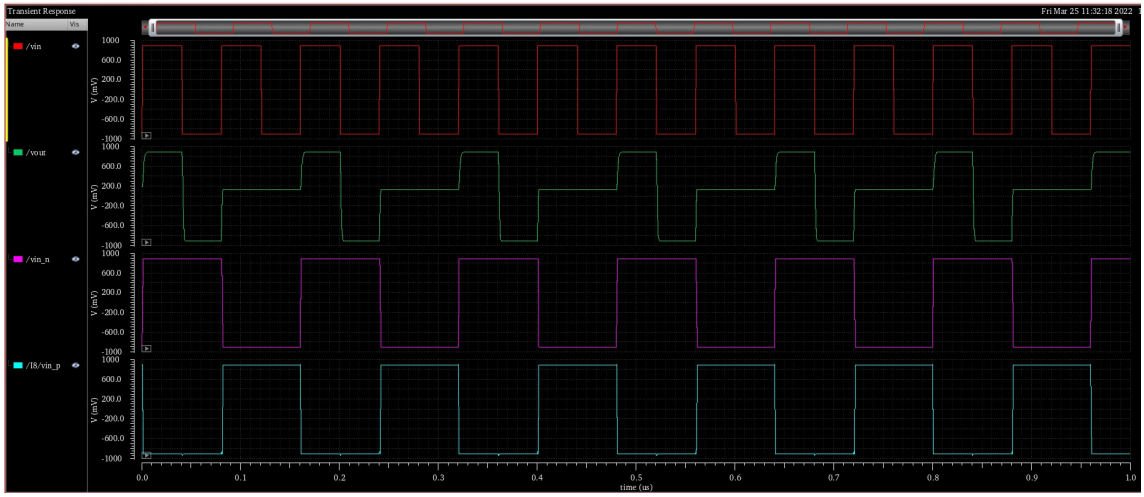


Figure 5.2: Transmission Gate Switch Simulation Waveform

5.3 Two Stage Operational Amplifier (Class AB Output Stage)

Fig.5.3 shows the gain and phase margin of the two stage operational amplifier.

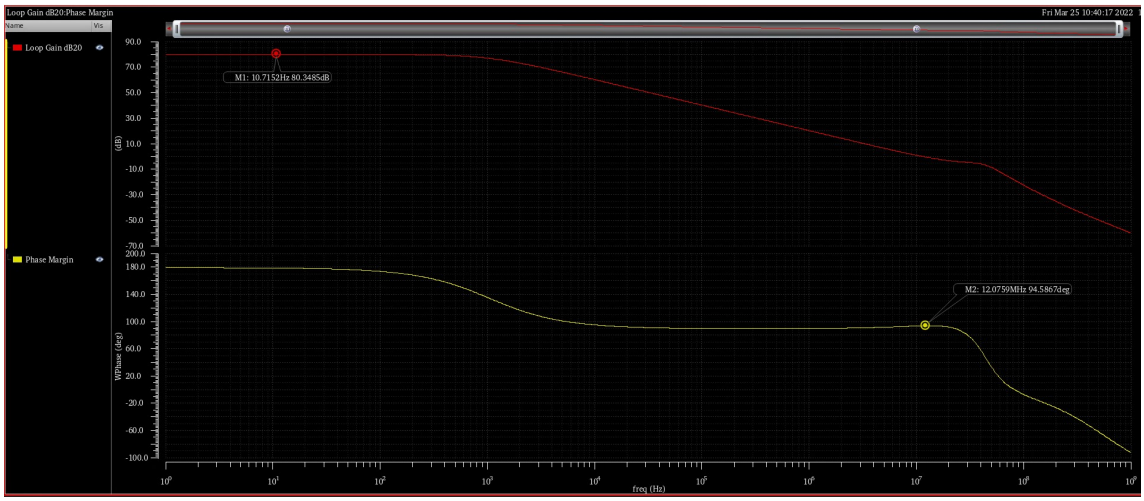


Figure 5.3: Gain and Phase Margin Simulation Waveform

5.3.1 CMRR

Fig.5.4 shows the common mode gain of the two stage operational amplifier. The CMRR is calculated by subtracting the common mode gain from the differential gain.

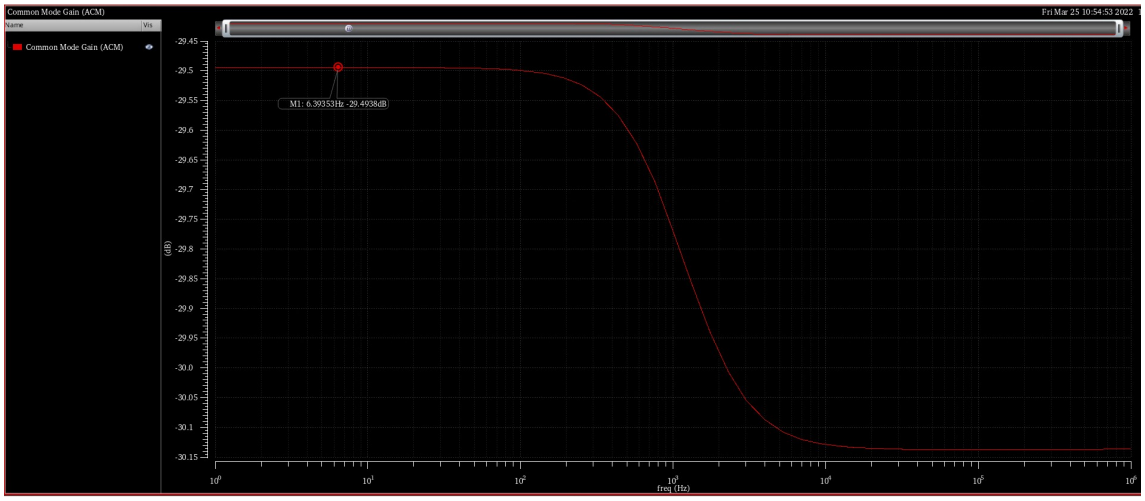


Figure 5.4: CMRR Simulation Waveform

5.3.2 ICMR

The Fig.5.5 shows the Input Common mode range of the two stage operational amplifier.

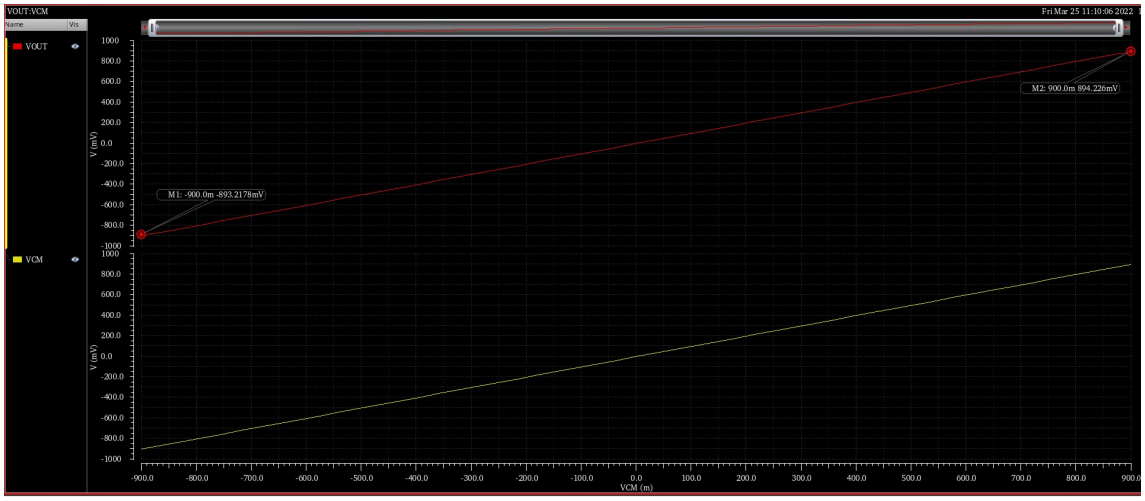


Figure 5.5: ICMR Simulation Waveform

5.3.3 Output Swing

Fig.5.6 shows the output voltage swing of the two stage operational amplifier. The maximum output voltage swings closer to the VDD voltage is 872.13 mV having a headroom voltage of 27.83 mV. The maximum output voltage swings closer to the VSS voltage is -888.34 mV having a headroom voltage of 11.6 mV.

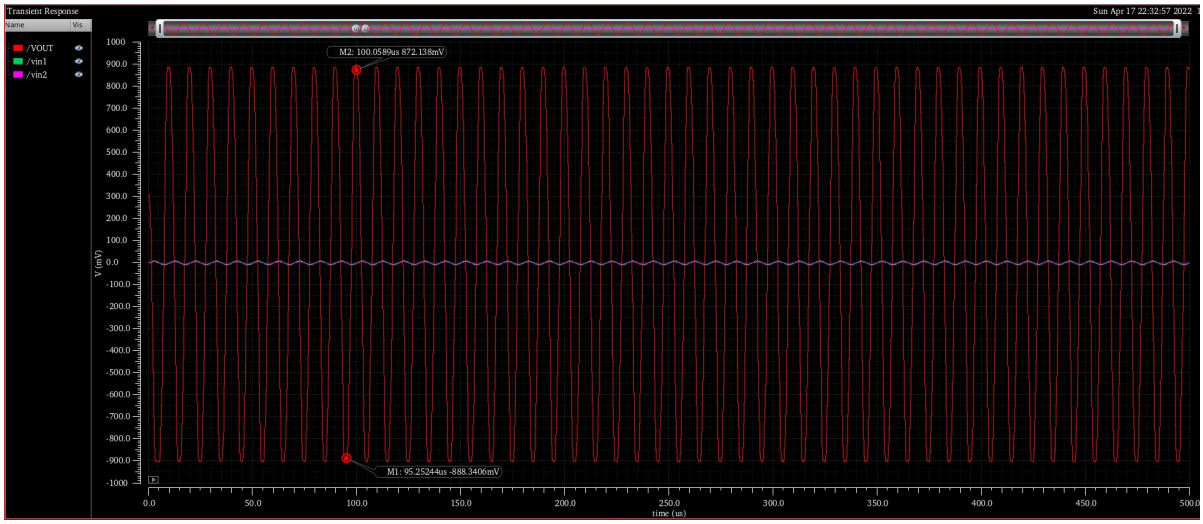


Figure 5.6: Output Swing Simulation Waveform

The results of two stage op-amp are summarized in Table.5.1.

Table 5.1: Op-Amp Simulation Results

Parameter	Value
Loop Gain	80.34 dB
Unity Gain Frequency	12.07 MHz
Phase Margin	94.58º
CMRR	109.7 dB
ICMR	-893.21 mV to 894.22 mV
Output Swing	-888.34 mV to 872.13 mV

5.4 Variable Gain Amplifier

The primary purpose of the Variable Gain Amplifier is to vary the gain as per need. In this design of the VGA, the gain of the circuit can be varied by selecting the switches required. Based on the selection of the switches, the resistors get turned ON. This in turn varies the gain of the VGA. This circuit is digitally controlled by controlling the inputs of the switches. Fig 5.7 shows the waveform of the output of the VGA based on the selection of the switches that is turned ON. The formula for calculating the gain of the circuit is given by the equation 5.1.

$$-\frac{Vout}{Vin} = e^{2X_i} \tag{5.1}$$

Where,

$$X_i = x + 0.84(i-2) \tag{5.2}$$

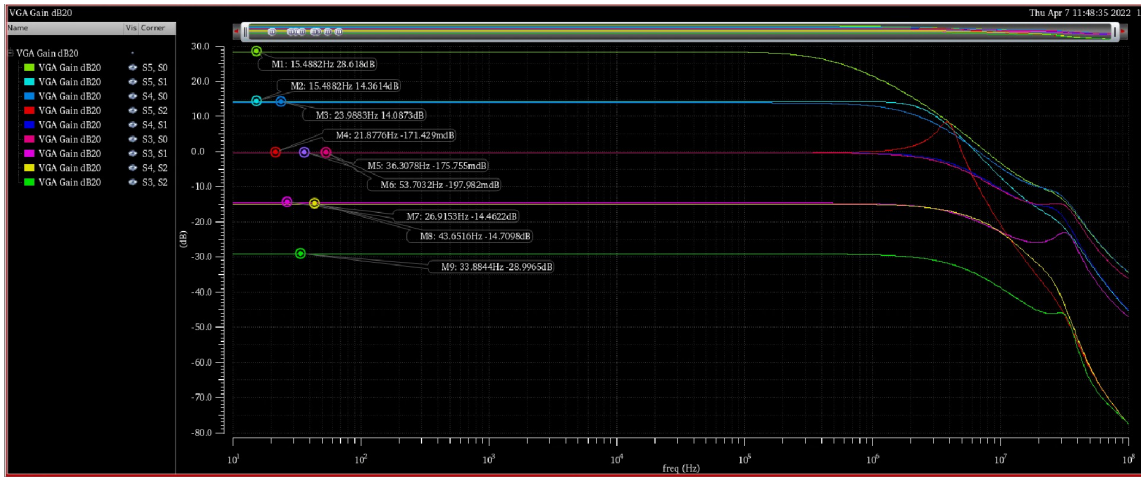


Figure 5.7: VGA Simulation Waveform

The results of the VGA based on the switches which is turned ON is summarized in Ta-

ble.5.2[3].

Table 5.2: VGA Gain Results

Switches ON	Gain	Gain
S3, S2	$e^{-3.36}R$	-28.99 dB
S4, S2	$e^{-1.68}R$	-14.71 dB
S3, S1	$e^{-1.68}R$	-14.46 dB
S3, S0	1	-197.9 mdB
S4, S1	1	-175.7 mdB
S5, S2	1	-171.4 mdB
S4, S0	$e^{+1.68}R$	14.09 dB
S5, S1	$e^{+1.68}R$	14.36 dB
S5, S0	$e^{+3.36}R$	28.62 dB

5.5 Total Current and Power

The total current in the circuit is -369.05 nA and the total power is given by multiplying the output voltage with the total current which results in the total power of $6.80989512e^{-11}W$. Fig 5.8. shows the output voltage and the total output current of the circuit.

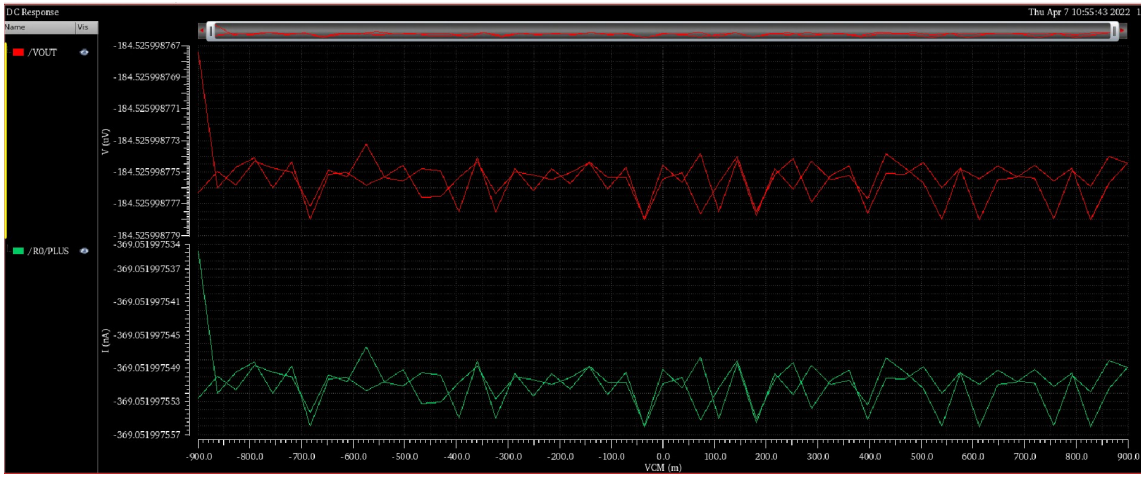


Figure 5.8: Total Current Simulation Waveform

The results are summarized in Table.5.3 and the total power is calculated using equation 5.3.

$$Power = Voltage * Current \tag{5.3}$$

Table 5.3: Total Current and Power

Parameter	Value
Vout	-184.051 μV
Total Current ($Resistance = 500\ \Omega$)	-369.051 nA
Total Power	$6.80989512e^{-11}W$

Chapter 6

Layout

The layout of the circuit is designing the schematic at the various levels of the layers. The layout design should be aware of multiple critical issues and those should be addressed. Examples of the critical analog layout issues are the parasitics, noise, electromigration, and matching. The noise can be generated by the resistors and the other active devices in the circuit. These can be limited by the usage of the strong substrate connections. The noise generated by the routing lines creates cross-talk and that in turn changes the simulation result. Such noises can be reduced by the concept of shielding. Shielding essentially means separating the noisy routing lines from the other routing lines by adding parallel routing lines connected to ground. Matching is very critical in analog layout design. Matching techniques eliminates or greatly reduces the process variation errors introduced.Some of the critical matching circuit areas are the differential pair and current mirrors in the analog circuit. There are two basic types of matching. The first one is the common-centroid and the second one is the interdigitization. Interdigitization means multi fingered transistors are split and arranged in alternating fashion. Common centroid means that the devices are split uniformly along the axis and so that these devices are matched under all process variations. The most common place the transistors are

common centroid are the differential pair. Electromigration decides the current carrying capacity of the metal lines. The current carrying capacity changes based on the width and length of the routing lines. If the design contains a current hungry circuit, careful considerations should be done while doing the floor-plan of the circuit.

There are some basic steps to be considered while doing the layout of the circuit. The primary step is the Floor-plan. In Floor-planning the devices are laid out based on the matching of the devices, routing distances, critical devices. The second step is to consider the power planning. In this step, it is necessary to consider the routing metal in which the power comes in and how it is distributed to the devices. The third step is to consider the routing of the critical signals. In this step, careful considerations is given to the routing of the critical parts of the circuit. The fourth step is to consider the routing of the supporting signals. In this step, the routing of the enables and other non-critical routing is performed. The fifth step is to make circuit LVS clean. This step means the Layout has to match the connections exactly the schematic without any shorts and opens. The final step is the DRC. This steps means that the layout has to match and pass all the design rule checks. Some of the design rule checks are minimum width, minimum spacing, minimum extension, minimum enclosures, voltage dependent rules.

6.1 Inverter

The layout of the inverter consists of a PMOS and NMOS. The PMOS lies in the n-well and NMOS lies in the p substrates. The drains of the transistors are connected using the Metal 1 and it is the output of the inverter. The poly of the transistors are connected together acting as the gate. It is generally recommended to avoid routing using the poly, since poly is highly resistive in nature. The NMOS is connected to the substrate using the ptap and the PMOS is

connected to the substrate using the ntap as shown in Fig. 6.1. DRC and LVS are clean as shown in Fig. 6.2 and Fig. 6.3 .

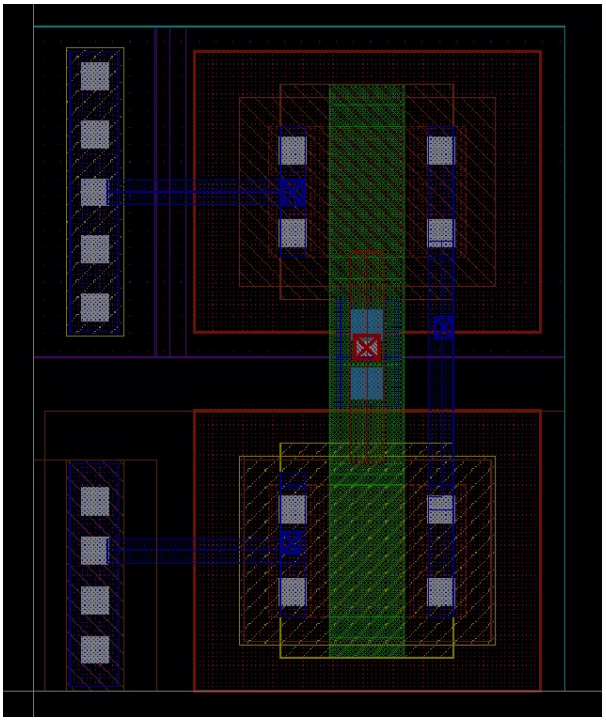


Figure 6.1: Inverter - Layout

Figure 6.2: DRC

Figure 6.3: LVS

6.2 Transmission Gate Switches

The layout of the transmission gate switches as shown in Fig.6.4 is laid out in a manner that the signals don't cross each other in the same metal layers and thus avoiding cross talks. The floor-plan of the transmission gates is designed in such a way that the substrate contact is shared with the inverter and do not need a repeated substrate connection. There is redundancy of vias in the source and drain connections of the transistor. The reason for the redundancy is that even if a single via fails, there are multiple vias to support the connections. As a rule of thumb in the layout, it is better to add as many vias as possible in the connections so that the via resistance reduces and has a greater electromigration limit. DRC and LVS are clean as shown in Fig.6.5 and Fig.6.6

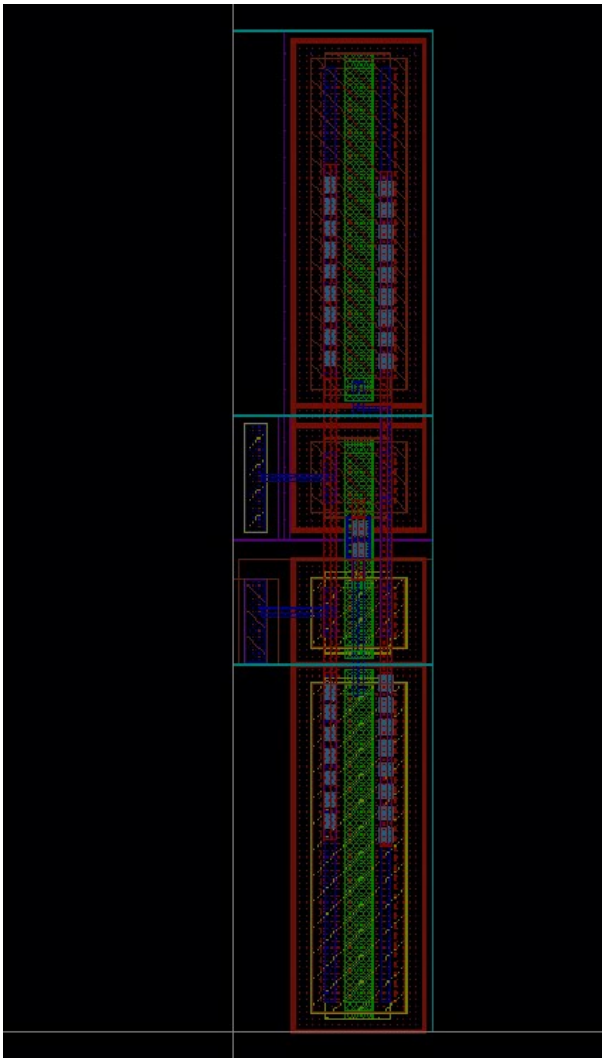


Figure 6.4: Transmission Gate Switches - Layout

Figure 6.5: DRC

Figure 6.6: LVS

6.3 Two Stage Operational Amplifier

The layout of the Op-amp has higher metal layers. The compensation capacitor is made of metal layers 10 and 11. In order to connect the transistors to the capacitors higher metal layers have to be used. The differential pair used in the op-amp have common centroid pattern. The current mirrors used in the op-amp have interdigitization. These matching techniques have been used so that they do not face the gradient effects. The layout has followed the metal direction orientation. The metal 1 can be routed in any direction, metal 2 only in vertical di-

rection, metal 3 only in horizontal direction. The metal direction orientation is very important while doing the layout. The reason for that is it allows easier crossing of metals horizontally and vertically. If this is not followed the possibility of getting locked within a loop is pretty high. The compensation capacitor is shown in Fig.6.7 and the transistors are shown in Fig.6.8. The inputs pins of the op-amp are in metal 3. DRC and LVS are clean as shown in Fig.6.9 and Fig.6.10.

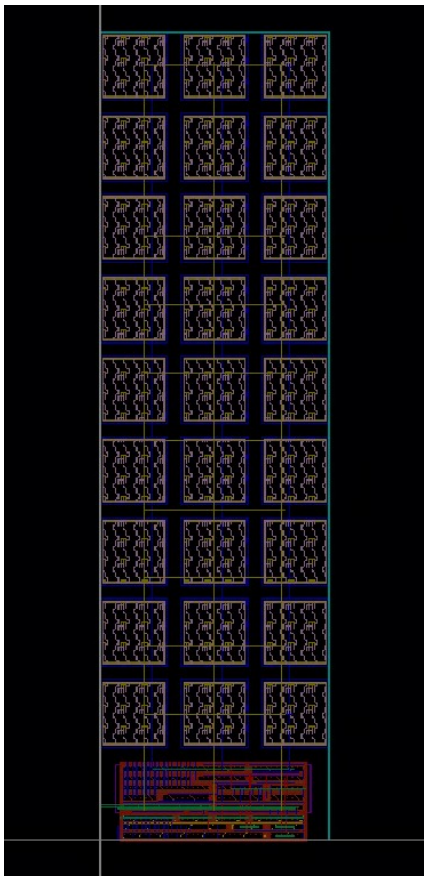


Figure 6.7: Two Stage Op-amp - Layout

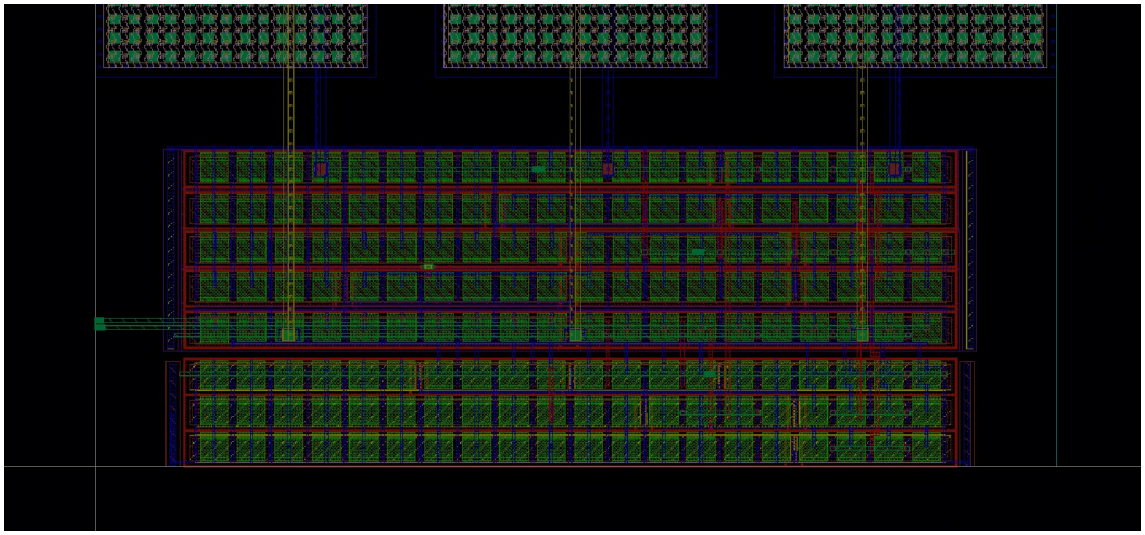


Figure 6.8: Transistors - Zoomed View Layout

Figure 6.9: DRC

Figure 6.10: LVS

6.4 VGA

Fig.6.11 shows the Voltage Gain Amplifier Layout. The op-amp layout has been places on either ends and the resistors and the switches are places in the center. This floor-plan of the layout has been done so that there is no empty space and also the routing lines are short and so there is no extensive resistance in the metal lines. The resistors used in the layout are poly resistors. The advantage of poly is that they are highly resistive and so they provide high resistance in a very small area. The majority of the area of the VGA is occupied by the compensation capacitors and the resistors. The total height of the VGA is 98.68 μm and the total width of the VGA is 96.07 μm. The total area of the VGA is 9480.1876 μm^2. DRC and LVS are clean as shown in Fig.6.12 and Fig.6.13.

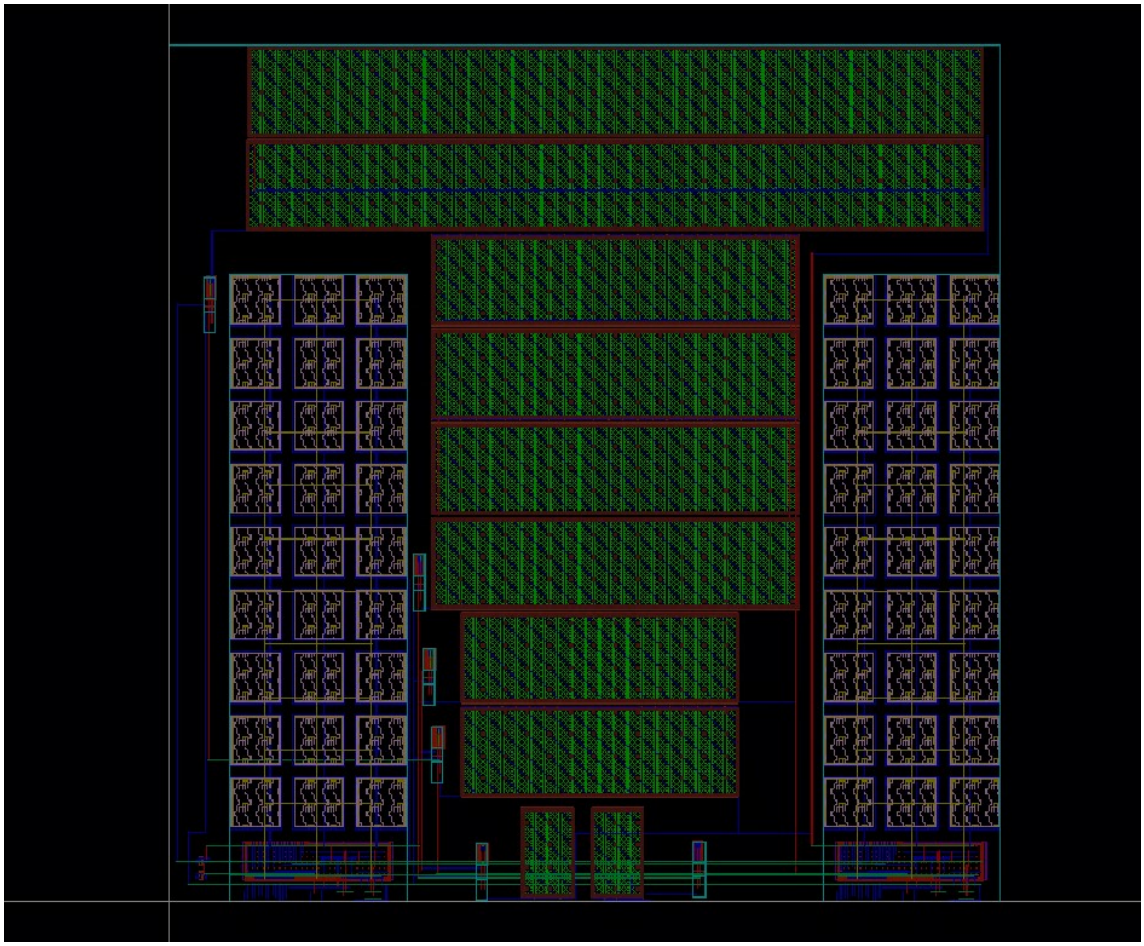


Figure 6.11: VGA - Layout

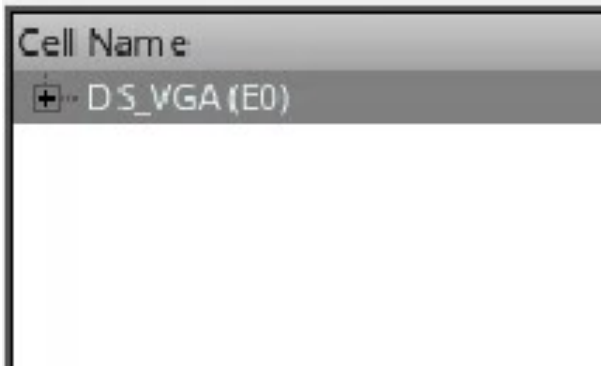


Figure 6.12: DRC

Figure 6.13: LVS

Chapter 7

Conclusion

In this project, CMOS variable gain amplifier (VGA) with digital control has been designed using transmission gate switches, operational amplifiers and resistors in 45 nm technology. The range of the variable gain amplifier ranges from -28.99 dB to 28.62 dB. The power consumption of the variable gain amplifier is $6.80989512e^{-11}\ W$ and the total current is -369.05 nA. The variable gain amplifier has been laid out and made to meet the design rule checks in 45 nm and match the schematic and has been verified using the PVS tool suite.

7.1 Future Work

The digitally controlled VGA has been successfully designed and simulated. A few suggestions for a continued effort in this project are presented here:

- The selection of the transmission gate switches can be automated based on the required outputs.
- The bias current for the circuit can be provided with a circuit rather than as a stimuli.

- Different topologies of the operational amplifiers can be used to increase the gain range of the variable gain amplifier.

References

[1] Dipesh Panchal and Amisha Naik. 0.25V Bulk Driven Variable Gain Amplifier using gmb/Idrain Method for Ultra-Low Power Low Voltage Biomedical Applications. In *2020 5th International Conference on Communication and Electronics Systems (ICCES)*. IEEE, jun 2020. doi:10.1109/icces48766.2020.9138036.

[2] T. M. Hassan and S. A. Mahmoud. New CMOS digitally controlled variable gain amplifier. In *2008 International Conference on Microelectronics*. IEEE, dec 2008. doi:10.1109/icm.2008.5393795.

[3] Sandhya Purighalla and Brent Maundy. Improved dynamic range, digitally-controlled linear-in-dB CMOS variable gain amplifier. In *2011 IEEE International Symposium of Circuits and Systems (ISCAS)*. IEEE, may 2011. doi:10.1109/iscas.2011.5938116.

[4] D. M. Binkley. Tradeoffs and Optimization in Analog CMOS Design. In *2007 14th International Conference on Mixed Design of Integrated Circuits and Systems*. IEEE, jun 2007. doi:10.1109/mixdes.2007.4286119.

[5] R. Jacob Baker. *CMOS : circuit design, layout and simulation*. John Wiley & Sons, Inc., aug 2010. doi:10.1002/9780470891179.

[6] F. Silveira, D. Flandre, and P. G. A. Jespers. A gm/ID based methodology for the de-

sign of CMOS analog circuits and its application to the synthesis of a silicon-on-insulator micropower OTA. *IEEE Journal of Solid-State Circuits*, 31(9):1314–1319, 1996. URL: https://ieeexplore.ieee.org/document/535416, doi:10.1109/4.535416.

[7] Guillaume Pollissard-Quatremere, Geoffroy Gosset, and Denis Flandre. A modified gm/ID design methodology for deeply scaled CMOS technologies. *Analog Integrated Circuits and Signal Processing*, 78(3):771–784, sep 2013. doi:10.1007/s10470-013-0166-z.

[8] D. M. Binkley, C. E. Hopper, S. D. Tucker, B. C. Moss, J. M. Rochelle, and D. P. Foty. A CAD methodology for optimizing transistor current and sizing in analog CMOS design. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, 22(2):225–237, feb 2003. doi:10.1109/tcad.2002.806606.

[9] Debosmit Majumder, Shrey Khanna, and Aminul Islam. An ultralow-power low-voltage Class-AB Fully Differential Op Amp with cascoded input stage and indirect compensation. In *2015 International Conference on Industrial Instrumentation and Control (ICIC)*. IEEE, may 2015. doi:10.1109/iic.2015.7150909.

Appendix I

VGA Gain

S0 (mV)	S1 (mV)	S2 (mV)	S3 (mV)	S4 (mV)	S5 (mV)	VGA Gain (dB)	Voltage gain (V)
-900	-900	-900	-900	-900	-900	-169.2	3.465 n
-900	-900	-900	900	900	900	-140.4	95.65 n
-900	-900	-900	900	900	-900	-140.1	98.56 n
-900	-900	-900	900	-900	900	-138.9	113.5 n
-900	-900	-900	900	-900	-900	-138.6	117.6 n
-900	-900	-900	-900	900	900	-125.8	513 n
-900	-900	-900	-900	900	-900	-124.3	609.3 n
-900	-900	-900	-900	-900	900	-109.8	3.249 u
-900	-900	900	900	900	900	-30.79	28.87 m
-900	-900	900	900	900	-900	-30.53	29.74 m
-900	-900	900	900	-900	900	-29.31	34.25 m
-900	-900	900	900	-900	-900	-29	35.5 m
-900	900	-900	900	900	900	-16.26	153.9 m
-900	-900	900	-900	900	900	-16.2	154.8 m
-900	900	-900	900	900	-900	-16	158.5 m
-900	900	-900	900	-900	900	-14.77	182.6 m
-900	900	900	900	900	900	-14.77	182.7 m
-900	-900	900	-900	900	-900	-14.71	183.9 m
-900	900	900	900	900	-900	-14.51	188.3 m
-900	900	-900	900	-900	-900	-14.46	189.2 m
-900	900	900	900	-900	900	-13.28	216.8 m
-900	900	900	900	-900	-900	-12.97	224.6 m
900	-900	-900	900	900	900	-1.993	794.9 m
900	-900	-900	900	900	-900	-1.733	819.1 m
900	-900	900	900	900	900	-1.685	823.7 m
-900	-900	-900	-900	900	900	-1.669	825.2 m
900	-900	900	900	900	-900	-1.425	848.7 m
900	-900	-900	900	-900	900	-507.3 m	943.3 m
900	900	-900	900	900	900	-463.3 m	948.1 m
900	900	900	900	900	900	-204.3 m	976.8 m
900	900	-900	900	900	-900	-203.3 m	976.9 m
900	-900	900	900	-900	900	-199 m	977.4 m
900	-900	-900	900	-900	-900	-198 m	977.5 m
-900	900	900	-900	900	900	-176.7 m	979.9 m
-900	900	-900	-900	900	-900	-175.8 m	980 m
-900	-900	900	-900	-900	900	-171.4 m	980.5 m
900	900	900	900	900	-900	55.77 m	1.006
900	-900	900	900	-900	-900	110.4 m	1.013
900	900	-900	900	-900	900	1.023	1.125
900	900	900	900	-900	900	1.282	1.159
-900	900	900	-900	900	-900	1.316	1.164
900	900	-900	900	-900	-900	1.332	1.166
900	900	900	900	-900	-900	1.591	1.201
900	-900	-900	-900	900	900	12.59	4.263
900	-900	900	-900	900	900	12.9	4.417
900	-900	-900	-900	900	-900	14.09	5.062

900	900	-900	-900	900	900	14.12	5.084
-900	900	-900	-900	-900	900	14.36	5.225
900	900	900	-900	900	900	14.38	5.238
900	-900	900	-900	900	-900	14.4	5.245
900	900	-900	-900	900	-900	15.62	6.037
-900	900	900	-900	-900	900	15.85	6.204
900	900	900	-900	900	-900	15.88	6.22
900	-900	-900	-900	-900	900	28.62	26.97
900	-900	900	-900	-900	900	28.93	27.94
900	900	-900	-900	-900	900	30.15	32.16
900	900	900	-900	-900	900	30.4	33.13
-900	-900	900	-900	-900	-900	54.42	525.9
-900	900	-900	-900	-900	-900	82.27	12.99 K
-900	900	900	-900	-900	-900	83.12	14.32 K
900	-900	-900	-900	-900	-900	85.47	18.78 K
900	-900	900	-900	-900	-900	85.53	18.91 K
900	900	-900	-900	-900	-900	85.62	19.09 K
900	900	900	-900	-900	-900	85.66	19.19 K

Appendix II

Cadence Expression setup

II.1 Two Stage Op-Amp (Class AB Output Stage) - Gain Expression

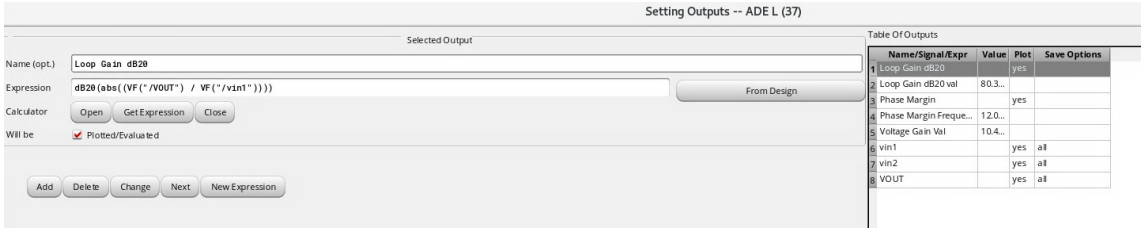


Figure II.1: Cadence Expression Setup - Gain in dB20

II.2 Two Stage Op-Amp (Class AB Output Stage) - Phase Margin Frequency Expression

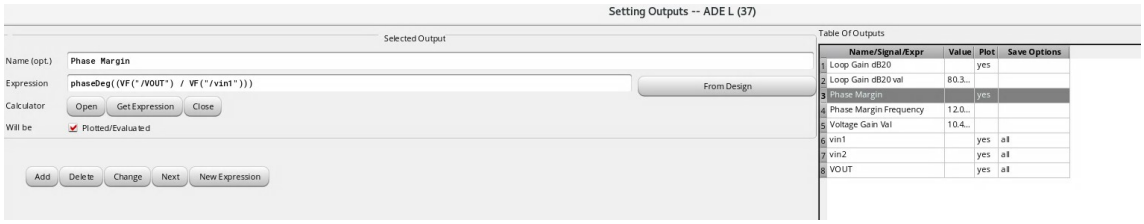


Figure II.2: Cadence Expression Setup - Phase Margin frequency

II.3 Two Stage Op-Amp (Class AB Output Stage) - Common Mode Gain Expression

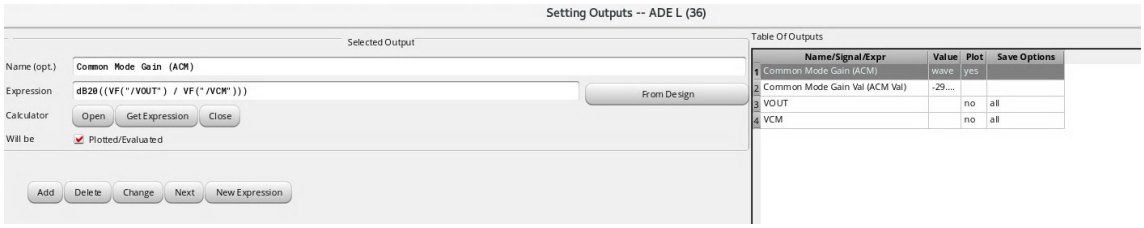


Figure II.3: Cadence Expression Setup - Common Mode Gain

II.4 Two Stage Op-Amp (Class AB Output Stage) - ICMR Expression

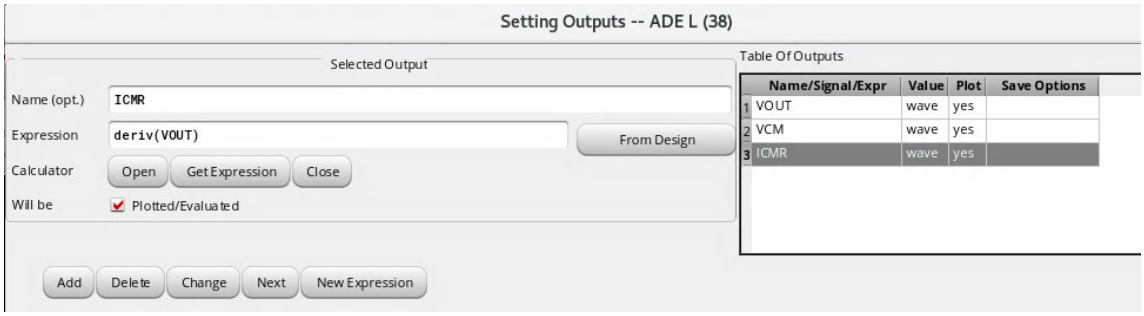


Figure II.4: Cadence Expression Setup - ICMR

II.5 Variable Gain Amplifier (VGA) - Gain Expression

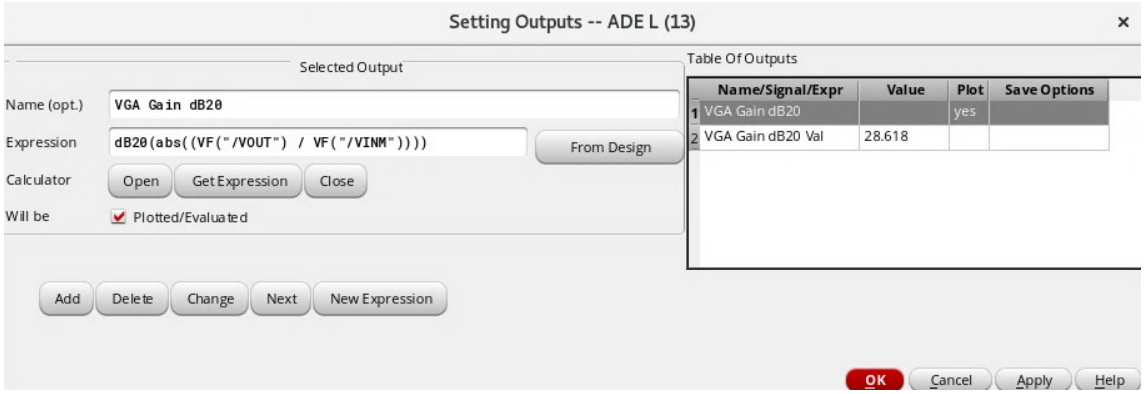


Figure II.5: Cadence Expression Setup - Gain

Appendix III

Cadence Virtuoso ADE window setup

III.1 Inverter

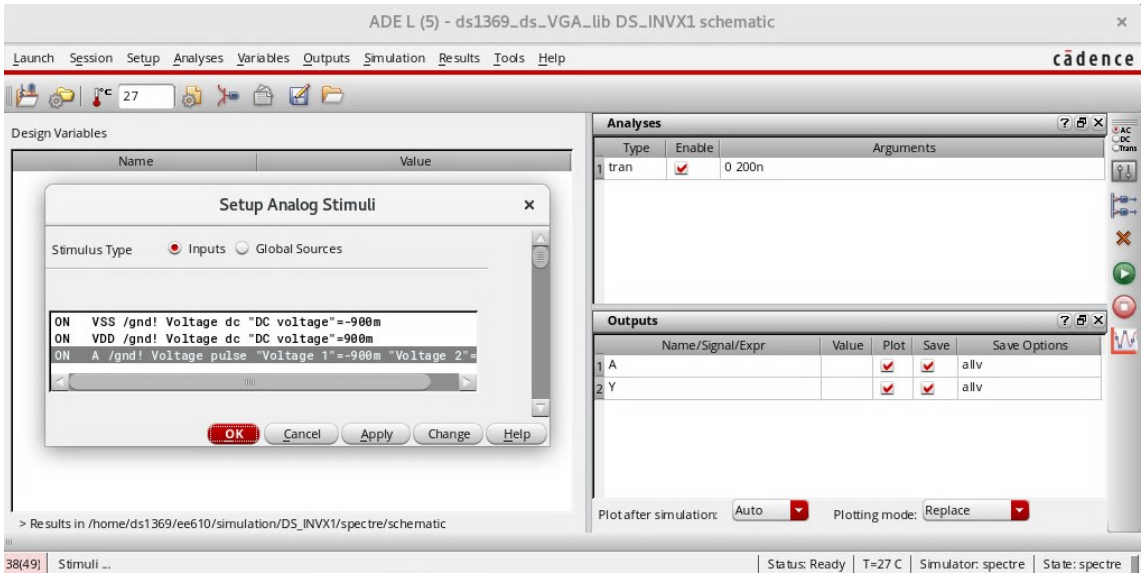


Figure III.1: Cadence setup window - Inverter

III.2 Transmission Gate Switch

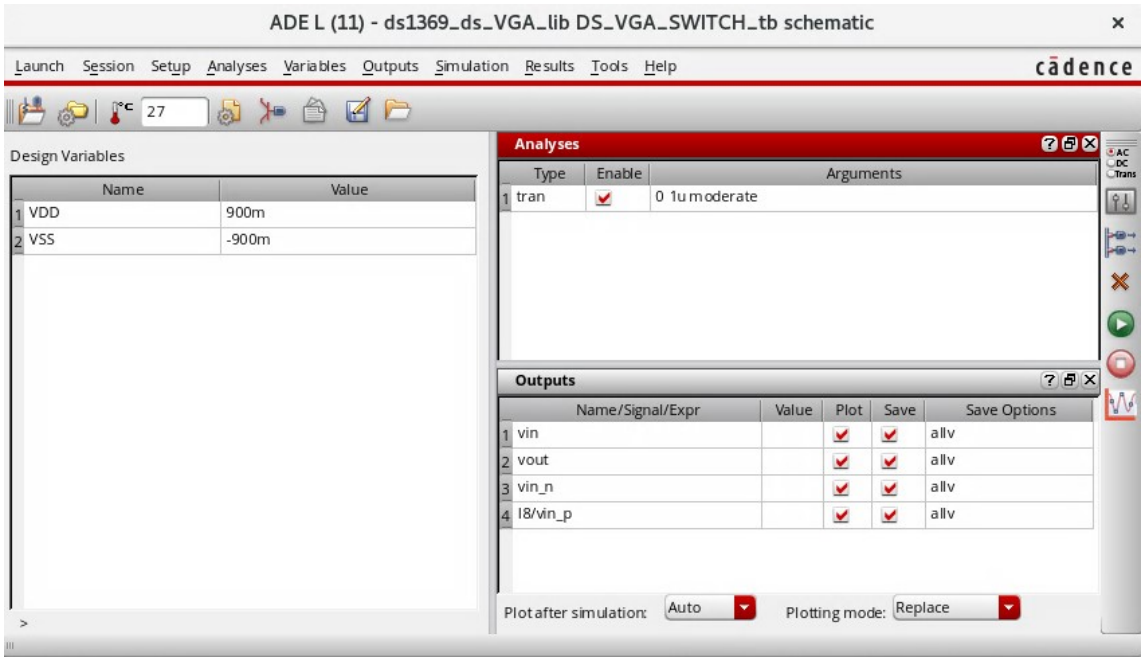


Figure III.2: Cadence setup window - Transmission Gate Switch

III.3 Two Stage Op-amp (Class AB Output Stage) - Gain and Phase Margin

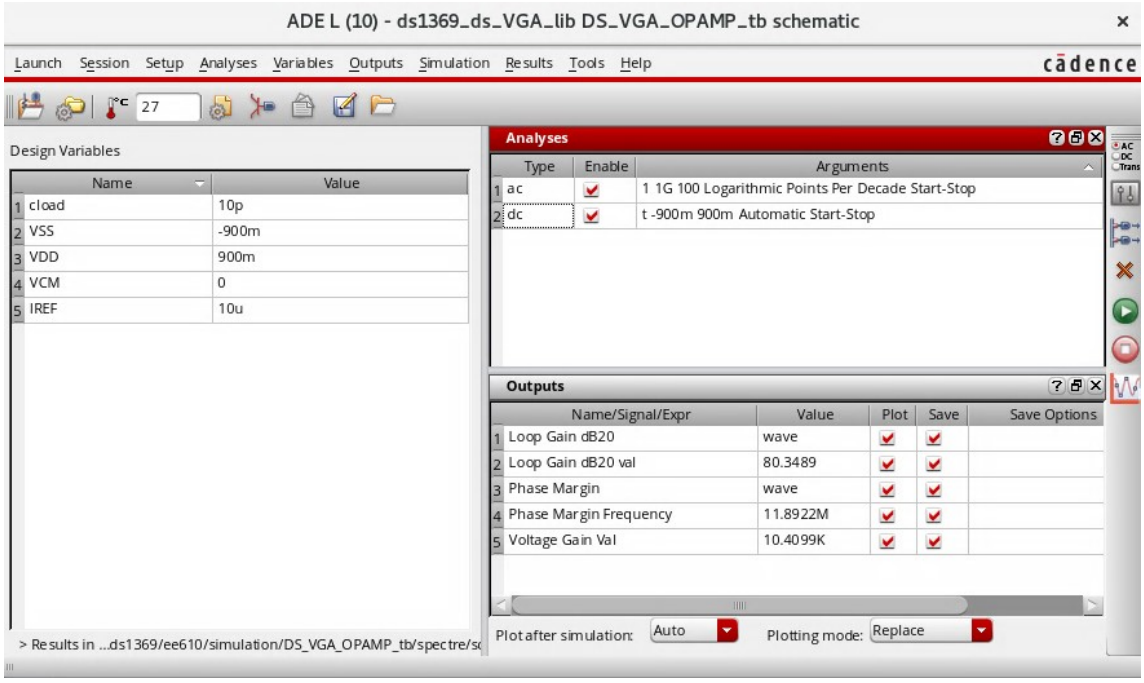


Figure III.3: Cadence setup window - Two Stage Op-amp (Class AB Output Stage) - Gain and Phase Margin

III.4 Two Stage Op-amp (Class AB Output Stage) - CMRR

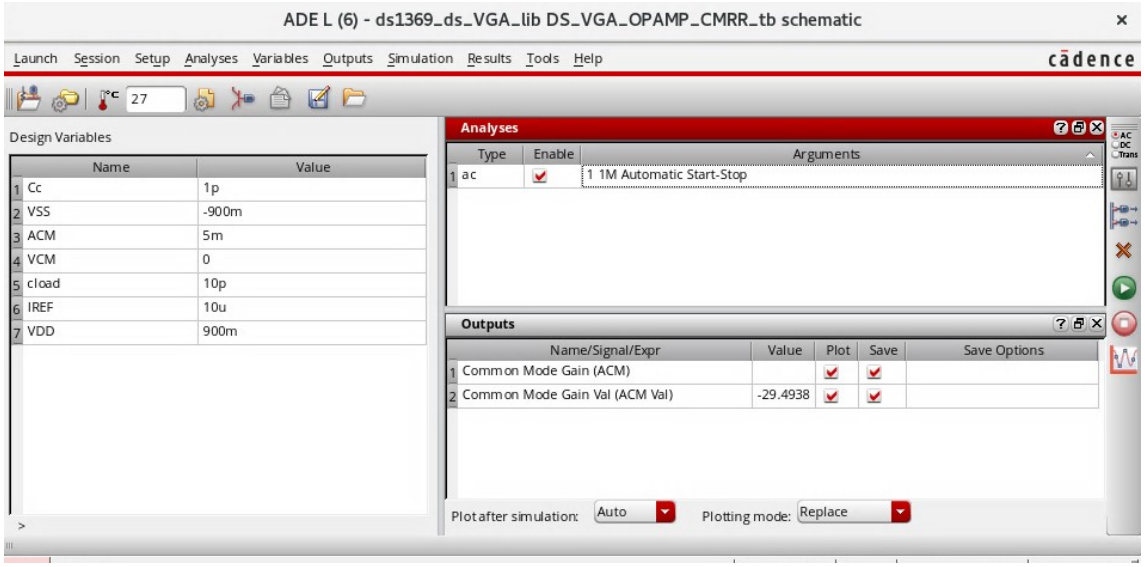


Figure III.4: Cadence setup window - Two Stage Op-amp (Class AB Output Stage) - CMRR

III.5 Two Stage Op-amp (Class AB Output Stage) - ICMR

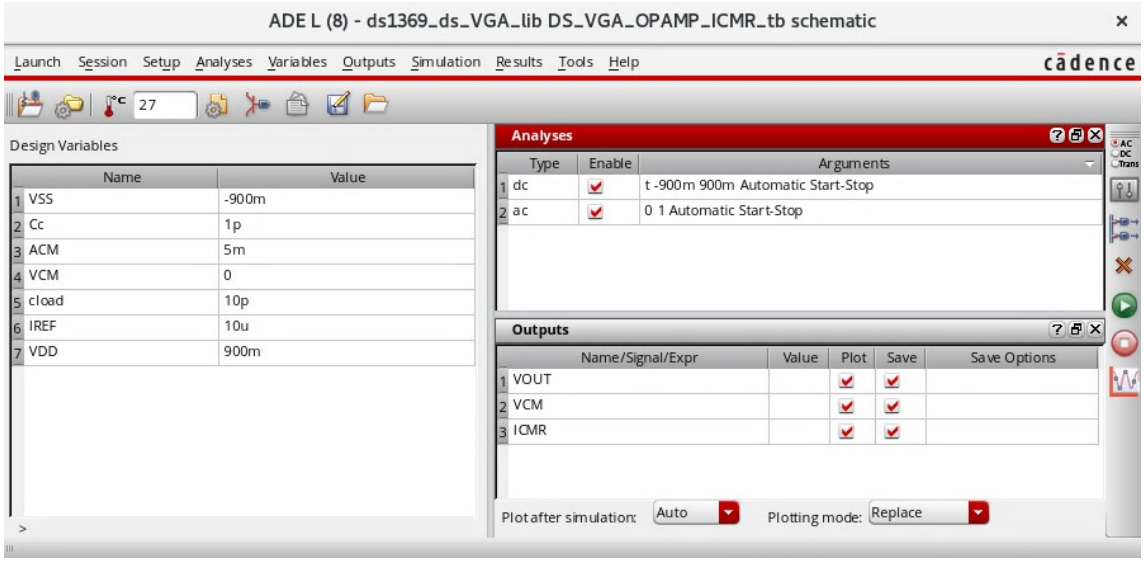


Figure III.5: Cadence setup window - Two Stage Op-amp (Class AB Output Stage) - ICMR

III.6 Two Stage Op-amp (Class AB Output Stage) - Output Swing

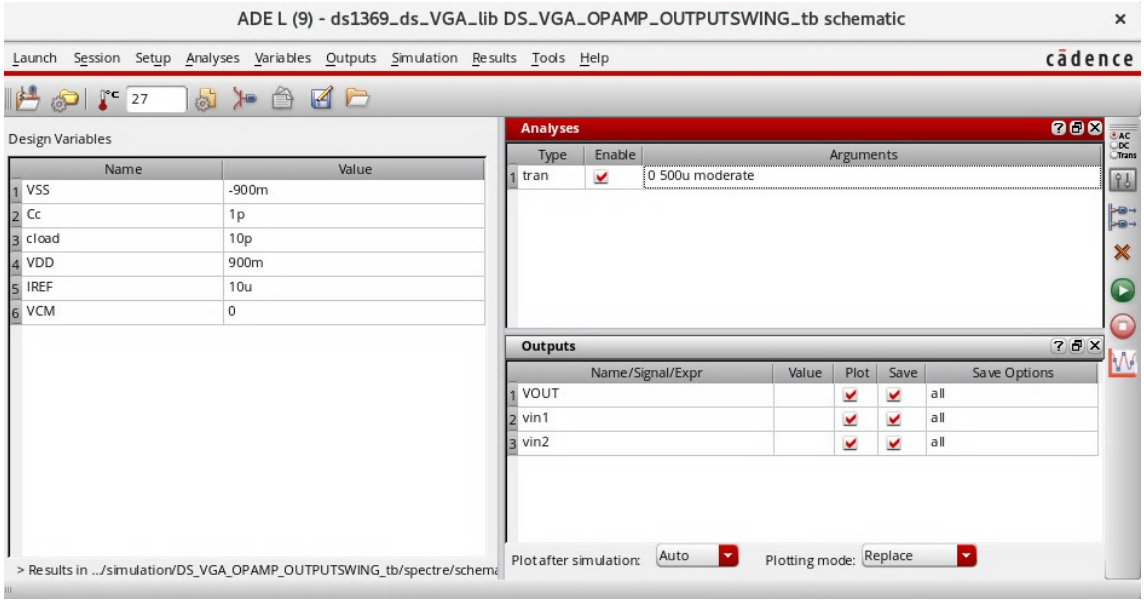


Figure III.6: Cadence setup window - Two Stage Op-amp (Class AB Output Stage) - Output Swing

III.7 Variable Gain Amplifier (VGA)

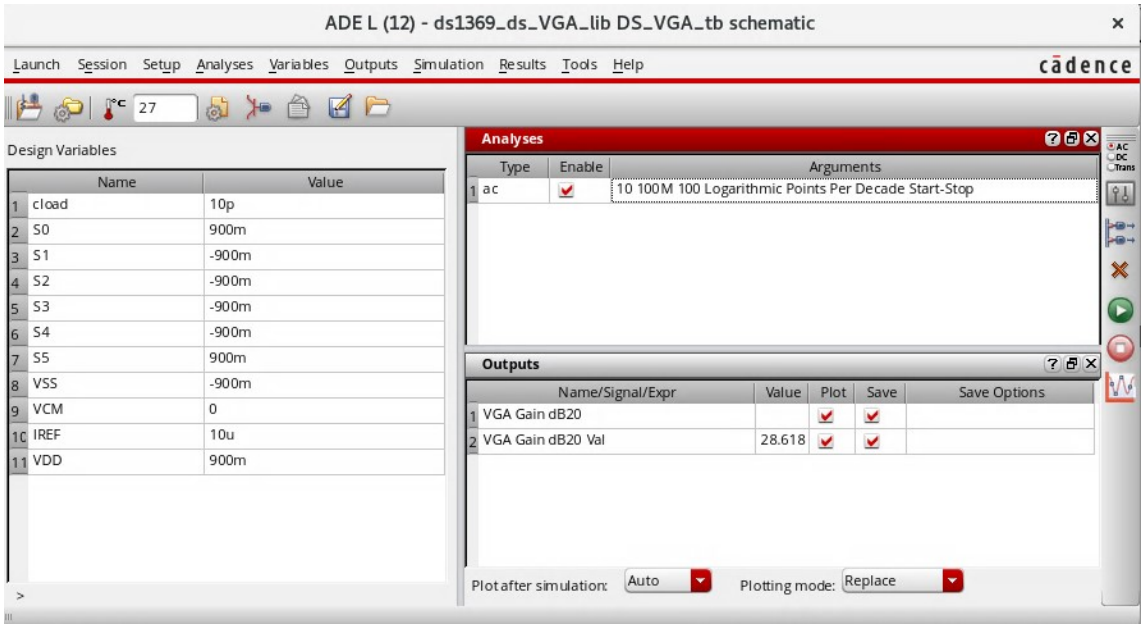


Figure III.7: Cadence setup window - Variable Gain Amplifier (VGA)

Appendix IV

Cadence SPI (spice/netlist) files

IV.1 Inverter SPI

```
1  * ++++++++++++++++++++++++++++++++++++++++++++++++++++++++ *
2  * CDL Netlist:                                             *
3  *                                                          *
4  * Cell Name   : DS_INVX1                                   *
5  * Netlisted   : Sun Apr 17 12:16:51 2022                   *
6  * PVS Version: 15.24-s451 Thu Jun  8 20:13:49 PDT 2017 *
7  * ++++++++++++++++++++++++++++++++++++++++++++++++++++++++ *
8  *.LDD
9  *.DEVTMPLT 0 MN(g45n1svt) _nmos1v ndiff_conn(D) poly_conn(G)
       ndiff_conn(S) psubstrate(B)
10 *.DEVTMPLT 1 MN(g45n1hvt) _nmos1v_hvt ndiff_conn(D) poly_conn(
       G) ndiff_conn(S) psubstrate(B)
```

```
11 *.DEVTMPLT 2 MN(g45n1lvt) _nmos1v_lvt ndiff_conn(D) poly_conn(
     G) ndiff_conn(S) psubstrate(B)
12 *.DEVTMPLT 3 MN(g45n1nvt) _nmos_12_native ndiff_conn(D)
     poly_conn(G) ndiff_conn(S) psubstrate(B)
13 *.DEVTMPLT 4 MN(g45n2svt) _nmos_25 ndiff_conn(D) poly_conn(G)
     ndiff_conn(S) psubstrate(B)
14 *.DEVTMPLT 5 MN(g45n2nvt) _nmos_25_native ndiff_conn(D)
     poly_conn(G) ndiff_conn(S) psubstrate(B)
15 *.DEVTMPLT 6 MN(g45ncap1) _nmoscap1v ndiff_conn(D) poly_conn(G
     ) ndiff_conn(S) psubstrate(B)
16 *.DEVTMPLT 7 MN(g45ncap2) _nmoscap2v ndiff_conn(D) poly_conn(G
     ) ndiff_conn(S) psubstrate(B)
17 *.DEVTMPLT 8 MP(g45p1svt) _pmos1v pdiff_conn(D) poly_conn(G)
     pdiff_conn(S) nwell_conn(B)
18 *.DEVTMPLT 9 MP(g45p1hvt) _pmos1v_hvt pdiff_conn(D) poly_conn(
     G) pdiff_conn(S) nwell_conn(B)
19 *.DEVTMPLT 10 MP(g45p1lvt) _pmos1v_lvt pdiff_conn(D) poly_conn
     (G) pdiff_conn(S) nwell_conn(B)
20 *.DEVTMPLT 11 MP(g45p2svt) _pmos2v pdiff_conn(D) poly_conn(G)
     pdiff_conn(S) nwell_conn(B)
21 *.DEVTMPLT 12 MP(g45pcap1) _pmoscap1v pdiff_conn(D) poly_conn(
     G) pdiff_conn(S) nwell_conn(B)
22 *.DEVTMPLT 13 MP(g45pcap2) _pmoscap2v pdiff_conn(D) poly_conn(
     G) pdiff_conn(S) nwell_conn(B)
```

```
23 *.DEVTMPLT 14 R(g45rm1) _resm1 metal1_conn(PLUS) metal1_conn(
    MINUS)
24 *.DEVTMPLT 15 R(g45rm2) _resm2 metal2_conn(PLUS) metal2_conn(
    MINUS)
25 *.DEVTMPLT 16 R(g45rm3) _resm3 metal3_conn(PLUS) metal3_conn(
    MINUS)
26 *.DEVTMPLT 17 R(g45rm4) _resm4 metal4_conn(PLUS) metal4_conn(
    MINUS)
27 *.DEVTMPLT 18 R(g45rm5) _resm5 metal5_conn(PLUS) metal5_conn(
    MINUS)
28 *.DEVTMPLT 19 R(g45rm6) _resm6 metal6_conn(PLUS) metal6_conn(
    MINUS)
29 *.DEVTMPLT 20 R(g45rm7) _resm7 metal7_conn(PLUS) metal7_conn(
    MINUS)
30 *.DEVTMPLT 21 R(g45rm8) _resm8 metal8_conn(PLUS) metal8_conn(
    MINUS)
31 *.DEVTMPLT 22 R(g45rm9) _resm9 metal9_conn(PLUS) metal9_conn(
    MINUS)
32 *.DEVTMPLT 23 R(g45rm10) _resm10 metal10_conn(PLUS)
    metal10_conn(MINUS)
33 *.DEVTMPLT 24 R(g45rm11) _resm11 metal11_conn(PLUS)
    metal11_conn(MINUS)
34 *.DEVTMPLT 25 R(g45rsnd) _ressndiff ndiff_conn(PLUS)
    ndiff_conn(MINUS) psubstrate(B)
```

```
35 *.DEVTMPLT 26 R(g45rnsnd) _resnsndiff ndiff_conn(PLUS)
     ndiff_conn(MINUS) psubstrate(B)
36 *.DEVTMPLT 27 R(g45rsnp) _ressnpoly poly_conn(PLUS) poly_conn(
     MINUS) psubstrate(B)
37 *.DEVTMPLT 28 R(g45rsnp) _ressnpoly_nw poly_conn(PLUS)
     poly_conn(MINUS) nwell_conn(B)
38 *.DEVTMPLT 29 R(g45rnsnp) _resnsnpoly poly_conn(PLUS)
     poly_conn(MINUS) psubstrate(B)
39 *.DEVTMPLT 30 R(g45rnsnp) _resnsnpoly_nw poly_conn(PLUS)
     poly_conn(MINUS) nwell_conn(B)
40 *.DEVTMPLT 31 R(g45rspd) _resspdiff pdiff_conn(PLUS)
     pdiff_conn(MINUS) nwell_conn(B)
41 *.DEVTMPLT 32 R(g45rnspd) _resnspdiff pdiff_conn(PLUS)
     pdiff_conn(MINUS) nwell_conn(B)
42 *.DEVTMPLT 33 R(g45rspp) _resspoly poly_conn(PLUS) poly_conn(
     MINUS) psubstrate(B)
43 *.DEVTMPLT 34 R(g45rspp) _resspoly_nw poly_conn(PLUS)
     poly_conn(MINUS) nwell_conn(B)
44 *.DEVTMPLT 35 R(g45rnspp) _resnspoly poly_conn(PLUS)
     poly_conn(MINUS) psubstrate(B)
45 *.DEVTMPLT 36 R(g45rnspp) _resnspoly_nw poly_conn(PLUS)
     poly_conn(MINUS) nwell_conn(B)
46 *.DEVTMPLT 37 R(g45rnws) _resnwsti nwell_conn(PLUS) nwell_conn
     (MINUS) psubstrate(B)
```

```
47 *.DEVTMPLT 38 R(g45rnwo) _resnwoxide nwell_conn(PLUS)
     nwell_conn(MINUS) psubstrate(B)
48 *.DEVTMPLT 39 D(g45nd1svt) _ndio psubstrate(PLUS) ndiff_conn(
     MINUS)
49 *.DEVTMPLT 40 D(g45nd1lvt) _ndio_lvt psubstrate(PLUS)
     ndiff_conn(MINUS)
50 *.DEVTMPLT 41 D(g45nd1hvt) _ndio_hvt psubstrate(PLUS)
     ndiff_conn(MINUS)
51 *.DEVTMPLT 42 D(g45nd1nvt) _ndio_nvt psubstrate(PLUS)
     ndiff_conn(MINUS)
52 *.DEVTMPLT 43 D(g45nd2svt) _ndio_2v psubstrate(PLUS)
     ndiff_conn(MINUS)
53 *.DEVTMPLT 44 D(g45nd2nvt) _ndio_2v_nvt psubstrate(PLUS)
     ndiff_conn(MINUS)
54 *.DEVTMPLT 45 D(g45pd1svt) _pdio pdiff_conn(PLUS) nwell_conn(
     MINUS)
55 *.DEVTMPLT 46 D(g45pd1lvt) _pdio_lvt pdiff_conn(PLUS)
     nwell_conn(MINUS)
56 *.DEVTMPLT 47 D(g45pd1hvt) _pdio_hvt pdiff_conn(PLUS)
     nwell_conn(MINUS)
57 *.DEVTMPLT 48 D(g45pd2svt) _pdio_2v pdiff_conn(PLUS)
     nwell_conn(MINUS)
58 *.DEVTMPLT 49 Q(g45vpnp2) _vpnp2 psubstrate(C) nwell_conn(B)
     pdiff_conn(E)
```

```
59 *.DEVTMPLT 50 Q(g45vpnp5) _vpnp5 psubstrate(C) nwell_conn(B)
       pdiff_conn(E)
60 *.DEVTMPLT 51 Q(g45vpnp10) _vpnp10 psubstrate(C) nwell_conn(B)
        pdiff_conn(E)
61 *.DEVTMPLT 52 Q(g45vnpn2) _npn2 nwell_conn(C) psubstrate(B)
       npn_emit(E)
62 *.DEVTMPLT 53 Q(g45vnpn5) _npn5 nwell_conn(C) psubstrate(B)
       npn_emit(E)
63 *.DEVTMPLT 54 Q(g45vnpn10) _npn10 nwell_conn(C) psubstrate(B)
       npn_emit(E)
64 *.DEVTMPLT 55 C(g45cmim) _mimcap CapMetal(PLUS) metal10_conn(
      MINUS) psubstrate(B)
65 *.DEVTMPLT 56 L(g45inda) _ind_a ind10(PLUS) ind11(MINUS)
       psubstrate(B)
66 *.DEVTMPLT 57 L(g45inds) _ind_s ind11(PLUS) ind11(MINUS)
       psubstrate(B)
67
68 * ++++++++++++++++++++++++++++++++++++++++++++++++++++++++ *
69 * Sub cell: L                                              *
70 * ++++++++++++++++++++++++++++++++++++++++++++++++++++++++ *
71 .subckt L PLUS MINUS B
72 .ends L
73
74 * ++++++++++++++++++++++++++++++++++++++++++++++++++++++++ *
75 * Sub cell: pmos2v$$5                                      *
```

```
76 * ++++++++++++++++++++++++++++++++++++++++++++++++++++++++ *
77 .subckt pmos2v$$5 1 2 3
78 ** N=4 EP=3 FDC=1
79 M0 1 3 2 1 g45p2svt L=1.8e-07 W=3.2e-07 AD=4.8e-14 AS=4.8e-14
     PD=9.4e-07 PS=9.4e-07 fw=3.2e-07 sa=1.5e-07 sb=1.5e-07 sca
     =20.9226 scb=0.0222886 scc=0.00079148 $X=0 $Y=0 $dt=11
80 .ends pmos2v$$5
81
82 * ++++++++++++++++++++++++++++++++++++++++++++++++++++++++ *
83 * Sub cell: nmos2v$$6                                      *
84 * ++++++++++++++++++++++++++++++++++++++++++++++++++++++++ *
85 .subckt nmos2v$$6 1 2 3
86 ** N=3 EP=3 FDC=1
87 M0 1 3 2 1 g45n2svt L=1.8e-07 W=3.2e-07 AD=4.8e-14 AS=4.8e-14
     PD=9.4e-07 PS=9.4e-07 fw=3.2e-07 sa=1.5e-07 sb=1.5e-07 sca
     =7.57282 scb=0.00541262 scc=0.000113799 $X=0 $Y=0 $dt=4
88 .ends nmos2v$$6
89
90 * ++++++++++++++++++++++++++++++++++++++++++++++++++++++++ *
91 * Sub cell: DS_INVX1                                       *
92 * ++++++++++++++++++++++++++++++++++++++++++++++++++++++++ *
93 .subckt DS_INVX1 A VDD VSS Y
94 ** N=4 EP=4 FDC=2
95 X1 VDD Y A pmos2v$$5 $T=1440 2100 0 0 $X=660 $Y=1620
96 X2 VSS Y A nmos2v$$6 $T=1440 360 0 0 $X=780 $Y=0
```

```
97 .ends DS_INVX1
```

Listing IV.1: Inverter SPI

IV.2 Transmission Gate Switch SPI

```
1  * ++++++++++++++++++++++++++++++++++++++++++++++++++++++++ *
2  * CDL Netlist:                                             *
3  *                                                          *
4  * Cell Name   : DS_VGA_SWITCH                              *
5  * Netlisted   : Sun Apr 17 12:27:09 2022                   *
6  * PVS Version: 15.24-s451 Thu Jun  8 20:13:49 PDT 2017 *
7  * ++++++++++++++++++++++++++++++++++++++++++++++++++++++++ *
8  *.LDD
9  *.DEVTMPLT 0 MN(g45n1svt) _nmos1v ndiff_conn(D) poly_conn(G)
       ndiff_conn(S) psubstrate(B)
10 *.DEVTMPLT 1 MN(g45n1hvt) _nmos1v_hvt ndiff_conn(D) poly_conn(
       G) ndiff_conn(S) psubstrate(B)
11 *.DEVTMPLT 2 MN(g45n1lvt) _nmos1v_lvt ndiff_conn(D) poly_conn(
       G) ndiff_conn(S) psubstrate(B)
12 *.DEVTMPLT 3 MN(g45n1nvt) _nmos_12_native ndiff_conn(D)
       poly_conn(G) ndiff_conn(S) psubstrate(B)
13 *.DEVTMPLT 4 MN(g45n2svt) _nmos_25 ndiff_conn(D) poly_conn(G)
       ndiff_conn(S) psubstrate(B)
14 *.DEVTMPLT 5 MN(g45n2nvt) _nmos_25_native ndiff_conn(D)
       poly_conn(G) ndiff_conn(S) psubstrate(B)
15 *.DEVTMPLT 6 MN(g45ncap1) _nmoscap1v ndiff_conn(D) poly_conn(G
       ) ndiff_conn(S) psubstrate(B)
```

```
16 *.DEVTMPLT 7 MN(g45ncap2) _nmoscap2v ndiff_conn(D) poly_conn(G
   ) ndiff_conn(S) psubstrate(B)
17 *.DEVTMPLT 8 MP(g45p1svt) _pmos1v pdiff_conn(D) poly_conn(G)
   pdiff_conn(S) nwell_conn(B)
18 *.DEVTMPLT 9 MP(g45p1hvt) _pmos1v_hvt pdiff_conn(D) poly_conn(
   G) pdiff_conn(S) nwell_conn(B)
19 *.DEVTMPLT 10 MP(g45p1lvt) _pmos1v_lvt pdiff_conn(D) poly_conn
   (G) pdiff_conn(S) nwell_conn(B)
20 *.DEVTMPLT 11 MP(g45p2svt) _pmos2v pdiff_conn(D) poly_conn(G)
   pdiff_conn(S) nwell_conn(B)
21 *.DEVTMPLT 12 MP(g45pcap1) _pmoscap1v pdiff_conn(D) poly_conn(
   G) pdiff_conn(S) nwell_conn(B)
22 *.DEVTMPLT 13 MP(g45pcap2) _pmoscap2v pdiff_conn(D) poly_conn(
   G) pdiff_conn(S) nwell_conn(B)
23 *.DEVTMPLT 14 R(g45rm1) _resm1 metal1_conn(PLUS) metal1_conn(
   MINUS)
24 *.DEVTMPLT 15 R(g45rm2) _resm2 metal2_conn(PLUS) metal2_conn(
   MINUS)
25 *.DEVTMPLT 16 R(g45rm3) _resm3 metal3_conn(PLUS) metal3_conn(
   MINUS)
26 *.DEVTMPLT 17 R(g45rm4) _resm4 metal4_conn(PLUS) metal4_conn(
   MINUS)
27 *.DEVTMPLT 18 R(g45rm5) _resm5 metal5_conn(PLUS) metal5_conn(
   MINUS)
```

```
28 *.DEVTMPLT 19 R(g45rm6) _resm6 metal6_conn(PLUS) metal6_conn(
     MINUS)
29 *.DEVTMPLT 20 R(g45rm7) _resm7 metal7_conn(PLUS) metal7_conn(
     MINUS)
30 *.DEVTMPLT 21 R(g45rm8) _resm8 metal8_conn(PLUS) metal8_conn(
     MINUS)
31 *.DEVTMPLT 22 R(g45rm9) _resm9 metal9_conn(PLUS) metal9_conn(
     MINUS)
32 *.DEVTMPLT 23 R(g45rm10) _resm10 metal10_conn(PLUS)
     metal10_conn(MINUS)
33 *.DEVTMPLT 24 R(g45rm11) _resm11 metal11_conn(PLUS)
     metal11_conn(MINUS)
34 *.DEVTMPLT 25 R(g45rsnd) _ressndiff ndiff_conn(PLUS)
     ndiff_conn(MINUS) psubstrate(B)
35 *.DEVTMPLT 26 R(g45rnsnd) _resnsndiff ndiff_conn(PLUS)
     ndiff_conn(MINUS) psubstrate(B)
36 *.DEVTMPLT 27 R(g45rsnp) _ressnpoly poly_conn(PLUS) poly_conn(
     MINUS) psubstrate(B)
37 *.DEVTMPLT 28 R(g45rsnp) _ressnpoly_nw poly_conn(PLUS)
     poly_conn(MINUS) nwell_conn(B)
38 *.DEVTMPLT 29 R(g45rnsnp) _resnsnpoly poly_conn(PLUS)
     poly_conn(MINUS) psubstrate(B)
39 *.DEVTMPLT 30 R(g45rnsnp) _resnsnpoly_nw poly_conn(PLUS)
     poly_conn(MINUS) nwell_conn(B)
```

```
40 *.DEVTMPLT 31 R(g45rspd) _resspdiff pdiff_conn(PLUS)
     pdiff_conn(MINUS) nwell_conn(B)
41 *.DEVTMPLT 32 R(g45rnspd) _resnspdiff pdiff_conn(PLUS)
     pdiff_conn(MINUS) nwell_conn(B)
42 *.DEVTMPLT 33 R(g45rspp) _ressppoly poly_conn(PLUS) poly_conn(
     MINUS) psubstrate(B)
43 *.DEVTMPLT 34 R(g45rspp) _ressppoly_nw poly_conn(PLUS)
     poly_conn(MINUS) nwell_conn(B)
44 *.DEVTMPLT 35 R(g45rnspp) _resnsppoly poly_conn(PLUS)
     poly_conn(MINUS) psubstrate(B)
45 *.DEVTMPLT 36 R(g45rnspp) _resnsppoly_nw poly_conn(PLUS)
     poly_conn(MINUS) nwell_conn(B)
46 *.DEVTMPLT 37 R(g45rnws) _resnwsti nwell_conn(PLUS) nwell_conn
     (MINUS) psubstrate(B)
47 *.DEVTMPLT 38 R(g45rnwo) _resnwoxide nwell_conn(PLUS)
     nwell_conn(MINUS) psubstrate(B)
48 *.DEVTMPLT 39 D(g45nd1svt) _ndio psubstrate(PLUS) ndiff_conn(
     MINUS)
49 *.DEVTMPLT 40 D(g45nd1lvt) _ndio_lvt psubstrate(PLUS)
     ndiff_conn(MINUS)
50 *.DEVTMPLT 41 D(g45nd1hvt) _ndio_hvt psubstrate(PLUS)
     ndiff_conn(MINUS)
51 *.DEVTMPLT 42 D(g45nd1nvt) _ndio_nvt psubstrate(PLUS)
     ndiff_conn(MINUS)
```

```
52 *.DEVTMPLT 43 D(g45nd2svt) _ndio_2v psubstrate(PLUS)
     ndiff_conn(MINUS)
53 *.DEVTMPLT 44 D(g45nd2nvt) _ndio_2v_nvt psubstrate(PLUS)
     ndiff_conn(MINUS)
54 *.DEVTMPLT 45 D(g45pd1svt) _pdio pdiff_conn(PLUS) nwell_conn(
     MINUS)
55 *.DEVTMPLT 46 D(g45pd1lvt) _pdio_lvt pdiff_conn(PLUS)
     nwell_conn(MINUS)
56 *.DEVTMPLT 47 D(g45pd1hvt) _pdio_hvt pdiff_conn(PLUS)
     nwell_conn(MINUS)
57 *.DEVTMPLT 48 D(g45pd2svt) _pdio_2v pdiff_conn(PLUS)
     nwell_conn(MINUS)
58 *.DEVTMPLT 49 Q(g45vpnp2) _vpnp2 psubstrate(C) nwell_conn(B)
     pdiff_conn(E)
59 *.DEVTMPLT 50 Q(g45vpnp5) _vpnp5 psubstrate(C) nwell_conn(B)
     pdiff_conn(E)
60 *.DEVTMPLT 51 Q(g45vpnp10) _vpnp10 psubstrate(C) nwell_conn(B)
      pdiff_conn(E)
61 *.DEVTMPLT 52 Q(g45vnpn2) _npn2 nwell_conn(C) psubstrate(B)
     npn_emit(E)
62 *.DEVTMPLT 53 Q(g45vnpn5) _npn5 nwell_conn(C) psubstrate(B)
     npn_emit(E)
63 *.DEVTMPLT 54 Q(g45vnpn10) _npn10 nwell_conn(C) psubstrate(B)
     npn_emit(E)
```

```
64 *.DEVTMPLT 55 C(g45cmim) _mimcap CapMetal(PLUS) metal10_conn(
     MINUS) psubstrate(B)
65 *.DEVTMPLT 56 L(g45inda) _ind_a ind10(PLUS) ind11(MINUS)
     psubstrate(B)
66 *.DEVTMPLT 57 L(g45inds) _ind_s ind11(PLUS) ind11(MINUS)
     psubstrate(B)
67
68 * ++++++++++++++++++++++++++++++++++++++++++++++++++++++++ *
69 * Sub cell: L                                              *
70 * ++++++++++++++++++++++++++++++++++++++++++++++++++++++++ *
71 .subckt L PLUS MINUS B
72 .ends L
73
74 * ++++++++++++++++++++++++++++++++++++++++++++++++++++++++ *
75 * Sub cell: pmos2v$$9                                      *
76 * ++++++++++++++++++++++++++++++++++++++++++++++++++++++++ *
77 .subckt pmos2v$$9 1 2 3
78 ** N=4 EP=3 FDC=1
79 M0 1 3 2 1 g45p2svt L=1.8e-07 W=3.2e-07 AD=4.8e-14 AS=4.8e-14
     PD=9.4e-07 PS=9.4e-07 fw=3.2e-07 sa=1.5e-07 sb=1.5e-07 sca
     =14.2397 scb=0.0134273 scc=0.000419873 $X=0 $Y=0 $dt=11
80 .ends pmos2v$$9
81
82 * ++++++++++++++++++++++++++++++++++++++++++++++++++++++++ *
83 * Sub cell: nmos2v$$10                                     *
```

```
84 * ++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++ *
85 .subckt nmos2v$$10 1 2 3
86 ** N=3 EP=3 FDC=1
87 M0 1 3 2 1 g45n2svt L=1.8e-07 W=3.2e-07 AD=4.8e-14 AS=4.8e-14
       PD=9.4e-07 PS=9.4e-07 fw=3.2e-07 sa=1.5e-07 sb=1.5e-07 sca
       =7.57282 scb=0.00541262 scc=0.000113799 $X=0 $Y=0 $dt=4
88 .ends nmos2v$$10
89
90 * ++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++ *
91 * Sub cell: DS_INVX1                                            *
92 * ++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++ *
93 .subckt DS_INVX1 VDD VSS A Y
94 ** N=4 EP=4 FDC=2
95 X1 VDD Y A pmos2v$$9 $T=1440 2100 0 0 $X=660 $Y=1620
96 X2 VSS Y A nmos2v$$10 $T=1440 360 0 0 $X=780 $Y=0
97 .ends DS_INVX1
98
99 * ++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++ *
100 * Sub cell: pmos2v$$11                                          *
101 * ++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++ *
102 .subckt pmos2v$$11 1 2 3 5
103 ** N=5 EP=4 FDC=1
104 M0 1 3 2 5 g45p2svt L=1.8e-07 W=2e-06 AD=3e-13 AS=3e-13 PD=4.3
       e-06 PS=4.3e-06 fw=2e-06 sa=1.5e-07 sb=1.5e-07 sca=11.1903
       scb=0.0100744 scc=0.000155967 $X=0 $Y=0 $dt=11
```

```
105 .ends pmos2v$$11
106
107 * ++++++++++++++++++++++++++++++++++++++++++++++++++++++++ *
108 * Sub cell: nmos2v$$12                                     *
109 * ++++++++++++++++++++++++++++++++++++++++++++++++++++++++ *
110 .subckt nmos2v$$12 1 2 3 4
111 ** N=4 EP=4 FDC=1
112 M0 1 3 2 4 g45n2svt L=1.8e-07 W=2e-06 AD=3e-13 AS=3e-13 PD=4.3
        e-06 PS=4.3e-06 fw=2e-06 sa=1.5e-07 sb=1.5e-07 sca=2.36608
        scb=5.00472e-05 scc=1.28342e-09 $X=0 $Y=0 $dt=4
113 .ends nmos2v$$12
114
115 * ++++++++++++++++++++++++++++++++++++++++++++++++++++++++ *
116 * Sub cell: DS_VGA_SWITCH                                  *
117 * ++++++++++++++++++++++++++++++++++++++++++++++++++++++++ *
118 .subckt DS_VGA_SWITCH VDD VSS vin vin_n vout
119 ** N=6 EP=5 FDC=4
120 X0 VDD VSS vin_n 4 DS_INVX1 $T=0 4720 0 0 $X=0 $Y=4720
121 X1 vin vout 4 VDD pmos2v$$11 $T=1440 8420 0 0 $X=660 $Y=7940
122 X2 vout vin vin_n VSS nmos2v$$12 $T=1800 360 1 180 $X=780 $Y=0
123 .ends DS_VGA_SWITCH
```

Listing IV.2: Transmission Gate Switch SPI

IV.3 Two Stage Op-amp (Class AB Output Stage) SPI

```
1  * ++++++++++++++++++++++++++++++++++++++++++++++++++++++++ *
2  * CDL Netlist:                                             *
3  *                                                          *
4  * Cell Name   : DS_VGA_OPAMP                               *
5  * Netlisted   : Sun Apr 17 12:39:07 2022                   *
6  * PVS Version: 15.24-s451 Thu Jun  8 20:13:49 PDT 2017 *
7  * ++++++++++++++++++++++++++++++++++++++++++++++++++++++++ *
8  *.LDD
9  *.DEVTMPLT 0 MN(g45n1svt) _nmos1v ndiff_conn(D) poly_conn(G)
       ndiff_conn(S) psubstrate(B)
10 *.DEVTMPLT 1 MN(g45n1hvt) _nmos1v_hvt ndiff_conn(D) poly_conn(
       G) ndiff_conn(S) psubstrate(B)
11 *.DEVTMPLT 2 MN(g45n1lvt) _nmos1v_lvt ndiff_conn(D) poly_conn(
       G) ndiff_conn(S) psubstrate(B)
12 *.DEVTMPLT 3 MN(g45n1nvt) _nmos_12_native ndiff_conn(D)
       poly_conn(G) ndiff_conn(S) psubstrate(B)
13 *.DEVTMPLT 4 MN(g45n2svt) _nmos_25 ndiff_conn(D) poly_conn(G)
       ndiff_conn(S) psubstrate(B)
14 *.DEVTMPLT 5 MN(g45n2nvt) _nmos_25_native ndiff_conn(D)
       poly_conn(G) ndiff_conn(S) psubstrate(B)
15 *.DEVTMPLT 6 MN(g45ncap1) _nmoscap1v ndiff_conn(D) poly_conn(G
       ) ndiff_conn(S) psubstrate(B)
```

```
16 *.DEVTMPLT 7 MN(g45ncap2) _nmoscap2v ndiff_conn(D) poly_conn(G
   ) ndiff_conn(S) psubstrate(B)
17 *.DEVTMPLT 8 MP(g45p1svt) _pmos1v pdiff_conn(D) poly_conn(G)
   pdiff_conn(S) nwell_conn(B)
18 *.DEVTMPLT 9 MP(g45p1hvt) _pmos1v_hvt pdiff_conn(D) poly_conn(
   G) pdiff_conn(S) nwell_conn(B)
19 *.DEVTMPLT 10 MP(g45p1lvt) _pmos1v_lvt pdiff_conn(D) poly_conn
   (G) pdiff_conn(S) nwell_conn(B)
20 *.DEVTMPLT 11 MP(g45p2svt) _pmos2v pdiff_conn(D) poly_conn(G)
   pdiff_conn(S) nwell_conn(B)
21 *.DEVTMPLT 12 MP(g45pcap1) _pmoscap1v pdiff_conn(D) poly_conn(
   G) pdiff_conn(S) nwell_conn(B)
22 *.DEVTMPLT 13 MP(g45pcap2) _pmoscap2v pdiff_conn(D) poly_conn(
   G) pdiff_conn(S) nwell_conn(B)
23 *.DEVTMPLT 14 R(g45rm1) _resm1 metal1_conn(PLUS) metal1_conn(
   MINUS)
24 *.DEVTMPLT 15 R(g45rm2) _resm2 metal2_conn(PLUS) metal2_conn(
   MINUS)
25 *.DEVTMPLT 16 R(g45rm3) _resm3 metal3_conn(PLUS) metal3_conn(
   MINUS)
26 *.DEVTMPLT 17 R(g45rm4) _resm4 metal4_conn(PLUS) metal4_conn(
   MINUS)
27 *.DEVTMPLT 18 R(g45rm5) _resm5 metal5_conn(PLUS) metal5_conn(
   MINUS)
```

```
28 *.DEVTMPLT 19 R(g45rm6) _resm6 metal6_conn(PLUS) metal6_conn(
     MINUS)
29 *.DEVTMPLT 20 R(g45rm7) _resm7 metal7_conn(PLUS) metal7_conn(
     MINUS)
30 *.DEVTMPLT 21 R(g45rm8) _resm8 metal8_conn(PLUS) metal8_conn(
     MINUS)
31 *.DEVTMPLT 22 R(g45rm9) _resm9 metal9_conn(PLUS) metal9_conn(
     MINUS)
32 *.DEVTMPLT 23 R(g45rm10) _resm10 metal10_conn(PLUS)
     metal10_conn(MINUS)
33 *.DEVTMPLT 24 R(g45rm11) _resm11 metal11_conn(PLUS)
     metal11_conn(MINUS)
34 *.DEVTMPLT 25 R(g45rsnd) _ressndiff ndiff_conn(PLUS)
     ndiff_conn(MINUS) psubstrate(B)
35 *.DEVTMPLT 26 R(g45rnsnd) _resnsndiff ndiff_conn(PLUS)
     ndiff_conn(MINUS) psubstrate(B)
36 *.DEVTMPLT 27 R(g45rsnp) _ressnpoly poly_conn(PLUS) poly_conn(
     MINUS) psubstrate(B)
37 *.DEVTMPLT 28 R(g45rsnp) _ressnpoly_nw poly_conn(PLUS)
     poly_conn(MINUS) nwell_conn(B)
38 *.DEVTMPLT 29 R(g45rnsnp) _resnsnpoly poly_conn(PLUS)
     poly_conn(MINUS) psubstrate(B)
39 *.DEVTMPLT 30 R(g45rnsnp) _resnsnpoly_nw poly_conn(PLUS)
     poly_conn(MINUS) nwell_conn(B)
```

```
40 *.DEVTMPLT 31 R(g45rspd) _resspdiff pdiff_conn(PLUS)
     pdiff_conn(MINUS) nwell_conn(B)
41 *.DEVTMPLT 32 R(g45rnspd) _resnspdiff pdiff_conn(PLUS)
     pdiff_conn(MINUS) nwell_conn(B)
42 *.DEVTMPLT 33 R(g45rspp) _ressppoly poly_conn(PLUS) poly_conn(
     MINUS) psubstrate(B)
43 *.DEVTMPLT 34 R(g45rspp) _ressppoly_nw poly_conn(PLUS)
     poly_conn(MINUS) nwell_conn(B)
44 *.DEVTMPLT 35 R(g45rnspp) _resnsppoly poly_conn(PLUS)
     poly_conn(MINUS) psubstrate(B)
45 *.DEVTMPLT 36 R(g45rnspp) _resnsppoly_nw poly_conn(PLUS)
     poly_conn(MINUS) nwell_conn(B)
46 *.DEVTMPLT 37 R(g45rnws) _resnwsti nwell_conn(PLUS) nwell_conn
     (MINUS) psubstrate(B)
47 *.DEVTMPLT 38 R(g45rnwo) _resnwoxide nwell_conn(PLUS)
     nwell_conn(MINUS) psubstrate(B)
48 *.DEVTMPLT 39 D(g45nd1svt) _ndio psubstrate(PLUS) ndiff_conn(
     MINUS)
49 *.DEVTMPLT 40 D(g45nd1lvt) _ndio_lvt psubstrate(PLUS)
     ndiff_conn(MINUS)
50 *.DEVTMPLT 41 D(g45nd1hvt) _ndio_hvt psubstrate(PLUS)
     ndiff_conn(MINUS)
51 *.DEVTMPLT 42 D(g45nd1nvt) _ndio_nvt psubstrate(PLUS)
     ndiff_conn(MINUS)
```

```
52 *.DEVTMPLT 43 D(g45nd2svt) _ndio_2v psubstrate(PLUS)
     ndiff_conn(MINUS)
53 *.DEVTMPLT 44 D(g45nd2nvt) _ndio_2v_nvt psubstrate(PLUS)
     ndiff_conn(MINUS)
54 *.DEVTMPLT 45 D(g45pd1svt) _pdio pdiff_conn(PLUS) nwell_conn(
     MINUS)
55 *.DEVTMPLT 46 D(g45pd1lvt) _pdio_lvt pdiff_conn(PLUS)
     nwell_conn(MINUS)
56 *.DEVTMPLT 47 D(g45pd1hvt) _pdio_hvt pdiff_conn(PLUS)
     nwell_conn(MINUS)
57 *.DEVTMPLT 48 D(g45pd2svt) _pdio_2v pdiff_conn(PLUS)
     nwell_conn(MINUS)
58 *.DEVTMPLT 49 Q(g45vpnp2) _vpnp2 psubstrate(C) nwell_conn(B)
     pdiff_conn(E)
59 *.DEVTMPLT 50 Q(g45vpnp5) _vpnp5 psubstrate(C) nwell_conn(B)
     pdiff_conn(E)
60 *.DEVTMPLT 51 Q(g45vpnp10) _vpnp10 psubstrate(C) nwell_conn(B)
      pdiff_conn(E)
61 *.DEVTMPLT 52 Q(g45vnpn2) _npn2 nwell_conn(C) psubstrate(B)
     npn_emit(E)
62 *.DEVTMPLT 53 Q(g45vnpn5) _npn5 nwell_conn(C) psubstrate(B)
     npn_emit(E)
63 *.DEVTMPLT 54 Q(g45vnpn10) _npn10 nwell_conn(C) psubstrate(B)
     npn_emit(E)
```

```
64 *.DEVTMPLT 55 C(g45cmim) _mimcap CapMetal(PLUS) metal10_conn(
     MINUS) psubstrate(B)
65 *.DEVTMPLT 56 L(g45inda) _ind_a ind10(PLUS) ind11(MINUS)
     psubstrate(B)
66 *.DEVTMPLT 57 L(g45inds) _ind_s ind11(PLUS) ind11(MINUS)
     psubstrate(B)
67
68 * ++++++++++++++++++++++++++++++++++++++++++++++++++++++++ *
69 * Sub cell: L                                              *
70 * ++++++++++++++++++++++++++++++++++++++++++++++++++++++++ *
71 .subckt L PLUS MINUS B
72 .ends L
73
74 * ++++++++++++++++++++++++++++++++++++++++++++++++++++++++ *
75 * Sub cell: pmos2v$$19                                     *
76 * ++++++++++++++++++++++++++++++++++++++++++++++++++++++++ *
77 .subckt pmos2v$$19 2
78 ** N=11 EP=1 FDC=8
79 M0 2 2 2 2 g45p2svt L=6e-07 W=4e-07 AD=8e-14 AS=6e-14 PD=1.2e
     -06 PS=1.1e-06 fw=4e-07 sa=1.5e-07 sb=2e-06 sca=3.00153 scb
     =9.80227e-05 scc=1.47329e-08 $X=0 $Y=0 $dt=11
80 M1 2 2 2 2 g45p2svt L=6e-07 W=4e-07 AD=8e-14 AS=8e-14 PD=1.2e
     -06 PS=1.2e-06 fw=4e-07 sa=9.5e-07 sb=2e-06 sca=2.67857 scb
     =4.09292e-05 scc=9.01501e-10 $X=1600 $Y=0 $dt=11
```

```
81 M2 2 2 2 2 g45p2svt L=6e-07 W=4e-07 AD=8e-14 AS=8e-14 PD=1.2e
     -06 PS=1.2e-06 fw=4e-07 sa=1.75e-06 sb=2e-06 sca=2.67857
     scb=4.09292e-05 scc=9.01501e-10 $X=3200 $Y=0 $dt=11
82 M3 2 2 2 2 g45p2svt L=6e-07 W=4e-07 AD=8e-14 AS=8e-14 PD=1.2e
     -06 PS=1.2e-06 fw=4e-07 sa=2e-06 sb=2e-06 sca=2.67857 scb
     =4.09292e-05 scc=9.01501e-10 $X=4800 $Y=0 $dt=11
83 M4 2 2 2 2 g45p2svt L=6e-07 W=4e-07 AD=8e-14 AS=8e-14 PD=1.2e
     -06 PS=1.2e-06 fw=4e-07 sa=2e-06 sb=2e-06 sca=2.67857 scb
     =4.09292e-05 scc=9.01501e-10 $X=6400 $Y=0 $dt=11
84 M5 2 2 2 2 g45p2svt L=6e-07 W=4e-07 AD=8e-14 AS=8e-14 PD=1.2e
     -06 PS=1.2e-06 fw=4e-07 sa=2e-06 sb=2e-06 sca=2.67857 scb
     =4.09292e-05 scc=9.01501e-10 $X=8000 $Y=0 $dt=11
85 M6 2 2 2 2 g45p2svt L=6e-07 W=4e-07 AD=8e-14 AS=8e-14 PD=1.2e
     -06 PS=1.2e-06 fw=4e-07 sa=2e-06 sb=2e-06 sca=2.67857 scb
     =4.09292e-05 scc=9.01501e-10 $X=9600 $Y=0 $dt=11
86 M7 2 2 2 2 g45p2svt L=6e-07 W=4e-07 AD=8e-14 AS=8e-14 PD=1.2e
     -06 PS=1.2e-06 fw=4e-07 sa=2e-06 sb=2e-06 sca=2.67857 scb
     =4.09292e-05 scc=9.01501e-10 $X=11200 $Y=0 $dt=11
87 .ends pmos2v$$19
88
89 * ++++++++++++++++++++++++++++++++++++++++++++++++++++++++++ *
90 * Sub cell: pmos2v$$20                                       *
91 * ++++++++++++++++++++++++++++++++++++++++++++++++++++++++++ *
92 .subckt pmos2v$$20 1 2 3 5
93 ** N=5 EP=4 FDC=10
```

```
94 M0 2 3 1 5 g45p2svt L=6e-07 W=4e-07 AD=8e-14 AS=8e-14 PD=1.2e
    -06 PS=1.2e-06 fw=4e-07 sa=2e-06 sb=2e-06 sca=8.4747 scb
    =0.00743239 scc=0.000298091 $X=0 $Y=0 $dt=11
95 M1 1 3 2 5 g45p2svt L=6e-07 W=4e-07 AD=8e-14 AS=8e-14 PD=1.2e
    -06 PS=1.2e-06 fw=4e-07 sa=2e-06 sb=2e-06 sca=8.4747 scb
    =0.00743239 scc=0.000298091 $X=1600 $Y=0 $dt=11
96 M2 2 3 1 5 g45p2svt L=6e-07 W=4e-07 AD=8e-14 AS=8e-14 PD=1.2e
    -06 PS=1.2e-06 fw=4e-07 sa=2e-06 sb=2e-06 sca=8.4747 scb
    =0.00743239 scc=0.000298091 $X=3200 $Y=0 $dt=11
97 M3 1 3 2 5 g45p2svt L=6e-07 W=4e-07 AD=8e-14 AS=8e-14 PD=1.2e
    -06 PS=1.2e-06 fw=4e-07 sa=2e-06 sb=2e-06 sca=8.4747 scb
    =0.00743239 scc=0.000298091 $X=4800 $Y=0 $dt=11
98 M4 2 3 1 5 g45p2svt L=6e-07 W=4e-07 AD=8e-14 AS=8e-14 PD=1.2e
    -06 PS=1.2e-06 fw=4e-07 sa=2e-06 sb=2e-06 sca=8.4747 scb
    =0.00743239 scc=0.000298091 $X=6400 $Y=0 $dt=11
99 M5 1 3 2 5 g45p2svt L=6e-07 W=4e-07 AD=8e-14 AS=8e-14 PD=1.2e
    -06 PS=1.2e-06 fw=4e-07 sa=2e-06 sb=2e-06 sca=8.4747 scb
    =0.00743239 scc=0.000298091 $X=8000 $Y=0 $dt=11
100 M6 2 3 1 5 g45p2svt L=6e-07 W=4e-07 AD=8e-14 AS=8e-14 PD=1.2e
    -06 PS=1.2e-06 fw=4e-07 sa=2e-06 sb=2e-06 sca=8.4747 scb
    =0.00743239 scc=0.000298091 $X=9600 $Y=0 $dt=11
101 M7 1 3 2 5 g45p2svt L=6e-07 W=4e-07 AD=8e-14 AS=8e-14 PD=1.2e
    -06 PS=1.2e-06 fw=4e-07 sa=2e-06 sb=1.75e-06 sca=8.4747 scb
    =0.00743239 scc=0.000298091 $X=11200 $Y=0 $dt=11
```

```
M8 2 3 1 5 g45p2svt L=6e-07 W=4e-07 AD=8e-14 AS=8e-14 PD=1.2e
    -06 PS=1.2e-06 fw=4e-07 sa=2e-06 sb=9.5e-07 sca=8.4747 scb
    =0.00743239 scc=0.000298091 $X=12800 $Y=0 $dt=11
M9 1 3 2 5 g45p2svt L=6e-07 W=4e-07 AD=6e-14 AS=8e-14 PD=1.1e
    -06 PS=1.2e-06 fw=4e-07 sa=2e-06 sb=1.5e-07 sca=8.79766 scb
    =0.00748949 scc=0.000298105 $X=14400 $Y=0 $dt=11
.ends pmos2v$$20

* ++++++++++++++++++++++++++++++++++++++++++++++++++++++++ *
* Sub cell: pmos2v$$21                                     *
* ++++++++++++++++++++++++++++++++++++++++++++++++++++++++ *
.subckt pmos2v$$21 2
** N=7 EP=1 FDC=4
M0 2 2 2 2 g45p2svt L=6e-07 W=4e-07 AD=8e-14 AS=6e-14 PD=1.2e
    -06 PS=1.1e-06 fw=4e-07 sa=1.5e-07 sb=2e-06 sca=2.98259 scb
    =9.24817e-05 scc=1.23329e-08 $X=0 $Y=0 $dt=11
M1 2 2 2 2 g45p2svt L=6e-07 W=4e-07 AD=8e-14 AS=8e-14 PD=1.2e
    -06 PS=1.2e-06 fw=4e-07 sa=9.5e-07 sb=2e-06 sca=2.67857 scb
    =4.09292e-05 scc=9.01501e-10 $X=1600 $Y=0 $dt=11
M2 2 2 2 2 g45p2svt L=6e-07 W=4e-07 AD=8e-14 AS=8e-14 PD=1.2e
    -06 PS=1.2e-06 fw=4e-07 sa=1.75e-06 sb=2e-06 sca=2.67857
    scb=4.09292e-05 scc=9.01501e-10 $X=3200 $Y=0 $dt=11
M3 2 2 2 2 g45p2svt L=6e-07 W=4e-07 AD=8e-14 AS=8e-14 PD=1.2e
    -06 PS=1.2e-06 fw=4e-07 sa=2e-06 sb=2e-06 sca=2.67857 scb
    =4.09292e-05 scc=9.01501e-10 $X=4800 $Y=0 $dt=11
```

```
115 .ends pmos2v$$21
116
117 * ++++++++++++++++++++++++++++++++++++++++++++++++++++++++ *
118 * Sub cell: pmos2v$$22                                     *
119 * ++++++++++++++++++++++++++++++++++++++++++++++++++++++++ *
120 .subckt pmos2v$$22 2 3 4
121 ** N=5 EP=3 FDC=6
122 M0 2 3 4 2 g45p2svt L=6e-07 W=4e-07 AD=8e-14 AS=8e-14 PD=1.2e
    -06 PS=1.2e-06 fw=4e-07 sa=2e-06 sb=2e-06 sca=8.4747 scb
    =0.00743239 scc=0.000298091 $X=0 $Y=0 $dt=11
123 M1 4 3 2 2 g45p2svt L=6e-07 W=4e-07 AD=8e-14 AS=8e-14 PD=1.2e
    -06 PS=1.2e-06 fw=4e-07 sa=2e-06 sb=2e-06 sca=8.4747 scb
    =0.00743239 scc=0.000298091 $X=1600 $Y=0 $dt=11
124 M2 2 3 4 2 g45p2svt L=6e-07 W=4e-07 AD=8e-14 AS=8e-14 PD=1.2e
    -06 PS=1.2e-06 fw=4e-07 sa=2e-06 sb=2e-06 sca=8.4747 scb
    =0.00743239 scc=0.000298091 $X=3200 $Y=0 $dt=11
125 M3 4 3 2 2 g45p2svt L=6e-07 W=4e-07 AD=8e-14 AS=8e-14 PD=1.2e
    -06 PS=1.2e-06 fw=4e-07 sa=2e-06 sb=1.75e-06 sca=8.4747 scb
    =0.00743239 scc=0.000298091 $X=4800 $Y=0 $dt=11
126 M4 2 3 4 2 g45p2svt L=6e-07 W=4e-07 AD=8e-14 AS=8e-14 PD=1.2e
    -06 PS=1.2e-06 fw=4e-07 sa=2e-06 sb=9.5e-07 sca=8.4747 scb
    =0.00743239 scc=0.000298091 $X=6400 $Y=0 $dt=11
127 M5 4 3 2 2 g45p2svt L=6e-07 W=4e-07 AD=6e-14 AS=8e-14 PD=1.1e
    -06 PS=1.2e-06 fw=4e-07 sa=2e-06 sb=1.5e-07 sca=8.77873 scb
    =0.00748395 scc=0.000298102 $X=8000 $Y=0 $dt=11
```

```
128 .ends pmos2v$$22
129
130 * ++++++++++++++++++++++++++++++++++++++++++++++++++++++++ *
131 * Sub cell: nmos2v$$23                                     *
132 * ++++++++++++++++++++++++++++++++++++++++++++++++++++++++ *
133 .subckt nmos2v$$23 1 2 3
134 ** N=3 EP=3 FDC=4
135 M0 3 1 2 3 g45n2svt L=6e-07 W=4e-07 AD=8e-14 AS=8e-14 PD=1.2e
    -06 PS=1.2e-06 fw=4e-07 sa=2e-06 sb=2e-06 sca=2.67857 scb
    =4.09292e-05 scc=9.01501e-10 $X=0 $Y=0 $dt=4
136 M1 2 1 3 3 g45n2svt L=6e-07 W=4e-07 AD=8e-14 AS=8e-14 PD=1.2e
    -06 PS=1.2e-06 fw=4e-07 sa=2e-06 sb=1.75e-06 sca=2.67857
    scb=4.09292e-05 scc=9.01501e-10 $X=1600 $Y=0 $dt=4
137 M2 3 1 2 3 g45n2svt L=6e-07 W=4e-07 AD=8e-14 AS=8e-14 PD=1.2e
    -06 PS=1.2e-06 fw=4e-07 sa=2e-06 sb=9.5e-07 sca=2.67857 scb
    =4.09292e-05 scc=9.01501e-10 $X=3200 $Y=0 $dt=4
138 M3 2 1 3 3 g45n2svt L=6e-07 W=4e-07 AD=6e-14 AS=8e-14 PD=1.1e
    -06 PS=1.2e-06 fw=4e-07 sa=2e-06 sb=1.5e-07 sca=2.67857 scb
    =4.09292e-05 scc=9.01501e-10 $X=4800 $Y=0 $dt=4
139 .ends nmos2v$$23
140
141 * ++++++++++++++++++++++++++++++++++++++++++++++++++++++++ *
142 * Sub cell: nmos2v$$24                                     *
143 * ++++++++++++++++++++++++++++++++++++++++++++++++++++++++ *
144 .subckt nmos2v$$24 1
```

```
145  ** N=17  EP=1  FDC=16
146  M0 1 1 1 1 g45n2svt L=6e-07 W=4e-07 AD=8e-14 AS=6e-14 PD=1.2e
     -06 PS=1.1e-06 fw=4e-07 sa=1.5e-07 sb=2e-06 sca=2.67857 scb
     =4.09292e-05 scc=9.01501e-10 $X=0 $Y=0 $dt=4
147  M1 1 1 1 1 g45n2svt L=6e-07 W=4e-07 AD=8e-14 AS=8e-14 PD=1.2e
     -06 PS=1.2e-06 fw=4e-07 sa=9.5e-07 sb=2e-06 sca=2.67857 scb
     =4.09292e-05 scc=9.01501e-10 $X=1600 $Y=0 $dt=4
148  M2 1 1 1 1 g45n2svt L=6e-07 W=4e-07 AD=8e-14 AS=8e-14 PD=1.2e
     -06 PS=1.2e-06 fw=4e-07 sa=1.75e-06 sb=2e-06 sca=2.67857
     scb=4.09292e-05 scc=9.01501e-10 $X=3200 $Y=0 $dt=4
149  M3 1 1 1 1 g45n2svt L=6e-07 W=4e-07 AD=8e-14 AS=8e-14 PD=1.2e
     -06 PS=1.2e-06 fw=4e-07 sa=2e-06 sb=2e-06 sca=2.67857 scb
     =4.09292e-05 scc=9.01501e-10 $X=4800 $Y=0 $dt=4
150  M4 1 1 1 1 g45n2svt L=6e-07 W=4e-07 AD=8e-14 AS=8e-14 PD=1.2e
     -06 PS=1.2e-06 fw=4e-07 sa=2e-06 sb=2e-06 sca=2.67857 scb
     =4.09292e-05 scc=9.01501e-10 $X=6400 $Y=0 $dt=4
151  M5 1 1 1 1 g45n2svt L=6e-07 W=4e-07 AD=8e-14 AS=8e-14 PD=1.2e
     -06 PS=1.2e-06 fw=4e-07 sa=2e-06 sb=2e-06 sca=2.67857 scb
     =4.09292e-05 scc=9.01501e-10 $X=8000 $Y=0 $dt=4
152  M6 1 1 1 1 g45n2svt L=6e-07 W=4e-07 AD=8e-14 AS=8e-14 PD=1.2e
     -06 PS=1.2e-06 fw=4e-07 sa=2e-06 sb=2e-06 sca=2.67857 scb
     =4.09292e-05 scc=9.01501e-10 $X=9600 $Y=0 $dt=4
153  M7 1 1 1 1 g45n2svt L=6e-07 W=4e-07 AD=8e-14 AS=8e-14 PD=1.2e
     -06 PS=1.2e-06 fw=4e-07 sa=2e-06 sb=2e-06 sca=2.67857 scb
     =4.09292e-05 scc=9.01501e-10 $X=11200 $Y=0 $dt=4
```

```
154 M8 1 1 1 1 g45n2svt L=6e-07 W=4e-07 AD=8e-14 AS=8e-14 PD=1.2e
    -06 PS=1.2e-06 fw=4e-07 sa=2e-06 sb=2e-06 sca=2.67857 scb
    =4.09292e-05 scc=9.01501e-10 $X=12800 $Y=0 $dt=4
155 M9 1 1 1 1 g45n2svt L=6e-07 W=4e-07 AD=8e-14 AS=8e-14 PD=1.2e
    -06 PS=1.2e-06 fw=4e-07 sa=2e-06 sb=2e-06 sca=2.67857 scb
    =4.09292e-05 scc=9.01501e-10 $X=14400 $Y=0 $dt=4
156 M10 1 1 1 1 g45n2svt L=6e-07 W=4e-07 AD=8e-14 AS=8e-14 PD=1.2e
    -06 PS=1.2e-06 fw=4e-07 sa=2e-06 sb=2e-06 sca=2.67857 scb
    =4.09292e-05 scc=9.01501e-10 $X=16000 $Y=0 $dt=4
157 M11 1 1 1 1 g45n2svt L=6e-07 W=4e-07 AD=8e-14 AS=8e-14 PD=1.2e
    -06 PS=1.2e-06 fw=4e-07 sa=2e-06 sb=2e-06 sca=2.67857 scb
    =4.09292e-05 scc=9.01501e-10 $X=17600 $Y=0 $dt=4
158 M12 1 1 1 1 g45n2svt L=6e-07 W=4e-07 AD=8e-14 AS=8e-14 PD=1.2e
    -06 PS=1.2e-06 fw=4e-07 sa=2e-06 sb=2e-06 sca=2.67857 scb
    =4.09292e-05 scc=9.01501e-10 $X=19200 $Y=0 $dt=4
159 M13 1 1 1 1 g45n2svt L=6e-07 W=4e-07 AD=8e-14 AS=8e-14 PD=1.2e
    -06 PS=1.2e-06 fw=4e-07 sa=2e-06 sb=2e-06 sca=2.67857 scb
    =4.09292e-05 scc=9.01501e-10 $X=20800 $Y=0 $dt=4
160 M14 1 1 1 1 g45n2svt L=6e-07 W=4e-07 AD=8e-14 AS=8e-14 PD=1.2e
    -06 PS=1.2e-06 fw=4e-07 sa=2e-06 sb=2e-06 sca=2.67857 scb
    =4.09292e-05 scc=9.01501e-10 $X=22400 $Y=0 $dt=4
161 M15 1 1 1 1 g45n2svt L=6e-07 W=4e-07 AD=8e-14 AS=8e-14 PD=1.2e
    -06 PS=1.2e-06 fw=4e-07 sa=2e-06 sb=2e-06 sca=2.67857 scb
    =4.09292e-05 scc=9.01501e-10 $X=24000 $Y=0 $dt=4
162 .ends nmos2v$$24
```

```
163
164 * ++++++++++++++++++++++++++++++++++++++++++++++++++++++++ *
165 * Sub cell: pmos2v$$25                                      *
166 * ++++++++++++++++++++++++++++++++++++++++++++++++++++++++ *
167 .subckt pmos2v$$25 2 3 4
168 ** N=5 EP=3 FDC=6
169 M0 4 2 3 4 g45p2svt L=6e-07 W=4e-07 AD=8e-14 AS=8e-14 PD=1.2e
    -06 PS=1.2e-06 fw=4e-07 sa=2e-06 sb=2e-06 sca=2.67857 scb
    =4.09292e-05 scc=9.01501e-10 $X=0 $Y=0 $dt=11
170 M1 3 2 4 4 g45p2svt L=6e-07 W=4e-07 AD=8e-14 AS=8e-14 PD=1.2e
    -06 PS=1.2e-06 fw=4e-07 sa=2e-06 sb=2e-06 sca=2.67857 scb
    =4.09292e-05 scc=9.01501e-10 $X=1600 $Y=0 $dt=11
171 M2 4 2 3 4 g45p2svt L=6e-07 W=4e-07 AD=8e-14 AS=8e-14 PD=1.2e
    -06 PS=1.2e-06 fw=4e-07 sa=2e-06 sb=2e-06 sca=2.67857 scb
    =4.09292e-05 scc=9.01501e-10 $X=3200 $Y=0 $dt=11
172 M3 3 2 4 4 g45p2svt L=6e-07 W=4e-07 AD=8e-14 AS=8e-14 PD=1.2e
    -06 PS=1.2e-06 fw=4e-07 sa=2e-06 sb=1.75e-06 sca=2.67857
    scb=4.09292e-05 scc=9.01501e-10 $X=4800 $Y=0 $dt=11
173 M4 4 2 3 4 g45p2svt L=6e-07 W=4e-07 AD=8e-14 AS=8e-14 PD=1.2e
    -06 PS=1.2e-06 fw=4e-07 sa=2e-06 sb=9.5e-07 sca=2.67857 scb
    =4.09292e-05 scc=9.01501e-10 $X=6400 $Y=0 $dt=11
174 M5 3 2 4 4 g45p2svt L=6e-07 W=4e-07 AD=6e-14 AS=8e-14 PD=1.1e
    -06 PS=1.2e-06 fw=4e-07 sa=2e-06 sb=1.5e-07 sca=2.98259 scb
    =9.24817e-05 scc=1.23329e-08 $X=8000 $Y=0 $dt=11
175 .ends pmos2v$$25
```

```
176
177 * ++++++++++++++++++++++++++++++++++++++++++++++++++++++++ *
178 * Sub cell: pmos2v$$27                                      *
179 * ++++++++++++++++++++++++++++++++++++++++++++++++++++++++ *
180 .subckt pmos2v$$27 1 2 3
181 ** N=4 EP=3 FDC=6
182 M0 1 2 3 1 g45p2svt L=6e-07 W=4e-07 AD=8e-14 AS=8e-14 PD=1.2e
    -06 PS=1.2e-06 fw=4e-07 sa=2e-06 sb=2e-06 sca=2.67857 scb
    =4.09292e-05 scc=9.01501e-10 $X=0 $Y=0 $dt=11
183 M1 3 2 1 1 g45p2svt L=6e-07 W=4e-07 AD=8e-14 AS=8e-14 PD=1.2e
    -06 PS=1.2e-06 fw=4e-07 sa=2e-06 sb=2e-06 sca=2.67857 scb
    =4.09292e-05 scc=9.01501e-10 $X=1600 $Y=0 $dt=11
184 M2 1 2 3 1 g45p2svt L=6e-07 W=4e-07 AD=8e-14 AS=8e-14 PD=1.2e
    -06 PS=1.2e-06 fw=4e-07 sa=2e-06 sb=2e-06 sca=2.67857 scb
    =4.09292e-05 scc=9.01501e-10 $X=3200 $Y=0 $dt=11
185 M3 3 2 1 1 g45p2svt L=6e-07 W=4e-07 AD=8e-14 AS=8e-14 PD=1.2e
    -06 PS=1.2e-06 fw=4e-07 sa=2e-06 sb=2e-06 sca=2.67857 scb
    =4.09292e-05 scc=9.01501e-10 $X=4800 $Y=0 $dt=11
186 M4 1 2 3 1 g45p2svt L=6e-07 W=4e-07 AD=8e-14 AS=8e-14 PD=1.2e
    -06 PS=1.2e-06 fw=4e-07 sa=2e-06 sb=2e-06 sca=2.67857 scb
    =4.09292e-05 scc=9.01501e-10 $X=6400 $Y=0 $dt=11
187 M5 3 2 1 1 g45p2svt L=6e-07 W=4e-07 AD=8e-14 AS=8e-14 PD=1.2e
    -06 PS=1.2e-06 fw=4e-07 sa=2e-06 sb=2e-06 sca=2.67857 scb
    =4.09292e-05 scc=9.01501e-10 $X=8000 $Y=0 $dt=11
188 .ends pmos2v$$27
```

```
189
190 * ++++++++++++++++++++++++++++++++++++++++++++++++++++++++ *
191 * Sub cell: pmos2v$$28                                      *
192 * ++++++++++++++++++++++++++++++++++++++++++++++++++++++++ *
193 .subckt pmos2v$$28 2 3
194 ** N=4 EP=2 FDC=6
195 M0 2 3 3 2 g45p2svt L=6e-07 W=4e-07 AD=8e-14 AS=8e-14 PD=1.2e
    -06 PS=1.2e-06 fw=4e-07 sa=2e-06 sb=2e-06 sca=2.67857 scb
    =4.09292e-05 scc=9.01501e-10 $X=0 $Y=0 $dt=11
196 M1 3 3 2 2 g45p2svt L=6e-07 W=4e-07 AD=8e-14 AS=8e-14 PD=1.2e
    -06 PS=1.2e-06 fw=4e-07 sa=2e-06 sb=2e-06 sca=2.67857 scb
    =4.09292e-05 scc=9.01501e-10 $X=1600 $Y=0 $dt=11
197 M2 2 3 3 2 g45p2svt L=6e-07 W=4e-07 AD=8e-14 AS=8e-14 PD=1.2e
    -06 PS=1.2e-06 fw=4e-07 sa=2e-06 sb=2e-06 sca=2.67857 scb
    =4.09292e-05 scc=9.01501e-10 $X=3200 $Y=0 $dt=11
198 M3 3 3 2 2 g45p2svt L=6e-07 W=4e-07 AD=8e-14 AS=8e-14 PD=1.2e
    -06 PS=1.2e-06 fw=4e-07 sa=2e-06 sb=2e-06 sca=2.67857 scb
    =4.09292e-05 scc=9.01501e-10 $X=4800 $Y=0 $dt=11
199 M4 2 3 3 2 g45p2svt L=6e-07 W=4e-07 AD=8e-14 AS=8e-14 PD=1.2e
    -06 PS=1.2e-06 fw=4e-07 sa=2e-06 sb=2e-06 sca=2.67857 scb
    =4.09292e-05 scc=9.01501e-10 $X=6400 $Y=0 $dt=11
200 M5 3 3 2 2 g45p2svt L=6e-07 W=4e-07 AD=8e-14 AS=8e-14 PD=1.2e
    -06 PS=1.2e-06 fw=4e-07 sa=2e-06 sb=2e-06 sca=2.67857 scb
    =4.09292e-05 scc=9.01501e-10 $X=8000 $Y=0 $dt=11
201 .ends pmos2v$$28
```

```
202
203 * ++++++++++++++++++++++++++++++++++++++++++++++++++++++++ *
204 * Sub cell: pmos2v$$29                                      *
205 * ++++++++++++++++++++++++++++++++++++++++++++++++++++++++ *
206 .subckt pmos2v$$29 2
207 ** N=17 EP=1 FDC=14
208 M0 2 2 2 2 g45p2svt L=6e-07 W=4e-07 AD=8e-14 AS=6e-14 PD=1.2e
    -06 PS=1.1e-06 fw=4e-07 sa=1.5e-07 sb=2e-06 sca=8.79766 scb
    =0.00748949 scc=0.000298105 $X=0 $Y=0 $dt=11
209 M1 2 2 2 2 g45p2svt L=6e-07 W=4e-07 AD=8e-14 AS=8e-14 PD=1.2e
    -06 PS=1.2e-06 fw=4e-07 sa=9.5e-07 sb=2e-06 sca=8.4747 scb
    =0.00743239 scc=0.000298091 $X=1600 $Y=0 $dt=11
210 M2 2 2 2 2 g45p2svt L=6e-07 W=4e-07 AD=8e-14 AS=8e-14 PD=1.2e
    -06 PS=1.2e-06 fw=4e-07 sa=1.75e-06 sb=2e-06 sca=8.4747 scb
    =0.00743239 scc=0.000298091 $X=3200 $Y=0 $dt=11
211 M3 2 2 2 2 g45p2svt L=6e-07 W=4e-07 AD=8e-14 AS=8e-14 PD=1.2e
    -06 PS=1.2e-06 fw=4e-07 sa=2e-06 sb=2e-06 sca=8.4747 scb
    =0.00743239 scc=0.000298091 $X=4800 $Y=0 $dt=11
212 M4 2 2 2 2 g45p2svt L=6e-07 W=4e-07 AD=8e-14 AS=8e-14 PD=1.2e
    -06 PS=1.2e-06 fw=4e-07 sa=2e-06 sb=2e-06 sca=8.4747 scb
    =0.00743239 scc=0.000298091 $X=6400 $Y=0 $dt=11
213 M5 2 2 2 2 g45p2svt L=6e-07 W=4e-07 AD=8e-14 AS=8e-14 PD=1.2e
    -06 PS=1.2e-06 fw=4e-07 sa=2e-06 sb=2e-06 sca=8.4747 scb
    =0.00743239 scc=0.000298091 $X=8000 $Y=0 $dt=11
```

```
214 M6 2 2 2 2 g45p2svt L=6e-07 W=4e-07 AD=8e-14 AS=8e-14 PD=1.2e
    -06 PS=1.2e-06 fw=4e-07 sa=2e-06 sb=2e-06 sca=8.4747 scb
    =0.00743239 scc=0.000298091 $X=9600 $Y=0 $dt=11
215 M7 2 2 2 2 g45p2svt L=6e-07 W=4e-07 AD=8e-14 AS=8e-14 PD=1.2e
    -06 PS=1.2e-06 fw=4e-07 sa=2e-06 sb=2e-06 sca=8.4747 scb
    =0.00743239 scc=0.000298091 $X=11200 $Y=0 $dt=11
216 M8 2 2 2 2 g45p2svt L=6e-07 W=4e-07 AD=8e-14 AS=8e-14 PD=1.2e
    -06 PS=1.2e-06 fw=4e-07 sa=2e-06 sb=2e-06 sca=8.4747 scb
    =0.00743239 scc=0.000298091 $X=12800 $Y=0 $dt=11
217 M9 2 2 2 2 g45p2svt L=6e-07 W=4e-07 AD=8e-14 AS=8e-14 PD=1.2e
    -06 PS=1.2e-06 fw=4e-07 sa=2e-06 sb=2e-06 sca=8.4747 scb
    =0.00743239 scc=0.000298091 $X=14400 $Y=0 $dt=11
218 M10 2 2 2 2 g45p2svt L=6e-07 W=4e-07 AD=8e-14 AS=8e-14 PD=1.2e
    -06 PS=1.2e-06 fw=4e-07 sa=2e-06 sb=2e-06 sca=8.4747 scb
    =0.00743239 scc=0.000298091 $X=16000 $Y=0 $dt=11
219 M11 2 2 2 2 g45p2svt L=6e-07 W=4e-07 AD=8e-14 AS=8e-14 PD=1.2e
    -06 PS=1.2e-06 fw=4e-07 sa=2e-06 sb=2e-06 sca=8.4747 scb
    =0.00743239 scc=0.000298091 $X=17600 $Y=0 $dt=11
220 M12 2 2 2 2 g45p2svt L=6e-07 W=4e-07 AD=8e-14 AS=8e-14 PD=1.2e
    -06 PS=1.2e-06 fw=4e-07 sa=2e-06 sb=2e-06 sca=8.4747 scb
    =0.00743239 scc=0.000298091 $X=19200 $Y=0 $dt=11
221 M13 2 2 2 2 g45p2svt L=6e-07 W=4e-07 AD=8e-14 AS=8e-14 PD=1.2e
    -06 PS=1.2e-06 fw=4e-07 sa=2e-06 sb=2e-06 sca=8.4747 scb
    =0.00743239 scc=0.000298091 $X=20800 $Y=0 $dt=11
222 .ends pmos2v$$29
```

```
223
224 * ++++++++++++++++++++++++++++++++++++++++++++++++++++++++ *
225 * Sub cell: pmos2v$$30                                      *
226 * ++++++++++++++++++++++++++++++++++++++++++++++++++++++++ *
227 .subckt pmos2v$$30 2
228 ** N=7 EP=1 FDC=4
229 M0 2 2 2 2 g45p2svt L=6e-07 W=4e-07 AD=8e-14 AS=8e-14 PD=1.2e
    -06 PS=1.2e-06 fw=4e-07 sa=2e-06 sb=2e-06 sca=2.67857 scb
    =4.09292e-05 scc=9.01501e-10 $X=0 $Y=0 $dt=11
230 M1 2 2 2 2 g45p2svt L=6e-07 W=4e-07 AD=8e-14 AS=8e-14 PD=1.2e
    -06 PS=1.2e-06 fw=4e-07 sa=2e-06 sb=1.75e-06 sca=2.67857
    scb=4.09292e-05 scc=9.01501e-10 $X=1600 $Y=0 $dt=11
231 M2 2 2 2 2 g45p2svt L=6e-07 W=4e-07 AD=8e-14 AS=8e-14 PD=1.2e
    -06 PS=1.2e-06 fw=4e-07 sa=2e-06 sb=9.5e-07 sca=2.67857 scb
    =4.09292e-05 scc=9.01501e-10 $X=3200 $Y=0 $dt=11
232 M3 2 2 2 2 g45p2svt L=6e-07 W=4e-07 AD=6e-14 AS=8e-14 PD=1.1e
    -06 PS=1.2e-06 fw=4e-07 sa=2e-06 sb=1.5e-07 sca=3.00153 scb
    =9.80227e-05 scc=1.47329e-08 $X=4800 $Y=0 $dt=11
233 .ends pmos2v$$30
234
235 * ++++++++++++++++++++++++++++++++++++++++++++++++++++++++ *
236 * Sub cell: nmos2v$$31                                      *
237 * ++++++++++++++++++++++++++++++++++++++++++++++++++++++++ *
238 .subckt nmos2v$$31 1 2 3
239 ** N=3 EP=3 FDC=4
```

```
240 M0 3 1 2 3 g45n2svt L=6e-07 W=4e-07 AD=8e-14 AS=8e-14 PD=1.2e
    -06 PS=1.2e-06 fw=4e-07 sa=2e-06 sb=2e-06 sca=5.61926 scb
    =0.00306339 scc=3.82378e-05 $X=0 $Y=0 $dt=4
241 M1 2 1 3 3 g45n2svt L=6e-07 W=4e-07 AD=8e-14 AS=8e-14 PD=1.2e
    -06 PS=1.2e-06 fw=4e-07 sa=2e-06 sb=2e-06 sca=5.61926 scb
    =0.00306339 scc=3.82378e-05 $X=1600 $Y=0 $dt=4
242 M2 3 1 2 3 g45n2svt L=6e-07 W=4e-07 AD=8e-14 AS=8e-14 PD=1.2e
    -06 PS=1.2e-06 fw=4e-07 sa=2e-06 sb=2e-06 sca=5.61926 scb
    =0.00306339 scc=3.82378e-05 $X=3200 $Y=0 $dt=4
243 M3 2 1 3 3 g45n2svt L=6e-07 W=4e-07 AD=8e-14 AS=8e-14 PD=1.2e
    -06 PS=1.2e-06 fw=4e-07 sa=2e-06 sb=2e-06 sca=5.61926 scb
    =0.00306339 scc=3.82378e-05 $X=4800 $Y=0 $dt=4
244 .ends nmos2v$$31
245
246 * ++++++++++++++++++++++++++++++++++++++++++++++++++++++++ *
247 * Sub cell: nmos2v$$32                                     *
248 * ++++++++++++++++++++++++++++++++++++++++++++++++++++++++ *
249 .subckt nmos2v$$32 1
250 ** N=7 EP=1 FDC=6
251 M0 1 1 1 1 g45n2svt L=6e-07 W=4e-07 AD=8e-14 AS=6e-14 PD=1.2e
    -06 PS=1.1e-06 fw=4e-07 sa=1.5e-07 sb=2e-06 sca=5.61926 scb
    =0.00306339 scc=3.82378e-05 $X=0 $Y=0 $dt=4
252 M1 1 1 1 1 g45n2svt L=6e-07 W=4e-07 AD=8e-14 AS=8e-14 PD=1.2e
    -06 PS=1.2e-06 fw=4e-07 sa=9.5e-07 sb=2e-06 sca=5.61926 scb
    =0.00306339 scc=3.82378e-05 $X=1600 $Y=0 $dt=4
```

```
253 M2 1 1 1 1 g45n2svt L=6e-07 W=4e-07 AD=8e-14 AS=8e-14 PD=1.2e
    -06 PS=1.2e-06 fw=4e-07 sa=1.75e-06 sb=2e-06 sca=5.61926
    scb=0.00306339 scc=3.82378e-05 $X=3200 $Y=0 $dt=4
254 M3 1 1 1 1 g45n2svt L=6e-07 W=4e-07 AD=8e-14 AS=8e-14 PD=1.2e
    -06 PS=1.2e-06 fw=4e-07 sa=2e-06 sb=2e-06 sca=5.61926 scb
    =0.00306339 scc=3.82378e-05 $X=4800 $Y=0 $dt=4
255 M4 1 1 1 1 g45n2svt L=6e-07 W=4e-07 AD=8e-14 AS=8e-14 PD=1.2e
    -06 PS=1.2e-06 fw=4e-07 sa=2e-06 sb=2e-06 sca=5.61926 scb
    =0.00306339 scc=3.82378e-05 $X=6400 $Y=0 $dt=4
256 M5 1 1 1 1 g45n2svt L=6e-07 W=4e-07 AD=8e-14 AS=8e-14 PD=1.2e
    -06 PS=1.2e-06 fw=4e-07 sa=2e-06 sb=2e-06 sca=5.61926 scb
    =0.00306339 scc=3.82378e-05 $X=8000 $Y=0 $dt=4
257 .ends nmos2v$$32
258
259 * ++++++++++++++++++++++++++++++++++++++++++++++++++++++++ *
260 * Sub cell: nmos2v$$33                                     *
261 * ++++++++++++++++++++++++++++++++++++++++++++++++++++++++ *
262 .subckt nmos2v$$33 1
263 ** N=7 EP=1 FDC=6
264 M0 1 1 1 1 g45n2svt L=6e-07 W=4e-07 AD=8e-14 AS=8e-14 PD=1.2e
    -06 PS=1.2e-06 fw=4e-07 sa=2e-06 sb=2e-06 sca=5.61926 scb
    =0.00306339 scc=3.82378e-05 $X=0 $Y=0 $dt=4
265 M1 1 1 1 1 g45n2svt L=6e-07 W=4e-07 AD=8e-14 AS=8e-14 PD=1.2e
    -06 PS=1.2e-06 fw=4e-07 sa=2e-06 sb=2e-06 sca=5.61926 scb
    =0.00306339 scc=3.82378e-05 $X=1600 $Y=0 $dt=4
```

```
266 M2 1 1 1 1 g45n2svt L=6e-07 W=4e-07 AD=8e-14 AS=8e-14 PD=1.2e
    -06 PS=1.2e-06 fw=4e-07 sa=2e-06 sb=2e-06 sca=5.61926 scb
    =0.00306339 scc=3.82378e-05 $X=3200 $Y=0 $dt=4
267 M3 1 1 1 1 g45n2svt L=6e-07 W=4e-07 AD=8e-14 AS=8e-14 PD=1.2e
    -06 PS=1.2e-06 fw=4e-07 sa=2e-06 sb=1.75e-06 sca=5.61926
    scb=0.00306339 scc=3.82378e-05 $X=4800 $Y=0 $dt=4
268 M4 1 1 1 1 g45n2svt L=6e-07 W=4e-07 AD=8e-14 AS=8e-14 PD=1.2e
    -06 PS=1.2e-06 fw=4e-07 sa=2e-06 sb=9.5e-07 sca=5.61926 scb
    =0.00306339 scc=3.82378e-05 $X=6400 $Y=0 $dt=4
269 M5 1 1 1 1 g45n2svt L=6e-07 W=4e-07 AD=6e-14 AS=8e-14 PD=1.1e
    -06 PS=1.2e-06 fw=4e-07 sa=2e-06 sb=1.5e-07 sca=5.61926 scb
    =0.00306339 scc=3.82378e-05 $X=8000 $Y=0 $dt=4
270 .ends nmos2v$$33
271
272 * ++++++++++++++++++++++++++++++++++++++++++++++++++++++++ *
273 * Sub cell: nmos2v$$34                                     *
274 * ++++++++++++++++++++++++++++++++++++++++++++++++++++++++ *
275 .subckt nmos2v$$34 1
276 ** N=13 EP=1 FDC=12
277 M0 1 1 1 1 g45n2svt L=6e-07 W=4e-07 AD=8e-14 AS=6e-14 PD=1.2e
    -06 PS=1.1e-06 fw=4e-07 sa=1.5e-07 sb=2e-06 sca=2.67857 scb
    =4.09292e-05 scc=9.01501e-10 $X=0 $Y=0 $dt=4
278 M1 1 1 1 1 g45n2svt L=6e-07 W=4e-07 AD=8e-14 AS=8e-14 PD=1.2e
    -06 PS=1.2e-06 fw=4e-07 sa=9.5e-07 sb=2e-06 sca=2.67857 scb
    =4.09292e-05 scc=9.01501e-10 $X=1600 $Y=0 $dt=4
```

```
279 M2 1 1 1 1 g45n2svt L=6e-07 W=4e-07 AD=8e-14 AS=8e-14 PD=1.2e
    -06 PS=1.2e-06 fw=4e-07 sa=1.75e-06 sb=2e-06 sca=2.67857
    scb=4.09292e-05 scc=9.01501e-10 $X=3200 $Y=0 $dt=4
280 M3 1 1 1 1 g45n2svt L=6e-07 W=4e-07 AD=8e-14 AS=8e-14 PD=1.2e
    -06 PS=1.2e-06 fw=4e-07 sa=2e-06 sb=2e-06 sca=2.67857 scb
    =4.09292e-05 scc=9.01501e-10 $X=4800 $Y=0 $dt=4
281 M4 1 1 1 1 g45n2svt L=6e-07 W=4e-07 AD=8e-14 AS=8e-14 PD=1.2e
    -06 PS=1.2e-06 fw=4e-07 sa=2e-06 sb=2e-06 sca=2.67857 scb
    =4.09292e-05 scc=9.01501e-10 $X=6400 $Y=0 $dt=4
282 M5 1 1 1 1 g45n2svt L=6e-07 W=4e-07 AD=8e-14 AS=8e-14 PD=1.2e
    -06 PS=1.2e-06 fw=4e-07 sa=2e-06 sb=2e-06 sca=2.67857 scb
    =4.09292e-05 scc=9.01501e-10 $X=8000 $Y=0 $dt=4
283 M6 1 1 1 1 g45n2svt L=6e-07 W=4e-07 AD=8e-14 AS=8e-14 PD=1.2e
    -06 PS=1.2e-06 fw=4e-07 sa=2e-06 sb=2e-06 sca=2.67857 scb
    =4.09292e-05 scc=9.01501e-10 $X=9600 $Y=0 $dt=4
284 M7 1 1 1 1 g45n2svt L=6e-07 W=4e-07 AD=8e-14 AS=8e-14 PD=1.2e
    -06 PS=1.2e-06 fw=4e-07 sa=2e-06 sb=2e-06 sca=2.67857 scb
    =4.09292e-05 scc=9.01501e-10 $X=11200 $Y=0 $dt=4
285 M8 1 1 1 1 g45n2svt L=6e-07 W=4e-07 AD=8e-14 AS=8e-14 PD=1.2e
    -06 PS=1.2e-06 fw=4e-07 sa=2e-06 sb=2e-06 sca=2.67857 scb
    =4.09292e-05 scc=9.01501e-10 $X=12800 $Y=0 $dt=4
286 M9 1 1 1 1 g45n2svt L=6e-07 W=4e-07 AD=8e-14 AS=8e-14 PD=1.2e
    -06 PS=1.2e-06 fw=4e-07 sa=2e-06 sb=2e-06 sca=2.67857 scb
    =4.09292e-05 scc=9.01501e-10 $X=14400 $Y=0 $dt=4
```

```
287 M10 1 1 1 1 g45n2svt L=6e-07 W=4e-07 AD=8e-14 AS=8e-14 PD=1.2e
    -06 PS=1.2e-06 fw=4e-07 sa=2e-06 sb=2e-06 sca=2.67857 scb
    =4.09292e-05 scc=9.01501e-10 $X=16000 $Y=0 $dt=4
288 M11 1 1 1 1 g45n2svt L=6e-07 W=4e-07 AD=8e-14 AS=8e-14 PD=1.2e
    -06 PS=1.2e-06 fw=4e-07 sa=2e-06 sb=2e-06 sca=2.67857 scb
    =4.09292e-05 scc=9.01501e-10 $X=17600 $Y=0 $dt=4
289 .ends nmos2v$$34
290
291 * ++++++++++++++++++++++++++++++++++++++++++++++++++++++++ *
292 * Sub cell: nmos2v$$35                                     *
293 * ++++++++++++++++++++++++++++++++++++++++++++++++++++++++ *
294 .subckt nmos2v$$35 1 2 3
295 ** N=3 EP=3 FDC=4
296 M0 1 2 3 1 g45n2svt L=6e-07 W=4e-07 AD=8e-14 AS=8e-14 PD=1.2e
    -06 PS=1.2e-06 fw=4e-07 sa=2e-06 sb=2e-06 sca=2.67857 scb
    =4.09292e-05 scc=9.01501e-10 $X=0 $Y=0 $dt=4
297 M1 3 2 1 1 g45n2svt L=6e-07 W=4e-07 AD=8e-14 AS=8e-14 PD=1.2e
    -06 PS=1.2e-06 fw=4e-07 sa=2e-06 sb=1.75e-06 sca=2.67857
    scb=4.09292e-05 scc=9.01501e-10 $X=1600 $Y=0 $dt=4
298 M2 1 2 3 1 g45n2svt L=6e-07 W=4e-07 AD=8e-14 AS=8e-14 PD=1.2e
    -06 PS=1.2e-06 fw=4e-07 sa=2e-06 sb=9.5e-07 sca=2.67857 scb
    =4.09292e-05 scc=9.01501e-10 $X=3200 $Y=0 $dt=4
299 M3 3 2 1 1 g45n2svt L=6e-07 W=4e-07 AD=6e-14 AS=8e-14 PD=1.1e
    -06 PS=1.2e-06 fw=4e-07 sa=2e-06 sb=1.5e-07 sca=2.67857 scb
    =4.09292e-05 scc=9.01501e-10 $X=4800 $Y=0 $dt=4
```

```
.ends nmos2v$$35

* ++++++++++++++++++++++++++++++++++++++++++++++++++++++++ *
* Sub cell: mimcap$$36                                     *
* ++++++++++++++++++++++++++++++++++++++++++++++++++++++++ *
.subckt mimcap$$36 1 2 3
** N=3 EP=3 FDC=1
C0 1 2 2.24003e-21 L=5.6e-06 W=5.6e-06 area=3.136e-11 pj=2.24e
    -05 $[g45cmim] $SUB=3 $X=0 $Y=0 $dt=55
.ends mimcap$$36

* ++++++++++++++++++++++++++++++++++++++++++++++++++++++++ *
* Sub cell: DS_VGA_OPAMP                                   *
* ++++++++++++++++++++++++++++++++++++++++++++++++++++++++ *
.subckt DS_VGA_OPAMP IREF VDD VINM VINP VOUT VSS
** N=11 EP=6 FDC=187
X168 VDD pmos2v$$19 $T=4470 10480 0 0 $X=3690 $Y=10000
X169 3 10 VINP VDD pmos2v$$20 $T=20490 5400 0 0 $X=19750 $Y
    =4920
X170 VDD pmos2v$$21 $T=4490 7160 0 0 $X=3710 $Y=6680
X171 VDD 8 VOUT pmos2v$$22 $T=26870 12240 0 0 $X=26130 $Y
    =11760
X172 11 8 VSS nmos2v$$23 $T=30070 1880 0 0 $X=29570 $Y=1520
X173 VSS nmos2v$$24 $T=4470 360 0 0 $X=3810 $Y=0
X174 6 8 VDD pmos2v$$25 $T=26870 10480 0 0 $X=26250 $Y=10000
```

```
322 X177 VDD 6 6 pmos2v$$27 $T=17270 10480 0 0 $X=16530 $Y=10000
323 X178 VDD IREF 10 pmos2v$$27 $T=20490 7160 0 0 $X=19750 $Y=6680
324 X179 VDD IREF 10 pmos2v$$27 $T=20490 8840 0 0 $X=19750 $Y=8360
325 X180 VDD IREF pmos2v$$28 $T=10890 7160 0 0 $X=10150 $Y=6680
326 X181 VDD pmos2v$$29 $T=4470 12240 0 0 $X=3690 $Y=11760
327 X182 VDD pmos2v$$30 $T=30090 7160 0 0 $X=29470 $Y=6680
328 X183 VDD pmos2v$$30 $T=30090 8840 0 0 $X=29470 $Y=8360
329 X184 11 3 VSS nmos2v$$31 $T=20470 3400 0 0 $X=19970 $Y=3040
330 X185 VSS nmos2v$$32 $T=4470 3400 0 0 $X=3810 $Y=3040
331 X186 VSS nmos2v$$33 $T=26870 3400 0 0 $X=26370 $Y=3040
332 X187 VSS nmos2v$$34 $T=4470 1880 0 0 $X=3810 $Y=1520
333 X188 VSS 3 VOUT nmos2v$$35 $T=30070 360 0 0 $X=29450 $Y=0
334 X189 3 VOUT VSS mimcap$$36 $T=400 16970 0 0 $X=0 $Y=16570
335 X190 3 VOUT VSS mimcap$$36 $T=400 31470 0 0 $X=0 $Y=31070
336 X191 3 VOUT VSS mimcap$$36 $T=400 45970 0 0 $X=0 $Y=45570
337 X192 3 VOUT VSS mimcap$$36 $T=400 60470 0 0 $X=0 $Y=60070
338 X193 3 VOUT VSS mimcap$$36 $T=400 74970 0 0 $X=0 $Y=74570
339 X194 3 VOUT VSS mimcap$$36 $T=400 89470 0 0 $X=0 $Y=89070
340 X195 3 VOUT VSS mimcap$$36 $T=400 103970 0 0 $X=0 $Y=103570
341 X196 3 VOUT VSS mimcap$$36 $T=400 118470 0 0 $X=0 $Y=118070
342 X197 3 VOUT VSS mimcap$$36 $T=400 132970 0 0 $X=0 $Y=132570
343 X198 3 VOUT VSS mimcap$$36 $T=14900 16970 0 0 $X=14500 $Y
    =16570
344 X199 3 VOUT VSS mimcap$$36 $T=14900 31470 0 0 $X=14500 $Y
    =31070
```

```
345 X200 3 VOUT VSS mimcap$$36 $T=14900 45970 0 0 $X=14500 $Y
    =45570
346 X201 3 VOUT VSS mimcap$$36 $T=14900 60470 0 0 $X=14500 $Y
    =60070
347 X202 3 VOUT VSS mimcap$$36 $T=14900 74970 0 0 $X=14500 $Y
    =74570
348 X203 3 VOUT VSS mimcap$$36 $T=14900 89470 0 0 $X=14500 $Y
    =89070
349 X204 3 VOUT VSS mimcap$$36 $T=14900 103970 0 0 $X=14500 $Y
    =103570
350 X205 3 VOUT VSS mimcap$$36 $T=14900 118470 0 0 $X=14500 $Y
    =118070
351 X206 3 VOUT VSS mimcap$$36 $T=14900 132970 0 0 $X=14500 $Y
    =132570
352 X207 3 VOUT VSS mimcap$$36 $T=29400 16970 0 0 $X=29000 $Y
    =16570
353 X208 3 VOUT VSS mimcap$$36 $T=29400 31470 0 0 $X=29000 $Y
    =31070
354 X209 3 VOUT VSS mimcap$$36 $T=29400 45970 0 0 $X=29000 $Y
    =45570
355 X210 3 VOUT VSS mimcap$$36 $T=29400 60470 0 0 $X=29000 $Y
    =60070
356 X211 3 VOUT VSS mimcap$$36 $T=29400 74970 0 0 $X=29000 $Y
    =74570
```

```
357 X212 3 VOUT VSS mimcap$$36 $T=29400 89470 0 0 $X=29000 $Y
    =89070
358 X213 3 VOUT VSS mimcap$$36 $T=29400 103970 0 0 $X=29000 $Y
    =103570
359 X214 3 VOUT VSS mimcap$$36 $T=29400 118470 0 0 $X=29000 $Y
    =118070
360 X215 3 VOUT VSS mimcap$$36 $T=29400 132970 0 0 $X=29000 $Y
    =132570
361 M0 11 11 VSS VSS g45n2svt L=6e-07 W=4e-07 AD=8e-14 AS=8e-14 PD
    =1.2e-06 PS=1.2e-06 fw=4e-07 sa=2e-06 sb=2e-06 sca=5.61926
    scb=0.00306339 scc=3.82378e-05 $X=14070 $Y=3400 $dt=4
362 M1 VSS 11 11 VSS g45n2svt L=6e-07 W=4e-07 AD=8e-14 AS=8e-14 PD
    =1.2e-06 PS=1.2e-06 fw=4e-07 sa=2e-06 sb=2e-06 sca=5.61926
    scb=0.00306339 scc=3.82378e-05 $X=15670 $Y=3400 $dt=4
363 M2 11 11 VSS VSS g45n2svt L=6e-07 W=4e-07 AD=8e-14 AS=8e-14 PD
    =1.2e-06 PS=1.2e-06 fw=4e-07 sa=2e-06 sb=2e-06 sca=5.61926
    scb=0.00306339 scc=3.82378e-05 $X=17270 $Y=3400 $dt=4
364 M3 VSS 11 11 VSS g45n2svt L=6e-07 W=4e-07 AD=8e-14 AS=8e-14 PD
    =1.2e-06 PS=1.2e-06 fw=4e-07 sa=2e-06 sb=2e-06 sca=5.61926
    scb=0.00306339 scc=3.82378e-05 $X=18870 $Y=3400 $dt=4
365 M4 6 3 VSS VSS g45n2svt L=6e-07 W=4e-07 AD=8e-14 AS=8e-14 PD
    =1.2e-06 PS=1.2e-06 fw=4e-07 sa=2e-06 sb=2e-06 sca=2.67857
    scb=4.09292e-05 scc=9.01501e-10 $X=23670 $Y=1880 $dt=4
366 M5 VSS 3 6 VSS g45n2svt L=6e-07 W=4e-07 AD=8e-14 AS=8e-14 PD
    =1.2e-06 PS=1.2e-06 fw=4e-07 sa=2e-06 sb=2e-06 sca=2.67857
```

```
scb=4.09292e-05 scc=9.01501e-10 $X=25270 $Y=1880 $dt=4
367 M6 6 3 VSS VSS g45n2svt L=6e-07 W=4e-07 AD=8e-14 AS=8e-14 PD
=1.2e-06 PS=1.2e-06 fw=4e-07 sa=2e-06 sb=2e-06 sca=2.67857
scb=4.09292e-05 scc=9.01501e-10 $X=26870 $Y=1880 $dt=4
368 M7 VSS 3 6 VSS g45n2svt L=6e-07 W=4e-07 AD=8e-14 AS=8e-14 PD
=1.2e-06 PS=1.2e-06 fw=4e-07 sa=2e-06 sb=2e-06 sca=2.67857
scb=4.09292e-05 scc=9.01501e-10 $X=28470 $Y=1880 $dt=4
369 M8 11 VINM 10 VDD g45p2svt L=6e-07 W=4e-07 AD=8e-14 AS=6e-14
PD=1.2e-06 PS=1.1e-06 fw=4e-07 sa=1.5e-07 sb=2e-06 sca
=8.77873 scb=0.00748395 scc=0.000298102 $X=4490 $Y=5400 $dt
=11
370 M9 VDD VDD VDD VDD g45p2svt L=6e-07 W=4e-07 AD=8e-14 AS=6e-14
PD=1.2e-06 PS=1.1e-06 fw=4e-07 sa=1.5e-07 sb=2e-06 sca
=2.98259 scb=9.24817e-05 scc=1.23329e-08 $X=4490 $Y=8840
$dt=11
371 M10 10 VINM 11 VDD g45p2svt L=6e-07 W=4e-07 AD=8e-14 AS=8e-14
PD=1.2e-06 PS=1.2e-06 fw=4e-07 sa=9.5e-07 sb=2e-06 sca
=8.4747 scb=0.00743239 scc=0.000298091 $X=6090 $Y=5400 $dt
=11
372 M11 VDD VDD VDD VDD g45p2svt L=6e-07 W=4e-07 AD=8e-14 AS=8e-14
PD=1.2e-06 PS=1.2e-06 fw=4e-07 sa=9.5e-07 sb=2e-06 sca
=2.67857 scb=4.09292e-05 scc=9.01501e-10 $X=6090 $Y=8840
$dt=11
373 M12 11 VINM 10 VDD g45p2svt L=6e-07 W=4e-07 AD=8e-14 AS=8e-14
PD=1.2e-06 PS=1.2e-06 fw=4e-07 sa=1.75e-06 sb=2e-06 sca
```

```
=8.4747 scb=0.00743239 scc=0.000298091 $X=7690 $Y=5400 $dt
=11
374 M13 VDD VDD VDD VDD g45p2svt L=6e-07 W=4e-07 AD=8e-14 AS=8e-14
PD=1.2e-06 PS=1.2e-06 fw=4e-07 sa=1.75e-06 sb=2e-06 sca
=2.67857 scb=4.09292e-05 scc=9.01501e-10 $X=7690 $Y=8840
$dt=11
375 M14 10 VINM 11 VDD g45p2svt L=6e-07 W=4e-07 AD=8e-14 AS=8e-14
PD=1.2e-06 PS=1.2e-06 fw=4e-07 sa=2e-06 sb=2e-06 sca=8.4747
scb=0.00743239 scc=0.000298091 $X=9290 $Y=5400 $dt=11
376 M15 VDD VDD VDD VDD g45p2svt L=6e-07 W=4e-07 AD=8e-14 AS=8e-14
PD=1.2e-06 PS=1.2e-06 fw=4e-07 sa=2e-06 sb=2e-06 sca
=2.67857 scb=4.09292e-05 scc=9.01501e-10 $X=9290 $Y=8840
$dt=11
377 M16 11 VINM 10 VDD g45p2svt L=6e-07 W=4e-07 AD=8e-14 AS=8e-14
PD=1.2e-06 PS=1.2e-06 fw=4e-07 sa=2e-06 sb=2e-06 sca=8.4747
scb=0.00743239 scc=0.000298091 $X=10890 $Y=5400 $dt=11
378 M17 VDD VDD VDD VDD g45p2svt L=6e-07 W=4e-07 AD=8e-14 AS=8e-14
PD=1.2e-06 PS=1.2e-06 fw=4e-07 sa=2e-06 sb=2e-06 sca
=2.67857 scb=4.09292e-05 scc=9.01501e-10 $X=10890 $Y=8840
$dt=11
379 M18 10 VINM 11 VDD g45p2svt L=6e-07 W=4e-07 AD=8e-14 AS=8e-14
PD=1.2e-06 PS=1.2e-06 fw=4e-07 sa=2e-06 sb=2e-06 sca=8.4747
scb=0.00743239 scc=0.000298091 $X=12490 $Y=5400 $dt=11
380 M19 VDD VDD VDD VDD g45p2svt L=6e-07 W=4e-07 AD=8e-14 AS=8e-14
PD=1.2e-06 PS=1.2e-06 fw=4e-07 sa=2e-06 sb=2e-06 sca
```

```
=2.67857 scb=4.09292e-05 scc=9.01501e-10 $X=12490 $Y=8840
$dt=11
381 M20 11 VINM 10 VDD g45p2svt L=6e-07 W=4e-07 AD=8e-14 AS=8e-14
PD=1.2e-06 PS=1.2e-06 fw=4e-07 sa=2e-06 sb=2e-06 sca=8.4747
scb=0.00743239 scc=0.000298091 $X=14090 $Y=5400 $dt=11
382 M21 VDD VDD VDD VDD g45p2svt L=6e-07 W=4e-07 AD=8e-14 AS=8e-14
PD=1.2e-06 PS=1.2e-06 fw=4e-07 sa=2e-06 sb=2e-06 sca
=2.67857 scb=4.09292e-05 scc=9.01501e-10 $X=14090 $Y=8840
$dt=11
383 M22 10 VINM 11 VDD g45p2svt L=6e-07 W=4e-07 AD=8e-14 AS=8e-14
PD=1.2e-06 PS=1.2e-06 fw=4e-07 sa=2e-06 sb=2e-06 sca=8.4747
scb=0.00743239 scc=0.000298091 $X=15690 $Y=5400 $dt=11
384 M23 VDD VDD VDD VDD g45p2svt L=6e-07 W=4e-07 AD=8e-14 AS=8e-14
PD=1.2e-06 PS=1.2e-06 fw=4e-07 sa=2e-06 sb=2e-06 sca
=2.67857 scb=4.09292e-05 scc=9.01501e-10 $X=15690 $Y=8840
$dt=11
385 M24 11 VINM 10 VDD g45p2svt L=6e-07 W=4e-07 AD=8e-14 AS=8e-14
PD=1.2e-06 PS=1.2e-06 fw=4e-07 sa=2e-06 sb=2e-06 sca=8.4747
scb=0.00743239 scc=0.000298091 $X=17290 $Y=5400 $dt=11
386 M25 VDD VDD VDD VDD g45p2svt L=6e-07 W=4e-07 AD=8e-14 AS=8e-14
PD=1.2e-06 PS=1.2e-06 fw=4e-07 sa=2e-06 sb=2e-06 sca
=2.67857 scb=4.09292e-05 scc=9.01501e-10 $X=17290 $Y=8840
$dt=11
387 M26 10 VINM 11 VDD g45p2svt L=6e-07 W=4e-07 AD=8e-14 AS=8e-14
PD=1.2e-06 PS=1.2e-06 fw=4e-07 sa=2e-06 sb=2e-06 sca=8.4747
```

```
      scb=0.00743239 scc=0.000298091 $X=18890 $Y=5400 $dt=11
388 M27 VDD VDD VDD VDD g45p2svt L=6e-07 W=4e-07 AD=8e-14 AS=8e-14
      PD=1.2e-06 PS=1.2e-06 fw=4e-07 sa=2e-06 sb=2e-06 sca
     =2.67857 scb=4.09292e-05 scc=9.01501e-10 $X=18890 $Y=8840
     $dt=11
389 .ends DS_VGA_OPAMP
```

Listing IV.3: Two Stage Op-amp (Class AB Output Stage) SPI

IV.4 Variable Gain Amplifier (VGA) SPI

```
1  * ++++++++++++++++++++++++++++++++++++++++++++++++++++++++ *
2  * CDL Netlist:                                             *
3  *                                                          *
4  * Cell Name   : DS_VGA                                     *
5  * Netlisted   : Sun Apr 17 11:53:13 2022                   *
6  * PVS Version: 15.24-s451 Thu Jun  8 20:13:49 PDT 2017 *
7  * ++++++++++++++++++++++++++++++++++++++++++++++++++++++++ *
8  *.LDD
9  *.DEVTMPLT 0 MN(g45n1svt) _nmos1v ndiff_conn(D) poly_conn(G)
       ndiff_conn(S) psubstrate(B)
10 *.DEVTMPLT 1 MN(g45n1hvt) _nmos1v_hvt ndiff_conn(D) poly_conn(
       G) ndiff_conn(S) psubstrate(B)
11 *.DEVTMPLT 2 MN(g45n1lvt) _nmos1v_lvt ndiff_conn(D) poly_conn(
       G) ndiff_conn(S) psubstrate(B)
12 *.DEVTMPLT 3 MN(g45n1nvt) _nmos_12_native ndiff_conn(D)
       poly_conn(G) ndiff_conn(S) psubstrate(B)
13 *.DEVTMPLT 4 MN(g45n2svt) _nmos_25 ndiff_conn(D) poly_conn(G)
       ndiff_conn(S) psubstrate(B)
14 *.DEVTMPLT 5 MN(g45n2nvt) _nmos_25_native ndiff_conn(D)
       poly_conn(G) ndiff_conn(S) psubstrate(B)
15 *.DEVTMPLT 6 MN(g45ncap1) _nmoscap1v ndiff_conn(D) poly_conn(G
       ) ndiff_conn(S) psubstrate(B)
```

```
16 *.DEVTMPLT 7 MN(g45ncap2) _nmoscap2v ndiff_conn(D) poly_conn(G
   ) ndiff_conn(S) psubstrate(B)
17 *.DEVTMPLT 8 MP(g45p1svt) _pmos1v pdiff_conn(D) poly_conn(G)
   pdiff_conn(S) nwell_conn(B)
18 *.DEVTMPLT 9 MP(g45p1hvt) _pmos1v_hvt pdiff_conn(D) poly_conn(
   G) pdiff_conn(S) nwell_conn(B)
19 *.DEVTMPLT 10 MP(g45p1lvt) _pmos1v_lvt pdiff_conn(D) poly_conn
   (G) pdiff_conn(S) nwell_conn(B)
20 *.DEVTMPLT 11 MP(g45p2svt) _pmos2v pdiff_conn(D) poly_conn(G)
   pdiff_conn(S) nwell_conn(B)
21 *.DEVTMPLT 12 MP(g45pcap1) _pmoscap1v pdiff_conn(D) poly_conn(
   G) pdiff_conn(S) nwell_conn(B)
22 *.DEVTMPLT 13 MP(g45pcap2) _pmoscap2v pdiff_conn(D) poly_conn(
   G) pdiff_conn(S) nwell_conn(B)
23 *.DEVTMPLT 14 R(g45rm1) _resm1 metal1_conn(PLUS) metal1_conn(
   MINUS)
24 *.DEVTMPLT 15 R(g45rm2) _resm2 metal2_conn(PLUS) metal2_conn(
   MINUS)
25 *.DEVTMPLT 16 R(g45rm3) _resm3 metal3_conn(PLUS) metal3_conn(
   MINUS)
26 *.DEVTMPLT 17 R(g45rm4) _resm4 metal4_conn(PLUS) metal4_conn(
   MINUS)
27 *.DEVTMPLT 18 R(g45rm5) _resm5 metal5_conn(PLUS) metal5_conn(
   MINUS)
```

```
28 *.DEVTMPLT 19 R(g45rm6) _resm6 metal6_conn(PLUS) metal6_conn(
     MINUS)
29 *.DEVTMPLT 20 R(g45rm7) _resm7 metal7_conn(PLUS) metal7_conn(
     MINUS)
30 *.DEVTMPLT 21 R(g45rm8) _resm8 metal8_conn(PLUS) metal8_conn(
     MINUS)
31 *.DEVTMPLT 22 R(g45rm9) _resm9 metal9_conn(PLUS) metal9_conn(
     MINUS)
32 *.DEVTMPLT 23 R(g45rm10) _resm10 metal10_conn(PLUS)
     metal10_conn(MINUS)
33 *.DEVTMPLT 24 R(g45rm11) _resm11 metal11_conn(PLUS)
     metal11_conn(MINUS)
34 *.DEVTMPLT 25 R(g45rsnd) _ressndiff ndiff_conn(PLUS)
     ndiff_conn(MINUS) psubstrate(B)
35 *.DEVTMPLT 26 R(g45rnsnd) _resnsndiff ndiff_conn(PLUS)
     ndiff_conn(MINUS) psubstrate(B)
36 *.DEVTMPLT 27 R(g45rsnp) _ressnpoly poly_conn(PLUS) poly_conn(
     MINUS) psubstrate(B)
37 *.DEVTMPLT 28 R(g45rsnp) _ressnpoly_nw poly_conn(PLUS)
     poly_conn(MINUS) nwell_conn(B)
38 *.DEVTMPLT 29 R(g45rnsnp) _resnsnpoly poly_conn(PLUS)
     poly_conn(MINUS) psubstrate(B)
39 *.DEVTMPLT 30 R(g45rnsnp) _resnsnpoly_nw poly_conn(PLUS)
     poly_conn(MINUS) nwell_conn(B)
```

```
40 *.DEVTMPLT 31 R(g45rspd) _resspdiff pdiff_conn(PLUS)
     pdiff_conn(MINUS) nwell_conn(B)
41 *.DEVTMPLT 32 R(g45rnspd) _resnspdiff pdiff_conn(PLUS)
     pdiff_conn(MINUS) nwell_conn(B)
42 *.DEVTMPLT 33 R(g45rspp) _ressppoly poly_conn(PLUS) poly_conn(
     MINUS) psubstrate(B)
43 *.DEVTMPLT 34 R(g45rspp) _ressppoly_nw poly_conn(PLUS)
     poly_conn(MINUS) nwell_conn(B)
44 *.DEVTMPLT 35 R(g45rnspp) _resnsppoly poly_conn(PLUS)
     poly_conn(MINUS) psubstrate(B)
45 *.DEVTMPLT 36 R(g45rnspp) _resnsppoly_nw poly_conn(PLUS)
     poly_conn(MINUS) nwell_conn(B)
46 *.DEVTMPLT 37 R(g45rnws) _resnwsti nwell_conn(PLUS) nwell_conn
     (MINUS) psubstrate(B)
47 *.DEVTMPLT 38 R(g45rnwo) _resnwoxide nwell_conn(PLUS)
     nwell_conn(MINUS) psubstrate(B)
48 *.DEVTMPLT 39 D(g45nd1svt) _ndio psubstrate(PLUS) ndiff_conn(
     MINUS)
49 *.DEVTMPLT 40 D(g45nd1lvt) _ndio_lvt psubstrate(PLUS)
     ndiff_conn(MINUS)
50 *.DEVTMPLT 41 D(g45nd1hvt) _ndio_hvt psubstrate(PLUS)
     ndiff_conn(MINUS)
51 *.DEVTMPLT 42 D(g45nd1nvt) _ndio_nvt psubstrate(PLUS)
     ndiff_conn(MINUS)
```

```
52 *.DEVTMPLT 43 D(g45nd2svt) _ndio_2v psubstrate(PLUS)
       ndiff_conn(MINUS)
53 *.DEVTMPLT 44 D(g45nd2nvt) _ndio_2v_nvt psubstrate(PLUS)
       ndiff_conn(MINUS)
54 *.DEVTMPLT 45 D(g45pd1svt) _pdio pdiff_conn(PLUS) nwell_conn(
      MINUS)
55 *.DEVTMPLT 46 D(g45pd1lvt) _pdio_lvt pdiff_conn(PLUS)
       nwell_conn(MINUS)
56 *.DEVTMPLT 47 D(g45pd1hvt) _pdio_hvt pdiff_conn(PLUS)
       nwell_conn(MINUS)
57 *.DEVTMPLT 48 D(g45pd2svt) _pdio_2v pdiff_conn(PLUS)
       nwell_conn(MINUS)
58 *.DEVTMPLT 49 Q(g45vpnp2) _vpnp2 psubstrate(C) nwell_conn(B)
       pdiff_conn(E)
59 *.DEVTMPLT 50 Q(g45vpnp5) _vpnp5 psubstrate(C) nwell_conn(B)
       pdiff_conn(E)
60 *.DEVTMPLT 51 Q(g45vpnp10) _vpnp10 psubstrate(C) nwell_conn(B)
        pdiff_conn(E)
61 *.DEVTMPLT 52 Q(g45vnpn2) _npn2 nwell_conn(C) psubstrate(B)
       npn_emit(E)
62 *.DEVTMPLT 53 Q(g45vnpn5) _npn5 nwell_conn(C) psubstrate(B)
       npn_emit(E)
63 *.DEVTMPLT 54 Q(g45vnpn10) _npn10 nwell_conn(C) psubstrate(B)
       npn_emit(E)
```

```
64 *.DEVTMPLT 55 C(g45cmim) _mimcap CapMetal(PLUS) metal10_conn(
     MINUS) psubstrate(B)
65 *.DEVTMPLT 56 L(g45inda) _ind_a ind10(PLUS) ind11(MINUS)
     psubstrate(B)
66 *.DEVTMPLT 57 L(g45inds) _ind_s ind11(PLUS) ind11(MINUS)
     psubstrate(B)
67
68 * ++++++++++++++++++++++++++++++++++++++++++++++++++++++++ *
69 * Sub cell: L                                              *
70 * ++++++++++++++++++++++++++++++++++++++++++++++++++++++++ *
71 .subckt L PLUS MINUS B
72 .ends L
73
74 * ++++++++++++++++++++++++++++++++++++++++++++++++++++++++ *
75 * Sub cell: pmos2v$$27                                     *
76 * ++++++++++++++++++++++++++++++++++++++++++++++++++++++++ *
77 .subckt pmos2v$$27 1
78 ** N=10 EP=1 FDC=8
79 M0 1 1 1 1 g45p2svt L=6e-07 W=4e-07 AD=8e-14 AS=6e-14 PD=1.2e
     -06 PS=1.1e-06 fw=4e-07 sa=1.5e-07 sb=2e-06 sca=3.00153 scb
     =9.80227e-05 scc=1.47329e-08 $X=0 $Y=0 $dt=11
80 M1 1 1 1 1 g45p2svt L=6e-07 W=4e-07 AD=8e-14 AS=8e-14 PD=1.2e
     -06 PS=1.2e-06 fw=4e-07 sa=9.5e-07 sb=2e-06 sca=2.67857 scb
     =4.09292e-05 scc=9.01501e-10 $X=1600 $Y=0 $dt=11
```

```
81 M2 1 1 1 1 g45p2svt L=6e-07 W=4e-07 AD=8e-14 AS=8e-14 PD=1.2e
    -06 PS=1.2e-06 fw=4e-07 sa=1.75e-06 sb=2e-06 sca=2.67857
    scb=4.09292e-05 scc=9.01501e-10 $X=3200 $Y=0 $dt=11
82 M3 1 1 1 1 g45p2svt L=6e-07 W=4e-07 AD=8e-14 AS=8e-14 PD=1.2e
    -06 PS=1.2e-06 fw=4e-07 sa=2e-06 sb=2e-06 sca=2.67857 scb
    =4.09292e-05 scc=9.01501e-10 $X=4800 $Y=0 $dt=11
83 M4 1 1 1 1 g45p2svt L=6e-07 W=4e-07 AD=8e-14 AS=8e-14 PD=1.2e
    -06 PS=1.2e-06 fw=4e-07 sa=2e-06 sb=2e-06 sca=2.67857 scb
    =4.09292e-05 scc=9.01501e-10 $X=6400 $Y=0 $dt=11
84 M5 1 1 1 1 g45p2svt L=6e-07 W=4e-07 AD=8e-14 AS=8e-14 PD=1.2e
    -06 PS=1.2e-06 fw=4e-07 sa=2e-06 sb=2e-06 sca=2.67857 scb
    =4.09292e-05 scc=9.01501e-10 $X=8000 $Y=0 $dt=11
85 M6 1 1 1 1 g45p2svt L=6e-07 W=4e-07 AD=8e-14 AS=8e-14 PD=1.2e
    -06 PS=1.2e-06 fw=4e-07 sa=2e-06 sb=2e-06 sca=2.67857 scb
    =4.09292e-05 scc=9.01501e-10 $X=9600 $Y=0 $dt=11
86 M7 1 1 1 1 g45p2svt L=6e-07 W=4e-07 AD=8e-14 AS=8e-14 PD=1.2e
    -06 PS=1.2e-06 fw=4e-07 sa=2e-06 sb=2e-06 sca=2.67857 scb
    =4.09292e-05 scc=9.01501e-10 $X=11200 $Y=0 $dt=11
87 .ends pmos2v$$27
88
89 * ++++++++++++++++++++++++++++++++++++++++++++++++++++++++ *
90 * Sub cell: pmos2v$$28                                     *
91 * ++++++++++++++++++++++++++++++++++++++++++++++++++++++++ *
92 .subckt pmos2v$$28 1 2 3 5
93 ** N=5 EP=4 FDC=10
```

```
94 M0 1 2 3 5 g45p2svt L=6e-07 W=4e-07 AD=8e-14 AS=8e-14 PD=1.2e
    -06 PS=1.2e-06 fw=4e-07 sa=2e-06 sb=2e-06 sca=8.4747 scb
    =0.00743239 scc=0.000298091 $X=0 $Y=0 $dt=11
95 M1 3 2 1 5 g45p2svt L=6e-07 W=4e-07 AD=8e-14 AS=8e-14 PD=1.2e
    -06 PS=1.2e-06 fw=4e-07 sa=2e-06 sb=2e-06 sca=8.4747 scb
    =0.00743239 scc=0.000298091 $X=1600 $Y=0 $dt=11
96 M2 1 2 3 5 g45p2svt L=6e-07 W=4e-07 AD=8e-14 AS=8e-14 PD=1.2e
    -06 PS=1.2e-06 fw=4e-07 sa=2e-06 sb=2e-06 sca=8.4747 scb
    =0.00743239 scc=0.000298091 $X=3200 $Y=0 $dt=11
97 M3 3 2 1 5 g45p2svt L=6e-07 W=4e-07 AD=8e-14 AS=8e-14 PD=1.2e
    -06 PS=1.2e-06 fw=4e-07 sa=2e-06 sb=2e-06 sca=8.4747 scb
    =0.00743239 scc=0.000298091 $X=4800 $Y=0 $dt=11
98 M4 1 2 3 5 g45p2svt L=6e-07 W=4e-07 AD=8e-14 AS=8e-14 PD=1.2e
    -06 PS=1.2e-06 fw=4e-07 sa=2e-06 sb=2e-06 sca=8.4747 scb
    =0.00743239 scc=0.000298091 $X=6400 $Y=0 $dt=11
99 M5 3 2 1 5 g45p2svt L=6e-07 W=4e-07 AD=8e-14 AS=8e-14 PD=1.2e
    -06 PS=1.2e-06 fw=4e-07 sa=2e-06 sb=2e-06 sca=8.4747 scb
    =0.00743239 scc=0.000298091 $X=8000 $Y=0 $dt=11
100 M6 1 2 3 5 g45p2svt L=6e-07 W=4e-07 AD=8e-14 AS=8e-14 PD=1.2e
    -06 PS=1.2e-06 fw=4e-07 sa=2e-06 sb=2e-06 sca=8.4747 scb
    =0.00743239 scc=0.000298091 $X=9600 $Y=0 $dt=11
101 M7 3 2 1 5 g45p2svt L=6e-07 W=4e-07 AD=8e-14 AS=8e-14 PD=1.2e
    -06 PS=1.2e-06 fw=4e-07 sa=2e-06 sb=1.75e-06 sca=8.4747 scb
    =0.00743239 scc=0.000298091 $X=11200 $Y=0 $dt=11
```

```
M8 1 2 3 5 g45p2svt L=6e-07 W=4e-07 AD=8e-14 AS=8e-14 PD=1.2e
    -06 PS=1.2e-06 fw=4e-07 sa=2e-06 sb=9.5e-07 sca=8.4747 scb
    =0.00743239 scc=0.000298091 $X=12800 $Y=0 $dt=11
M9 3 2 1 5 g45p2svt L=6e-07 W=4e-07 AD=6e-14 AS=8e-14 PD=1.1e
    -06 PS=1.2e-06 fw=4e-07 sa=2e-06 sb=1.5e-07 sca=8.79766 scb
    =0.00748949 scc=0.000298105 $X=14400 $Y=0 $dt=11
.ends pmos2v$$28

* ++++++++++++++++++++++++++++++++++++++++++++++++++++++++ *
* Sub cell: pmos2v$$29                                      *
* ++++++++++++++++++++++++++++++++++++++++++++++++++++++++ *
.subckt pmos2v$$29 1
** N=6 EP=1 FDC=4
M0 1 1 1 1 g45p2svt L=6e-07 W=4e-07 AD=8e-14 AS=6e-14 PD=1.2e
    -06 PS=1.1e-06 fw=4e-07 sa=1.5e-07 sb=2e-06 sca=2.98259 scb
    =9.24817e-05 scc=1.23329e-08 $X=0 $Y=0 $dt=11
M1 1 1 1 1 g45p2svt L=6e-07 W=4e-07 AD=8e-14 AS=8e-14 PD=1.2e
    -06 PS=1.2e-06 fw=4e-07 sa=9.5e-07 sb=2e-06 sca=2.67857 scb
    =4.09292e-05 scc=9.01501e-10 $X=1600 $Y=0 $dt=11
M2 1 1 1 1 g45p2svt L=6e-07 W=4e-07 AD=8e-14 AS=8e-14 PD=1.2e
    -06 PS=1.2e-06 fw=4e-07 sa=1.75e-06 sb=2e-06 sca=2.67857
    scb=4.09292e-05 scc=9.01501e-10 $X=3200 $Y=0 $dt=11
M3 1 1 1 1 g45p2svt L=6e-07 W=4e-07 AD=8e-14 AS=8e-14 PD=1.2e
    -06 PS=1.2e-06 fw=4e-07 sa=2e-06 sb=2e-06 sca=2.67857 scb
    =4.09292e-05 scc=9.01501e-10 $X=4800 $Y=0 $dt=11
```

```
.ends pmos2v$$29

* ++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++ *
* Sub cell: pmos2v$$30                                           *
* ++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++ *
.subckt pmos2v$$30 1 2 3
** N=4 EP=3 FDC=6
M0 1 2 3 1 g45p2svt L=6e-07 W=4e-07 AD=8e-14 AS=8e-14 PD=1.2e
    -06 PS=1.2e-06 fw=4e-07 sa=2e-06 sb=2e-06 sca=8.4747 scb
    =0.00743239 scc=0.000298091 $X=0 $Y=0 $dt=11
M1 3 2 1 1 g45p2svt L=6e-07 W=4e-07 AD=8e-14 AS=8e-14 PD=1.2e
    -06 PS=1.2e-06 fw=4e-07 sa=2e-06 sb=2e-06 sca=8.4747 scb
    =0.00743239 scc=0.000298091 $X=1600 $Y=0 $dt=11
M2 1 2 3 1 g45p2svt L=6e-07 W=4e-07 AD=8e-14 AS=8e-14 PD=1.2e
    -06 PS=1.2e-06 fw=4e-07 sa=2e-06 sb=2e-06 sca=8.4747 scb
    =0.00743239 scc=0.000298091 $X=3200 $Y=0 $dt=11
M3 3 2 1 1 g45p2svt L=6e-07 W=4e-07 AD=8e-14 AS=8e-14 PD=1.2e
    -06 PS=1.2e-06 fw=4e-07 sa=2e-06 sb=1.75e-06 sca=8.4747 scb
    =0.00743239 scc=0.000298091 $X=4800 $Y=0 $dt=11
M4 1 2 3 1 g45p2svt L=6e-07 W=4e-07 AD=8e-14 AS=8e-14 PD=1.2e
    -06 PS=1.2e-06 fw=4e-07 sa=2e-06 sb=9.5e-07 sca=8.4747 scb
    =0.00743239 scc=0.000298091 $X=6400 $Y=0 $dt=11
M5 3 2 1 1 g45p2svt L=6e-07 W=4e-07 AD=6e-14 AS=8e-14 PD=1.1e
    -06 PS=1.2e-06 fw=4e-07 sa=2e-06 sb=1.5e-07 sca=8.77873 scb
    =0.00748395 scc=0.000298102 $X=8000 $Y=0 $dt=11
```

```
128 .ends pmos2v$$30
129
130 * ++++++++++++++++++++++++++++++++++++++++++++++++++++++++ *
131 * Sub cell: nmos2v$$31                                     *
132 * ++++++++++++++++++++++++++++++++++++++++++++++++++++++++ *
133 .subckt nmos2v$$31 1 2 3
134 ** N=3 EP=3 FDC=4
135 M0 3 1 2 3 g45n2svt L=6e-07 W=4e-07 AD=8e-14 AS=8e-14 PD=1.2e
    -06 PS=1.2e-06 fw=4e-07 sa=2e-06 sb=2e-06 sca=2.67857 scb
    =4.09292e-05 scc=9.01501e-10 $X=0 $Y=0 $dt=4
136 M1 2 1 3 3 g45n2svt L=6e-07 W=4e-07 AD=8e-14 AS=8e-14 PD=1.2e
    -06 PS=1.2e-06 fw=4e-07 sa=2e-06 sb=1.75e-06 sca=2.67857
    scb=4.09292e-05 scc=9.01501e-10 $X=1600 $Y=0 $dt=4
137 M2 3 1 2 3 g45n2svt L=6e-07 W=4e-07 AD=8e-14 AS=8e-14 PD=1.2e
    -06 PS=1.2e-06 fw=4e-07 sa=2e-06 sb=9.5e-07 sca=2.67857 scb
    =4.09292e-05 scc=9.01501e-10 $X=3200 $Y=0 $dt=4
138 M3 2 1 3 3 g45n2svt L=6e-07 W=4e-07 AD=6e-14 AS=8e-14 PD=1.1e
    -06 PS=1.2e-06 fw=4e-07 sa=2e-06 sb=1.5e-07 sca=2.67857 scb
    =4.09292e-05 scc=9.01501e-10 $X=4800 $Y=0 $dt=4
139 .ends nmos2v$$31
140
141 * ++++++++++++++++++++++++++++++++++++++++++++++++++++++++ *
142 * Sub cell: nmos2v$$32                                     *
143 * ++++++++++++++++++++++++++++++++++++++++++++++++++++++++ *
144 .subckt nmos2v$$32 1
```

```
145 ** N=17 EP=1 FDC=16
146 M0 1 1 1 1 g45n2svt L=6e-07 W=4e-07 AD=8e-14 AS=6e-14 PD=1.2e
    -06 PS=1.1e-06 fw=4e-07 sa=1.5e-07 sb=2e-06 sca=2.67857 scb
    =4.09292e-05 scc=9.01501e-10 $X=0 $Y=0 $dt=4
147 M1 1 1 1 1 g45n2svt L=6e-07 W=4e-07 AD=8e-14 AS=8e-14 PD=1.2e
    -06 PS=1.2e-06 fw=4e-07 sa=9.5e-07 sb=2e-06 sca=2.67857 scb
    =4.09292e-05 scc=9.01501e-10 $X=1600 $Y=0 $dt=4
148 M2 1 1 1 1 g45n2svt L=6e-07 W=4e-07 AD=8e-14 AS=8e-14 PD=1.2e
    -06 PS=1.2e-06 fw=4e-07 sa=1.75e-06 sb=2e-06 sca=2.67857
    scb=4.09292e-05 scc=9.01501e-10 $X=3200 $Y=0 $dt=4
149 M3 1 1 1 1 g45n2svt L=6e-07 W=4e-07 AD=8e-14 AS=8e-14 PD=1.2e
    -06 PS=1.2e-06 fw=4e-07 sa=2e-06 sb=2e-06 sca=2.67857 scb
    =4.09292e-05 scc=9.01501e-10 $X=4800 $Y=0 $dt=4
150 M4 1 1 1 1 g45n2svt L=6e-07 W=4e-07 AD=8e-14 AS=8e-14 PD=1.2e
    -06 PS=1.2e-06 fw=4e-07 sa=2e-06 sb=2e-06 sca=2.67857 scb
    =4.09292e-05 scc=9.01501e-10 $X=6400 $Y=0 $dt=4
151 M5 1 1 1 1 g45n2svt L=6e-07 W=4e-07 AD=8e-14 AS=8e-14 PD=1.2e
    -06 PS=1.2e-06 fw=4e-07 sa=2e-06 sb=2e-06 sca=2.67857 scb
    =4.09292e-05 scc=9.01501e-10 $X=8000 $Y=0 $dt=4
152 M6 1 1 1 1 g45n2svt L=6e-07 W=4e-07 AD=8e-14 AS=8e-14 PD=1.2e
    -06 PS=1.2e-06 fw=4e-07 sa=2e-06 sb=2e-06 sca=2.67857 scb
    =4.09292e-05 scc=9.01501e-10 $X=9600 $Y=0 $dt=4
153 M7 1 1 1 1 g45n2svt L=6e-07 W=4e-07 AD=8e-14 AS=8e-14 PD=1.2e
    -06 PS=1.2e-06 fw=4e-07 sa=2e-06 sb=2e-06 sca=2.67857 scb
    =4.09292e-05 scc=9.01501e-10 $X=11200 $Y=0 $dt=4
```

```
154 M8 1 1 1 1 g45n2svt L=6e-07 W=4e-07 AD=8e-14 AS=8e-14 PD=1.2e
    -06 PS=1.2e-06 fw=4e-07 sa=2e-06 sb=2e-06 sca=2.67857 scb
    =4.09292e-05 scc=9.01501e-10 $X=12800 $Y=0 $dt=4
155 M9 1 1 1 1 g45n2svt L=6e-07 W=4e-07 AD=8e-14 AS=8e-14 PD=1.2e
    -06 PS=1.2e-06 fw=4e-07 sa=2e-06 sb=2e-06 sca=2.67857 scb
    =4.09292e-05 scc=9.01501e-10 $X=14400 $Y=0 $dt=4
156 M10 1 1 1 1 g45n2svt L=6e-07 W=4e-07 AD=8e-14 AS=8e-14 PD=1.2e
    -06 PS=1.2e-06 fw=4e-07 sa=2e-06 sb=2e-06 sca=2.67857 scb
    =4.09292e-05 scc=9.01501e-10 $X=16000 $Y=0 $dt=4
157 M11 1 1 1 1 g45n2svt L=6e-07 W=4e-07 AD=8e-14 AS=8e-14 PD=1.2e
    -06 PS=1.2e-06 fw=4e-07 sa=2e-06 sb=2e-06 sca=2.67857 scb
    =4.09292e-05 scc=9.01501e-10 $X=17600 $Y=0 $dt=4
158 M12 1 1 1 1 g45n2svt L=6e-07 W=4e-07 AD=8e-14 AS=8e-14 PD=1.2e
    -06 PS=1.2e-06 fw=4e-07 sa=2e-06 sb=2e-06 sca=2.67857 scb
    =4.09292e-05 scc=9.01501e-10 $X=19200 $Y=0 $dt=4
159 M13 1 1 1 1 g45n2svt L=6e-07 W=4e-07 AD=8e-14 AS=8e-14 PD=1.2e
    -06 PS=1.2e-06 fw=4e-07 sa=2e-06 sb=2e-06 sca=2.67857 scb
    =4.09292e-05 scc=9.01501e-10 $X=20800 $Y=0 $dt=4
160 M14 1 1 1 1 g45n2svt L=6e-07 W=4e-07 AD=8e-14 AS=8e-14 PD=1.2e
    -06 PS=1.2e-06 fw=4e-07 sa=2e-06 sb=2e-06 sca=2.67857 scb
    =4.09292e-05 scc=9.01501e-10 $X=22400 $Y=0 $dt=4
161 M15 1 1 1 1 g45n2svt L=6e-07 W=4e-07 AD=8e-14 AS=8e-14 PD=1.2e
    -06 PS=1.2e-06 fw=4e-07 sa=2e-06 sb=2e-06 sca=2.67857 scb
    =4.09292e-05 scc=9.01501e-10 $X=24000 $Y=0 $dt=4
162 .ends nmos2v$$32
```

```
163
164 * ++++++++++++++++++++++++++++++++++++++++++++++++++++++++ *
165 * Sub cell: pmos2v$$33                                      *
166 * ++++++++++++++++++++++++++++++++++++++++++++++++++++++++ *
167 .subckt pmos2v$$33 1 2 3
168 ** N=4 EP=3 FDC=6
169 M0 3 1 2 3 g45p2svt L=6e-07 W=4e-07 AD=8e-14 AS=8e-14 PD=1.2e
        -06 PS=1.2e-06 fw=4e-07 sa=2e-06 sb=2e-06 sca=2.67857 scb
        =4.09292e-05 scc=9.01501e-10 $X=0 $Y=0 $dt=11
170 M1 2 1 3 3 g45p2svt L=6e-07 W=4e-07 AD=8e-14 AS=8e-14 PD=1.2e
        -06 PS=1.2e-06 fw=4e-07 sa=2e-06 sb=2e-06 sca=2.67857 scb
        =4.09292e-05 scc=9.01501e-10 $X=1600 $Y=0 $dt=11
171 M2 3 1 2 3 g45p2svt L=6e-07 W=4e-07 AD=8e-14 AS=8e-14 PD=1.2e
        -06 PS=1.2e-06 fw=4e-07 sa=2e-06 sb=2e-06 sca=2.67857 scb
        =4.09292e-05 scc=9.01501e-10 $X=3200 $Y=0 $dt=11
172 M3 2 1 3 3 g45p2svt L=6e-07 W=4e-07 AD=8e-14 AS=8e-14 PD=1.2e
        -06 PS=1.2e-06 fw=4e-07 sa=2e-06 sb=1.75e-06 sca=2.67857
        scb=4.09292e-05 scc=9.01501e-10 $X=4800 $Y=0 $dt=11
173 M4 3 1 2 3 g45p2svt L=6e-07 W=4e-07 AD=8e-14 AS=8e-14 PD=1.2e
        -06 PS=1.2e-06 fw=4e-07 sa=2e-06 sb=9.5e-07 sca=2.67857 scb
        =4.09292e-05 scc=9.01501e-10 $X=6400 $Y=0 $dt=11
174 M5 2 1 3 3 g45p2svt L=6e-07 W=4e-07 AD=6e-14 AS=8e-14 PD=1.1e
        -06 PS=1.2e-06 fw=4e-07 sa=2e-06 sb=1.5e-07 sca=2.98259 scb
        =9.24817e-05 scc=1.23329e-08 $X=8000 $Y=0 $dt=11
175 .ends pmos2v$$33
```

```
176
177 * ++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++ *
178 * Sub cell: pmos2v$$35                                           *
179 * ++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++ *
180 .subckt pmos2v$$35 1 2 3
181 ** N=4 EP=3 FDC=6
182 M0 1 2 3 1 g45p2svt L=6e-07 W=4e-07 AD=8e-14 AS=8e-14 PD=1.2e
    -06 PS=1.2e-06 fw=4e-07 sa=2e-06 sb=2e-06 sca=2.67857 scb
    =4.09292e-05 scc=9.01501e-10 $X=0 $Y=0 $dt=11
183 M1 3 2 1 1 g45p2svt L=6e-07 W=4e-07 AD=8e-14 AS=8e-14 PD=1.2e
    -06 PS=1.2e-06 fw=4e-07 sa=2e-06 sb=2e-06 sca=2.67857 scb
    =4.09292e-05 scc=9.01501e-10 $X=1600 $Y=0 $dt=11
184 M2 1 2 3 1 g45p2svt L=6e-07 W=4e-07 AD=8e-14 AS=8e-14 PD=1.2e
    -06 PS=1.2e-06 fw=4e-07 sa=2e-06 sb=2e-06 sca=2.67857 scb
    =4.09292e-05 scc=9.01501e-10 $X=3200 $Y=0 $dt=11
185 M3 3 2 1 1 g45p2svt L=6e-07 W=4e-07 AD=8e-14 AS=8e-14 PD=1.2e
    -06 PS=1.2e-06 fw=4e-07 sa=2e-06 sb=2e-06 sca=2.67857 scb
    =4.09292e-05 scc=9.01501e-10 $X=4800 $Y=0 $dt=11
186 M4 1 2 3 1 g45p2svt L=6e-07 W=4e-07 AD=8e-14 AS=8e-14 PD=1.2e
    -06 PS=1.2e-06 fw=4e-07 sa=2e-06 sb=2e-06 sca=2.67857 scb
    =4.09292e-05 scc=9.01501e-10 $X=6400 $Y=0 $dt=11
187 M5 3 2 1 1 g45p2svt L=6e-07 W=4e-07 AD=8e-14 AS=8e-14 PD=1.2e
    -06 PS=1.2e-06 fw=4e-07 sa=2e-06 sb=2e-06 sca=2.67857 scb
    =4.09292e-05 scc=9.01501e-10 $X=8000 $Y=0 $dt=11
188 .ends pmos2v$$35
```

```
189
190 * ++++++++++++++++++++++++++++++++++++++++++++++++++++++++ *
191 * Sub cell: pmos2v$$36                                      *
192 * ++++++++++++++++++++++++++++++++++++++++++++++++++++++++ *
193 .subckt pmos2v$$36 1 2
194 ** N=3 EP=2 FDC=6
195 M0 1 2 2 1 g45p2svt L=6e-07 W=4e-07 AD=8e-14 AS=8e-14 PD=1.2e
    -06 PS=1.2e-06 fw=4e-07 sa=2e-06 sb=2e-06 sca=2.67857 scb
    =4.09292e-05 scc=9.01501e-10 $X=0 $Y=0 $dt=11
196 M1 2 2 1 1 g45p2svt L=6e-07 W=4e-07 AD=8e-14 AS=8e-14 PD=1.2e
    -06 PS=1.2e-06 fw=4e-07 sa=2e-06 sb=2e-06 sca=2.67857 scb
    =4.09292e-05 scc=9.01501e-10 $X=1600 $Y=0 $dt=11
197 M2 1 2 2 1 g45p2svt L=6e-07 W=4e-07 AD=8e-14 AS=8e-14 PD=1.2e
    -06 PS=1.2e-06 fw=4e-07 sa=2e-06 sb=2e-06 sca=2.67857 scb
    =4.09292e-05 scc=9.01501e-10 $X=3200 $Y=0 $dt=11
198 M3 2 2 1 1 g45p2svt L=6e-07 W=4e-07 AD=8e-14 AS=8e-14 PD=1.2e
    -06 PS=1.2e-06 fw=4e-07 sa=2e-06 sb=2e-06 sca=2.67857 scb
    =4.09292e-05 scc=9.01501e-10 $X=4800 $Y=0 $dt=11
199 M4 1 2 2 1 g45p2svt L=6e-07 W=4e-07 AD=8e-14 AS=8e-14 PD=1.2e
    -06 PS=1.2e-06 fw=4e-07 sa=2e-06 sb=2e-06 sca=2.67857 scb
    =4.09292e-05 scc=9.01501e-10 $X=6400 $Y=0 $dt=11
200 M5 2 2 1 1 g45p2svt L=6e-07 W=4e-07 AD=8e-14 AS=8e-14 PD=1.2e
    -06 PS=1.2e-06 fw=4e-07 sa=2e-06 sb=2e-06 sca=2.67857 scb
    =4.09292e-05 scc=9.01501e-10 $X=8000 $Y=0 $dt=11
201 .ends pmos2v$$36
```

```
202
203 * ++++++++++++++++++++++++++++++++++++++++++++++++++++++++ *
204 * Sub cell: pmos2v$$37                                     *
205 * ++++++++++++++++++++++++++++++++++++++++++++++++++++++++ *
206 .subckt pmos2v$$37 1
207 ** N=16 EP=1 FDC=14
208 M0 1 1 1 1 g45p2svt L=6e-07 W=4e-07 AD=8e-14 AS=6e-14 PD=1.2e
    -06 PS=1.1e-06 fw=4e-07 sa=1.5e-07 sb=2e-06 sca=8.79766 scb
    =0.00748949 scc=0.000298105 $X=0 $Y=0 $dt=11
209 M1 1 1 1 1 g45p2svt L=6e-07 W=4e-07 AD=8e-14 AS=8e-14 PD=1.2e
    -06 PS=1.2e-06 fw=4e-07 sa=9.5e-07 sb=2e-06 sca=8.4747 scb
    =0.00743239 scc=0.000298091 $X=1600 $Y=0 $dt=11
210 M2 1 1 1 1 g45p2svt L=6e-07 W=4e-07 AD=8e-14 AS=8e-14 PD=1.2e
    -06 PS=1.2e-06 fw=4e-07 sa=1.75e-06 sb=2e-06 sca=8.4747 scb
    =0.00743239 scc=0.000298091 $X=3200 $Y=0 $dt=11
211 M3 1 1 1 1 g45p2svt L=6e-07 W=4e-07 AD=8e-14 AS=8e-14 PD=1.2e
    -06 PS=1.2e-06 fw=4e-07 sa=2e-06 sb=2e-06 sca=8.4747 scb
    =0.00743239 scc=0.000298091 $X=4800 $Y=0 $dt=11
212 M4 1 1 1 1 g45p2svt L=6e-07 W=4e-07 AD=8e-14 AS=8e-14 PD=1.2e
    -06 PS=1.2e-06 fw=4e-07 sa=2e-06 sb=2e-06 sca=8.4747 scb
    =0.00743239 scc=0.000298091 $X=6400 $Y=0 $dt=11
213 M5 1 1 1 1 g45p2svt L=6e-07 W=4e-07 AD=8e-14 AS=8e-14 PD=1.2e
    -06 PS=1.2e-06 fw=4e-07 sa=2e-06 sb=2e-06 sca=8.4747 scb
    =0.00743239 scc=0.000298091 $X=8000 $Y=0 $dt=11
```

```
214 M6 1 1 1 1 g45p2svt L=6e-07 W=4e-07 AD=8e-14 AS=8e-14 PD=1.2e
    -06 PS=1.2e-06 fw=4e-07 sa=2e-06 sb=2e-06 sca=8.4747 scb
    =0.00743239 scc=0.000298091 $X=9600 $Y=0 $dt=11
215 M7 1 1 1 1 g45p2svt L=6e-07 W=4e-07 AD=8e-14 AS=8e-14 PD=1.2e
    -06 PS=1.2e-06 fw=4e-07 sa=2e-06 sb=2e-06 sca=8.4747 scb
    =0.00743239 scc=0.000298091 $X=11200 $Y=0 $dt=11
216 M8 1 1 1 1 g45p2svt L=6e-07 W=4e-07 AD=8e-14 AS=8e-14 PD=1.2e
    -06 PS=1.2e-06 fw=4e-07 sa=2e-06 sb=2e-06 sca=8.4747 scb
    =0.00743239 scc=0.000298091 $X=12800 $Y=0 $dt=11
217 M9 1 1 1 1 g45p2svt L=6e-07 W=4e-07 AD=8e-14 AS=8e-14 PD=1.2e
    -06 PS=1.2e-06 fw=4e-07 sa=2e-06 sb=2e-06 sca=8.4747 scb
    =0.00743239 scc=0.000298091 $X=14400 $Y=0 $dt=11
218 M10 1 1 1 1 g45p2svt L=6e-07 W=4e-07 AD=8e-14 AS=8e-14 PD=1.2e
    -06 PS=1.2e-06 fw=4e-07 sa=2e-06 sb=2e-06 sca=8.4747 scb
    =0.00743239 scc=0.000298091 $X=16000 $Y=0 $dt=11
219 M11 1 1 1 1 g45p2svt L=6e-07 W=4e-07 AD=8e-14 AS=8e-14 PD=1.2e
    -06 PS=1.2e-06 fw=4e-07 sa=2e-06 sb=2e-06 sca=8.4747 scb
    =0.00743239 scc=0.000298091 $X=17600 $Y=0 $dt=11
220 M12 1 1 1 1 g45p2svt L=6e-07 W=4e-07 AD=8e-14 AS=8e-14 PD=1.2e
    -06 PS=1.2e-06 fw=4e-07 sa=2e-06 sb=2e-06 sca=8.4747 scb
    =0.00743239 scc=0.000298091 $X=19200 $Y=0 $dt=11
221 M13 1 1 1 1 g45p2svt L=6e-07 W=4e-07 AD=8e-14 AS=8e-14 PD=1.2e
    -06 PS=1.2e-06 fw=4e-07 sa=2e-06 sb=2e-06 sca=8.4747 scb
    =0.00743239 scc=0.000298091 $X=20800 $Y=0 $dt=11
222 .ends pmos2v$$37
```

```
223
224 * ++++++++++++++++++++++++++++++++++++++++++++++++++++++++ *
225 * Sub cell: pmos2v$$38                                      *
226 * ++++++++++++++++++++++++++++++++++++++++++++++++++++++++ *
227 .subckt pmos2v$$38 1
228 ** N=6 EP=1 FDC=4
229 M0 1 1 1 1 g45p2svt L=6e-07 W=4e-07 AD=8e-14 AS=8e-14 PD=1.2e
    -06 PS=1.2e-06 fw=4e-07 sa=2e-06 sb=2e-06 sca=2.67857 scb
    =4.09292e-05 scc=9.01501e-10 $X=0 $Y=0 $dt=11
230 M1 1 1 1 1 g45p2svt L=6e-07 W=4e-07 AD=8e-14 AS=8e-14 PD=1.2e
    -06 PS=1.2e-06 fw=4e-07 sa=2e-06 sb=1.75e-06 sca=2.67857
    scb=4.09292e-05 scc=9.01501e-10 $X=1600 $Y=0 $dt=11
231 M2 1 1 1 1 g45p2svt L=6e-07 W=4e-07 AD=8e-14 AS=8e-14 PD=1.2e
    -06 PS=1.2e-06 fw=4e-07 sa=2e-06 sb=9.5e-07 sca=2.67857 scb
    =4.09292e-05 scc=9.01501e-10 $X=3200 $Y=0 $dt=11
232 M3 1 1 1 1 g45p2svt L=6e-07 W=4e-07 AD=6e-14 AS=8e-14 PD=1.1e
    -06 PS=1.2e-06 fw=4e-07 sa=2e-06 sb=1.5e-07 sca=3.00153 scb
    =9.80227e-05 scc=1.47329e-08 $X=4800 $Y=0 $dt=11
233 .ends pmos2v$$38
234
235 * ++++++++++++++++++++++++++++++++++++++++++++++++++++++++ *
236 * Sub cell: nmos2v$$39                                      *
237 * ++++++++++++++++++++++++++++++++++++++++++++++++++++++++ *
238 .subckt nmos2v$$39 1 2 3
239 ** N=3 EP=3 FDC=4
```

```
240 M0 3 1 2 3 g45n2svt L=6e-07 W=4e-07 AD=8e-14 AS=8e-14 PD=1.2e
    -06 PS=1.2e-06 fw=4e-07 sa=2e-06 sb=2e-06 sca=5.61926 scb
    =0.00306339 scc=3.82378e-05 $X=0 $Y=0 $dt=4
241 M1 2 1 3 3 g45n2svt L=6e-07 W=4e-07 AD=8e-14 AS=8e-14 PD=1.2e
    -06 PS=1.2e-06 fw=4e-07 sa=2e-06 sb=2e-06 sca=5.61926 scb
    =0.00306339 scc=3.82378e-05 $X=1600 $Y=0 $dt=4
242 M2 3 1 2 3 g45n2svt L=6e-07 W=4e-07 AD=8e-14 AS=8e-14 PD=1.2e
    -06 PS=1.2e-06 fw=4e-07 sa=2e-06 sb=2e-06 sca=5.61926 scb
    =0.00306339 scc=3.82378e-05 $X=3200 $Y=0 $dt=4
243 M3 2 1 3 3 g45n2svt L=6e-07 W=4e-07 AD=8e-14 AS=8e-14 PD=1.2e
    -06 PS=1.2e-06 fw=4e-07 sa=2e-06 sb=2e-06 sca=5.61926 scb
    =0.00306339 scc=3.82378e-05 $X=4800 $Y=0 $dt=4
244 .ends nmos2v$$39
245
246 * ++++++++++++++++++++++++++++++++++++++++++++++++++++++++ *
247 * Sub cell: nmos2v$$40                                     *
248 * ++++++++++++++++++++++++++++++++++++++++++++++++++++++++ *
249 .subckt nmos2v$$40 1
250 ** N=7 EP=1 FDC=6
251 M0 1 1 1 1 g45n2svt L=6e-07 W=4e-07 AD=8e-14 AS=6e-14 PD=1.2e
    -06 PS=1.1e-06 fw=4e-07 sa=1.5e-07 sb=2e-06 sca=5.61926 scb
    =0.00306339 scc=3.82378e-05 $X=0 $Y=0 $dt=4
252 M1 1 1 1 1 g45n2svt L=6e-07 W=4e-07 AD=8e-14 AS=8e-14 PD=1.2e
    -06 PS=1.2e-06 fw=4e-07 sa=9.5e-07 sb=2e-06 sca=5.61926 scb
    =0.00306339 scc=3.82378e-05 $X=1600 $Y=0 $dt=4
```

```
253 M2 1 1 1 1 g45n2svt L=6e-07 W=4e-07 AD=8e-14 AS=8e-14 PD=1.2e
    -06 PS=1.2e-06 fw=4e-07 sa=1.75e-06 sb=2e-06 sca=5.61926
    scb=0.00306339 scc=3.82378e-05 $X=3200 $Y=0 $dt=4
254 M3 1 1 1 1 g45n2svt L=6e-07 W=4e-07 AD=8e-14 AS=8e-14 PD=1.2e
    -06 PS=1.2e-06 fw=4e-07 sa=2e-06 sb=2e-06 sca=5.61926 scb
    =0.00306339 scc=3.82378e-05 $X=4800 $Y=0 $dt=4
255 M4 1 1 1 1 g45n2svt L=6e-07 W=4e-07 AD=8e-14 AS=8e-14 PD=1.2e
    -06 PS=1.2e-06 fw=4e-07 sa=2e-06 sb=2e-06 sca=5.61926 scb
    =0.00306339 scc=3.82378e-05 $X=6400 $Y=0 $dt=4
256 M5 1 1 1 1 g45n2svt L=6e-07 W=4e-07 AD=8e-14 AS=8e-14 PD=1.2e
    -06 PS=1.2e-06 fw=4e-07 sa=2e-06 sb=2e-06 sca=5.61926 scb
    =0.00306339 scc=3.82378e-05 $X=8000 $Y=0 $dt=4
257 .ends nmos2v$$40
258
259 * ++++++++++++++++++++++++++++++++++++++++++++++++++++++++ *
260 * Sub cell: nmos2v$$41                                     *
261 * ++++++++++++++++++++++++++++++++++++++++++++++++++++++++ *
262 .subckt nmos2v$$41 1
263 ** N=7 EP=1 FDC=6
264 M0 1 1 1 1 g45n2svt L=6e-07 W=4e-07 AD=8e-14 AS=8e-14 PD=1.2e
    -06 PS=1.2e-06 fw=4e-07 sa=2e-06 sb=2e-06 sca=5.61926 scb
    =0.00306339 scc=3.82378e-05 $X=0 $Y=0 $dt=4
265 M1 1 1 1 1 g45n2svt L=6e-07 W=4e-07 AD=8e-14 AS=8e-14 PD=1.2e
    -06 PS=1.2e-06 fw=4e-07 sa=2e-06 sb=2e-06 sca=5.61926 scb
    =0.00306339 scc=3.82378e-05 $X=1600 $Y=0 $dt=4
```

```
266 M2 1 1 1 1 g45n2svt L=6e-07 W=4e-07 AD=8e-14 AS=8e-14 PD=1.2e
    -06 PS=1.2e-06 fw=4e-07 sa=2e-06 sb=2e-06 sca=5.61926 scb
    =0.00306339 scc=3.82378e-05 $X=3200 $Y=0 $dt=4
267 M3 1 1 1 1 g45n2svt L=6e-07 W=4e-07 AD=8e-14 AS=8e-14 PD=1.2e
    -06 PS=1.2e-06 fw=4e-07 sa=2e-06 sb=1.75e-06 sca=5.61926
    scb=0.00306339 scc=3.82378e-05 $X=4800 $Y=0 $dt=4
268 M4 1 1 1 1 g45n2svt L=6e-07 W=4e-07 AD=8e-14 AS=8e-14 PD=1.2e
    -06 PS=1.2e-06 fw=4e-07 sa=2e-06 sb=9.5e-07 sca=5.61926 scb
    =0.00306339 scc=3.82378e-05 $X=6400 $Y=0 $dt=4
269 M5 1 1 1 1 g45n2svt L=6e-07 W=4e-07 AD=6e-14 AS=8e-14 PD=1.1e
    -06 PS=1.2e-06 fw=4e-07 sa=2e-06 sb=1.5e-07 sca=5.61926 scb
    =0.00306339 scc=3.82378e-05 $X=8000 $Y=0 $dt=4
270 .ends nmos2v$$41
271
272 * ++++++++++++++++++++++++++++++++++++++++++++++++++++++++ *
273 * Sub cell: nmos2v$$42                                     *
274 * ++++++++++++++++++++++++++++++++++++++++++++++++++++++++ *
275 .subckt nmos2v$$42 1
276 ** N=13 EP=1 FDC=12
277 M0 1 1 1 1 g45n2svt L=6e-07 W=4e-07 AD=8e-14 AS=6e-14 PD=1.2e
    -06 PS=1.1e-06 fw=4e-07 sa=1.5e-07 sb=2e-06 sca=2.67857 scb
    =4.09292e-05 scc=9.01501e-10 $X=0 $Y=0 $dt=4
278 M1 1 1 1 1 g45n2svt L=6e-07 W=4e-07 AD=8e-14 AS=8e-14 PD=1.2e
    -06 PS=1.2e-06 fw=4e-07 sa=9.5e-07 sb=2e-06 sca=2.67857 scb
    =4.09292e-05 scc=9.01501e-10 $X=1600 $Y=0 $dt=4
```

```
279 M2 1 1 1 1 g45n2svt L=6e-07 W=4e-07 AD=8e-14 AS=8e-14 PD=1.2e
    -06 PS=1.2e-06 fw=4e-07 sa=1.75e-06 sb=2e-06 sca=2.67857
    scb=4.09292e-05 scc=9.01501e-10 $X=3200 $Y=0 $dt=4
280 M3 1 1 1 1 g45n2svt L=6e-07 W=4e-07 AD=8e-14 AS=8e-14 PD=1.2e
    -06 PS=1.2e-06 fw=4e-07 sa=2e-06 sb=2e-06 sca=2.67857 scb
    =4.09292e-05 scc=9.01501e-10 $X=4800 $Y=0 $dt=4
281 M4 1 1 1 1 g45n2svt L=6e-07 W=4e-07 AD=8e-14 AS=8e-14 PD=1.2e
    -06 PS=1.2e-06 fw=4e-07 sa=2e-06 sb=2e-06 sca=2.67857 scb
    =4.09292e-05 scc=9.01501e-10 $X=6400 $Y=0 $dt=4
282 M5 1 1 1 1 g45n2svt L=6e-07 W=4e-07 AD=8e-14 AS=8e-14 PD=1.2e
    -06 PS=1.2e-06 fw=4e-07 sa=2e-06 sb=2e-06 sca=2.67857 scb
    =4.09292e-05 scc=9.01501e-10 $X=8000 $Y=0 $dt=4
283 M6 1 1 1 1 g45n2svt L=6e-07 W=4e-07 AD=8e-14 AS=8e-14 PD=1.2e
    -06 PS=1.2e-06 fw=4e-07 sa=2e-06 sb=2e-06 sca=2.67857 scb
    =4.09292e-05 scc=9.01501e-10 $X=9600 $Y=0 $dt=4
284 M7 1 1 1 1 g45n2svt L=6e-07 W=4e-07 AD=8e-14 AS=8e-14 PD=1.2e
    -06 PS=1.2e-06 fw=4e-07 sa=2e-06 sb=2e-06 sca=2.67857 scb
    =4.09292e-05 scc=9.01501e-10 $X=11200 $Y=0 $dt=4
285 M8 1 1 1 1 g45n2svt L=6e-07 W=4e-07 AD=8e-14 AS=8e-14 PD=1.2e
    -06 PS=1.2e-06 fw=4e-07 sa=2e-06 sb=2e-06 sca=2.67857 scb
    =4.09292e-05 scc=9.01501e-10 $X=12800 $Y=0 $dt=4
286 M9 1 1 1 1 g45n2svt L=6e-07 W=4e-07 AD=8e-14 AS=8e-14 PD=1.2e
    -06 PS=1.2e-06 fw=4e-07 sa=2e-06 sb=2e-06 sca=2.67857 scb
    =4.09292e-05 scc=9.01501e-10 $X=14400 $Y=0 $dt=4
```

```
287 M10 1 1 1 1 g45n2svt L=6e-07 W=4e-07 AD=8e-14 AS=8e-14 PD=1.2e
    -06 PS=1.2e-06 fw=4e-07 sa=2e-06 sb=2e-06 sca=2.67857 scb
    =4.09292e-05 scc=9.01501e-10 $X=16000 $Y=0 $dt=4
288 M11 1 1 1 1 g45n2svt L=6e-07 W=4e-07 AD=8e-14 AS=8e-14 PD=1.2e
    -06 PS=1.2e-06 fw=4e-07 sa=2e-06 sb=2e-06 sca=2.67857 scb
    =4.09292e-05 scc=9.01501e-10 $X=17600 $Y=0 $dt=4
289 .ends nmos2v$$42
290
291 * ++++++++++++++++++++++++++++++++++++++++++++++++++++++++ *
292 * Sub cell: nmos2v$$43                                     *
293 * ++++++++++++++++++++++++++++++++++++++++++++++++++++++++ *
294 .subckt nmos2v$$43 1 2 3
295 ** N=3 EP=3 FDC=4
296 M0 1 2 3 1 g45n2svt L=6e-07 W=4e-07 AD=8e-14 AS=8e-14 PD=1.2e
    -06 PS=1.2e-06 fw=4e-07 sa=2e-06 sb=2e-06 sca=2.67857 scb
    =4.09292e-05 scc=9.01501e-10 $X=0 $Y=0 $dt=4
297 M1 3 2 1 1 g45n2svt L=6e-07 W=4e-07 AD=8e-14 AS=8e-14 PD=1.2e
    -06 PS=1.2e-06 fw=4e-07 sa=2e-06 sb=1.75e-06 sca=2.67857
    scb=4.09292e-05 scc=9.01501e-10 $X=1600 $Y=0 $dt=4
298 M2 1 2 3 1 g45n2svt L=6e-07 W=4e-07 AD=8e-14 AS=8e-14 PD=1.2e
    -06 PS=1.2e-06 fw=4e-07 sa=2e-06 sb=9.5e-07 sca=2.67857 scb
    =4.09292e-05 scc=9.01501e-10 $X=3200 $Y=0 $dt=4
299 M3 3 2 1 1 g45n2svt L=6e-07 W=4e-07 AD=6e-14 AS=8e-14 PD=1.1e
    -06 PS=1.2e-06 fw=4e-07 sa=2e-06 sb=1.5e-07 sca=2.67857 scb
    =4.09292e-05 scc=9.01501e-10 $X=4800 $Y=0 $dt=4
```

```
.ends nmos2v$$43

* ++++++++++++++++++++++++++++++++++++++++++++++++++++++++ *
* Sub cell: mimcap$$44                                     *
* ++++++++++++++++++++++++++++++++++++++++++++++++++++++++ *
.subckt mimcap$$44 1 2 3
** N=3 EP=3 FDC=1
C0 1 2 2.24003e-21 L=5.6e-06 W=5.6e-06 area=3.136e-11 pj=2.24e
    -05 $[g45cmim] $SUB=3 $X=0 $Y=0 $dt=55
.ends mimcap$$44

* ++++++++++++++++++++++++++++++++++++++++++++++++++++++++ *
* Sub cell: DS_VGA_OPAMP                                   *
* ++++++++++++++++++++++++++++++++++++++++++++++++++++++++ *
.subckt DS_VGA_OPAMP VINM VINP VSS VDD VOUT IREF
** N=51 EP=6 FDC=187
X169 VDD pmos2v$$27 $T=4470 10480 0 0 $X=3690 $Y=10000
X170 10 VINP 7 VDD pmos2v$$28 $T=20490 5400 0 0 $X=19750 $Y
    =4920
X171 VDD pmos2v$$29 $T=4490 7160 0 0 $X=3710 $Y=6680
X172 VDD 9 VOUT pmos2v$$30 $T=26870 12240 0 0 $X=26130 $Y
    =11760
X173 11 9 VSS nmos2v$$31 $T=30070 1880 0 0 $X=29570 $Y=1520
X174 VSS nmos2v$$32 $T=4470 360 0 0 $X=3810 $Y=0
X175 8 9 VDD pmos2v$$33 $T=26870 10480 0 0 $X=26250 $Y=10000
```

```
322 X178 VDD 8 8 pmos2v$$35 $T=17270 10480 0 0 $X=16530 $Y=10000
323 X179 VDD IREF 10 pmos2v$$35 $T=20490 7160 0 0 $X=19750 $Y=6680
324 X180 VDD IREF 10 pmos2v$$35 $T=20490 8840 0 0 $X=19750 $Y=8360
325 X181 VDD IREF pmos2v$$36 $T=10890 7160 0 0 $X=10150 $Y=6680
326 X182 VDD pmos2v$$37 $T=4470 12240 0 0 $X=3690 $Y=11760
327 X183 VDD pmos2v$$38 $T=30090 7160 0 0 $X=29470 $Y=6680
328 X184 VDD pmos2v$$38 $T=30090 8840 0 0 $X=29470 $Y=8360
329 X185 11 7 VSS nmos2v$$39 $T=20470 3400 0 0 $X=19970 $Y=3040
330 X186 VSS nmos2v$$40 $T=4470 3400 0 0 $X=3810 $Y=3040
331 X187 VSS nmos2v$$41 $T=26870 3400 0 0 $X=26370 $Y=3040
332 X188 VSS nmos2v$$42 $T=4470 1880 0 0 $X=3810 $Y=1520
333 X189 VSS 7 VOUT nmos2v$$43 $T=30070 360 0 0 $X=29450 $Y=0
334 X190 7 VOUT VSS mimcap$$44 $T=400 16970 0 0 $X=0 $Y=16570
335 X191 7 VOUT VSS mimcap$$44 $T=400 31470 0 0 $X=0 $Y=31070
336 X192 7 VOUT VSS mimcap$$44 $T=400 45970 0 0 $X=0 $Y=45570
337 X193 7 VOUT VSS mimcap$$44 $T=400 60470 0 0 $X=0 $Y=60070
338 X194 7 VOUT VSS mimcap$$44 $T=400 74970 0 0 $X=0 $Y=74570
339 X195 7 VOUT VSS mimcap$$44 $T=400 89470 0 0 $X=0 $Y=89070
340 X196 7 VOUT VSS mimcap$$44 $T=400 103970 0 0 $X=0 $Y=103570
341 X197 7 VOUT VSS mimcap$$44 $T=400 118470 0 0 $X=0 $Y=118070
342 X198 7 VOUT VSS mimcap$$44 $T=400 132970 0 0 $X=0 $Y=132570
343 X199 7 VOUT VSS mimcap$$44 $T=14900 16970 0 0 $X=14500 $Y
    =16570
344 X200 7 VOUT VSS mimcap$$44 $T=14900 31470 0 0 $X=14500 $Y
    =31070
```

```
345 X201 7 VOUT VSS mimcap$$44 $T=14900 45970 0 0 $X=14500 $Y
    =45570
346 X202 7 VOUT VSS mimcap$$44 $T=14900 60470 0 0 $X=14500 $Y
    =60070
347 X203 7 VOUT VSS mimcap$$44 $T=14900 74970 0 0 $X=14500 $Y
    =74570
348 X204 7 VOUT VSS mimcap$$44 $T=14900 89470 0 0 $X=14500 $Y
    =89070
349 X205 7 VOUT VSS mimcap$$44 $T=14900 103970 0 0 $X=14500 $Y
    =103570
350 X206 7 VOUT VSS mimcap$$44 $T=14900 118470 0 0 $X=14500 $Y
    =118070
351 X207 7 VOUT VSS mimcap$$44 $T=14900 132970 0 0 $X=14500 $Y
    =132570
352 X208 7 VOUT VSS mimcap$$44 $T=29400 16970 0 0 $X=29000 $Y
    =16570
353 X209 7 VOUT VSS mimcap$$44 $T=29400 31470 0 0 $X=29000 $Y
    =31070
354 X210 7 VOUT VSS mimcap$$44 $T=29400 45970 0 0 $X=29000 $Y
    =45570
355 X211 7 VOUT VSS mimcap$$44 $T=29400 60470 0 0 $X=29000 $Y
    =60070
356 X212 7 VOUT VSS mimcap$$44 $T=29400 74970 0 0 $X=29000 $Y
    =74570
```

```
357 X213 7 VOUT VSS mimcap$$44 $T=29400 89470 0 0 $X=29000 $Y
    =89070
358 X214 7 VOUT VSS mimcap$$44 $T=29400 103970 0 0 $X=29000 $Y
    =103570
359 X215 7 VOUT VSS mimcap$$44 $T=29400 118470 0 0 $X=29000 $Y
    =118070
360 X216 7 VOUT VSS mimcap$$44 $T=29400 132970 0 0 $X=29000 $Y
    =132570
361 M0 VSS 11 11 VSS g45n2svt L=6e-07 W=4e-07 AD=8e-14 AS=8e-14 PD
    =1.2e-06 PS=1.2e-06 fw=4e-07 sa=2e-06 sb=2e-06 sca=5.61926
    scb=0.00306339 scc=3.82378e-05 $X=14070 $Y=3400 $dt=4
362 M1 11 11 VSS VSS g45n2svt L=6e-07 W=4e-07 AD=8e-14 AS=8e-14 PD
    =1.2e-06 PS=1.2e-06 fw=4e-07 sa=2e-06 sb=2e-06 sca=5.61926
    scb=0.00306339 scc=3.82378e-05 $X=15670 $Y=3400 $dt=4
363 M2 VSS 11 11 VSS g45n2svt L=6e-07 W=4e-07 AD=8e-14 AS=8e-14 PD
    =1.2e-06 PS=1.2e-06 fw=4e-07 sa=2e-06 sb=2e-06 sca=5.61926
    scb=0.00306339 scc=3.82378e-05 $X=17270 $Y=3400 $dt=4
364 M3 11 11 VSS VSS g45n2svt L=6e-07 W=4e-07 AD=8e-14 AS=8e-14 PD
    =1.2e-06 PS=1.2e-06 fw=4e-07 sa=2e-06 sb=2e-06 sca=5.61926
    scb=0.00306339 scc=3.82378e-05 $X=18870 $Y=3400 $dt=4
365 M4 VSS 7 8 VSS g45n2svt L=6e-07 W=4e-07 AD=8e-14 AS=8e-14 PD
    =1.2e-06 PS=1.2e-06 fw=4e-07 sa=2e-06 sb=2e-06 sca=2.67857
    scb=4.09292e-05 scc=9.01501e-10 $X=23670 $Y=1880 $dt=4
366 M5 8 7 VSS VSS g45n2svt L=6e-07 W=4e-07 AD=8e-14 AS=8e-14 PD
    =1.2e-06 PS=1.2e-06 fw=4e-07 sa=2e-06 sb=2e-06 sca=2.67857
```

```
scb=4.09292e-05 scc=9.01501e-10 $X=25270 $Y=1880 $dt=4
367 M6 VSS 7 8 VSS g45n2svt L=6e-07 W=4e-07 AD=8e-14 AS=8e-14 PD
=1.2e-06 PS=1.2e-06 fw=4e-07 sa=2e-06 sb=2e-06 sca=2.67857
scb=4.09292e-05 scc=9.01501e-10 $X=26870 $Y=1880 $dt=4
368 M7 8 7 VSS VSS g45n2svt L=6e-07 W=4e-07 AD=8e-14 AS=8e-14 PD
=1.2e-06 PS=1.2e-06 fw=4e-07 sa=2e-06 sb=2e-06 sca=2.67857
scb=4.09292e-05 scc=9.01501e-10 $X=28470 $Y=1880 $dt=4
369 M8 11 VINM 10 VDD g45p2svt L=6e-07 W=4e-07 AD=8e-14 AS=6e-14
PD=1.2e-06 PS=1.1e-06 fw=4e-07 sa=1.5e-07 sb=2e-06 sca
=8.77873 scb=0.00748395 scc=0.000298102 $X=4490 $Y=5400 $dt
=11
370 M9 VDD VDD VDD VDD g45p2svt L=6e-07 W=4e-07 AD=8e-14 AS=6e-14
PD=1.2e-06 PS=1.1e-06 fw=4e-07 sa=1.5e-07 sb=2e-06 sca
=2.98259 scb=9.24817e-05 scc=1.23329e-08 $X=4490 $Y=8840
$dt=11
371 M10 10 VINM 11 VDD g45p2svt L=6e-07 W=4e-07 AD=8e-14 AS=8e-14
PD=1.2e-06 PS=1.2e-06 fw=4e-07 sa=9.5e-07 sb=2e-06 sca
=8.4747 scb=0.00743239 scc=0.000298091 $X=6090 $Y=5400 $dt
=11
372 M11 VDD VDD VDD VDD g45p2svt L=6e-07 W=4e-07 AD=8e-14 AS=8e-14
PD=1.2e-06 PS=1.2e-06 fw=4e-07 sa=9.5e-07 sb=2e-06 sca
=2.67857 scb=4.09292e-05 scc=9.01501e-10 $X=6090 $Y=8840
$dt=11
373 M12 11 VINM 10 VDD g45p2svt L=6e-07 W=4e-07 AD=8e-14 AS=8e-14
PD=1.2e-06 PS=1.2e-06 fw=4e-07 sa=1.75e-06 sb=2e-06 sca
```

```
=8.4747 scb=0.00743239 scc=0.000298091 $X=7690 $Y=5400 $dt
=11
374 M13 VDD VDD VDD VDD g45p2svt L=6e-07 W=4e-07 AD=8e-14 AS=8e-14
PD=1.2e-06 PS=1.2e-06 fw=4e-07 sa=1.75e-06 sb=2e-06 sca
=2.67857 scb=4.09292e-05 scc=9.01501e-10 $X=7690 $Y=8840
$dt=11
375 M14 10 VINM 11 VDD g45p2svt L=6e-07 W=4e-07 AD=8e-14 AS=8e-14
PD=1.2e-06 PS=1.2e-06 fw=4e-07 sa=2e-06 sb=2e-06 sca=8.4747
scb=0.00743239 scc=0.000298091 $X=9290 $Y=5400 $dt=11
376 M15 VDD VDD VDD VDD g45p2svt L=6e-07 W=4e-07 AD=8e-14 AS=8e-14
PD=1.2e-06 PS=1.2e-06 fw=4e-07 sa=2e-06 sb=2e-06 sca
=2.67857 scb=4.09292e-05 scc=9.01501e-10 $X=9290 $Y=8840
$dt=11
377 M16 11 VINM 10 VDD g45p2svt L=6e-07 W=4e-07 AD=8e-14 AS=8e-14
PD=1.2e-06 PS=1.2e-06 fw=4e-07 sa=2e-06 sb=2e-06 sca=8.4747
scb=0.00743239 scc=0.000298091 $X=10890 $Y=5400 $dt=11
378 M17 VDD VDD VDD VDD g45p2svt L=6e-07 W=4e-07 AD=8e-14 AS=8e-14
PD=1.2e-06 PS=1.2e-06 fw=4e-07 sa=2e-06 sb=2e-06 sca
=2.67857 scb=4.09292e-05 scc=9.01501e-10 $X=10890 $Y=8840
$dt=11
379 M18 10 VINM 11 VDD g45p2svt L=6e-07 W=4e-07 AD=8e-14 AS=8e-14
PD=1.2e-06 PS=1.2e-06 fw=4e-07 sa=2e-06 sb=2e-06 sca=8.4747
scb=0.00743239 scc=0.000298091 $X=12490 $Y=5400 $dt=11
380 M19 VDD VDD VDD VDD g45p2svt L=6e-07 W=4e-07 AD=8e-14 AS=8e-14
PD=1.2e-06 PS=1.2e-06 fw=4e-07 sa=2e-06 sb=2e-06 sca
```

```
=2.67857 scb=4.09292e-05 scc=9.01501e-10 $X=12490 $Y=8840
$dt=11
381 M20 11 VINM 10 VDD g45p2svt L=6e-07 W=4e-07 AD=8e-14 AS=8e-14
PD=1.2e-06 PS=1.2e-06 fw=4e-07 sa=2e-06 sb=2e-06 sca=8.4747
scb=0.00743239 scc=0.000298091 $X=14090 $Y=5400 $dt=11
382 M21 VDD VDD VDD VDD g45p2svt L=6e-07 W=4e-07 AD=8e-14 AS=8e-14
PD=1.2e-06 PS=1.2e-06 fw=4e-07 sa=2e-06 sb=2e-06 sca
=2.67857 scb=4.09292e-05 scc=9.01501e-10 $X=14090 $Y=8840
$dt=11
383 M22 10 VINM 11 VDD g45p2svt L=6e-07 W=4e-07 AD=8e-14 AS=8e-14
PD=1.2e-06 PS=1.2e-06 fw=4e-07 sa=2e-06 sb=2e-06 sca=8.4747
scb=0.00743239 scc=0.000298091 $X=15690 $Y=5400 $dt=11
384 M23 VDD VDD VDD VDD g45p2svt L=6e-07 W=4e-07 AD=8e-14 AS=8e-14
PD=1.2e-06 PS=1.2e-06 fw=4e-07 sa=2e-06 sb=2e-06 sca
=2.67857 scb=4.09292e-05 scc=9.01501e-10 $X=15690 $Y=8840
$dt=11
385 M24 11 VINM 10 VDD g45p2svt L=6e-07 W=4e-07 AD=8e-14 AS=8e-14
PD=1.2e-06 PS=1.2e-06 fw=4e-07 sa=2e-06 sb=2e-06 sca=8.4747
scb=0.00743239 scc=0.000298091 $X=17290 $Y=5400 $dt=11
386 M25 VDD VDD VDD VDD g45p2svt L=6e-07 W=4e-07 AD=8e-14 AS=8e-14
PD=1.2e-06 PS=1.2e-06 fw=4e-07 sa=2e-06 sb=2e-06 sca
=2.67857 scb=4.09292e-05 scc=9.01501e-10 $X=17290 $Y=8840
$dt=11
387 M26 10 VINM 11 VDD g45p2svt L=6e-07 W=4e-07 AD=8e-14 AS=8e-14
PD=1.2e-06 PS=1.2e-06 fw=4e-07 sa=2e-06 sb=2e-06 sca=8.4747
```

```
      scb=0.00743239 scc=0.000298091 $X=18890 $Y=5400 $dt=11
388 M27 VDD VDD VDD VDD g45p2svt L=6e-07 W=4e-07 AD=8e-14 AS=8e-14
      PD=1.2e-06 PS=1.2e-06 fw=4e-07 sa=2e-06 sb=2e-06 sca
      =2.67857 scb=4.09292e-05 scc=9.01501e-10 $X=18890 $Y=8840
      $dt=11
389 .ends DS_VGA_OPAMP
390
391 * ++++++++++++++++++++++++++++++++++++++++++++++++++++++++ *
392 * Sub cell: resnsppoly$$45                                 *
393 * ++++++++++++++++++++++++++++++++++++++++++++++++++++++++ *
394 .subckt resnsppoly$$45 1 2 3
395 ** N=3 EP=3 FDC=1
396 R0 2 1 1021.43 L=4.4e-07 W=2.8e-07 effW=2.8e-07 effL=4.4e-07
      segW=2.8e-07 segL=4.4e-07 $[g45rnspp] $SUB=3 $X=0 $Y=0 $dt
      =35
397 .ends resnsppoly$$45
398
399 * ++++++++++++++++++++++++++++++++++++++++++++++++++++++++ *
400 * Sub cell: pmos2v$$54                                     *
401 * ++++++++++++++++++++++++++++++++++++++++++++++++++++++++ *
402 .subckt pmos2v$$54 1 2 3
403 ** N=4 EP=3 FDC=1
404 M0 1 3 2 1 g45p2svt L=1.8e-07 W=3.2e-07 AD=4.8e-14 AS=4.8e-14
      PD=9.4e-07 PS=9.4e-07 fw=3.2e-07 sa=1.5e-07 sb=1.5e-07 sca
      =14.2397 scb=0.0134273 scc=0.000419873 $X=0 $Y=0 $dt=11
```

```
.ends pmos2v$$54

* ++++++++++++++++++++++++++++++++++++++++++++++++++++++++ *
* Sub cell: nmos2v$$55                                     *
* ++++++++++++++++++++++++++++++++++++++++++++++++++++++++ *
.subckt nmos2v$$55 1 2 3
** N=3 EP=3 FDC=1
M0 1 3 2 1 g45n2svt L=1.8e-07 W=3.2e-07 AD=4.8e-14 AS=4.8e-14
    PD=9.4e-07 PS=9.4e-07 fw=3.2e-07 sa=1.5e-07 sb=1.5e-07 sca
    =7.57282 scb=0.00541262 scc=0.000113799 $X=0 $Y=0 $dt=4
.ends nmos2v$$55

* ++++++++++++++++++++++++++++++++++++++++++++++++++++++++ *
* Sub cell: DS_INVX1                                       *
* ++++++++++++++++++++++++++++++++++++++++++++++++++++++++ *
.subckt DS_INVX1 VDD VSS A Y
** N=4 EP=4 FDC=2
X1 VDD Y A pmos2v$$54 $T=1440 2100 0 0 $X=660 $Y=1620
X2 VSS Y A nmos2v$$55 $T=1440 360 0 0 $X=780 $Y=0
.ends DS_INVX1

* ++++++++++++++++++++++++++++++++++++++++++++++++++++++++ *
* Sub cell: pmos2v$$56                                     *
* ++++++++++++++++++++++++++++++++++++++++++++++++++++++++ *
.subckt pmos2v$$56 1 2 3 5
```

```
** N=5 EP=4 FDC=1
M0 1 3 2 5 g45p2svt L=1.8e-07 W=2e-06 AD=3e-13 AS=3e-13 PD=4.3
    e-06 PS=4.3e-06 fw=2e-06 sa=1.5e-07 sb=1.5e-07 sca=11.1903
    scb=0.0100744 scc=0.000155967 $X=0 $Y=0 $dt=11
.ends pmos2v$$56

* ++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++ *
* Sub cell: nmos2v$$57                                          *
* ++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++ *
.subckt nmos2v$$57 1 2 3 4
** N=4 EP=4 FDC=1
M0 1 3 2 4 g45n2svt L=1.8e-07 W=2e-06 AD=3e-13 AS=3e-13 PD=4.3
    e-06 PS=4.3e-06 fw=2e-06 sa=1.5e-07 sb=1.5e-07 sca=2.36608
    scb=5.00472e-05 scc=1.28342e-09 $X=0 $Y=0 $dt=4
.ends nmos2v$$57

* ++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++ *
* Sub cell: DS_VGA_SWITCH                                       *
* ++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++ *
.subckt DS_VGA_SWITCH vin vout vin_n VDD VSS
** N=6 EP=5 FDC=4
X0 VDD VSS vin_n 6 DS_INVX1 $T=0 4720 0 0 $X=0 $Y=4720
X1 vin vout 6 VDD pmos2v$$56 $T=1440 8420 0 0 $X=660 $Y=7940
X2 vout vin vin_n VSS nmos2v$$57 $T=1800 360 1 180 $X=780 $Y=0
.ends DS_VGA_SWITCH
```

```
449
450 * ++++++++++++++++++++++++++++++++++++++++++++++++++++++++ *
451 * Sub cell: resnsppoly$$58                                  *
452 * ++++++++++++++++++++++++++++++++++++++++++++++++++++++++ *
453 .subckt resnsppoly$$58 1 2 3
454 ** N=52 EP=3 FDC=50
455 R0 1 52 4642.86 L=1e-05 W=1.4e-06 effW=1.4e-06 effL=1e-05 segW
    =1.4e-06 segL=1e-05 $[g45rnspp] $SUB=3 $X=0 $Y=0 $dt=35
456 R1 51 52 4642.86 L=1e-05 W=1.4e-06 effW=1.4e-06 effL=1e-05
    segW=1.4e-06 segL=1e-05 $[g45rnspp] $SUB=3 $X=3400 $Y=0 $dt
    =35
457 R2 51 50 4642.86 L=1e-05 W=1.4e-06 effW=1.4e-06 effL=1e-05
    segW=1.4e-06 segL=1e-05 $[g45rnspp] $SUB=3 $X=6800 $Y=0 $dt
    =35
458 R3 49 50 4642.86 L=1e-05 W=1.4e-06 effW=1.4e-06 effL=1e-05
    segW=1.4e-06 segL=1e-05 $[g45rnspp] $SUB=3 $X=10200 $Y=0
    $dt=35
459 R4 49 48 4642.86 L=1e-05 W=1.4e-06 effW=1.4e-06 effL=1e-05
    segW=1.4e-06 segL=1e-05 $[g45rnspp] $SUB=3 $X=13600 $Y=0
    $dt=35
460 R5 47 48 4642.86 L=1e-05 W=1.4e-06 effW=1.4e-06 effL=1e-05
    segW=1.4e-06 segL=1e-05 $[g45rnspp] $SUB=3 $X=17000 $Y=0
    $dt=35
461 R6 47 46 4642.86 L=1e-05 W=1.4e-06 effW=1.4e-06 effL=1e-05
    segW=1.4e-06 segL=1e-05 $[g45rnspp] $SUB=3 $X=20400 $Y=0
```

```
$dt=35
462 R7 45 46 4642.86 L=1e-05 W=1.4e-06 effW=1.4e-06 effL=1e-05
    segW=1.4e-06 segL=1e-05 $[g45rnspp] $SUB=3 $X=23800 $Y=0
    $dt=35
463 R8 45 44 4642.86 L=1e-05 W=1.4e-06 effW=1.4e-06 effL=1e-05
    segW=1.4e-06 segL=1e-05 $[g45rnspp] $SUB=3 $X=27200 $Y=0
    $dt=35
464 R9 43 44 4642.86 L=1e-05 W=1.4e-06 effW=1.4e-06 effL=1e-05
    segW=1.4e-06 segL=1e-05 $[g45rnspp] $SUB=3 $X=30600 $Y=0
    $dt=35
465 R10 43 42 4642.86 L=1e-05 W=1.4e-06 effW=1.4e-06 effL=1e-05
    segW=1.4e-06 segL=1e-05 $[g45rnspp] $SUB=3 $X=34000 $Y=0
    $dt=35
466 R11 41 42 4642.86 L=1e-05 W=1.4e-06 effW=1.4e-06 effL=1e-05
    segW=1.4e-06 segL=1e-05 $[g45rnspp] $SUB=3 $X=37400 $Y=0
    $dt=35
467 R12 41 40 4642.86 L=1e-05 W=1.4e-06 effW=1.4e-06 effL=1e-05
    segW=1.4e-06 segL=1e-05 $[g45rnspp] $SUB=3 $X=40800 $Y=0
    $dt=35
468 R13 39 40 4642.86 L=1e-05 W=1.4e-06 effW=1.4e-06 effL=1e-05
    segW=1.4e-06 segL=1e-05 $[g45rnspp] $SUB=3 $X=44200 $Y=0
    $dt=35
469 R14 39 38 4642.86 L=1e-05 W=1.4e-06 effW=1.4e-06 effL=1e-05
    segW=1.4e-06 segL=1e-05 $[g45rnspp] $SUB=3 $X=47600 $Y=0
    $dt=35
```

```
470 R15 37 38 4642.86 L=1e-05 W=1.4e-06 effW=1.4e-06 effL=1e-05
    segW=1.4e-06 segL=1e-05 $[g45rnspp] $SUB=3 $X=51000 $Y=0
    $dt=35
471 R16 37 36 4642.86 L=1e-05 W=1.4e-06 effW=1.4e-06 effL=1e-05
    segW=1.4e-06 segL=1e-05 $[g45rnspp] $SUB=3 $X=54400 $Y=0
    $dt=35
472 R17 35 36 4642.86 L=1e-05 W=1.4e-06 effW=1.4e-06 effL=1e-05
    segW=1.4e-06 segL=1e-05 $[g45rnspp] $SUB=3 $X=57800 $Y=0
    $dt=35
473 R18 35 34 4642.86 L=1e-05 W=1.4e-06 effW=1.4e-06 effL=1e-05
    segW=1.4e-06 segL=1e-05 $[g45rnspp] $SUB=3 $X=61200 $Y=0
    $dt=35
474 R19 33 34 4642.86 L=1e-05 W=1.4e-06 effW=1.4e-06 effL=1e-05
    segW=1.4e-06 segL=1e-05 $[g45rnspp] $SUB=3 $X=64600 $Y=0
    $dt=35
475 R20 33 32 4642.86 L=1e-05 W=1.4e-06 effW=1.4e-06 effL=1e-05
    segW=1.4e-06 segL=1e-05 $[g45rnspp] $SUB=3 $X=68000 $Y=0
    $dt=35
476 R21 31 32 4642.86 L=1e-05 W=1.4e-06 effW=1.4e-06 effL=1e-05
    segW=1.4e-06 segL=1e-05 $[g45rnspp] $SUB=3 $X=71400 $Y=0
    $dt=35
477 R22 31 30 4642.86 L=1e-05 W=1.4e-06 effW=1.4e-06 effL=1e-05
    segW=1.4e-06 segL=1e-05 $[g45rnspp] $SUB=3 $X=74800 $Y=0
    $dt=35
```

```
478 R23 29 30 4642.86 L=1e-05 W=1.4e-06 effW=1.4e-06 effL=1e-05
    segW=1.4e-06 segL=1e-05 $[g45rnspp] $SUB=3 $X=78200 $Y=0
    $dt=35
479 R24 29 28 4642.86 L=1e-05 W=1.4e-06 effW=1.4e-06 effL=1e-05
    segW=1.4e-06 segL=1e-05 $[g45rnspp] $SUB=3 $X=81600 $Y=0
    $dt=35
480 R25 27 28 4642.86 L=1e-05 W=1.4e-06 effW=1.4e-06 effL=1e-05
    segW=1.4e-06 segL=1e-05 $[g45rnspp] $SUB=3 $X=85000 $Y=0
    $dt=35
481 R26 27 26 4642.86 L=1e-05 W=1.4e-06 effW=1.4e-06 effL=1e-05
    segW=1.4e-06 segL=1e-05 $[g45rnspp] $SUB=3 $X=88400 $Y=0
    $dt=35
482 R27 25 26 4642.86 L=1e-05 W=1.4e-06 effW=1.4e-06 effL=1e-05
    segW=1.4e-06 segL=1e-05 $[g45rnspp] $SUB=3 $X=91800 $Y=0
    $dt=35
483 R28 25 24 4642.86 L=1e-05 W=1.4e-06 effW=1.4e-06 effL=1e-05
    segW=1.4e-06 segL=1e-05 $[g45rnspp] $SUB=3 $X=95200 $Y=0
    $dt=35
484 R29 23 24 4642.86 L=1e-05 W=1.4e-06 effW=1.4e-06 effL=1e-05
    segW=1.4e-06 segL=1e-05 $[g45rnspp] $SUB=3 $X=98600 $Y=0
    $dt=35
485 R30 23 22 4642.86 L=1e-05 W=1.4e-06 effW=1.4e-06 effL=1e-05
    segW=1.4e-06 segL=1e-05 $[g45rnspp] $SUB=3 $X=102000 $Y=0
    $dt=35
```

```
486 R31 21 22 4642.86 L=1e-05 W=1.4e-06 effW=1.4e-06 effL=1e-05
    segW=1.4e-06 segL=1e-05 $[g45rnspp] $SUB=3 $X=105400 $Y=0
    $dt=35
487 R32 21 20 4642.86 L=1e-05 W=1.4e-06 effW=1.4e-06 effL=1e-05
    segW=1.4e-06 segL=1e-05 $[g45rnspp] $SUB=3 $X=108800 $Y=0
    $dt=35
488 R33 19 20 4642.86 L=1e-05 W=1.4e-06 effW=1.4e-06 effL=1e-05
    segW=1.4e-06 segL=1e-05 $[g45rnspp] $SUB=3 $X=112200 $Y=0
    $dt=35
489 R34 19 18 4642.86 L=1e-05 W=1.4e-06 effW=1.4e-06 effL=1e-05
    segW=1.4e-06 segL=1e-05 $[g45rnspp] $SUB=3 $X=115600 $Y=0
    $dt=35
490 R35 17 18 4642.86 L=1e-05 W=1.4e-06 effW=1.4e-06 effL=1e-05
    segW=1.4e-06 segL=1e-05 $[g45rnspp] $SUB=3 $X=119000 $Y=0
    $dt=35
491 R36 17 16 4642.86 L=1e-05 W=1.4e-06 effW=1.4e-06 effL=1e-05
    segW=1.4e-06 segL=1e-05 $[g45rnspp] $SUB=3 $X=122400 $Y=0
    $dt=35
492 R37 15 16 4642.86 L=1e-05 W=1.4e-06 effW=1.4e-06 effL=1e-05
    segW=1.4e-06 segL=1e-05 $[g45rnspp] $SUB=3 $X=125800 $Y=0
    $dt=35
493 R38 15 14 4642.86 L=1e-05 W=1.4e-06 effW=1.4e-06 effL=1e-05
    segW=1.4e-06 segL=1e-05 $[g45rnspp] $SUB=3 $X=129200 $Y=0
    $dt=35
```

```
494 R39 13 14 4642.86 L=1e-05 W=1.4e-06 effW=1.4e-06 effL=1e-05
    segW=1.4e-06 segL=1e-05 $[g45rnspp] $SUB=3 $X=132600 $Y=0
    $dt=35
495 R40 13 12 4642.86 L=1e-05 W=1.4e-06 effW=1.4e-06 effL=1e-05
    segW=1.4e-06 segL=1e-05 $[g45rnspp] $SUB=3 $X=136000 $Y=0
    $dt=35
496 R41 11 12 4642.86 L=1e-05 W=1.4e-06 effW=1.4e-06 effL=1e-05
    segW=1.4e-06 segL=1e-05 $[g45rnspp] $SUB=3 $X=139400 $Y=0
    $dt=35
497 R42 11 10 4642.86 L=1e-05 W=1.4e-06 effW=1.4e-06 effL=1e-05
    segW=1.4e-06 segL=1e-05 $[g45rnspp] $SUB=3 $X=142800 $Y=0
    $dt=35
498 R43 9 10 4642.86 L=1e-05 W=1.4e-06 effW=1.4e-06 effL=1e-05
    segW=1.4e-06 segL=1e-05 $[g45rnspp] $SUB=3 $X=146200 $Y=0
    $dt=35
499 R44 9 8 4642.86 L=1e-05 W=1.4e-06 effW=1.4e-06 effL=1e-05 segW
    =1.4e-06 segL=1e-05 $[g45rnspp] $SUB=3 $X=149600 $Y=0 $dt
    =35
500 R45 7 8 4642.86 L=1e-05 W=1.4e-06 effW=1.4e-06 effL=1e-05 segW
    =1.4e-06 segL=1e-05 $[g45rnspp] $SUB=3 $X=153000 $Y=0 $dt
    =35
501 R46 7 6 4642.86 L=1e-05 W=1.4e-06 effW=1.4e-06 effL=1e-05 segW
    =1.4e-06 segL=1e-05 $[g45rnspp] $SUB=3 $X=156400 $Y=0 $dt
    =35
```

```
502 R47 5 6 4642.86 L=1e-05 W=1.4e-06 effW=1.4e-06 effL=1e-05 segW
    =1.4e-06 segL=1e-05 $[g45rnspp] $SUB=3 $X=159800 $Y=0 $dt
    =35
503 R48 5 4 4642.86 L=1e-05 W=1.4e-06 effW=1.4e-06 effL=1e-05 segW
    =1.4e-06 segL=1e-05 $[g45rnspp] $SUB=3 $X=163200 $Y=0 $dt
    =35
504 R49 2 4 4642.86 L=1e-05 W=1.4e-06 effW=1.4e-06 effL=1e-05 segW
    =1.4e-06 segL=1e-05 $[g45rnspp] $SUB=3 $X=166600 $Y=0 $dt
    =35
505 .ends resnsppoly$$58
506
507 * ++++++++++++++++++++++++++++++++++++++++++++++++++++++++ *
508 * Sub cell: resnsppoly$$59                                 *
509 * ++++++++++++++++++++++++++++++++++++++++++++++++++++++++ *
510 .subckt resnsppoly$$59 1 2 3
511 ** N=27 EP=3 FDC=25
512 R0 1 27 4642.86 L=1e-05 W=1.4e-06 effW=1.4e-06 effL=1e-05 segW
    =1.4e-06 segL=1e-05 $[g45rnspp] $SUB=3 $X=0 $Y=0 $dt=35
513 R1 26 27 4642.86 L=1e-05 W=1.4e-06 effW=1.4e-06 effL=1e-05
    segW=1.4e-06 segL=1e-05 $[g45rnspp] $SUB=3 $X=3400 $Y=0 $dt
    =35
514 R2 26 25 4642.86 L=1e-05 W=1.4e-06 effW=1.4e-06 effL=1e-05
    segW=1.4e-06 segL=1e-05 $[g45rnspp] $SUB=3 $X=6800 $Y=0 $dt
    =35
```

```
515 R3 24 25 4642.86 L=1e-05 W=1.4e-06 effW=1.4e-06 effL=1e-05
    segW=1.4e-06 segL=1e-05 $[g45rnspp] $SUB=3 $X=10200 $Y=0
    $dt=35
516 R4 24 23 4642.86 L=1e-05 W=1.4e-06 effW=1.4e-06 effL=1e-05
    segW=1.4e-06 segL=1e-05 $[g45rnspp] $SUB=3 $X=13600 $Y=0
    $dt=35
517 R5 22 23 4642.86 L=1e-05 W=1.4e-06 effW=1.4e-06 effL=1e-05
    segW=1.4e-06 segL=1e-05 $[g45rnspp] $SUB=3 $X=17000 $Y=0
    $dt=35
518 R6 22 21 4642.86 L=1e-05 W=1.4e-06 effW=1.4e-06 effL=1e-05
    segW=1.4e-06 segL=1e-05 $[g45rnspp] $SUB=3 $X=20400 $Y=0
    $dt=35
519 R7 20 21 4642.86 L=1e-05 W=1.4e-06 effW=1.4e-06 effL=1e-05
    segW=1.4e-06 segL=1e-05 $[g45rnspp] $SUB=3 $X=23800 $Y=0
    $dt=35
520 R8 20 19 4642.86 L=1e-05 W=1.4e-06 effW=1.4e-06 effL=1e-05
    segW=1.4e-06 segL=1e-05 $[g45rnspp] $SUB=3 $X=27200 $Y=0
    $dt=35
521 R9 18 19 4642.86 L=1e-05 W=1.4e-06 effW=1.4e-06 effL=1e-05
    segW=1.4e-06 segL=1e-05 $[g45rnspp] $SUB=3 $X=30600 $Y=0
    $dt=35
522 R10 18 17 4642.86 L=1e-05 W=1.4e-06 effW=1.4e-06 effL=1e-05
    segW=1.4e-06 segL=1e-05 $[g45rnspp] $SUB=3 $X=34000 $Y=0
    $dt=35
```

```
523 R11 16 17 4642.86 L=1e-05 W=1.4e-06 effW=1.4e-06 effL=1e-05
    segW=1.4e-06 segL=1e-05 $[g45rnspp] $SUB=3 $X=37400 $Y=0
    $dt=35
524 R12 16 15 4642.86 L=1e-05 W=1.4e-06 effW=1.4e-06 effL=1e-05
    segW=1.4e-06 segL=1e-05 $[g45rnspp] $SUB=3 $X=40800 $Y=0
    $dt=35
525 R13 14 15 4642.86 L=1e-05 W=1.4e-06 effW=1.4e-06 effL=1e-05
    segW=1.4e-06 segL=1e-05 $[g45rnspp] $SUB=3 $X=44200 $Y=0
    $dt=35
526 R14 14 13 4642.86 L=1e-05 W=1.4e-06 effW=1.4e-06 effL=1e-05
    segW=1.4e-06 segL=1e-05 $[g45rnspp] $SUB=3 $X=47600 $Y=0
    $dt=35
527 R15 12 13 4642.86 L=1e-05 W=1.4e-06 effW=1.4e-06 effL=1e-05
    segW=1.4e-06 segL=1e-05 $[g45rnspp] $SUB=3 $X=51000 $Y=0
    $dt=35
528 R16 12 11 4642.86 L=1e-05 W=1.4e-06 effW=1.4e-06 effL=1e-05
    segW=1.4e-06 segL=1e-05 $[g45rnspp] $SUB=3 $X=54400 $Y=0
    $dt=35
529 R17 10 11 4642.86 L=1e-05 W=1.4e-06 effW=1.4e-06 effL=1e-05
    segW=1.4e-06 segL=1e-05 $[g45rnspp] $SUB=3 $X=57800 $Y=0
    $dt=35
530 R18 10 9 4642.86 L=1e-05 W=1.4e-06 effW=1.4e-06 effL=1e-05
    segW=1.4e-06 segL=1e-05 $[g45rnspp] $SUB=3 $X=61200 $Y=0
    $dt=35
```

```
531 R19 8 9 4642.86 L=1e-05 W=1.4e-06 effW=1.4e-06 effL=1e-05 segW
    =1.4e-06 segL=1e-05 $[g45rnspp] $SUB=3 $X=64600 $Y=0 $dt=35
532 R20 8 7 4642.86 L=1e-05 W=1.4e-06 effW=1.4e-06 effL=1e-05 segW
    =1.4e-06 segL=1e-05 $[g45rnspp] $SUB=3 $X=68000 $Y=0 $dt=35
533 R21 6 7 4642.86 L=1e-05 W=1.4e-06 effW=1.4e-06 effL=1e-05 segW
    =1.4e-06 segL=1e-05 $[g45rnspp] $SUB=3 $X=71400 $Y=0 $dt=35
534 R22 6 5 4642.86 L=1e-05 W=1.4e-06 effW=1.4e-06 effL=1e-05 segW
    =1.4e-06 segL=1e-05 $[g45rnspp] $SUB=3 $X=74800 $Y=0 $dt=35
535 R23 4 5 4642.86 L=1e-05 W=1.4e-06 effW=1.4e-06 effL=1e-05 segW
    =1.4e-06 segL=1e-05 $[g45rnspp] $SUB=3 $X=78200 $Y=0 $dt=35
536 R24 4 2 4642.86 L=1e-05 W=1.4e-06 effW=1.4e-06 effL=1e-05 segW
    =1.4e-06 segL=1e-05 $[g45rnspp] $SUB=3 $X=81600 $Y=0 $dt=35
537 .ends resnsppoly$$59
538
539 * ++++++++++++++++++++++++++++++++++++++++++++++++++++++++ *
540 * Sub cell: resnsppoly$$60                                  *
541 * ++++++++++++++++++++++++++++++++++++++++++++++++++++++++ *
542 .subckt resnsppoly$$60 1 2 3
543 ** N=22 EP=3 FDC=20
544 R0 1 22 5000 L=1e-05 W=1.3e-06 effW=1.3e-06 effL=1e-05 segW
    =1.3e-06 segL=1e-05 $[g45rnspp] $SUB=3 $X=0 $Y=0 $dt=35
545 R1 21 22 5000 L=1e-05 W=1.3e-06 effW=1.3e-06 effL=1e-05 segW
    =1.3e-06 segL=1e-05 $[g45rnspp] $SUB=3 $X=3200 $Y=0 $dt=35
546 R2 21 20 5000 L=1e-05 W=1.3e-06 effW=1.3e-06 effL=1e-05 segW
    =1.3e-06 segL=1e-05 $[g45rnspp] $SUB=3 $X=6400 $Y=0 $dt=35
```

```
547 R3 19 20 5000 L=1e-05 W=1.3e-06 effW=1.3e-06 effL=1e-05 segW
    =1.3e-06 segL=1e-05 $[g45rnspp] $SUB=3 $X=9600 $Y=0 $dt=35
548 R4 19 18 5000 L=1e-05 W=1.3e-06 effW=1.3e-06 effL=1e-05 segW
    =1.3e-06 segL=1e-05 $[g45rnspp] $SUB=3 $X=12800 $Y=0 $dt=35
549 R5 17 18 5000 L=1e-05 W=1.3e-06 effW=1.3e-06 effL=1e-05 segW
    =1.3e-06 segL=1e-05 $[g45rnspp] $SUB=3 $X=16000 $Y=0 $dt=35
550 R6 17 16 5000 L=1e-05 W=1.3e-06 effW=1.3e-06 effL=1e-05 segW
    =1.3e-06 segL=1e-05 $[g45rnspp] $SUB=3 $X=19200 $Y=0 $dt=35
551 R7 15 16 5000 L=1e-05 W=1.3e-06 effW=1.3e-06 effL=1e-05 segW
    =1.3e-06 segL=1e-05 $[g45rnspp] $SUB=3 $X=22400 $Y=0 $dt=35
552 R8 15 14 5000 L=1e-05 W=1.3e-06 effW=1.3e-06 effL=1e-05 segW
    =1.3e-06 segL=1e-05 $[g45rnspp] $SUB=3 $X=25600 $Y=0 $dt=35
553 R9 13 14 5000 L=1e-05 W=1.3e-06 effW=1.3e-06 effL=1e-05 segW
    =1.3e-06 segL=1e-05 $[g45rnspp] $SUB=3 $X=28800 $Y=0 $dt=35
554 R10 13 12 5000 L=1e-05 W=1.3e-06 effW=1.3e-06 effL=1e-05 segW
    =1.3e-06 segL=1e-05 $[g45rnspp] $SUB=3 $X=32000 $Y=0 $dt=35
555 R11 11 12 5000 L=1e-05 W=1.3e-06 effW=1.3e-06 effL=1e-05 segW
    =1.3e-06 segL=1e-05 $[g45rnspp] $SUB=3 $X=35200 $Y=0 $dt=35
556 R12 11 10 5000 L=1e-05 W=1.3e-06 effW=1.3e-06 effL=1e-05 segW
    =1.3e-06 segL=1e-05 $[g45rnspp] $SUB=3 $X=38400 $Y=0 $dt=35
557 R13 9 10 5000 L=1e-05 W=1.3e-06 effW=1.3e-06 effL=1e-05 segW
    =1.3e-06 segL=1e-05 $[g45rnspp] $SUB=3 $X=41600 $Y=0 $dt=35
558 R14 9 8 5000 L=1e-05 W=1.3e-06 effW=1.3e-06 effL=1e-05 segW
    =1.3e-06 segL=1e-05 $[g45rnspp] $SUB=3 $X=44800 $Y=0 $dt=35
```

```
559 R15 7 8 5000 L=1e-05 W=1.3e-06 effW=1.3e-06 effL=1e-05 segW
    =1.3e-06 segL=1e-05 $[g45rnspp] $SUB=3 $X=48000 $Y=0 $dt=35
560 R16 7 6 5000 L=1e-05 W=1.3e-06 effW=1.3e-06 effL=1e-05 segW
    =1.3e-06 segL=1e-05 $[g45rnspp] $SUB=3 $X=51200 $Y=0 $dt=35
561 R17 5 6 5000 L=1e-05 W=1.3e-06 effW=1.3e-06 effL=1e-05 segW
    =1.3e-06 segL=1e-05 $[g45rnspp] $SUB=3 $X=54400 $Y=0 $dt=35
562 R18 5 4 5000 L=1e-05 W=1.3e-06 effW=1.3e-06 effL=1e-05 segW
    =1.3e-06 segL=1e-05 $[g45rnspp] $SUB=3 $X=57600 $Y=0 $dt=35
563 R19 2 4 5000 L=1e-05 W=1.3e-06 effW=1.3e-06 effL=1e-05 segW
    =1.3e-06 segL=1e-05 $[g45rnspp] $SUB=3 $X=60800 $Y=0 $dt=35
564 .ends resnsppoly$$60
565
566 * ++++++++++++++++++++++++++++++++++++++++++++++++++++++++ *
567 * Sub cell: resnsppoly$$61                                  *
568 * ++++++++++++++++++++++++++++++++++++++++++++++++++++++++ *
569 .subckt resnsppoly$$61 1 2 3
570 ** N=6 EP=3 FDC=4
571 R0 1 6 5371.9 L=1e-05 W=1.21e-06 effW=1.21e-06 effL=1e-05 segW
    =1.21e-06 segL=1e-05 $[g45rnspp] $SUB=3 $X=0 $Y=0 $dt=35
572 R1 5 6 5371.9 L=1e-05 W=1.21e-06 effW=1.21e-06 effL=1e-05 segW
    =1.21e-06 segL=1e-05 $[g45rnspp] $SUB=3 $X=3020 $Y=0 $dt=35
573 R2 5 4 5371.9 L=1e-05 W=1.21e-06 effW=1.21e-06 effL=1e-05 segW
    =1.21e-06 segL=1e-05 $[g45rnspp] $SUB=3 $X=6040 $Y=0 $dt=35
574 R3 2 4 5371.9 L=1e-05 W=1.21e-06 effW=1.21e-06 effL=1e-05 segW
    =1.21e-06 segL=1e-05 $[g45rnspp] $SUB=3 $X=9060 $Y=0 $dt=35
```

```
.ends resnsppoly$$61

* ++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++ *
* Sub cell: DS_VGA                                                *
* ++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++ *
.subckt DS_VGA IREF S0 S1 S2 S3 S4 S5 VDD VINM VINP
+ VOUT VSS
** N=39 EP=12 FDC=648
X42 5 VINP VSS VDD 6 IREF DS_VGA_OPAMP $T=14160 0 0 0 $X=14160
    $Y=0
X43 9 VINP VSS VDD VOUT IREF DS_VGA_OPAMP $T=151140 0 0 0 $X
    =151140 $Y=0
X44 5 VINM VSS resnsppoly$$45 $T=7190 5430 0 0 $X=6100 $Y=4890
X45 5 6 VSS resnsppoly$$45 $T=7240 9600 1 0 $X=6150 $Y=8180
X46 9 14 S3 VDD VSS DS_VGA_SWITCH $T=8170 131030 0 0 $X=8170
    $Y=131030
X47 6 16 S0 VDD VSS DS_VGA_SWITCH $T=56490 67050 0 0 $X=56490
    $Y=67050
X48 6 18 S1 VDD VSS DS_VGA_SWITCH $T=58890 45360 0 0 $X=58890
    $Y=45360
X49 9 20 S4 VDD VSS DS_VGA_SWITCH $T=60750 27280 0 0 $X=60750
    $Y=27280
X50 9 22 S5 VDD VSS DS_VGA_SWITCH $T=70970 290 0 0 $X=70970 $Y
    =290
```

```
592 X51 6 24 S2 VDD VSS DS_VGA_SWITCH $T=123850 820 1 180 $X
    =121270 $Y=820
593 X52 14 1 VSS resnsppoly$$58 $T=18490 155090 0 0 $X=18210 $Y
    =154550
594 X53 1 VOUT VSS resnsppoly$$58 $T=18560 176820 0 0 $X=18280 $Y
    =176280
595 X54 16 3 VSS resnsppoly$$59 $T=61080 67860 0 0 $X=60800 $Y
    =67320
596 X55 2 3 VSS resnsppoly$$59 $T=61080 89660 0 0 $X=60800 $Y
    =89120
597 X56 2 8 VSS resnsppoly$$59 $T=61080 111460 0 0 $X=60800 $Y
    =110920
598 X57 9 8 VSS resnsppoly$$59 $T=61080 133260 0 0 $X=60800 $Y
    =132720
599 X58 20 VOUT VSS resnsppoly$$60 $T=67880 24390 0 0 $X=67600 $Y
    =23850
600 X59 18 9 VSS resnsppoly$$60 $T=67880 46060 0 0 $X=67600 $Y
    =45520
601 X60 22 VOUT VSS resnsppoly$$61 $T=81720 1030 0 0 $X=81440 $Y
    =490
602 X61 24 9 VSS resnsppoly$$61 $T=97860 1030 0 0 $X=97580 $Y=490
603 .ends DS_VGA
```

Listing IV.4: Variable Gain Amplifier (VGA) SPI