Comparison of Minority Carrier Lifetime Measurement by Surface Charge and Capacitance -Time Analysis

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Abstract - Minority carrier lifetimes are a useful parameter in both the design and manufacture of discrete and integrated circuits. With today's emphasis on MOS technology, minority carriers are used as a "process cleanliness" tool in a manufacturing environment. The purpose of this project is to compare the two available carrier lifetime tests, namely the Semitest Surface Charge Analyzer (SCA) and capacitance-time and seeing if the relationship is linear. Being linear, the more process intensive capacitance-time test can be avoided and all pertinent data can be extracted via the SCA, therefore increasing product cycle time and time to market. 200A thermal oxide gate capacitors were manufactured and tested, SCA analysis was taken with the oxide grown prior to aluminum evaporation.

1. INTRODUCTION

Minority carrier lifetimes of semiconductors are a very important parameter in the design and fabrication of bipolar integrated circuits and discrete transistors. MOS devices do not rely as heavily on carrier lifetime for performance issues, instead lifetimes are being used in a manufacturing role as a simple test to detect lifetime-killing impurities recombination centers which are commonly known as *traps*. Essentially it is a "process cleanliness monitor".

The first of two methods, the Semitest Surface Charge Analyzer, generates carriers using photon emission from a probe that comes in contact with an oxidized silicon substrate. These photons at λ=560nm and an energy E=2.2ev change the balance of charges in the silicon (bandgap=1.12ev) to generate the electron hole pairs. The SCA measures and plots the depletion width (W_D) vs. induced charge (Q_{ind}) and then computes values for the wafer type (p,n), doping concentration (N_{sc}), oxide charge (Q_{ox}), the density of interface states (D_{it}) as well as other related parameters including minority carrier lifetimes (τ_s) which is the parameter of interest for this project. The probe schematic is shown in Figure 1.

The second method, Capacitance-Time (C-t), is a simple test that uses a capacitance meter with a "lifetime" feature. This feature allows the meter to pulse a voltage to a MOS capacitor instead of the usual capacitance-voltage method of sweeping from negative to positive (or vice versa depending on wafer type). An analog gauge on the capacitance meter deflects with the change in capacitance. In order to visually see the data, both an X-Y plotter and an oscilloscope were connected to the output of the capacitance meter. The voltage of the C-t test starts in deep depletion ($2\phi_F$) and is pulsed into strong inversion ($2\phi_F$ + (8 to10)ϕ_t). From the relaxation curve data, the minority carrier lifetimes are extracted using the equation, the basis of the Zerbst plot, below. A linear equation, the slope of which gives the minority carrier lifetime.

$$-\frac{d\left(\frac{C_o}{C}\right)^2}{dt} = \left(\frac{2n_iC_o}{N_BC_F\tau_{g'}}\right)\left(\frac{C_F}{C-1}\right) + \frac{2n_iC_{os'}}{K_s\varepsilon_o N}$$

Equation 1: Zerbst Plot equation to extract carrier lifetimes

II. EXPERIMENTAL PROCEDURES

Six p-type silicon wafers with a resistivity of 5-10 Ω-cm <100> were oxidized in an O_2 ambient at 975°C for 20 minutes to grow a ~200A oxide. Particle counts and Surface Charge Analyzer (SCA) data was collected and mapped for all six wafers. As a baseline measurement, the two with the lowest

carrier lifetime were used since further degradation of lifetime might not be measurable with the capacitance-time equipment. The remaining four were then placed in a "dirty" oxidation tube at 1000°C for 120 minutes so as to theoretically degrade the lifetimes with the introduction of impurities. Particle counts and SCA data was collected and mapped for these four. Of the four, two had a degraded lifetime of approximately 30% which was expected. The remaining two, D_4 and D_5, were degraded to the point that reliable data could not be taken. In fact, according to the SCA, the lifetimes went up by two times and the background concentration was increased by an order of magnitude. Needless to say, these wafers were then scrapped. The remaining four wafers had aluminum evaporated on the fronts and photolithography using a capacitor array mask was done. During the develop process, wafer D_2 was destroyed due to equipment error.

Aluminum etch was completed using, clean phosphoric acid. Preparation for backside contacts involved coating the front of the wafer with photoresist, hardbaking and etching the remaining 200A of oxide off the back. Al/Si (1%) was then sputtered and sintered in a 450°C forming gas (N_2/H_2) ambient for 20 minutes.

Wafer #	τg Initial	τg (+120min)	%Difference
D1	136.5	N/A	N/A
D2	194.8	N/A	N/A
D3	214.4	141.6	-0.340
D4	201.1	247.6	0.231
D5	201.1	----	----
D6	212.9	149.5	-0.298

Figure 1: SCA lifetime data comparison from initial measurements and after 120min anneal.

Capacitance-time tests were done using the Micromanipulator Model 410 C-V meter which was attached to an X-Y plotter, Tektronix oscilloscope, and Keithley voltmeter. A covered probe box was used to remove electron hole pair generation due to light. An output from the oscilloscope was supposed to be used to trigger the capacitance meter to start the test. Unfortunately, a 5v output from the o-scope could not be done, instead a manual trigger device consisting of a 9v battery and voltage divider was used with a voltage output of 5.3 volts. This allowed the acquisition of data from the capacitance meter. Two capacitor areas were measured 500kμm^2 and 2Mμm^2.

III. RESULTS AND DISCUSSION

Degradation of carrier lifetimes as measured by the Surface Charge Analyzer is seen in Figure 1. The 120 minute anneal in Argon gas produced a drop in lifetime of 30% which was expected.

For an unknown reason, minority carrier lifetimes could not be achieved using the capacitance-time method. Shown in Figure 2 below is both a capacitance vs. voltage and capacitance vs time plots for wafer D6. These show a good C/V plot but the C-t plot shows no relaxation from the initial trigger.

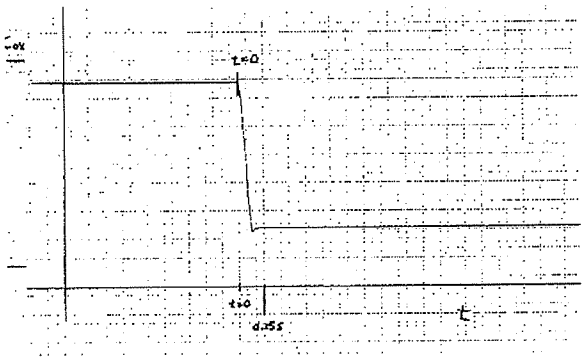

Figure 2a,b: Capacitance/Voltage and Capacitance Time curves for p-type wafers. Notice the small relaxation time in 2b.

The small blip shortly after t=0 is assumed to be the relaxation time. Questioning whether or not the lifetime was too short or too long, a very long time was plotted, this was on the order of one hour. After that one hour, no change was seen in the curves.

In order to verify whether or not the test was working at all, an n-type wafer was tested. As shown in Figures 3a and 3b, the test did work.

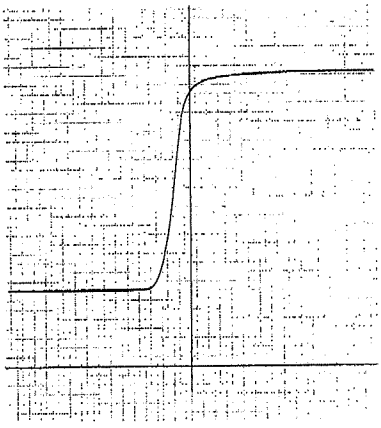

Figure 3a: C/V plot for n-type wafer

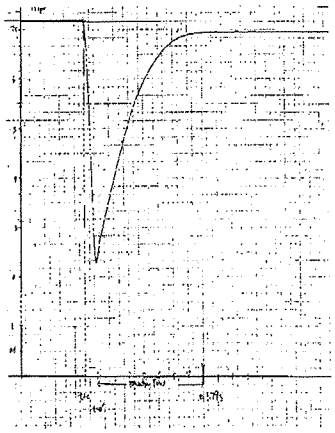

Figure 3b: C-t plot for n-type wafer

Figure 3a shows the C/V plot for the capacitor, this shows that the capacitor is good and not leaking. Figure 3b, the C-t plot, shows that the relaxation time was 1.8 seconds and a measurable curve was achieved which allows the carrier lifetime to be extracted using the Zerbst plot equation (Equation 1). The results are shown below in Figures 4a and 4b.

Minority lifetime was calculated with a FORTRAN program written by Dr. Michael Jackson for his Ph.D dissertation to be 0.1μs with a correlation coefficient of 0.9846.

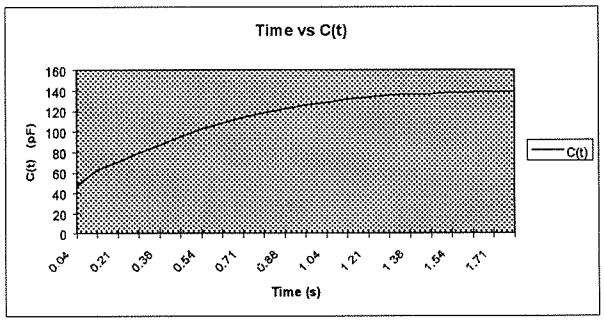

Figure 4a: Measured Data form curve.

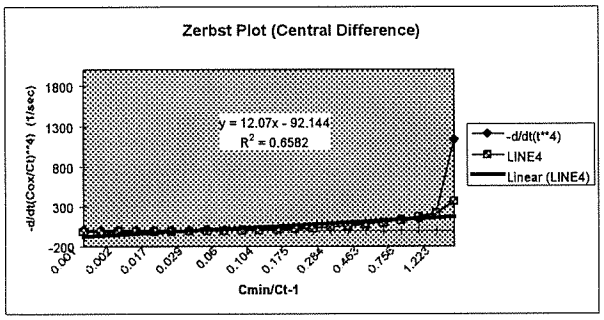

Figure 4b: Zerbst Plot data. Correlation of 0.9846

IV. CONCLUSION

Unfortunately data correlation could not be done. Further investigation into capacitance-time testing for p-type wafers will continue. N-type substrates, however, did work to the point of data collection. A carrier lifetime of 0.1μs was calculated using the Zerbst plot equation.

A theory as to why the test did not work for the p-type wafers in that the background doping of the substrate was too low. Positive oxide charges in the 200A thermally grown gate oxide will attract negative carriers to the SiO_2/Si surface, when the layer is inverted under the aluminum gate, the charges at the interface are attracted to the lower potential-well therefore increasing the density of carriers as well as decreasing the minority carrier lifetime dramatically to the point of it being unmeasurable. This would account for the small "blip" in Figure 2b. Another theory may involve the oxide thickness as it relates to Cox. For the n-type wafers, the measured oxide thickness was 460A whereas the thickness for the p-type wafers was only 200A. Investigation of n-type wafers with 200A oxide is currently taking place.

V. ACKNOWLEDGMENTS

I would like to thank Dr. Michael Jackson for this project, and starting my interest in capacitance measurements. Dr. Santosh Kurinec for her advise and help with minority carrier lifetime papers. Finally the equipment engineers in RIT's cleanroom deserve much praise for their dedication and patience to both the students and the program. Thank You.

VI. REFERENCES

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David Lundeen a graduate from Rochester Institute of Technology's undergraduate program in Microelectronic Engineering is presently employed with Motorola SPS in Mesa, AZ in the Manufacturing Engineering Rotation Program. For three years he co-oped with Motorola in various position from electrical test to electromigration reliability testing. His professional interests include thin film technology and ion implantation.