Stacked Floating Gate EEPROM

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Abstract - **The concept of SFG-EEPROM involves the replacement of the standard EEPROM's floating gate with a multi-layer stacked of Silicon (Si) and Silicon Dioxide (SiO_2). This multi-layer stack of Si and SiO_2 is either deposited via sputtering or CVD and followed by annealing (see *Figure 1*). Carriers will be injected from the n+ polysilicon layer into the multi-stacked layers, and those carriers will be confined to the silicon crystallites with the thin oxide barriers between silicon layers. The distribution of charge within the stack will alter the field-effect on the underlying silicon substrate. This type of structure may result in lower operating voltage, faster write/erase cycles, the elimination of "over-erase" problems, and the utilization of only a single transistor EEPROM cell. The purpose of this experiment was to determine the feasibility of this idea and the initial results conclude that this concept works. However, more experiments and characterizations need to be done, in order to further confirm the feasibility, and determine the reliability of this device.**

I. OBJECTIVE

The main purpose of this project was to determine the feasibility of SFG-EEPROM by investigating the ability of charge tunneling through thin oxide sublayers and the ability of the multilayer stack to freeze the charge distribution (no leakage after time). A study of the dielectric quality of the sputter deposited oxide was also necessary due to the important function of the oxide sublayers.

II. INTRODUCTION

Standard EEPROM structures involve Fowler-Nordheim tunneling through a very thin tunnel oxide in order to transmit charges from the substrate to a floating gate structure. A high voltage on a control gate is used to set up a high electric field (~7MV/cm) which allows electrons to tunnel from the Si substrate through the SiO_2 triangular potential barrier into the conduction band of the floating gate. Charges are transferred back and forth between the floating gate and the substrate in order to write and erase a bit. The bit is read by applying a much lower voltage signal on the control gate, and measuring the resulting current through the transistor structure.

The concept of a stacked floating gate would involve the shifting of charges within a stack of material, instead of tunneling charges on or off the floating gate. The floating gate is a multi-layer stack of Si and SiO_2, either deposited via sputtering or CVD, followed by annealing (see *Figure 1*). With the thin oxide barriers between silicon layers, carriers will be confined to the silicon crystallites. However, with the assistance of an appropriate electric field, carriers can undergo direct tunneling through the very thin (~20-100Å) barriers and shift within the floating stack. The placement of charge within the stack will determine the field-effect on the underlying transistor in the silicon substrate.

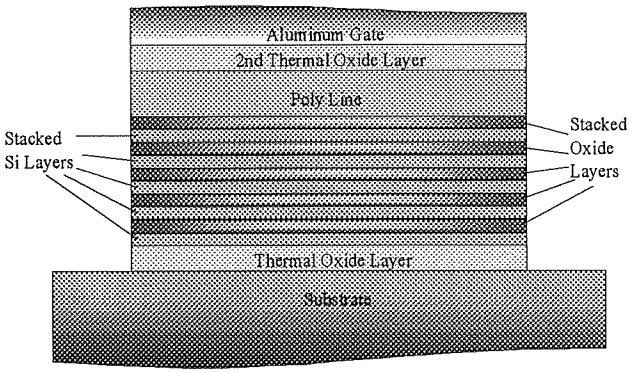

Figure 1. Cross-section of the SFG-EPROM capacitor structure.

A non-destructive read would take place at a low control-gate bias and a write and erase cycle takes place at a higher control gate bias. The write bias (negative voltage) will inject electrons from the n+

poly layer onto the multilayer stack, which can be removed by an erase bias (positive voltage).

This type of structure may result in lower operating voltage and faster write/erase cycles, due to the direct tunneling nature. With field assistance, carriers can directly tunnel through the thin oxide layers without waiting for the triangular energy barrier to reach appropriate thickness so the carrier can tunnel through as in Fowler-Nordheim tunneling. The SFG-EEPROM may also eliminate "over-erase" problems. After a write bias is removed, coulombic force causes charges to repel each other, relaxing to an equilibrium condition. It is a self-limiting process, in that, the amount of charges will always remain the same. Furthermore, the write, read and erase function can all be done from the same control gate, so there is no need for an extra transistor for write and erase function as in a standard EEPROM cell. The SFG-EEPROM, thus, is a single cell EEPROM. Finally, all the mechanisms of the SFG-EEPROM, especially the carrier injection mechanism, are done above the substrate. Therefore, this device can function not just on the silicon substrate.

III. EXPERIMENTAL DESIGN

A simple full factorial designed experiment was used with four oxide thickness splits and two annealing splits (with and without furnace oxidation). The chosen factors will affect the oxide sublayer quality, and several responses were used to determine which treatment produces the best working device combination. Four oxide thickness were used in order to determine the oxide sublayer thickness which can hold the charge distribution and reduce leakage. The two annealing splits were used to determine the effect of an O_2 ambient anneal on the quality of the sputtered oxide layer. The total time which the wafers spent in the furnace remained constant. The entire experiment design is shown in the diagram below (*Figure 2*):

IV. PROCEDURE

The key parameter for this device to work properly is the quality and thickness of the sputtered oxide sublayers. The first step in this investigation was to characterize the sputtered SiO_2 material.

A layer of oxide was sputtered for about 500Å thick by rf-sputtering using a Perkin-Elmer 2400 sputter system on the p-type wafers. Those wafers were than being Rapid Thermal Annealed (RTP) and ran through four different annealing splits. These splits were needed in order to determine the effect of temperature and ambient on the quality of the oxide and interface. After that, the front side and the backside of the wafers were Aluminum sputtered and patterned. Capacitors were made. The C-V analysis and dielectric breakdown tests were done to characterize the sputtered oxide films.

Once the sputtered oxide material was characterized, the next step was to fabricate the capacitor structures. The SFG-EPROM was investigated by making simple capacitors instead of the full transistor structure because the region that was primarily interested was the stacked region.

First, a 300Å thermal oxide was grown, in order to isolate the memory storing structure with the transistor or substrate. Wafers were then sputter deposited with multilayer structures of amorphous silicon and SiO_2 (10 periods, 20 layers) with variation in thickness (25 - 100Å) of the oxide barrier layers. The amorphous silicon thickness was fixed at 140Å. After sputter deposition, the wafers were RTP and ran through two furnace annealing splits. This will re-crystallize the amorphous Si layers and modifying the structure of the SiO_2 sub-layers and interfaces. A 6000Å LPCVD poly was then deposited on top of the stacked layers. This will form the carrier injection source layer. Then, the second thermal oxidation with 500Å thick was done. This will isolate the poly and the control gate (Aluminum) layer. Subsequently, a 6000Å Aluminum was deposited and the control gate layer

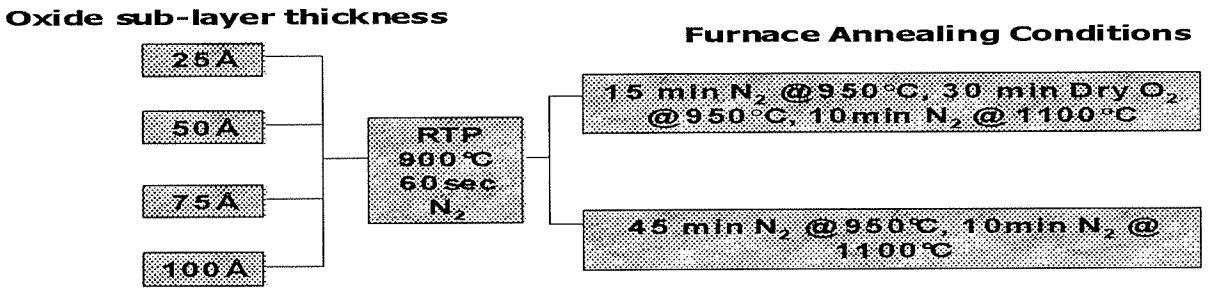

Figure 2 Experiment design splits diagram

was formed. A photo lithography process was followed after that, in order to pattern the control gate. The lateral dimension of the whole device structure was defined by SF_6 Reactive Ion Etching (RIE) from control gate down to the substrate. Finally, the backside of the wafers were then etched clean and Aluminum was sputtered and followed by H_2/N_2 sintering (the final device structure is shown in *Figure 1*). C-V analysis was done in order to test the feasibility of these devices.

V. TESTING METHOD

The C-V analysis was utilized to test the functionality of this device. A 10V-voltage sweep was determined to be sufficient to program and erase the SFG-EEPROM cell. In other words, 10V is enough to induce a reasonable hyteresis in the C-V plot. Voltage was swept from -10V, which was at write condition, to 10V, which was at erase condition. Then it was retraced, from Erase (10V) condition ending in Write (-10V) condition. A hysteresis is observed if the device works correctly (Refer to *Figure 3*). The amount of hyteresis will determine the amount of charges stored in the stacked layers. Then the bias was taken away and the device was left in the zero-bias condition for 5 minutes. This time would be sufficient for the device to relax (self-limiting process, until it reaches equilibrium). The charge relaxation would shift the C-V curve to the left. In order to quantify this shift, the

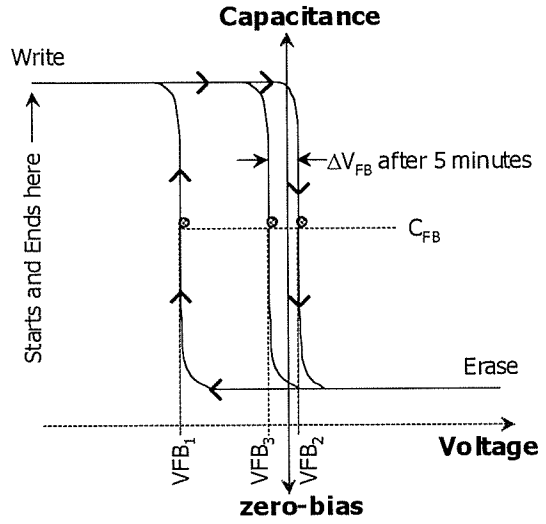

Figure 3. Typical C-V testing for this experiment

change of the Flat Band voltage (ΔV_{FB}) was determined. Since all the curves exhibited a steep slope, the Flat Band voltage was assumed to be at the center of the curve for simplicity. At a constant Flat Band Capacitance (C_{FB}), the difference of the voltage will be the ΔV_{FB}. ΔV_{FB} should be a very low number but non-zero. The curve was then retraced but this time the voltage was not swept with a margin of 10V. It was just traced up and down the curve in order to observe if there is any shifting at the curve. A leaky device would not be able to withstand a slight voltage change thus it would shift. Contrary, a good and robust device would not shift even if the bias voltage was very high. The degree of robustness was determined by the minimum voltage at which a left-shift in the C-V was observed.

VI. RESULTS

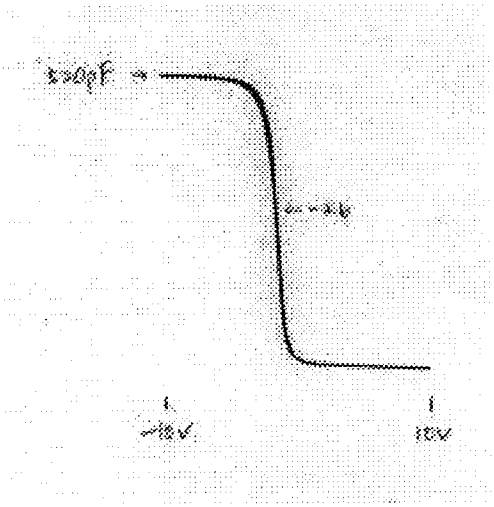

Figure 4. C-V plot of device with 25Å oxide and O_2 anneal.

The C-V plot with poor, average and excellent results for different oxide thickness and annealing conditions are shown below:

Figure 4 is for the device which has the treatment combination of 25Å oxide thickness with O_2 anneal. The C-V curve (see *Figure 4*) showed no hysteresis and therefore, the ΔV_{FB} was not able to measured. This indicates that the stacked layer in this device is not able to store any charge. This may be due the thin oxide sublayers. The oxide sublayers might have condensed after anneal, therefore, the thickness can be much lower than 25Å.

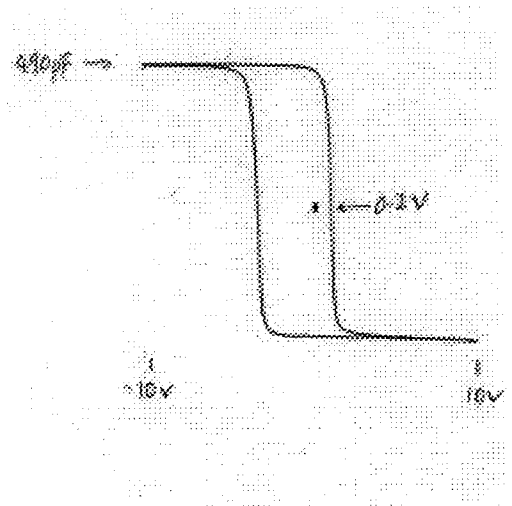

Figure 5. C-V plot of device with 75Å oxide and without O_2 anneal.

The hystesesis for this device (*Figure 5*) is very big (2.22V). That means the stacked layer in this device can store a lot of charges. However, the ΔV_{FB} is also a large number, 0.5V. This indicates that the charges in the stacked layer leaked out a lot during relaxation. In other words, the leakage is very high. The "Read Shift" in this device is excellent. The curve did not shift until the apply bias was greater than +8V (from V_{FB}).

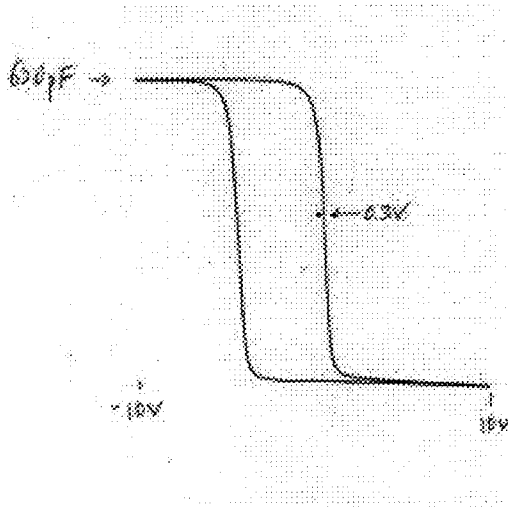

Figure 6. C-V plot of device with 100Å oxide and with O_2 anneal.

Figure 6 above shows the best working device. It had a reasonable hyteresis (2.5V), a little change in ΔV_{FB} (0.12V) and excellent "Read Shift" test result. The curve did not shift until the bias was greater than 5V from V_{FB}. The exact thickness of the 100Å oxide sublayer was not known due to the changes in the oxide structure during annealing (possible densification). A further characterization on these devices is needed to determine other parameters such as charge retention time and write/erase cycle times.

VII. CONCLUSION

The SFG-EEPROM concept seems feasible but more works need to be done in order to further determine the usability and robustness of this kind of device. The future work should include a complete characterization of the sputtered and annealed oxide film, a transient (Capacitance vs. time) and retention time measurements and an advanced device modeling which includes charge transport (tunneling current), transient analysis or write/erase time (available carriers) and charge retention (potential barriers).

The sputtered oxide films exhibited reasonable dielectric properties after annealing. The device which performed the best (i.e. with large hysteresis, small zero-V_{FB} and very little "read-shift") utilized "100Å oxide" sub-layers.

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