Process Development for Porous Silicon Light-Emitting Devices

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Abstract - **The primary focus of this project was to continue process development of integrated PSi-based (porous silicon) LEDs. Porous silicon is a light-emitting material formed by electrochemical etching of the silicon substrate, resulting in the formation of pores and wire-like silicon structures [1]. This study investigates new strategies in the effort to advance the implementation of PSi-based LEDs with standard CMOS technology by providing devices that are substrate-based, electrically isolated, array-addressable and voltage modulated. Existing problems with porous silicon LEDs include high bias operation, low external quantum efficiency (EQE), and poor stability. This work has resulted in the fabrication of LEDs with significantly improved performance, however further device optimization is required.**

I. Introduction:

Porous silicon (PSi) has attracted much interest in the effort to integrate silicon circuitry with optoelectronic devices. The ability to fabricate light-emitting devices (LEDs) that are easily implemented with standard CMOS technology would greatly expand the use of silicon as an optoelectronic material, which could be applied to data transceivers, optical interconnects, and monolithic substrate displays. Crystalline silicon, an indirect bandgap semiconductor is an inefficient light-emitting material. Porous silicon, formed by anodic etching of a silicon wafer surface, has demonstrated excellent room temperature photoluminescence (PL) at ~8% external quantum efficiency (EQE)[2]. Electroluminescent devices have been fabricated that report a 0.2% EQE [2]. Practical application has been a serious problem, however due to issues such as efficiency and stability.

The fabrication of this relatively simple device involves numerous factors that require optimization, each of which can have a significant effect on several responses including the photoluminescence, electroluminescence, I-V characteristics, and stability of the device. Several screening runs and experiments were performed in an attempt to narrow down the list to a few factors, and find a desirable design space to explore. Factors investigated include surface type, annealing conditions, contact material, and anodization settings. Response parameters, which quantify the LED performance, include spectra, I-V characteristics, threshold conditions, uniformity of emission, and stability.

II. Theory and device fabrication:

Crystalline silicon is an indirect bandgap semiconductor with a bangap of 1.12 eV (room temperature). This results in luminescence below the visible spectrum, and low efficiency due to competing recombination effects. Luminescence efficiency can be increased when non-radiative recombination events are suppressed and/or the radiative recombination rate is increased.

The effective bandgap of a material depends upon the confinement distance. The bandgap of a material widens due to quantum confinement when the size of the silicon structure becomes small enough. Nanoscale silicon structures that are well passivated have shown an advantage over bulk silicon in decreasing non-radiative recombination, and by increasing the bandgap of silicon the photon emission can be pushed into the visible region. The pure quantum confinement model was originally proposed by Canham [1] to explain luminescence in porous silicon.

PSi is a material formed by electrochemical anodization of crystalline silicon using an HF/ethanol mixture. Pores on the order of 50 nm are formed by preferential etching, which results in wire-like silicon structures ~2-3 nm wide (shown in fig. 1). Variations in the anodization process and silicon dopant level can vary the PSi thickness and porosity ranging from the extremely porous to low porosity. This effects the silicon structure size, and mechanical stability.

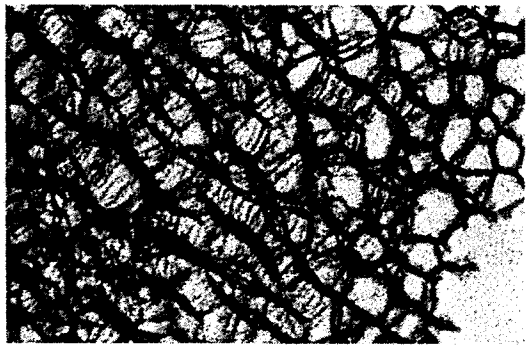

Fig. 1 - TEM image of porous silicon. (Image courtesy of A.G. Cullis of the UK's Defense Research Agency.)

The basic fabrication sequence for bulk film devices previously developed at RIT goes as follows: 10Ωcm p-type (100) oriented crystalline silicon wafers, with a heavily doped p^+ surface layer, are anodized in a 1:1 HF/ethanol solution. The typical current density used during anodization was approximately 3.5 mA/cm^2 for a time of 4 min. The p^+ region, following anodization, is transformed to a mesoporous layer (porosity ~ 40%), while the underlying p^- silicon becomes a nanoporous layer (porosity ~ 75-80%). The typical thickness of the resultant porous silicon layer is approximately 4000 Å. Following anodization, an anneal is performed to passivate the PSi layer. A polysilicon film is then deposited using LPCVD, and selectively doped n^+ to form the device cathode. Indium-tin-oxide (ITO), or aluminum (Al) contacts are sputtered on the polysilicon, and backside Al is deposited to form an ohmic contact to the substrate [3]. Fig. 2 shows a cross-sectional view of the device.

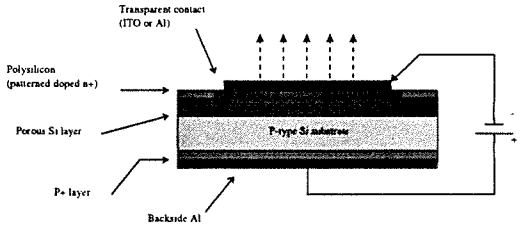

Fig. 2 - Schematic cross section of porous silicon light-emitting diode, capable of light emission at visible wavelengths.

III. Experiments and evaluation:

Optimization of this device has been difficult due to the number of factors involved, each of which have a significant impact on the photoluminescence (PL), electroluminescence (EL), carrier transport, and stability of the device. Formation of the porous silicon material alone can be altered by several factors.

Process development for this project included a total of three separate designed experiments. The first two experiments were used to narrow factors, and to find a desirable design space to explore. The final designed experiment used optimized results from the previous DOEs and further explored additional factors.

Post-anodization annealing of the PSi layer was investigated first. Photoluminescences (PL) was the response examined following anodization, which was performed in an N_2 ambient for 20 minutes. Temperature was varied from 700°C to 1000°C. Small samples were used, therefore; push and pull temperatures were equal to the soak temperature. Push and pull rates were also kept constant. Should a high intensity PL response occur, it was thought that an increase in EL response may be possible.

The second designed experiment involved investigating the post-anodization anneal. A long with additional, factors such as an HF dip, and an n^+ implant (following the annealing of the PSi layer) were investigated. Previous results showed that the formation of a *pn* junction within the PSi layer may have increased luminescence. The HF dip was a new process design. The idea behind using the HF dip (following the post-anodization anneal) was to etch away oxide that was preventing electrical transport, but still maintain the passivated surface. The main purpose of this experiment was to test EL response with the higher temperature annealing.

The final experiment investigated anodization conditions (surface layer, current density, and time), and post-anodization anneal versus no annealing. It was shown in a previous sample that an ITO contact with no poly, or annealing displayed good uniformity and decent I-V characteristics. The device was short-lived, however. The effect of no annealing was compared to the optimal annealing conditions determined from the first two experiments.

The purpose of investigating anodization conditions was to analyze the effect of the type of PSi layer formed on EL response. The strategy for use of the p^+ surface layer was to create a less porous surface to deposit the poly cathode over. Two treatment combinations were done with only the p^- substrate during anodization, which is a higher porosity. Also, a thick PSi layer was thought to be inhibiting electrical transport. A decreased anodization time was used for two treatment combinations (3.5 mA/cm^2 for 3 min., p^+ layer). The same thickness was used for another two treatment combinations, however the current density was 1 mA/cm^2 through the p^+ layer and 3.5 mA/cm^2 into the p^- layer. The use of a lower current density creates a slightly less porous surface, and increases the amount of time necessary to etch through the p^+ layer.

IV. Results:

Figure 3 shows the measured voltage versus the anodization time. The contact potential between the wafer surface and the HF/ethanol solution shows the difference between a p^+ and p^- surface layer. The current density was kept constant at 3.5 mA/cm^2 (with the exception of the final DOE). The key reaction for the anodization process is shown below:

$$Si + 2HF + 2h^+ \rightarrow SiF_2 + 2H^+$$

Holes are necessary for the reaction to occur. As can be seen in figure 3, the solution (80 mL) is degrading due to ion depletion after only two wafers have been processed. Limiting two wafers/80 mL of solution has optimized the anodization process further.

As mentioned before, the p^+ region, following anodization, is transformed to a mesoporous layer, while the underlying p^- silicon becomes a nanoporous layer. The typical thickness of the resultant porous silicon layer is approximately 4000 Å.

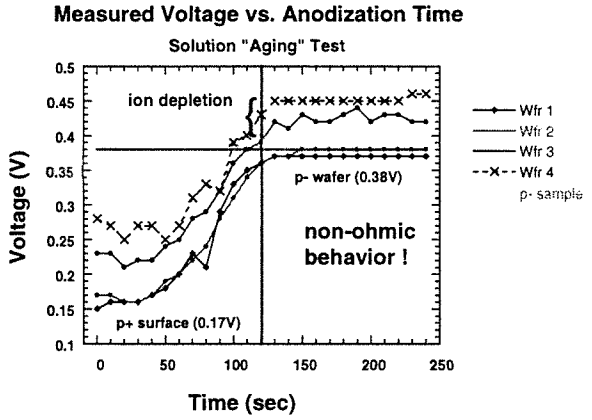

Fig. 3 - Measured voltage versus anodization time for four separate wafers processed in sequence with current density of 3.5 mA/cm^2. The change in voltage as the p^+ material is consumed indicates non-ohmic transport during etching.

Optimal photoluminescence (PL) was found to occur with 950°C N_2 annealed sample; PL degraded at higher temperatures. An N_2 anneal is used to inhibit oxidation. A thick oxide layer is detrimental to device performance. The results from the post-anodization DOE are shown in fig. 4.

Replicate runs were performed to determine if the actual PL peak was at 950°C. The procedure was identical, however the temperatures examined were from 900°C to 1000°C in intervals of 25°. The results confirmed what is shown in figure 4, the peak remained at ~950°C.

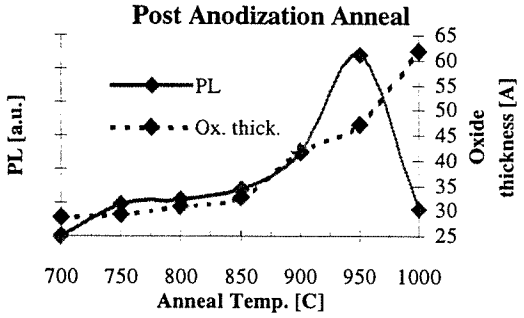

Fig. 4 - Photoluminescence response and oxide thickness versus post-anodization annealing temperature. The amount of oxide grown was measured at the edge of a wafer, using a nanospec. This correlates to the degree of oxidation of the PSi.

Electroluminescence depends on the ability to flow current through the device. Although optimal PL occurred at 950°C, the oxide thickness starts to increase rapidly in this temperature region, which can limit electrical transport. For this reason, the post-anodization anneal was investigated in the second DOE with 900°C and 950°C as the factor levels.

Factors investigated next included an HF dip, an n^+ implant, and the N_2 anneal (all following anodization). The HF dip method (50:1 dilute HF for 3 sec.) was an attempt to remove oxide that may be suppressing electrical transport, and the implant was investigated to try and repeat previous results. Both the HF dip method and the n^+ implant provided little, or no assistance in effectively increasing EL or carrier transport.

Samples annealed at 950°C, were found to suppress electrical transport. However, the 900°C annealed samples were able to flow current. EL was observed on a sample that had no HF dip, or n^+ implant. The uniformity and stability of this sample showed good potential. The luminescence is extremely dim and at a very high bias, however. The bias needed to achieve this was on the order of ~30 V. Some measured results of this device are shown on figure 6, which will be discussed later.

The final DOE examined the PSi layer (porosity and thickness), the 900°C anneal versus no post-anodization anneal, and an aluminum (Al) versus indium-tin-oxide (ITO) top contact. The samples with no anneal were able to flow current with no difficulty, however no luminescence was observed. Some passivation of the surface appears to be necessary to obtain efficient EL.

The device structure that provided the best luminescence and rectifying behavior was the 900°C annealed p^- layer, with an Al top contact. Figure 5 shows the measured I-V characteristics of this structure.

The other identical treatment combination, with no anneal, is shown in this figure also. I-V measurements were obtained using a HP4145 Parameter Analyzer.

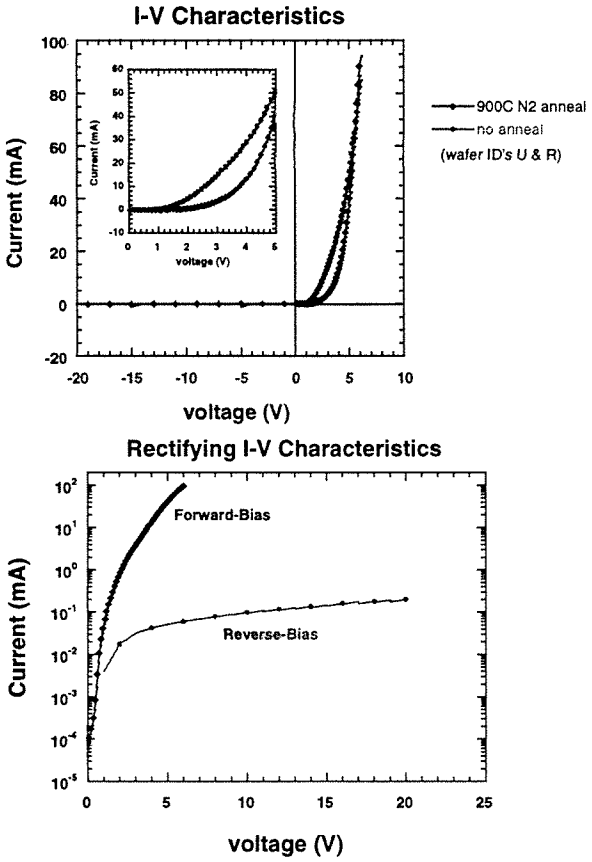

Fig. 5 - Measured I-V characteristics showing *a.)* the difference of a 900°C annealed sample versus no anneal. Both show excellent rectifying behavior, however luminescence was only observed from the annealed sample. *b.)* the difference between forward and reverse bias of annealed sample.

The annealed sample appears to have a better exponential fit, and flows almost 50 mA of current at a bias of only 5 V. Typically previous devices would destructively breakdown at this level of current flow, however the bias would be much higher. The sample with no anneal is comparable to this sample, however no luminescence is evident. Possibly due to lack of passivating the PSi material

Threshold voltage (voltage when emission can be detected by the human eye) for this device (annealed sample) was ~5 V, the lowest achieved from a device fabricated at RIT. Typical threshold voltages were anywhere from 10 - 30 V. Luminescence at that high of a bias may not be that practical. A threshold of 5 V, however is very reasonable.

The forward bias characteristics of several devices are shown in figure 6. EL was observed from each device shown on this plot, with the exception of wfr #7 (ITO contact). The threshold observed varies tremendously from each device, however.

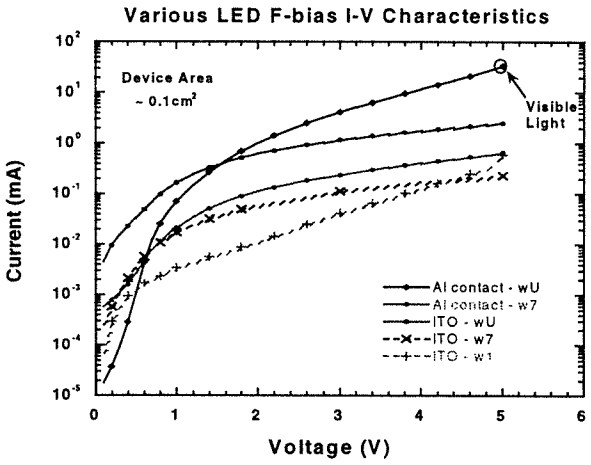

Fig. 6 - Forward bias characteristics for electroluminescent devices. Notice the difference in both the magnitude of the current and the slope of the line of the Al contact (wfr U) compared to the other devices.

The two devices shown in figure 5 were plotted again in figure 7. The forward bias results are plotted versus the square root of the voltage. An exponential line has been fitted to the 900°C anneal sample, which shows reasonable fit after some threshold voltage. This fits well with the Poole-Frenkel fit for thermionic emission [4].

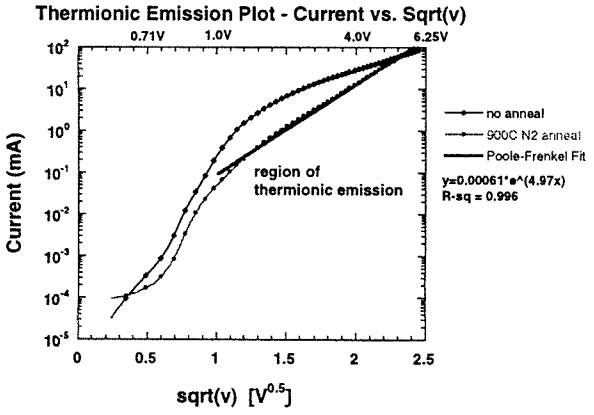

Fig. 7 - Current versus square root of the voltage for same devices shown in figure 5. Displays an exponential fit after some threshold voltage as been reached.

Stability and uniformity of the 900°C, p- layer, with Al contact device were also examined during a

long-exposure photograph. The device was forward biased, with a large current flow, for approximately two hours and showed no degradation in operation.

The picture (not shown) also reveals that the entire n^+ poly cathode appears to be emitting. The Al contact prevents transmission, but appears to provide uniform current flow through the cathode.

The EL spectra of this device was measured by collecting light using lenses and focusing the light into a monochrometer. The result is shown below in figure 8. Emission at the peak is approximately 1.9 eV, which corresponds to a 652 nm wavelength. The EL observed is a yellowish-orange, which agrees with the measured result.

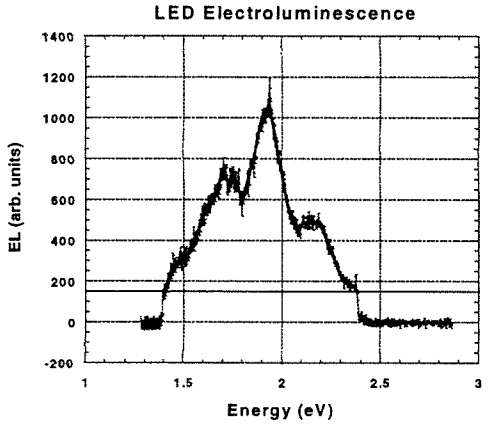

Fig. 8 - EL spectra from a 900°C anneal, p- layer, with Al top contact sample. Interference effects are noticeable; possibly due to the poly layer.

V. Conclusion

An optimized porous silicon LED was not achieved, however the best device to date at RIT was fabricated. The passivation of the PSi (porous silicon) layer was found to be necessary for luminescence. A 900°C anneal was shown to provide reasonable luminescence without over-oxidation. The p^+ surface layer, used to provide a low porous surface for the poly cathode deposition, appears to degrade both luminescence and electrical transport. A thin p^- layer (nanoporous material) showed promising results. The device that demonstrated the best uniformity, stability, and rectifying behavior was a 900°C annealed p^- surface with an aluminum top contact. The Al was also found to have a greater stability than indium-tin-oxide (ITO).

Additional work requires further investigation and optimization near this design space. Several factors have been narrowed, or eliminated. The device showed reasonable characteristics, however it is a ways away from a commercial device.

VI. Acknowledgments

I would like to thank Karl Hirschman and the department of Microelectronic Engineering at RIT for supporting this work. I hope this helps Karl move one step closer to achieving his Ph.D.

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