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Interpretation and Physical Modeling of Electronic Transport and Defect States in IGZO Thin-Film Transistors

Muhammad Salahuddin Kabir
mk7565@rit.edu

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Interpretation and Physical Modeling of Electronic Transport and Defect States in IGZO Thin-Film Transistors

by

Muhammad Salahuddin Kabir

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Kate Gleason College of Engineering

Rochester Institute of Technology
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Muhammad Salahuddin Kabir

Committee Approval:

We, the undersigned committee members, certify that we have advised and/or supervised the candidate on the work described in this dissertation. We further certify that we have reviewed the dissertation manuscript and approve it in partial fulfilment of the requirements of the degree of Doctor of Philosophy in Microsystems Engineering.

_____

Dr. Karl D. Hirschman Date
Professor, Electrical and Microelectronic Engineering

_____

Dr. Bruce W. Smith Date
Professor, Microsystems Engineering

_____

Dr. Santosh Kurinec Date
Professor, Electrical and Microelectronic Engineering

_____

Dr. Michael Pierce Date
Associate Professor, School of Chemistry and Material Science

_____

Dr. Robert G. Manley Date
Committee Member, Corning Incorporated

_____

Dr. Christopher Lewis Date
Associate Professor, External Committee Member

Certified by:

_____

Dr. Stefan Preble Date
Director, Microsystems Engineering Program

ABSTRACT

Kate Gleason College of Engineering
Rochester Institute of Technology

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Author: Muhammad Salahuddin Kabir

Advisor: Karl D. Hirschman

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This work is a comprehensive study on the interpretation and modeling of electronic transport behavior and defect states in indium-gallium-zinc-oxide (IGZO) TFTs. Key studies have focused on advancing the state of IGZO TFTs by addressing several challenges in device stability, scaling, and device modeling. These studies have provided new insight on the associated mechanisms and have resulted in the realization of scaled thin-film transistors that exhibit excellent electrical performance and stability. This work has demonstrated the ability to scale the conventional inverted staggered IGZO TFT down to one micron channel length, with excellent on-state and off-state performance where the $V_T \approx 1$ V, $\mu_{eff} = 12$ cm^2/Vs, $I_{leak} \leq 10^{-12}$ A/μm and SS ≈ 160 mV/dec.

The working source/drain electrodes are direct metal contact regions to the IGZO, which requires several microns of gate overlap to provide ohmic behavior with minimal series resistance and ensure tolerance to overlay error. New results utilizing ion implantation for self-aligned source/drain regions present a path towards submicron channel length. This strategy offers a reduction in channel length as well as

parasitic capacitance, which translates to improvement in RC delay and associated voltage losses due to charge-sharing. The realization of self-aligned TFTs using boron ion implantation for selective activation was introduced in a first-time report of boron-doped IGZO.

Cryogenic measurements made on long-channel devices has revealed temperature-dependent behavior that is not explained by existing TCAD models employed for defect states and carrier mobility. A completely new device model using Silvaco Atlas has been established which properly accounts for the role of donor-like oxygen vacancy defects, acceptor-like band-tail states, acceptor-like interface traps, and a temperature-dependent intrinsic channel mobility. The developed model demonstrates a remarkable match to transfer characteristics measured at T = 150 K to room temperature. A power-law fit for the $\mu_{ch} = f(T)$ relationship, which resembles $\mu \sim T^{+3/2}$ behavior consistent with ionized defect scattering. The mobility model is expressly independent of carrier concentration, without dependence on the applied gate bias. The device model is consistent with a compact model developed for circuit simulation (SPICE) that has been recently refined to include on-state and off-state operation.

While IGZO is the only AOS technology mature enough for commercialization, the effective electron channel mobility $\mu_{eff} \sim 10$ cm^2/Vs presents a performance limitation. Other candidate AOS materials which have higher reported channel mobility values have also been investigated; specifically, indium-tungsten-oxide (IWO) and indium-gallium-tin-oxide (ITGO). These investigations serve as preliminary studies; device characteristics support the claims of high channel mobility; however the influence of defect states clearly indicates the need for further process development. The advancements realized in IGZO TFTs in this work will serve as a foundation for these alternative AOS materials.

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LIST OF ACRONYMS

Acronym	Meaning
TFT	Thin-Film Transistor
OLED	Organic Light Emitting Diode
a-Si:H	Amorphous Hydrogenated Silicon
PECVD	Plasma Enhanced Chemical Vapor Deposition
ELA	Excimer Laser Anneal
IGZO	Indium Gallium Zinc Oxide
LTPS	Low Temperature Polycrystalline Silicon
BG, TG, DG	Bottom-Gate, Top-Gate, Double-Gate
S/D	Source-Drain
TCAD	Technology Computer-Aided Design
SA	Self-Aligned
IWO	Indium Tungsten Oxide
ITGO	Indium Tin Gallium Oxide
GIDL	Gate Induced Drain Leakage
TEOS	Tetraethyl Orthosilicate
HMDS	Hexamethyldisilazane
DIBL	Drain Induced Barrier Lowering
DOS	Density of States
CBM	Conduction Band Minima
VBM	Valence Band Maxima
PBS, NBS	Positive Bias Stress, Negative Bias Stress
NBIS	Negative Bias Illumination Stress
TABL	Trap Associated Barrier Lowering
ALD	Atomic Layer Deposition
BTS	Band Tail States
UST	Universal Schottky Tunneling
PhAT	Phonon Assisted Tunneling

Chapter 1. INTRODUCTION

With the advancement in display technology more stringent manufacturing and performance requirements are necessary. Large area uniformity, low-temperature compatibility, transparency to visible lights are some of the major concerns. Several challenges emerge with the growing requirements of next generation displays. They are more observable in high pixel density display and fast switching speed applications. Both require TFTs with high mobility semiconductor for an improved current drive to minimize delay times [1]. In OLED displays a small threshold voltage (V_T) shift of 0.1 V is enough to change the brightness by 20% [2]. Compensations circuits are used to counteract these instabilities which increase the fabrication cost and time. The on/off current ratio is an important parameter since on current determines the rate at which the pixels are charged, and the off current establishes the required refresh rate of a pixel.

1.1 THIN-FILM TRANSISTORS (TFTS)

The first thin-film transistor was proposed and patented in 1933 [3] but it was not realized until 1963, when P.K. Weimer at RCA laboratory fabricated the first TFT using CdS [4]. The first active-matrix LCD (AMLCD) using CdSe TFTs was demonstrated in 1973 [5]. The demonstration of TFT using a-Si for AMLCD applications gained worldwide attention for the next few decades [6], [7].

1.2 OVERVIEW

Amorphous hydrogenated silicon (a-Si:H) is widely used in the display industry for the past three decades as the channel material for TFTs. It is low temperature compatible and can be deposited using plasma enhanced chemical vapor deposition (PECVD) below 350°C. Due to its amorphous structure the large area electrical uniformity is good. Also, it is a well understood and low-cost material.

Table 1-I:Alternative candidates for replacement of a-Si:H.

	a-Si:H	**ELA-LTPS**	**IGZO**
Microstructure	Amorphous	Polycrystalline	Amorphous
Mobility ($cm^2/V \cdot s$)	~1	>100	~10
Device Type	NMOS	CMOS	NMOS
Process Complexity	Low	High	Low
V_T Uniformity	Good	Poor	Good
V_T Stability	Poor	Good	To be improved
Challenges	Performance	Yield, Scalability	Reliability

However, the research community has been investigating alternative materials to replace the a-Si:H due to its limitation in low electron mobility as shown in Table 1-I. The growing market for flexible and transparent display application has increased demand of large area display with higher resolution, low power consumption, lighter and faster electronic devices. Two most probable candidates are low temperature polycrystalline silicon (LTPS) and amorphous oxide semiconductors (AOS).

Although the low temperature polysilicon (LTPS) shows a large increase in field-effect mobility (μ_{FE}), the electrical uniformity is very poor due to its grain boundaries in crystalline structure. To mitigate this issue amorphous metal oxide semiconductors have been considered due to both their high mobility and large-scale uniformity. Their conduction path is mainly comprised of s-orbitals contributed by heavy metal cations. The large overlap between neighboring s-orbitals makes them insensitive to bond distortion and allows band conduction to occur, even in an amorphous material [8].

Zinc oxide garnered interest as one of the first oxide semiconductors, unfortunately the polycrystalline structure of the film caused uniformity issue on large scale. Amorphous oxide semiconductor (AOS) eliminates this limitation due to its non-crystalline nature. AOS devices also exhibit very low-leakage current because it benefits from a wide bandgap. However, several challenges with AOS TFTs must be resolved before it is widely adopted in the flat panel display (FPD) industry. Some of these challenges include gate bias instability [9]–[11], illumination stress instability [12], thermal instability [13], hot carrier effects [14].

Since the first report in 2004 by Nomura et al., amorphous IGZO has established itself as the most researched AOS [15]. Deposition techniques for IGZO films include sputtering [16], PLD [17], solution-based technique [18], [19]. They are expected to have better uniformity compared to LTPS with low cost of manufacturing. IGZO can have a uniform amorphous state owing to the multiple metal oxides having different lattice structures [8]. The mobility of IGZO increases with increase in the concentration of Indium and decrease with Gallium. However, increasing Indium content and decreasing Gallium concentration also causes the problem of stability due to oxygen vacancies [20]. Studies conducted by Nomura et al. on the composition of the material is shown in Figure 1.1.

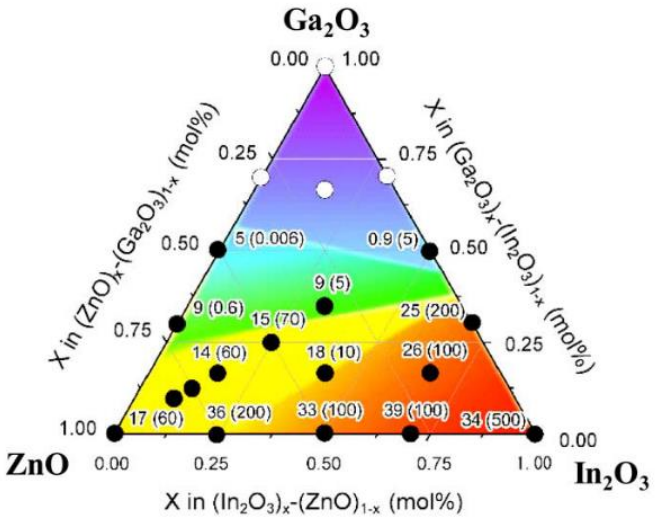
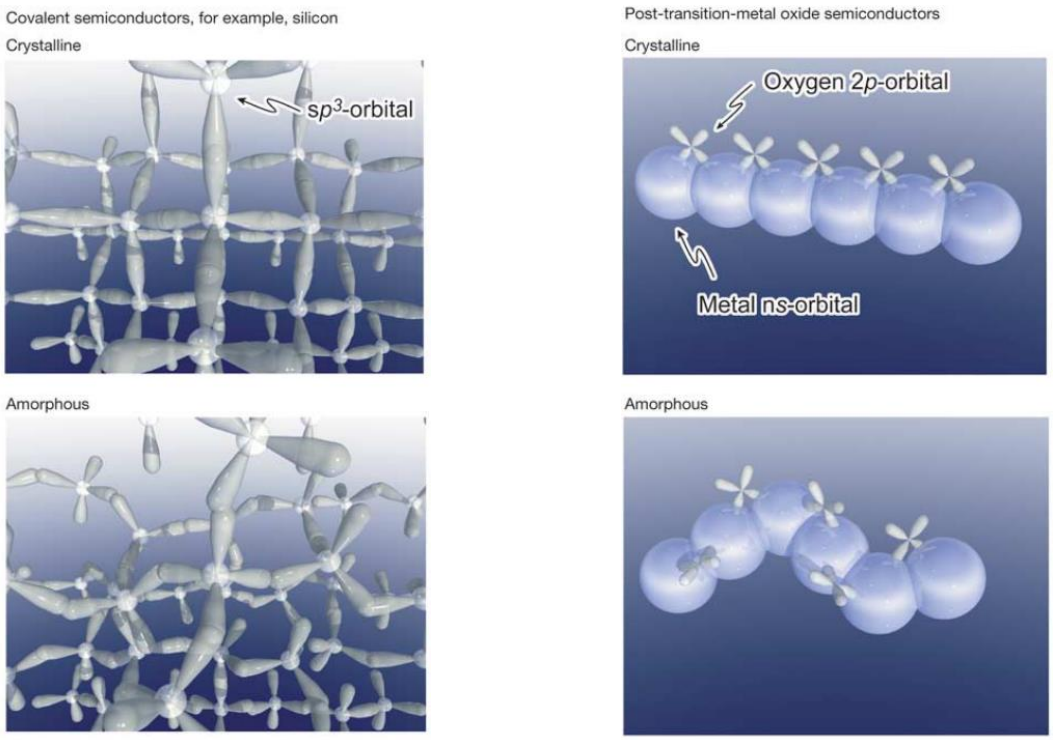


Figure 1.1: Room-temperature Hall mobility and carrier concentration as functions of chemical composition. Values outside and inside parentheses show Hall mobility in cm^2/Vs and carrier concentration in $\times 10^{18}$ cm^{-3}, respectively [20].

Since Ga_2O_3 is more stable due to a stronger bond between Ga and O, the addition of Ga improves the reproducibility and stability [20], [21]. Like ZnO, the conductivity of IGZO is also attributed to oxygen vacancies and conductivity can be increased by the addition of hydrogen [22]. Although used different composition of IGZO have been used, IGZO with 1:1:1:4 ratio is most widely used because of the improved stability over other compositions [20].

The outermost electronic configuration of the metal cation in IGZO is $(n-1)d^{10}ns^0$ [15]. The outermost 's' orbitals have large radii as well as spherical symmetry which render significant overlap with adjacent orbitals possible irrespective of any disorder. Even the amorphous state exhibits high mobility owing to the efficient transport path which is shown in Figure 1.2b. This type of overlap is absent in a-Si:H, which have highly directional sp^3 covalent bonding as shown in Figure 1.2a.



(a) (b)

Figure 1.2: Schematic of conduction in (a) Si and (b) AOS. Adapted from [15].

Several display companies have joined to develop this type of TFTs and have demonstrated a variety of prototype displays adopting oxide semiconductor including electronic papers [23], liquid crystal displays [24], and organic light-emitting diode displays. High electron mobility, low processing temperature, electrical uniformity, low leakage current, compatibility to a-Si TFT fabrication process, transparency to visible light, and compatibility with flexible substrates are some of the main properties of IGZO which make it the most promising candidate to be adopted in the next generation displays.

1.3 MOTIVATION

With the growing expectations of customers, display technology is moving rapidly and innovative solutions are needed for the next generation technology. Among all the material options IGZO has been proven to be the most viable replacement for a-Si:H. Advantages include but are not limited to process compatibility with existing technology, amorphous channel has large scale uniformity advantage, low temperature processing allows for flexible electronics integration, and optical transparency provides a high aperture ratio. Different TFT electrode configurations (bottom gate-BG, top gate-TG, double gate-DG) can be utilized for suitable applications. However, the main issue with IGZO TFTs is the instabilities caused by thermal stress, bias stress, illumination stress. Thus, it is necessary to understand the mechanisms to realize stable IGZO TFTs. Scaling the channel length (e.g. $L \leq 2$ μm) and integrating the devices on glass or flexible substrates can have major impact on the display industry. To achieve submicron IGZO TFTs, self-aligned strategy can be explored where the channel length is not defined by the metal S/D distance but the gate dimension. Self-aligned devices also have reduced parasitic capacitances which will be advantageous to implement as the backplane of the display structure. Next-generation AOS materials such as IWO and ITGO have added benefits such as higher mobility and lower annealing temperature respectively, however they also come with additional challenges.

1.4 GOALS OF THIS STUDY

The goal of this study can be broadly categorized as establishing a foundation for IGZO TFTs that demonstrates high performance, good stability, scalability to short channel dimensions, supports backplane integration, and provides a solid understanding of the fundamentals of device operation.

The following listing summarizes the key accomplishments achieved in each component/element of investigation.

- Performance of thermal stress tests on IGZO TFTs with different gate-electrode configurations and identify thermal stress instabilities. Deposition of a capping layer on the back-channel passivation of IGZO TFTs was implemented to reduce the thermal stress induced instability.
- A TCAD material model refined for passivated devices by incorporating interface defect states and validated by predicting the behavior at different temperatures which is verified experimentally. A hypothesis based on TCAD simulation is proposed for the electrical modeling of DIBL-like behavior and suppressed through modifications in process integration.
- Fabrication of scaled IGZO TFTs with channel length as small as L = 1 μm: This includes process modification including dielectric material & thickness, passivation thickness, annealing ambient & temperature, and contact metallurgy. The devices show enhancement-mode BG device operation with steep subthreshold characteristics and excellent stability.
- Source/drain activation using plasma immersion and ion implantation: Experiments with treatment-last and anneal-last activation on SA devices and evaluate results via electrical characterization. Development of an integration strategy for coplanar TG TFT, inverted-staggered BG TFT: process for SA-BG devices on silicon and glass substrates, with refined experiments on SA-BG devices.
- Initial investigations of IWO and ITGO as next-generation channel materials: This includes process development for thin-film deposition, process integration, thin-film characterization, TFT fabrication and experiments with annealing ambient.

1.5 DOCUMENT OUTLINE

In this document, the first chapter provides the motivation behind the investigation into amorphous oxide semiconductor TFTs. The remainder of the document is organized as follows:

Chapter 2 outlines the baseline BG TFT fabrication process for unpassivated and passivated devices. Then the default Atlas IGZO model (TCAD) is presented which matches well with unpassivated TFT behavior after minor modification. However, the physical model of the passivated device required significant modifications to match device operation which is described.

Chapter 3 discusses some complex behaviors observed in IGZO TFTs. Hypothesis based on the extensive experimental data is presented and supported by Atlas TCAD simulation established in Chapter 4. Encapsulation of finished TFT is investigated for stability against thermal and bias stress treatments.

Chapter 4 is dedicated to the TCAD model refinement of the TFT operation using Silvaco® Atlas™. Default IGZO material model is used for predicting the current-voltage characteristics. The influence of different defect states on the TFT behavior is discussed which helps in understanding the underlying physics behind the device operation. The material model is adjusted to match with the experimental data at different temperatures. Interface defect states are added to the IGZO material model to develop an understanding of the passivation process for IGZO TFTs. Charge transport behavior in IGZO is studied using low-temperature measurements down to 10 K.

Chapter 5 discusses the process development for scaled IGZO TFT. Refinement in both BG dielectric and passivation is described in detail. Associated changes in annealing ambient is necessary as this is intimately related to the passivation film. The scaled devices show superior

performance in terms of SS, I_{on}/I_{off}, and thermal and gate bias stress stability. The established process is fully compatible with glass substrates which is necessary for the intended application in display technology. Chapter 6 is dedicated to self-aligned IGZO TFT process development.

Chapter 7 shows preliminary investigation into next-generation AOS materials. Process development for IWO sputtering is discussed in detail, establishing the impact of oxygen partial pressure, target conditioning, and passivation annealing on TFT characteristics. An initial study on ITGO is also presented, with TFT characteristics demonstrating dependence on the oxygen partial pressure during sputter deposition.

Chapter 8 concludes the thesis by providing a summary of key contributions with suggestions on further work.

Chapter 2. IGZO TFT FABRICATION & DEVICE MODELING

Defect states play multiple roles which establish both conductive properties of the material as well as anomalies in device behavior. Therefore, the interpretation of these states is of considerable importance. This chapter details the fabrication processes of bottom-gate IGZO TFT and electrical characterization. The initial discussion establishes a baseline process with and without passivation material added to the back-channel interface. Next focus is to characterize the electronic defect states in IGZO film for its application in thin film electronics through TCAD modeling using Silvaco® Atlas™.

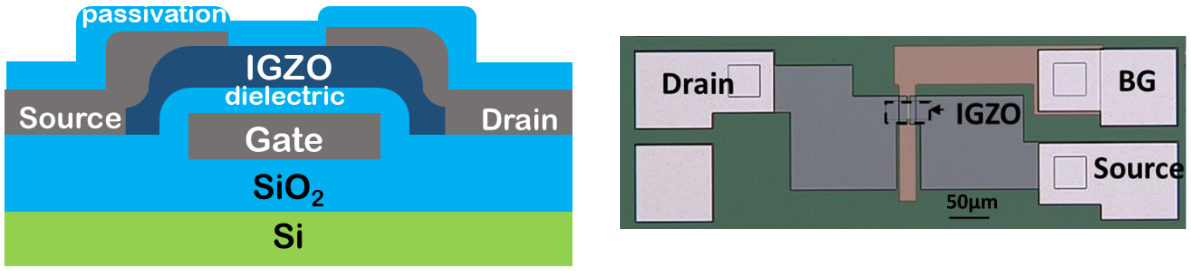
2.1 BASELINE BG TFT

IGZO TFTs were fabricated in BG configurations on a thick isolation oxide (~500 nm SiO_2) thermally grown on silicon wafers. A 50nm Mo gate electrode was sputtered and patterned, followed by a 100 nm SiO_2 gate dielectric deposited by PECVD (TEOS precursor, 390 °C). The SiO_2 was densified in N_2 ambient for 2 hours at 600 °C in furnace.

The channel material IGZO was deposited in an Applied Materials Centura RF sputter system in a single wafer, load-locked chamber using 12.8 inch $InGaZnO_4$ target with a substrate chuck temperature of 200 °C. The deposition pressure was established ~2.3 mT and the sputter power was ramped to 600 W with a 50 W/s rate to avoid any initial shock to the target; subsequently the

power was increased to 750 W for film deposition. The wafers were prebaked at 200 °C in a separate chamber before IGZO sputter for desorption of any water molecules on the surface. A 50 nm IGZO layer was sputtered (dep rate ~0.7 nm/s) using an $InGaZnO_4$ (1:1:1:4) target in an argon ambient with 7% oxygen. The IGZO mesa was patterned and etched using dilute HCl. Source/drain electrodes were then defined using sputtered Mo/Al bilayer with a lift-off technique. At this point the devices can be used as unpassivated BG device after an anneal in N_2 at 400 °C for 30min and opening the gate and source/drain contact regions using 10:1 buffered HF.

For passivated devices a second 100 nm PECVD SiO_2 layer was then deposited as the passivation material after the source/drain lift-off. This was followed by an 8-hour O_2 anneal at 400 °C with a 2-hour controlled ramp-down in O_2 ambient. Here, Figure 2.1(a) shows the cross-section schematic of a passivated BG TFT and Figure 2.1(b) shows a top-down view of the fabricated device.



(a) (b)

Figure 2.1: (a) Cross-section schematic of a passivated BG TFT, unpassivated BG device does not have the passivation on top, (b) top-down view of the fabricated BG device

Electrical testing was done on TFT structures using a B1500 semiconductor device parameter analyzer. TFT channel dimensions are as indicated. All I_D-V_{GS} transfer characteristics presented were taken with a gate voltage up-sweep and medium measurement integration time unless otherwise noted, with low-drain and high-drain bias conditions at 0.1 V and 10 V, respectively.

The anneal for this passivated device with 100nm SiO_2 is very long (10 hours with ramp down) and is a bottleneck for high volume manufacturing in industry. Additional investigation to minimize the anneal time and associated parameter changes is discussed in Chapter 5.

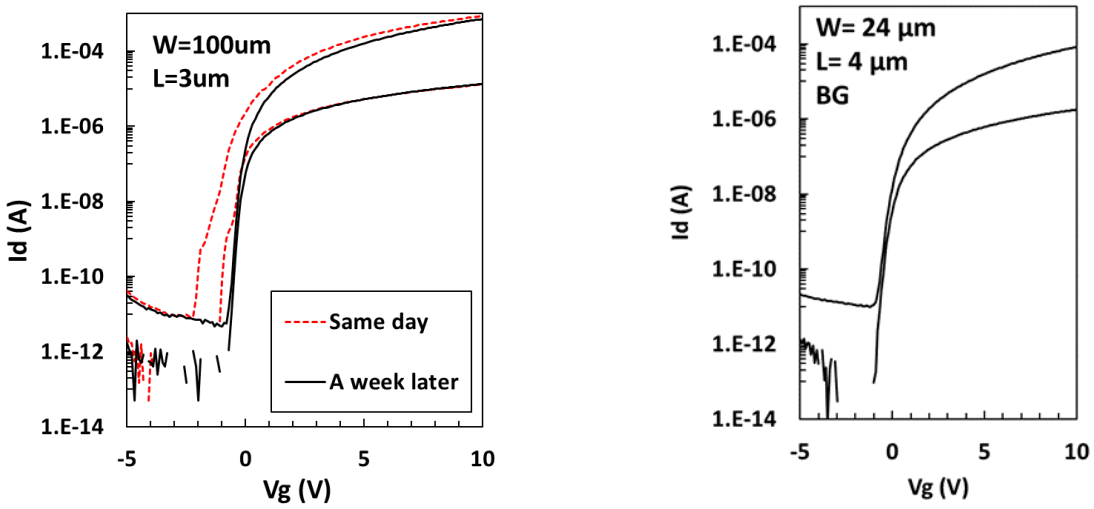


Figure 2.2: Transfer characteristics of IGZO TFTs with BG configuration (a) Unpassivated [25] & (b) Passivated device [26]. Drain bias conditions are 0.1V and 10V.

The unpassivated TFT shows distortion and DIBL-like behavior when tested immediately after fabrication. The DIBL like behavior is removed through a ripening process and is channel length dependent as shown in Figure 2.2a. The detail of this DIBL-like behavior is explained in 3.2. The passivated device shows negligible DIBL effect at a channel length of L=4µm as seen in Figure 2.2b. To further understand the underlying electrical mechanisms and effect of defect states on IGZO TFTs, a complementary study using TCAD simulation is discussed next. Table 2-I shows an objective comparison of different device parameters for poor, good, and excellent electrostatic behavior.

Table 2-I: Objective comparison of select device parameters that reflects specified electrical behavior.

Parameter	Poor	Good	Excellent
V_T (V)	-5	0	+1
SS (mV/decade)	500	200	120
$I_{leakage}$ (A/μm)	10^{-8}	10^{-10}	10^{-12}
μ_{eff} (cm^2/Vs)	5	10	12

2.2 TCAD MODELING OF IGZO TFTS

IGZO exhibits n-type conductivity due to the presence of defects, i.e., oxygen vacancies (V_O). The process variables may contribute to the defect levels and degrade the transistor characteristics; therefore, it is important to understand the influence of these defects on device operation. Device simulation captures the influence of each variable on the transistor operation independently. Furthermore, it allows visualization of various physical effects such as the potential distribution in the TFT channel region and defect state occupancy, which assists in understanding the underlying physics of defect mechanisms.

There has been a significant amount of work published on the extraction of defect state parameters by applying analytical solutions to measured C-V and I-V characteristics on TFT structure [27]–[29] however, such models do not differentiate between bulk-film defects and interface defects (e.g. fixed charge, interface traps) which may dominate non-ideal behavior [27], [30]. Analytical solutions are mathematically very complex and require several assumptions and simplifications to reach to a closed form solution, which is not required for TCAD simulation.

Amorphous materials have a high density of sub-gap states due to incomplete bonding, random arrangements of atoms and variations in bonding angle [31]. The Atlas TFT module allows the

energy distribution of states to be defined, which is essential for accurate simulation of disordered material systems such as IGZO.

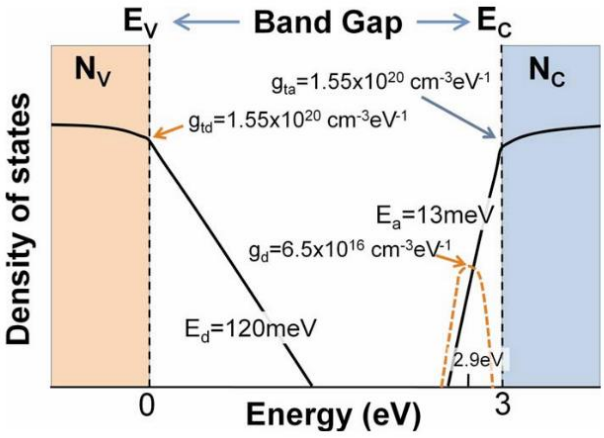


Figure 2.3: Proposed DOS model for IGZO. E_C and E_V are conduction and valence band edge energies, respectively. Solid curves within the bandgap represent the exponentially distributed band-tail states (g_{CBa},g_{VBd}), while the dash curve near the conduction band edge represents the Gaussian-distributed donor like O_V states (g_{Gd}) [32].

Amorphous semiconductor trap states can be donor-like or acceptor-like and are described by exponentially decaying band-tail states, and deep states following a Gaussian distribution as shown in Figure 2.3. The following four functions serve as the mathematical definition of the trapping mechanisms in a disordered channel film for a TFT. For the numerical analysis in ATLAS, these densities of states are defined as [33]:

$$g_{TA}(E) = N_{TA} \exp\left(\frac{E - E_C}{W_{TA}}\right) \quad 2.1$$

$$g_{TD}(E) = N_{TD} \exp\left(\frac{E_v - E}{W_{TD}}\right) \quad 2.2$$

$$g_{GA}(E) = N_{GA} \exp\left[-\left(\frac{E_{GA} - E}{W_{GA}}\right)^2\right] \quad 2.3$$

$$g_{GD}(E) = N_{GD} \exp\left[-\left(\frac{E-E_{GD}}{W_{GD}}\right)^2\right] \quad 2.4$$

- $g_{TA}(E)$ and $g_{TD}(E)$ represent the density of acceptor-like conduction band-tail states and donor-like valence band-tail states, respectively
- E_c and E_v are energy levels at the conduction band (CB) and valance band edge (VB)
- N_{TA} (N_{TD}) is the density of acceptor-like (donor-like) states in the tail distribution at the conduction band (valence band) edge
- W_{TA} (W_{TD}) is the characteristic decay energy of conduction (valance) band-tail states
- $g_{GA}(E)$ and $g_{GD}(E)$ represent the density of acceptor-like and donor-like states (oxygen-vacancies, V_O)
- N_{GA} (N_{GD}) is the peak value for acceptor-like (donor-like) states, defining a Gaussian distribution
- E_{GA} (E_{GD}) is the mean energy defining a Gaussian distribution for acceptor-like (donor-like) states
- W_{GA} (W_{GD}) is the standard deviation of Gaussian distribution for acceptor-like (donor-like) states.

Once the DOS is defined using Equations 2.1-2.4 the density of ionized acceptor and donor like states is given by [33]:

$$p_T = \int_{Ev}^{Ec} g_{TA}(E) \cdot f_{TA}(E,n,p)dE + \int_{Ev}^{Ec} g_{GA}(E) \cdot f_{GA}(E,n,p)dE \quad 2.5$$

$$n_T = \int_{Ev}^{Ec} g_{TD}(E) \cdot f_{TD}(E,n,p)dE + \int_{Ev}^{Ec} g_{GD}(E) \cdot f_{GD}(E,n,p)dE \quad 2.6$$

Where, $f_{TA}(E,n,p)$ and $f_{GA}(E,n,p)$ are the ionization probabilities for the tail & Gaussian acceptor states and $f_{TD}(E,n,p)$ and $f_{GD}(E,n,p)$ are the ionization probabilities for the donor states.

The above equations for ionized trap states consider a continuous distribution of defect states. When using discrete energy levels, the integral terms are replaced by summations over the number of discrete energy levels, defined by *NUMA* and *NUMD* for acceptor and donor states respectively.

$$p_T = \sum_{i=0}^{NUMA} \left(f_{TA}(E_i,n,p). \int_{-\infty}^{+\infty} g_{TA}(E)\, dE + f_{GA}(E_i,n,p). \int_{-\infty}^{+\infty} g_{GA}(E)\, dE \right) \quad 2.7$$

$$n_T = \sum_{i=0}^{NUMD} \left(f_{TD}(E_i,n,p). \int_{-\infty}^{+\infty} g_{TD}(E)\, dE + f_{GD}(E_i,n,p). \int_{-\infty}^{+\infty} g_{GD}(E)\, dE \right) \quad 2.8$$

The default model parameters used in Atlas for IGZO material are given in Table 2-II. The DOS distribution is shown in Figure 2.4, using the parameters from Table 2-II.

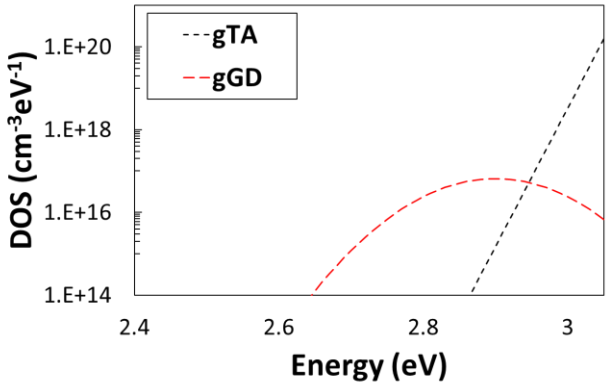


Figure 2.4: Density of states (DOS) distribution in the energy gap of IGZO in Atlas simulation. Here, gTA is the acceptor like tail states near the conduction band and gGD represents the donor like gaussian behavior due to oxygen vacanies close to the conduction band.

Table 2-II: Model parameters used for IGZO material. The notation in brackets is consistent with the earlier notations used e.g. V_O for oxygen vacancies.

Symbol	**Atlas default Value** [32]
Band gap	3.05 eV
Electron affinity	4.16 eV
Relative permittivity	10
Intrinsic Electron mobility	15.0 $cm^2/V{\cdot}s$
Vo (Gaussian)	
N_{GD} (N_{Vo})	6.5×10^{16} $cm^{-3}eV^{-1}$
E_{GD} (E_{Vo})	2.9 eV
W_{GD} (W_{Vo})	0.1 eV
Band-Tail States	
N_{TA} (CB_{TN})	1.55×10^{20} cm^{-3} eV^{-1}
W_{TA} (CB_{WN})	0.013 eV

The distribution of electrons in the conduction band is given by the product of the effective conduction band density states (N_C) and probability of state occupancy by an electron. The equation is given in 2.9:

$$n = N_C f(E_C) \qquad 2.9$$

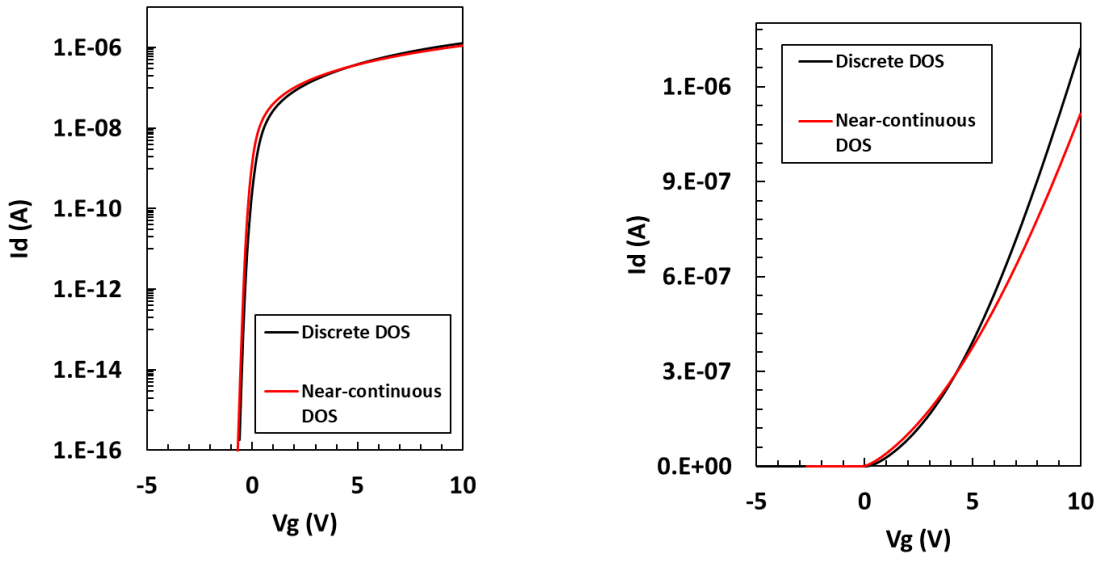
Where $f(E_C)$ is the Fermi function which defines the probability of state occupancy at E_C and N_C

is the effective conduction band DOS which establishes the electron concentration as a function of E_F. N_C is a direct input parameter in Atlas simulation which is dependent on the effective electron mass (m_e^*) of the semiconductor and is given by equation 2.10 [32]. The default model uses NC300=N_C (@300 K) = 5×10^{18} cm^{-3} which is the calculated value consistent with m_e^*=0.34m_0. However, in Atlas the NC300 and m_e^* are separate degrees of freedom as model inputs.

$$NC300 = N_C\,(@300K) = 2\left(\frac{2\pi m_e^* kT}{h^2}\right)^{\frac{3}{2}} = 2.51\text{x}10^{19}\,(m_e^*/m_0)^{1.5}\,cm^{-3} \qquad 2.10$$

$$N_C = \left(\frac{T}{300\text{ K}}\right)^{\frac{3}{2}} NC300 \qquad 2.11$$

For solutions with a continuous distribution of defect states, Atlas defaults to mathematical interpolation and equations 2.5 and 2.6 are solved by optimizing the run-time/accuracy loss trade-off. Thus, defects defined by a discrete trap states distribution is used with optimized settings of 128 and 64 levels (discrete) for acceptor and donor states, respectively, which balanced the trade-off between accuracy and simulation run-time [32].



(a) (b)

Figure 2.5: Comparison of simulated electrical characteristics with number of discrete levels in (a)log scale and (b)linear scale. Although there is negligible difference, the discrete DOS is used hereafter to minimize run-time.

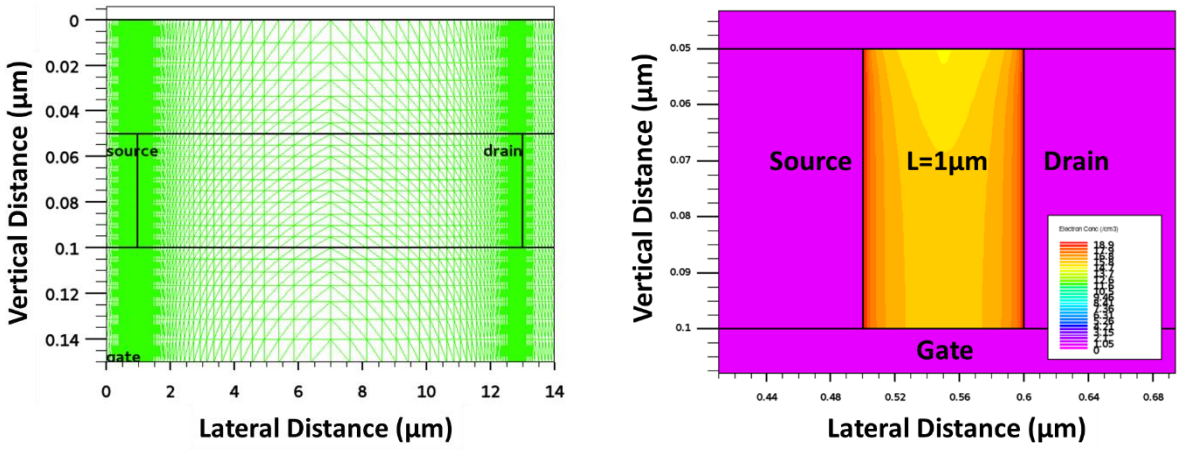
Increasing the number of these levels to 512 (near-continuous DOS) drastically increased the simulation run-time by a factor of twenty (e.g., 3 hours vs. 10 min) with a negligible difference in simulation results as shown in Figure 2.5. Additional material model parameters were defined to represent electrical properties. A constant-mobility model was used which is taken to be independent of doping concentration, carrier densities and electric field. The Schottky contact model was used to define the effective contact potential between the contact metal and IGZO. Regarding carrier statistics, the Fermi-Dirac model was implemented to account for degenerate semiconductor behavior [32].

2.2.1 Simulation Structure

The TCAD structure film thicknesses are consistent with actual fabricated device described in 5.3. The device structure and mesh configuration used for simulation are shown in Figure 2.6a, with modifications in source/drain regions (*e.g.*, contact dimensions, gate overlap) that enabled reasonable simulation time without compromise in simulation accuracy. This mesh configuration takes the channel length into account for finer mesh calculation and is scalable. The gate and S/D overlap of 1 µm is used. In fabricated TFTs this overlap is 10 µm, however, decreasing it to 1 µm did not change the simulation results. Therefore, an overlap of 1 µm is used to reduce the simulation time. A channel length of L=12 µm is used for comparison with experimental results. It should also be noted that, in Atlas we have used a horizontal structure where the SD contact regions are connected at the sides of the channel material to observe various electronic properties (potential, DOS, electron concentration) using the horizontal cutline.

Molybdenum was used as the gate metal defined by the work function (ϕ_M = 4.53 eV). For S/D contact regions the metal work function is set to ϕ_M = 4.13 eV (ϕ_M of aluminum) to accurately

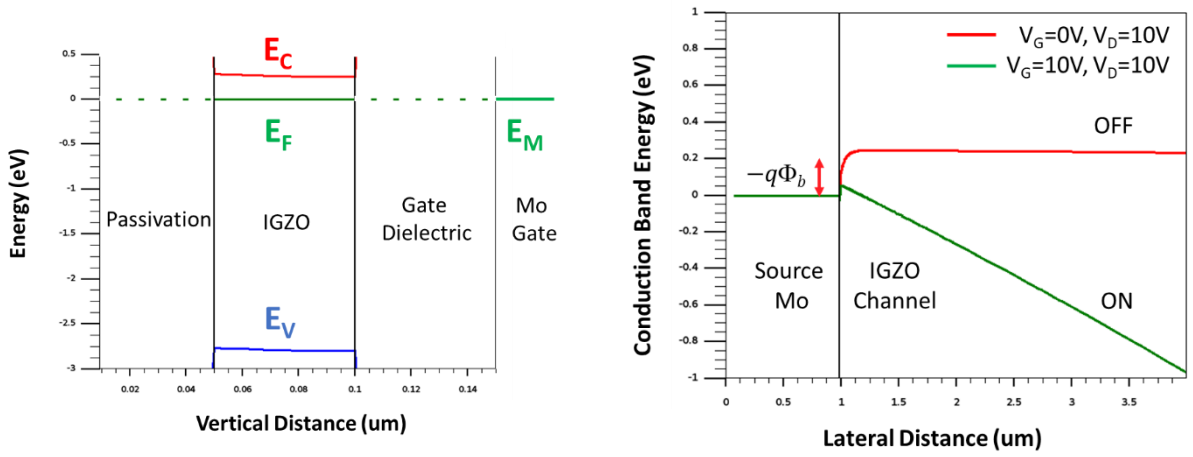
represent the true M-S contact which is dominated by interface states and demonstrates ohmic behavior. The electron concentration across the IGZO channel, for the default defect distribution, is shown in Figure 2.6b for zero bias condition. Due to difference in metal work-function, the IGZO regions below S/D show accumulation of electrons near the contacts. The Mo gate electrode creates slight accumulation region at the gate dielectric interface for the same reason.



(a) (b)

Figure 2.6: (a) Cross-section of BG TFT structure showing the mesh used for simulation.Finer mesh is used in IGZO channel and at IGZO/SiO_2 interface for improved accuracy. The channel length is 12 µm and gate & S/D overlap is 1 µm. (b) Electron concentration contours in IGZO channel (L=100nm, scaled for illustration only) for zero bias condition. The default defect distribution is used. Higher electron density near the S/D metal (aluminum) is due to the M-S workfunction difference.

Energy band diagram is given in Figure 2.7a which shows the different energy levels for conduction band (E_C), valence band (E_V), Fermi level (E_F) and metal level (E_M) for V_D=V_G=0V. Here the configuration is a bottom gate, and the dielectric is located at the interface between IGZO channel and bottom gate metal Mo, where the passivation and dielectric both are SiO_2. In Figure 2.7b the conduction band energy near the source end of the device shows the conditions at high drain bias (V_{DS}=10V) for V_{GS}=0V and V_{GS}=10V.



(a) (b)

Figure 2.7: (a) Energy band along the thickness of the device showing conduction band (E_C), valence band (E_V), Fermi level (E_F), metal level (E_M) where $V_{DS}=V_{GS}=0V$, the electron concentration is ~$10^{-14}cm^{-3}$ and (b) Conduction band energy near the source end of the device showing for $V_G=0$ & 10V at high drain bias ($V_{DS}=10V$).

2.2.2 Default Atlas model

Fung et al. reported a 2D model of IGZO TFT where the calculated results show that the channel has a very sharp conduction band-tail slope distribution (E_a=13 meV) and ohmic-like S/D contacts are operative with very low contact resistance i.e., 2.7×10^{-3} ohm-cm^2 [32]. In Atlas, the default IGZO model employs the values reported in [32] by Fung et al. which is given in Table 2-II. For unpassivated BG device, decreasing the N_{VO} value from 6.5×10^{16} cm^{-3}eV^{-1} to 2.0×10^{16} cm^{-3}eV^{-1} shifted the I_D-V_{GS} characteristics towards right. Reducing the mobility value from 15.0 cm^2/Vs to 12.7 cm^2/Vs gave a perfect overlay of simulation with the experimental data, both in linear and saturation mode as shown in Figure 2.8. The TCAD parameters used for modified unpassivated device is given in Table 2-III.

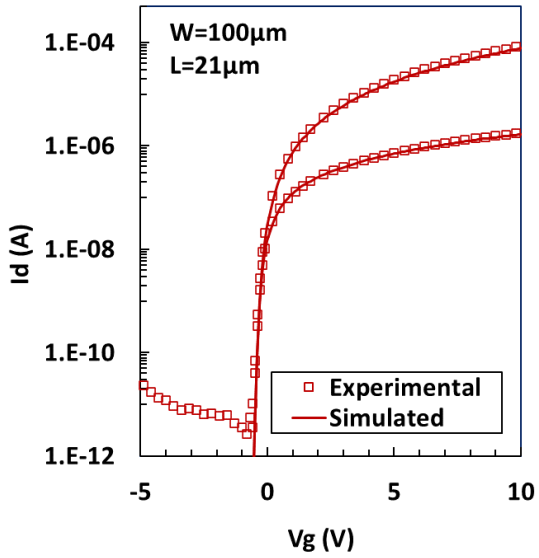


Figure 2.8: Unpassivated TFT showing excellent match with TCAD simulated characteristics using modified unpassivated TCAD parameters from Table 2-III [25].

However, when these values are used to simulate a passivated bottom-gate IGZO TFT with L=12 um and W=24 um it does not match well with the experimental results as shown in Figure 2.9. As seen from Figure 2.9 the simulated characteristic does not have the pronounced concave upward behavior as is expected from AOS TFTs. The band-tail states are responsible for this concave upward behavior. When V_{GS} increases, the E_F moves closer to Ec and the acceptor like tail states start filling by trapping the accumulated electrons. This results in a lower level of accumulation charge and lower transconductance (g_m) until the electron traps are full.

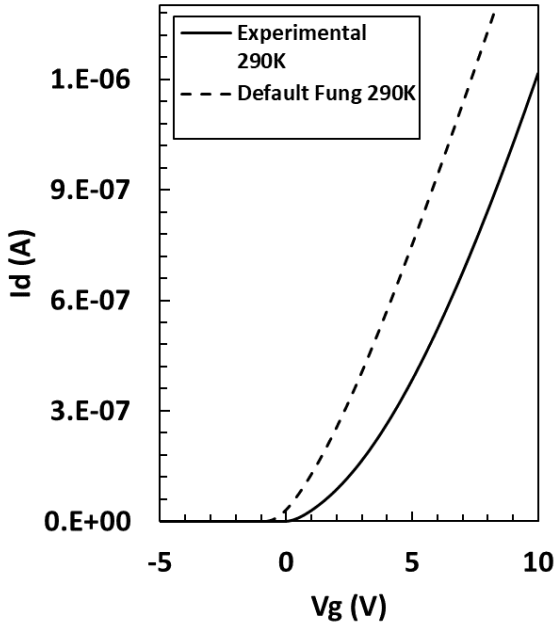


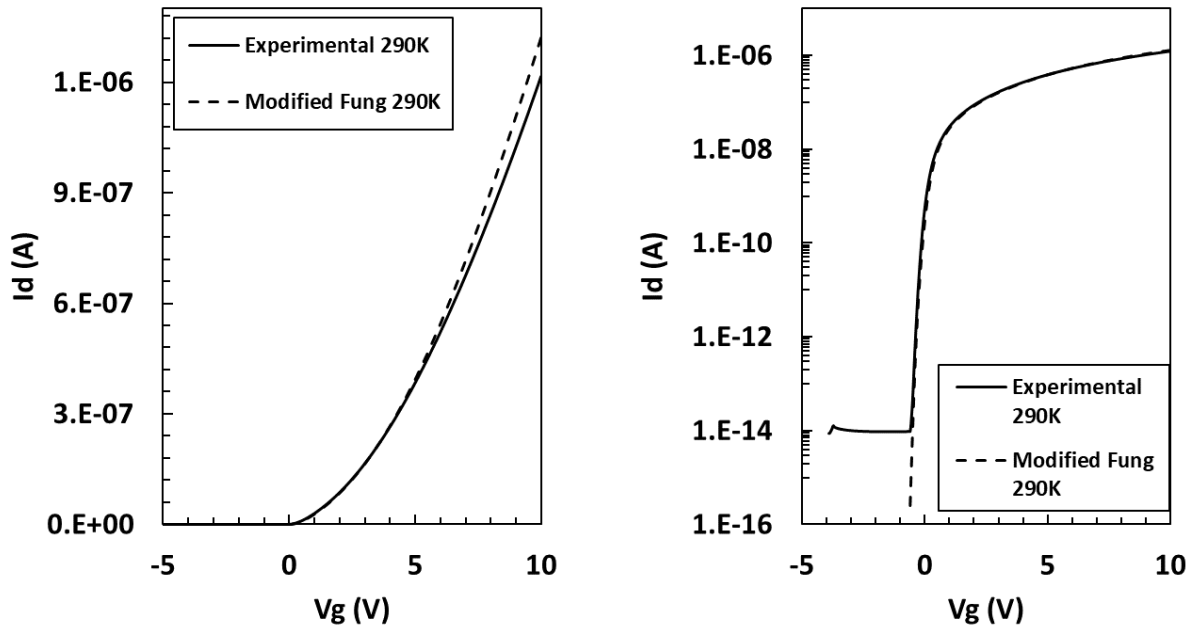
Figure 2.9: Using default Atlas IGZO parameters in Table 2-II, comparison between experimental and simulated I-V at 290K.

2.3 MODIFIED IGZO ATLAS MODEL

After adjusting the N_{TA} and W_{TA} parameters and increasing the intrinsic mobility to 19 cm^2/Vs the simulated results matched reasonably with experimental behavior at room temperature as shown in Figure 2.10. Also fixed charge $Q_f/q=5\times10^{10}$ cm^{-2} was included to match with the experimental V_T. In addition, acceptor like IT states *i.e.,* $NTA_{IT}=5\times10^{13}$ $cm^{-2}eV^{-1}$ and $WTA_{IT}=0.07$ eV, are included to match up the subthreshold behavior. Figure 2.10 shows the comparison between experimental and simulated I-V characteristics with modified passivated parameters from Table 2-III. While the parameter values for the characteristic match cannot be uniquely solved, an extensive investigation in model refinement has arrived at these values; details of which will be presented in Chapter 4.

Table 2-III: Modified IGZO ATLAS model parameters for unpassivated and passivated device

Symbol	**Atlas default Value** [32]	**Modified unpassivated device value** [34]	**Modified passivated device value [This work]**
Band gap	3.05 eV	3.05 eV	3.05 eV
Electron affinity	4.16 eV	4.16 eV	4.16 eV
Relative permittivity	10	10	10
Intrinsic Electron mobility	15.0 $cm^2/V{\cdot}s$	12.7 $cm^2/V{\cdot}s$	19.0 $cm^2/V{\cdot}s$
Vo (Gaussian)			
N_{GD} (N_{Vo})	6.5×10^{16} $cm^{-3}eV^{-1}$	2×10^{16} $cm^{-3}eV^{-1}$	2×10^{16} $cm^{-3}eV^{-1}$
E_{GD} (E_{Vo})	2.9 eV	2.9 eV	2.9 eV
W_{GD} (W_{Vo})	0.1 eV	0.1 eV	0.1 eV
Band-Tail States			
N_{TA} (CB_{TN})	1.55×10^{20} cm^{-3} eV^{-1}	1.55×10^{20} cm^{-3} eV^{-1}	3.25×10^{20} cm^{-3} eV^{-1}
W_{TA} (CB_{WN})	0.013 eV	0.013 eV	0.02 eV
Interface States			
NTA_{IT}	-	-	5×10^{13} cm^{-2} eV^{-1}
WTA_{IT}	-	-	0.07 eV
Q_F/q	-	-	5×10^{10} cm^{-2}



(a) (b)

Figure 2.10: Comparison of experimental vs simulated passivated I-V with using modified passivated parameters from Table 2-III.

2.4 SUMMARY

Comprehensive understanding of IGZO material is key to successful TFT fabrication. Thus, this chapter extends the understanding of unpassivated TFT characteristics using the default Atlas model and details the modification necessary for passivated device. Here, the details of band-tail states and oxygen vacancy defect is discussed. Although the unpassivated TFT show a great match to the simulated device using default IGZO Atlas parameters, the passivated device show significant mismatch. After adding interface trap states and modifying band-tail states, a reasonable match is achieved between experimental and simulated results. The details of modified passivated TFT device TCAD modeling is discussed in much detail in Chapter 4.

Chapter 3. DEFECT PASSIVATION & STABILITY OF IGZO TFTS

IGZO TFTs are very prone to degradation due to different stress mechanism i.e., thermal stress [13], bias stress [35], illumination stress [36] or combinations of different stresses [37]. Before they are widely adopted a better understanding of the defect states related to the instability of the TFTs is needed. This chapter will discuss the passivation of defect states, improving thermal stress stability, and bias stress stability.

3.1 LITERATURE REVIEW

Although IGZO TFTs exhibit large scale uniformity and higher mobility when compared to a-Si:H, the stability is very poor for unannealed TFTs [38]. Annealing in oxidizing ambient is crucial to control the semiconducting behavior of IGZO. It has been found that the electrical conductivity increases with annealing temperature up to 300℃ and then starts decreasing in a pure oxygen ambient [39]. This is indirect evidence that O_2 does not have sufficient oxidizing power to passivate the defects below 300℃.

Gate bias stress tests have been performed to examine the stability of different gate electrode configurations [40]. The instabilities in unpassivated bottom gate devices primarily originates from the exposed back-channel surface to the atmosphere. This exposed surface adsorb/desorb oxygen and water molecules [41], [42]. This issue is solved by using a dense, gas-tight passivation layer. The modern IGZO TFTs consists of this passivation layer made of SiO_2 [40], SiN_x [43], TiO_x [44]. For annealed IGZO TFTs the bias stress resulted in a parallel shift, i.e. the mobility and *SS* are not changed. This behavior has been explained using the formation of deep traps which inhibit the density of free electron in the channel. The bias stress induced degradation of IGZO is attributed to the charge trapping effect. The ΔV_T follows a stretched exponential given by equation 3.1 as follows:

$$\Delta V_T = V_0\{1-\exp[-(t/\tau)^{\beta}]\} \qquad 3.1$$

Where, ΔV_T is the V_T shift after stress, $V_0 = V_g - V_T$, t is stress time, τ represents the characteristic trapping time constant, and β is the stretched-exponential exponent. Furthermore, $\tau = \tau_0 \exp(E_{\tau,trap}/kT)$ represents the characteristic trapping time of carriers, $E_{\tau,trap}$ is the average effective energy barrier that electrons in the IGZO TFT channel need to overcome for injection into the insulator, k is the Boltzmann's constant, and τ_0 is the thermal pre-factor for emission over the barrier [14].

Thermal stress instability is another issue for IGZO TFTs as the subsequent steps might require a high temperature environment. Also, for the reliability of the devices they should withstand a high temperature for a long period of time. The proposed mechanism is discussed in detail in section 3.3.

Illumination stress testing is also very important for IGZO TFTs because of their use in FPDs.

As shown in Figure 3.1, IGZO TFTs respond to photon energies above 2.3 eV which is below the band gap of IGZO (3.05 eV). As the threshold photon energy correspond well to the sub-gap density of states (DOS) energies above valence band maxima (VBM), it is thus credited to the electron excitation from the deep sub-gap states to the conduction band [45].

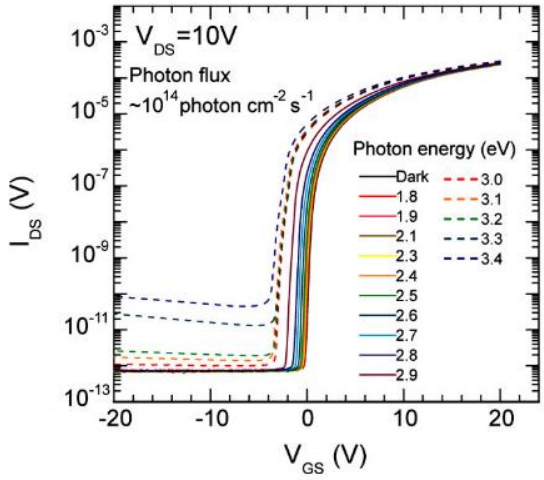


Figure 3.1 Transfer characteristics of IGZO TFTs in dark and under monochromatic light illumination with photon energies ranging from 1.8 eV to 3.4 eV (λ=700-365 nm). Adapted from [45].

This effect is enhanced when negative bias stress is also applied along the illumination also known as NBIS stress. In [12], a hole trap model has been proposed to explain the NBIS instability where the photoexcitation occurs from valence band to electron sub-gap traps. These electrons are localized at the sub-gap traps and holes are transported in a gate-channel interface or a gate insulator trap. Another mechanism was considered but with the Fermi level in the channel much higher in the band gap (i.e., around 2.5 eV above VBM) for the usual electron density and small sub-gap DOS near conduction band minima (CBM). As this cannot explain the excitation to electron traps, a sub-gap photon excitation is considered where it is from the deep sub-gap DOS to the conduction band [21].

3.2 TRAP ASSOCIATED BARRIER LOWERING (TABL)

The readiness of IGZO surface to interact with the ambient air is responsible for non-ideal electrical response observed in transistors such as threshold voltage shift under room ambient storage [38], bias-stress induced instabilities [46] and other distortions observed in transfer characteristics [47]. One such non-ideal electrical response is the separation of low and high drain bias transfer characteristics in the subthreshold region which is reminiscent of drain induced barrier lowering (DIBL) observed in conventional MOSFETs. Figure 3.2 shows the DIBL-like behavior in the transfer characteristics of an unpassivated long channel bottom-gate (BG) device tested immediately after annealing (dashed line). This behavior has been presented in literature, but the issue has been generally omitted from discussion or assigned to short-channel behavior even when the channel dimensions are in the range of several microns [48]. From TCAD simulation with the IGZO material model, including interface traps, and the physical device structure parameters, DIBL should not become apparent until the channel length is scaled below 1 μm [26]. Therefore, a proper understanding of the underlying physical mechanism behind this phenomenon in "long" channel IGZO devices is required.

It has been hypothesized that the physical origin of this behavior is due to the inhomogeneous distribution of donor-like interface trap states at the IGZO back-channel, creating macroscopic domains of different charge density [40], [49]. At high drain voltage, the drain overcomes the potential barriers associated with passivated back-channel regions, thus allowing device turn-on at a reduced gate voltage. The dependence of transistor turn-on voltage on drain bias results in DIBL-like behavior, referred to as "Trap Associated Barrier Lowering (TABL)". This behavior eventually disappears if the unpassivated back-channel is exposed to air, which is akin to a ripening

process and thus referred to hereafter. However, TABL remains stable if present on passivated devices. The subsequent sections present a comprehensive investigation on TABL, supported by TCAD simulation. Modifications to the annealing conditions and process integration details have also rendered TABL negligible on BG devices.

3.2.1 IGZO Back-Channel Ripening

Figure 3.2 shows the transfer characteristics of an unpassivated long-channel (L≥12µm) BG device tested immediately after 400°C O_2 anneal showing TABL, with perfect subthreshold overlay of low and high drain bias conditions following the ripening process over two days in room air. While an electrical model has not been previously proposed, this observed improvement in device performance over time has been reported and attributed to desorption of H_2O [47] or elimination of process induced defects. While these mechanisms may be operative in certain cases where moisture is present or specific processes are used (i.e. plasma etching [50]), TABL exhibited by the passivated device in Figure 3.3 tested immediately following a 400 °C anneal cannot be related to either of these issues. Note that devices stored in vacuum after the annealing process did not exhibit any improvement over time, which confirms that the ripening process relies on exposure of the IGZO back-channel to the air ambient. The ripening time required to eliminate TABL in unpassivated devices was observed to be channel length dependent. For a long-channel (L≥12µm) device one day of ripening appeared sufficient, whereas a scaled TFT typically required a week. The behavior is also statistical in nature, for example 90% devices may show TABL when tested immediately after annealing, however the percentage drops down to 10% after a day of room ambient storage.

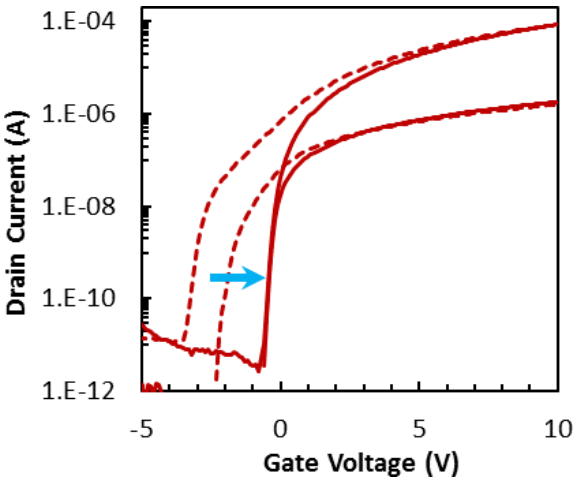


Figure 3.2: Transfer characteristics of an unpassivated TFT tested immediately after annealing (dashed line) showing TABL. After a two-day storage in room ambient the characteristics do not exhibit TABL (solid line)[40] .

The appearance of TABL in long-channel devices indicates that it is not a short-channel effect, and thus the mechanism would be expectedly different than DIBL. However, similar to DIBL the effect is observed to be channel length dependent. Figure 3.3 shows the TABL for BG passivated device. In this case the IGZO back-channel is not exposed to air and the ripening process is not operative; TABL remains stable indefinitely. The influence on passivated devices has been attributed to back-channel donor-like interface traps which remain following the SiO_2 deposition and annealing processes [40]. The long-channel passivated device demonstrates minor subthreshold separation and slope degradation, whereas the separation in the scaled TFT is more pronounced. The L = 3 μm TFT transfer characteristics in the Figure 3.3 inset show the severity of the distortions for scaled devices.

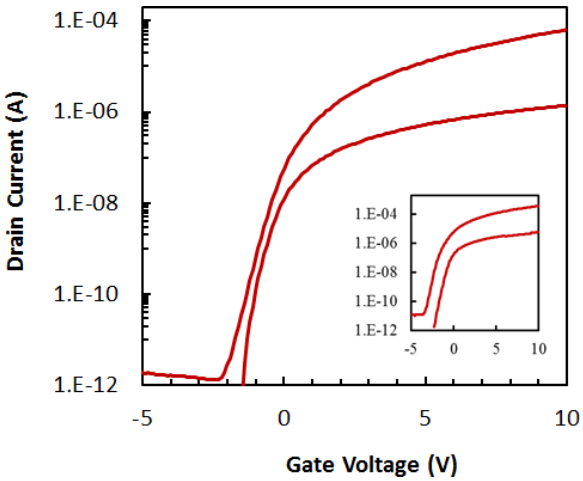


Figure 3.3: Measured data for a L=21 µm BG device with 100 nm SiO_2 passivation, showing TABL. Inset shows the transfer characteristics for L=3 µm device showing pronounced distortions for a scaled device [40].

Bottom-gate devices demonstrate weak control over back-channel interface traps, which indicates that the origin of TABL is at the IGZO back-channel surface/interface. To determine if TABL and ripening are surface phenomena, the unpassivated device shown in Figure 3.4 was partially etched in dilute HCl to remove the back-channel surface layer. Figure 3.4 shows associated transfer characteristics which reveal that TABL is re-established, appearing as a freshly prepared device. A two-day ripening period in air reversed the shift, separation and distortion, which infers that TABL and ripening are surface phenomena rather than changes in properties of the bulk IGZO film.

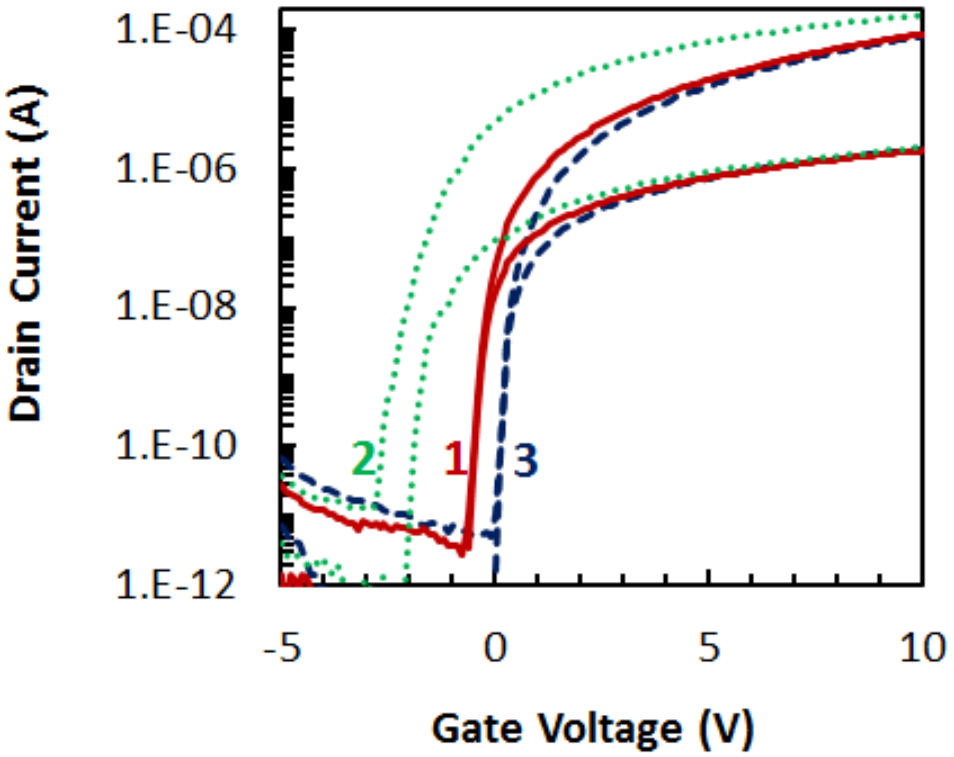
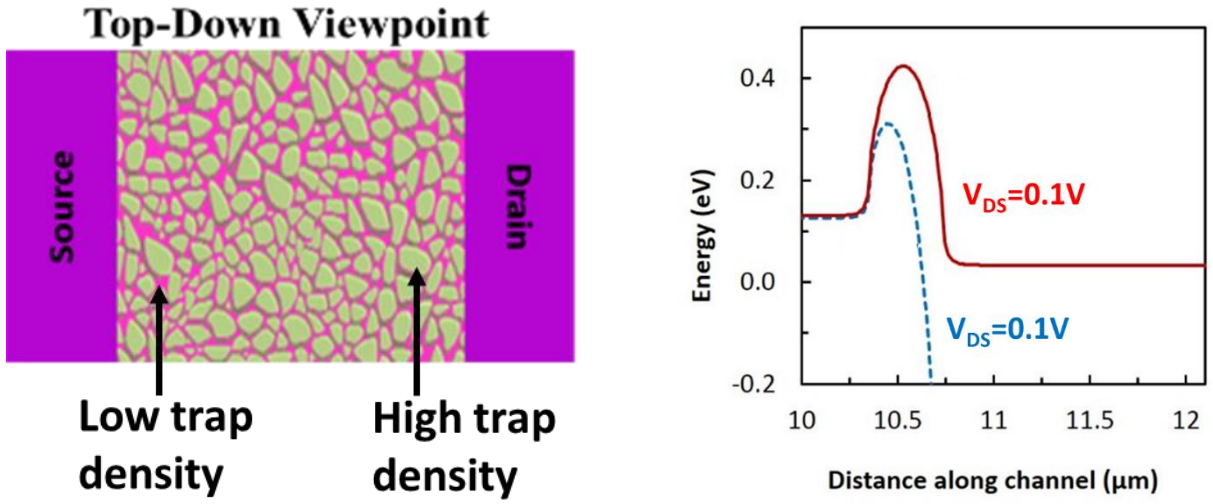


Figure 3.4: Ripened transfer characteristics (#1) as shown in Figure 3.2 followed by a partial etch of the IGZO back-channel surface, showing restoration of TABL behavior (#2). Characteristics measured after two days of ripening result in elimination of separation and distortion (#3). The shift between the initial and final ripened characteristics (#1 & #3) is attributed to the respective IGZO channel thickness[25] .

3.2.2 Hypothesis on the Mechanism of TABL

It is proposed that TABL is due to the inhomogeneous passivation of donor traps at the IGZO interface that presents regions with distinctly different effective charge levels. This results in a series/parallel network of channel regions to complete the electron pathway from source to drain. Figure 3.5a shows a schematic model of this concept.



(a) (b)

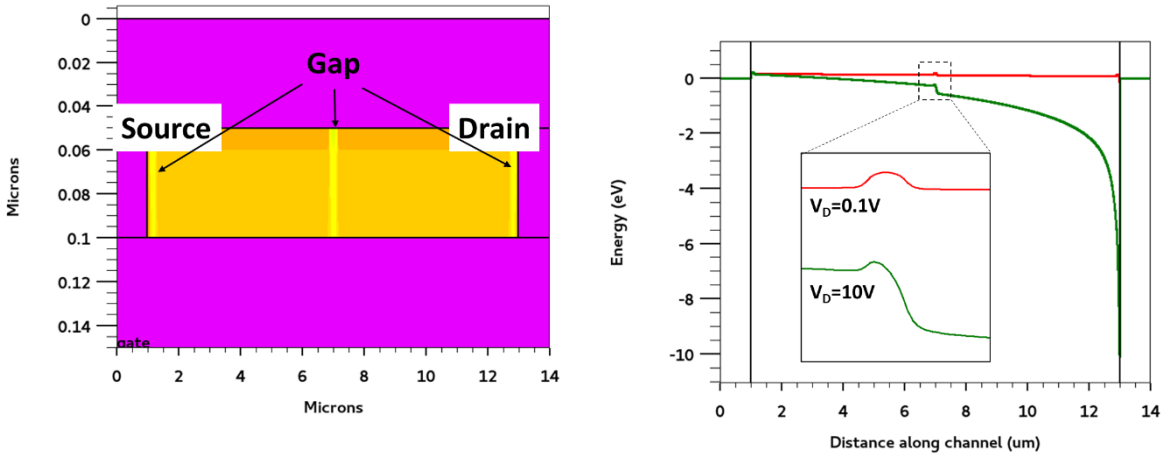
Figure 3.5: (a) Schematic model for the TABL origin, showing a cobblestone arrangement of donor-rich interface defect regions separated by low-charge gaps [40]. (b) Conduction band energy across the channel at low and high drain bias showing the barrier created by the low charge pocket (gap). At high drain bias (dashed line) the barrier is lowered [25].

Figure 3.5b shows the conduction band energy across the channel at low and high drain biases. At high V_{DS}, the drain dominates causing the lowering of barrier associated with back surface traps. This lowering of barrier results in an earlier turn-on at high drain bias. For low drain bias, the pockets of low charge dominate, and the device turns on at higher V_{GS}. This difference in turn-on voltage for low and high drain bias is revealed as TABL. The current flow is dominated by highly resistive (low back-channel surface charge) regions; a long channel device has a higher probability to create low-charge gap regions during a short ripening process time. During the ripening process back-channel interface traps are effectively passivated through interaction with air ambient at room temperature, presumably through adsorption of oxygen [39]. This may coincide with the displacement of H_2O at the back-channel surface, thereby resulting in simultaneous TABL suppression, steeper subthreshold, and a characteristic right-shift. The

ripening time dependence on channel length can be explained by a statistical distribution in the size of passivated back-channel surface regions. The ripening process can interrupt the interconnected pathway anywhere along the channel length, and thus is more favorable for long-channel devices. Scaled devices require a longer ripening time to widen passivated gaps, which also must compensate for higher lateral fields.

3.2.3 TABL Modeling

The inclusion of nanoscale regions within a device channel of several microns presents an inherent tradeoff between an accurate structural representation and numerical convergence. If donor-rich interface regions are separated from each other by narrow gap regions without donor states, then the accumulation of gaps can be represented by three gaps within the channel. TCAD structures for "gap" devices were developed using the same material and interface state models as used for passivated devices given in Table 2-III. The gaps are submicron region void of donor interface trap states positioned at the source/IGZO interface, middle of the IGZO back-channel, and the drain/IGZO interface as shown in Figure 3.6a. While the simulation model uses oxygen donor interface states to represent the donor-rich regions, another donor mechanism may be operative such as the incorporation of hydrogen [51] or water [42]. It should be noted that the acceptor like interface trap states are still present in the gaps. Figure 3.6b shows the conduction band energy across the channel at low and high drain biases. At high V_{DS}, the drain dominates causing the lowering of barrier associated with back surface traps. This lowering of barrier results in an earlier turn-on at high drain bias. For low drain bias, the pockets of low charge dominate, and the device turns on at higher V_{GS}.



(a) (b)

Figure 3.6: (a) Simplified structure for TCAD simulation, representing the low-charge gaps with 3-gaps in the channel. Note that the scales used for the X & Y axes are significantly different. (b) TCAD simulation of a 3-gap structure showing the trap associated conduction band energy barriers in distributed fashion, with V_{GS} = 0 V. The gap for each device is a 0.1 µm region void of V_O donor interface trap states (Scenario #1 from Table 3-I). TABL is clearly operative at high drain bias. The inset shows a zoomed in scenario of the middle gap.

3.2.4 TABL Progression of IGZO BG TFT

The backchannel just after annealing has interface traps (ITs) at the gate dielectric/IGZO interface and/or passivation/IGZO interface. Firstly, acceptor like exponential IT remain constant throughout the ripening process and is the same in the gaps and the regions between the gaps. Then the IT parameters i.e., $NTA_{IT}=5\times10^{13}$ $cm^{-2}eV^{-1}$ and $WTA_{IT}=0.07$ eV have been used in ATLAS to match the subthreshold characteristics with experimental data at room temperature. The TABL is due to donor like gaussian ITs between the gap regions known as high trap region. These integrated donor like IT states reduce with the ripening of the device and thus the TABL is reduced or completely removed. Here, we discuss the successive progression of TABL as seen in BG TFT with different integrated donor ITs using gaussian donor parameters as shown in Table 3-I. While the values chosen for interface trap density and gap spacing were for demonstration purposes, the

TCAD simulations model the TABL of the BG device characteristics quite well. The donor like IT states are kept at the same energy as the oxygen vacancy donors *i.e.,* EOV_{IT}=2.9 eV.

Table 3-I: TABL successive progression using ATLAS Simulation

Scenario #	**Gap (µm)**	**NOV_{IT} ($cm^{-2}eV^{-1}$)**	**EOV_{IT} (eV)**	**WOV_{IT} (eV)**	**Integrated IT (cm^{-2})**
1	0	4×10^{12}	2.9	0.4	2.6×10^{12}
2	0.1	4×10^{12}		0.4	2.6×10^{12}
3	0.2	2×10^{12}		0.4	1.3×10^{12}
4	0.4	1×10^{12}		0.2	3.9×10^{11}
5	0.5	5×10^{11}		0.1	1.2×10^{11}
6	1	5×10^{11}		0.1	1.2×10^{11}

It is assumed that the just annealed device has a high level of donor IT states throughout the backchannel with no gap. A higher value of donor IT (NOV_{IT}) and a wider spread (WOV_{IT}) would then give a realistic I-V behavior. Here the subthreshold is very shallow with a pronounced TABL as shown in Figure 3.7a. By including gap regions at the backchannel with the same ITs, the subthreshold can be improved since the total inhomogeneity is reduced throughout the channel. However, the TABL is much more pronounced since the integrated IT is very high.

As a next step, we increased the gap size and decreased the donor IT coefficient value. Both changes helped to reduce the TABL and decreased the SS. After that, another increment of gap size and reduction of coefficient with the added reduction of spread helped in making the TABL almost negligible as seen in Figure 3.7b.

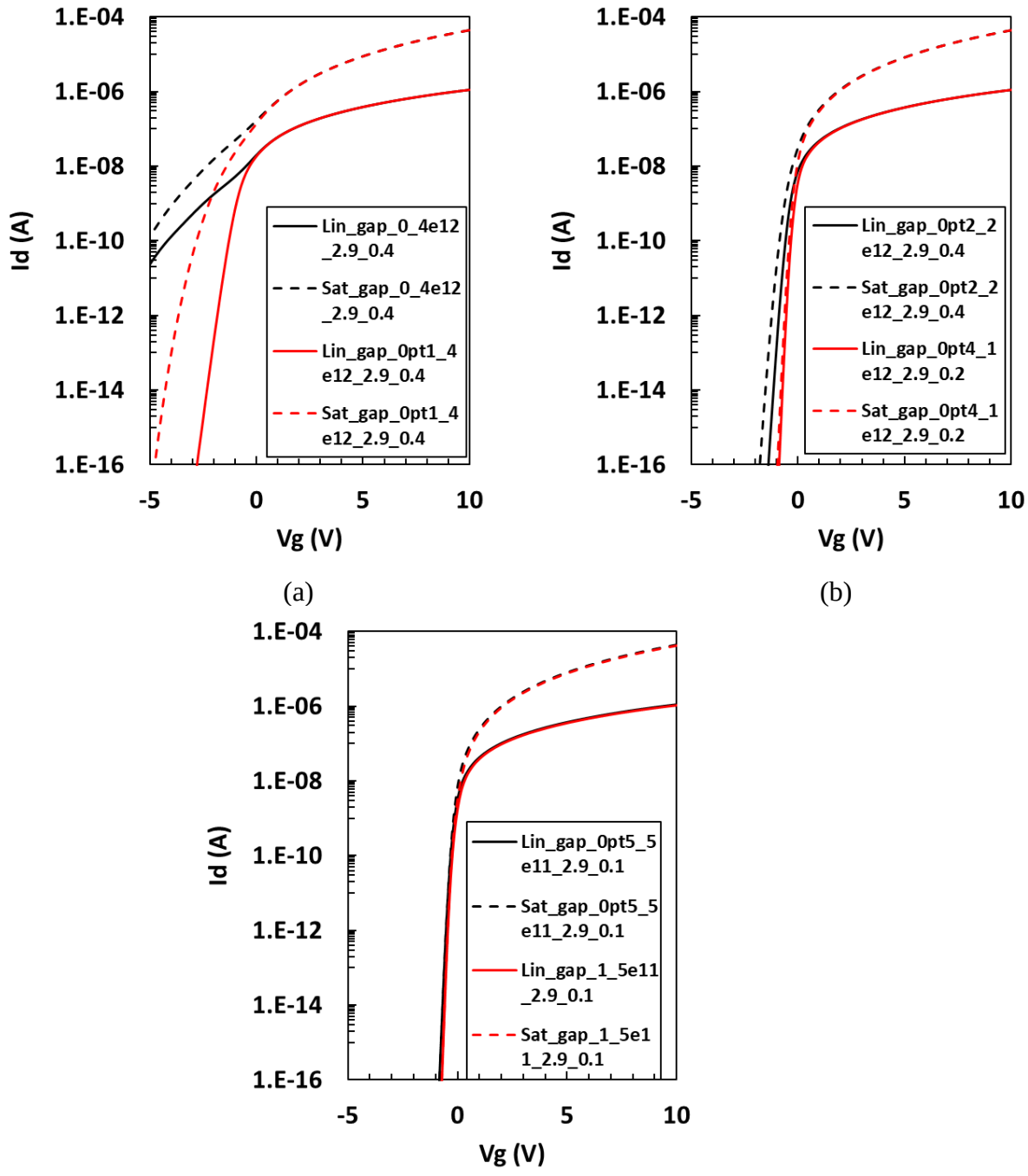


Figure 3.7: TABL scenario (a) #1 and scenario #2 , (b) scenario #3 and scenario #4 and (c) scenario #5 and scenario #6 from Table 3-I.

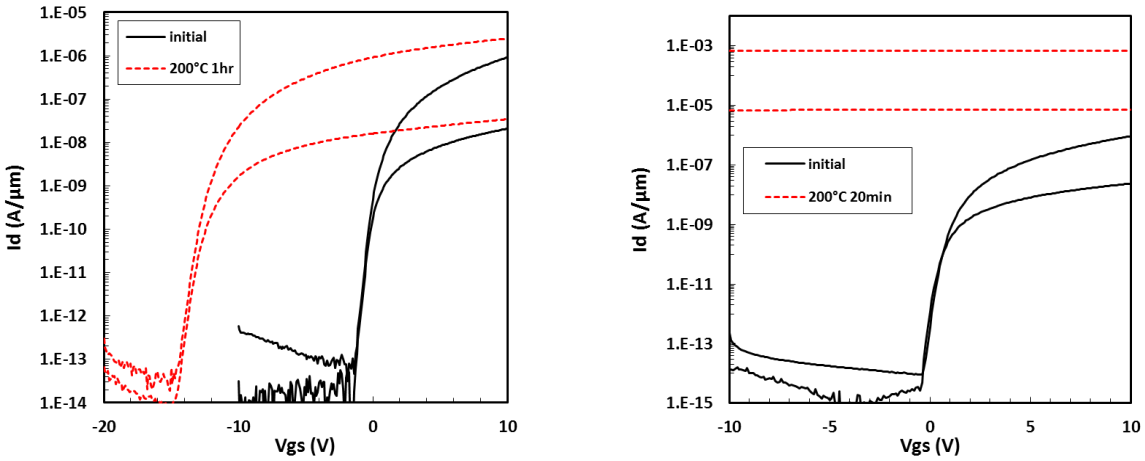
Now, if we increase the gap size further and reduce the coefficient and spread of the donor ITs the TABL is completely removed as seen in Figure 3.7c. Further increasing the gap size does not help with the TABL but it makes the SS lower. The TABL is negligible for extreme cases i.e., fresh device (all surface donor-traps) and ripened device (no surface donor-traps). Once the gap spacing is longer than a minimum distance, drain can no longer overcome the gap. Both low and high drain biases turn on at the same V_{GS}.

3.3 THERMAL STRESS STABILITY

Thermal stress stability of amorphous oxide semiconductor (AOS) TFTs is important as they may need to undergo high temperature processes even after completion. One such process would be chip-on-glass attachment, as the bonding mechanism require heat. Even though the initial characteristics may be stable upon completion, the performance might deteriorate upon subjecting the devices to future processes at elevated temperatures (e.g., $T \geq 100$ °C). To investigate the thermal stability of IGZO TFTs, devices are subjected to higher temperature for a long period of time.

Thermal stress instability is observed in both passivated double gate (DG) and bottom gate (BG) TFTs after the devices are subjected to elevated temperature. These devices are passivated with PECVD SiO_2 and a subsequent anneal at 400 °C is performed in O_2 ambient. The thermal stress instability is much more pronounced in DG than BG. Figure 3.8 shows the effect of a 200 °C hot plate bake on BG and DG TFTs with SiO_2 back-channel passivation. In the case of BG devices, a significant left shift in I-V characteristics was observed after an hour of stress. This effect was even more pronounced on DG devices which showed resistor-like characteristics following a 20-

minute hot plate bake. This observation was surprising, considering that the devices showed stable characteristics after the final passivation anneal at 400 °C.



(a) (b)

Figure 3.8: (a) BG and (b) DG L = 24 µm devices with SiO_2 back-channel passivation that demonstrate performance degradation or failure after 200 ℃ thermal treatment [13].

The PECVD silicon dioxide passivation layer is deposited using TEOS as a precursor, with process recipe details as follows: Power = 290 W, pressure = 9 Torr, TEOS flow (helium carrier)= 400 sccm, O_2 flow = 285 sccm. This PECVD oxide material was characterized in previous work using optical techniques and film stress measurements [52]. The film stress measured immediately after deposition was approximately +130 MPa (tensile), and over a time period of 20 days shifted to approximately -60 MPa (compressive). Changes in film stress of evaporated SiO_2 for optical coatings has been studied, with results showing a shift toward less compressive / more tensile during air ambient exposure over time [53]–[55].A chemical reaction between water vapor molecules and a porous SiO_2 structure is the proposed mechanism, involving the physical adsorption of water vapor molecules on the SiO_2 surface followed by a reaction of ad-species with Si and O atoms belonging Si–O–Si groups with weakened-bond sites. This proposed mechanism in evaporated oxide was supported by IR spectroscopy measurements showing an increase in the

concentration of Si–OH bonds with aging time. In contrast, the stress change in the PECVD oxide layer is in the opposite direction, shifting from tensile to compressive. High precision refractive index measurements were taken using a prism coupler technique, with an index value $n = 1.4429 \pm 0.0006$ ($\bar{x} \pm \sigma$) in comparison to $n = 1.4579 \pm 0.0001$ measured on a thermally grown SiO_2 layer. An index value n ~ 1 % lower than that of thermal oxide indicates a porous film, thus the observed change in stress may be due to the physical adsorption of water without involving a chemical reaction within the oxide material.

It is hypothesized that the IGZO TFTs show thermal instability due to the presence of H_2O within the SiO_2 passivation layer which can migrate to the interface between the passivation and the backchannel during thermal stress. Hoshino et al. demonstrated donor behavior in IGZO as a source of instability in unpassivated devices [47]. Both H_2O [46] and hydrogen [56] have been shown to have donor-like behavior in IGZO, thus supporting a higher level of electron channel charge. During thermal stress treatments on DG devices, it is proposed that H_2O at the interface of the top-gate aluminum reacts and forms AlO_x, liberating monatomic hydrogen [57] as depicted in Figure 3.9. The released hydrogen diffuses through the oxide layer to the SiO_2-IGZO interface and reacts with the IGZO surface/bulk. Experiments also revealed a channel length dependent phenomenon where relatively longer channel devices (i.e., L > 20 µm) started to degrade at lower duration of thermal stress compared to shorter devices which remained stable. This may be due to the extent at which water is removed from the back-channel region during the 400°C passivation anneal and is discussed further in section 3.3.3.

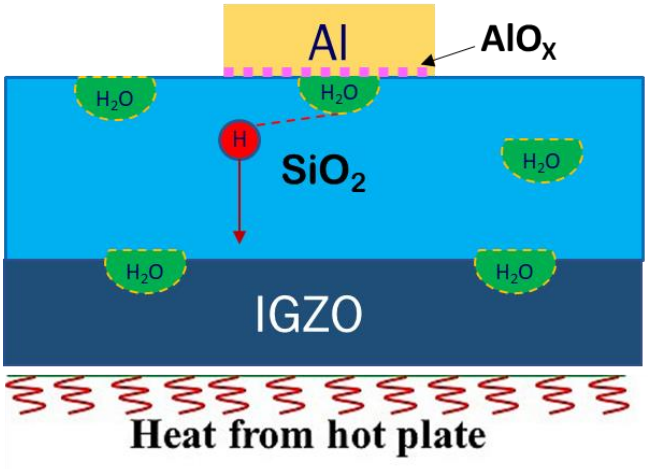


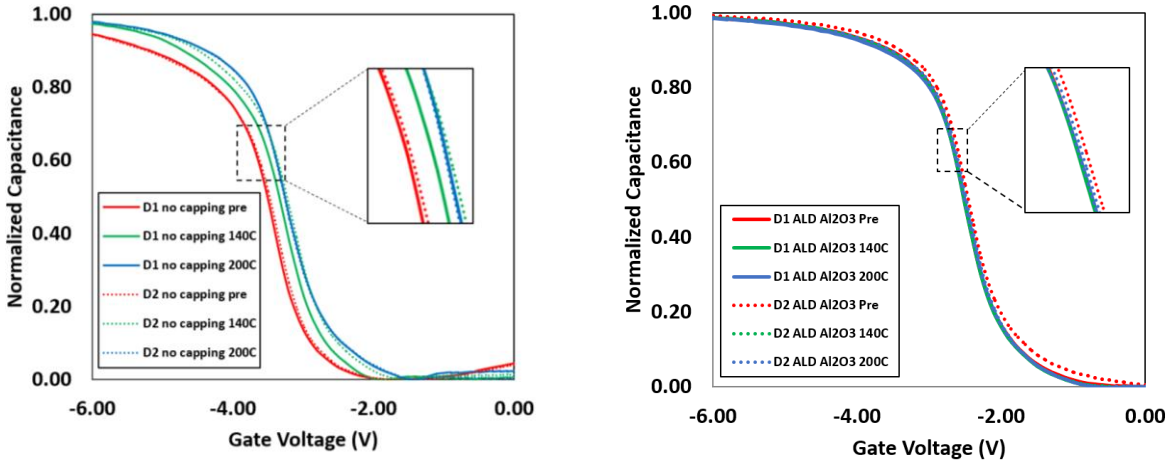
Figure 3.9: Proposed mechanism of thermal degradation. Monatomic hydrogen is generated by a reaction between H_2O and the top-gate metal in DG TFTs, and diffuses to the back-channel region [13]. AlO_X forming at the interface of the Al top gate and the passivation oxide.

3.3.1 MOSCAP Verification of Feasibility

A preliminary investigation was performed to establish the feasibility of the proposed thermal stress mechanism using silicon metal-oxide-semiconductor (MOS) capacitors. A major part of the proposed operative mechanism in the working hypothesis involves the availability of hydrogen. An investigation by sintering Si MOS capacitors (MOSCAPs) was done to further understand and verify the mechanism. Sintering is the process of annealing MOSCAPs at temperature T ~ 400 °C in forming gas (5% H_2 in N_2) to passivate interface traps with hydrogen. During this process any H_2O that is present in the oxide film can diffuse and react with the metal gate. This reaction effectively releases monatomic hydrogen which migrates to the Si-SiO_2 interface and is generally accepted as the primary mechanism operative in the passivation of interface traps [57].

Unsintered aluminum-gate MOSCAPs with and without a 10 nm thick capping layer of Al_2O_3 deposited using atomic layer deposition (ALD) in between the SiO_2 dielectric and gate electrode were investigated. The gate dielectric was the same PECVD process recipe as was used for IGZO back-channel passivation. The devices were subjected to a hot plate bake at 140-200 °C after metal

deposition to replicate the conditions seen for thermal stability experiments on IGZO TFTs. A flatband voltage (V_{FB}) shift $\Delta V_{FB} \sim 0.4$ V was observed on devices without a capping layer, as seen in Figure 3.10. With ALD Al_2O_3, they show almost zero V_{FB} shift after a 200 °C hot plate bake. This indicates there is some passivation of interface traps with hydrogen during the hot plate treatments on samples without capping, which is effectively suppressed on devices with the ALD Al_2O_3 capping layer. The lack of interface passivation with use of the Al_2O_3 capping layer ($\Delta V_{FB} \approx 0$ V) suggests that it may be an effective material at preventing diffusion of water to the IGZO back channel, as well as suppress the hydrogen liberation mechanism. A water-induced shift without the hydrogen released from the top-gate reaction would be less pronounced, as observed on BG devices.



(a) (b)

Figure 3.10: C-V characteristics of MOSCAPs (a) without capping layer and (b) with Al_2O_3 capping layer. Without capping, they show ~0.4 V shift in V_{FB} and with Al_2O_3 capping, the V_{FB} shift is ~0 V. Note that C-V characteristics from two separate devices are shown for each treatment [13].

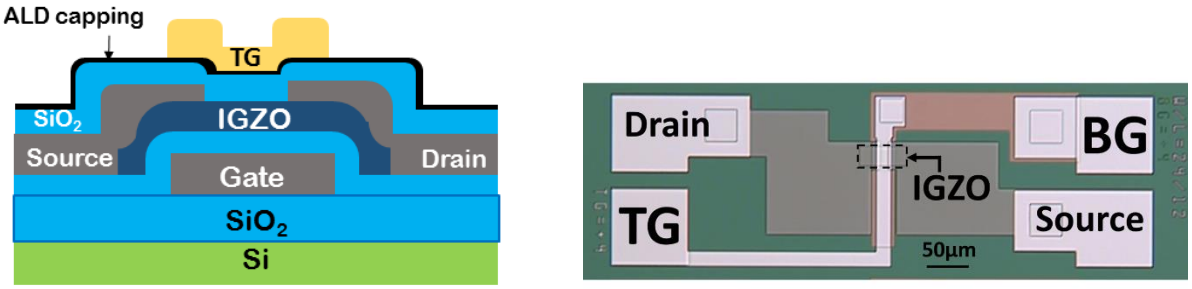
The MOScap results provide additional information that must be considered in the interpretation of TFT thermal instability, with the differences being due to the semiconductor response and not the dielectric materials which were common to both. There was a distinctive shift

in the positive direction on uncapped devices during the thermal treatment at 140 °C, and some additional shift at 200 °C, that was not present on capacitors with the Al_2O_3 capping layer. The replicate devices demonstrated near perfect overlay around the flatband condition. The shift is due to differences at the Si/SiO2 interface, with hydrogen passivation of Si dangling bonds being the only plausible explanation. The availability of hydrogen is markedly higher in the device without the ALD capping layer. These observations validate several aspects of the proposed mechanism for IGZO TFT thermal instability; the presence H_2O in the oxide layer, the diffusion of H_2O and subsequent liberation of hydrogen through the metal gate reaction, and the diffusion of hydrogen through the oxide layer to the semiconductor interface. While there may be other species present in the oxide layer such as hydroxyl groups (Si-OH) and non-bridging oxygen centers, any changes induced by these during the application of thermal stress (e.g. chemical reactions, ionization) would be common to both capped and uncapped devices. Any induced charge within the oxide would shift characteristics in the same fashion, whether the semiconductor is silicon or IGZO. Thus, the interpretation that adsorbed H_2O molecules are primarily responsible for the thermal instability of IGZO TFTs is well supported.

3.3.2 ALD Alumina as Capping Layer

IGZO TFTs were fabricated in BG and DG configurations on a thick isolation oxide (~500 nm SiO_2) thermally grown on silicon wafers. The fabrication details of baseline passivated BG are discussed in section 2.1. The DG process is an extension of the BG process sequence; after the passivation anneal step, the devices are capped with 10 nm Al_2O_3 film using ALD. The gate and source/drain contact regions were opened using 10:1 buffered HF. Top-gate electrodes (for DG device) and source/drain electrodes were then defined using evaporated Al with a lift-off

technique. Here, Figure 3.11 (a) shows the cross-section schematic of a DG TFT and Figure 3.11 (b) shows a top-down view of the fabricated device.



(a) (b)

Figure 3.11: (a) Cross-section schematic of a DG TFT with ALD capping layer. The DG device has the staggered electrode configuration of the BG device, with the addition of a co-planar top gate. Note that the bottom and top gate electrodes in the DG device are electrically connected through a contact not shown. (b) Top-down view of a fabricated DG TFT. Note that the IGZO channel is highlighted [13].

Electrical testing was done on TFT structures using a B1500 semiconductor device analyzer. TFT channel dimensions were width of 24 μm and length as indicated. All I_D-V_{GS} transfer characteristics presented were taken with a gate voltage up-sweep and medium measurement integration time unless otherwise noted, with low-drain and high-drain bias conditions at 0.1 V and 10 V, respectively. The devices were thermally stressed with a hot plate in ambient.

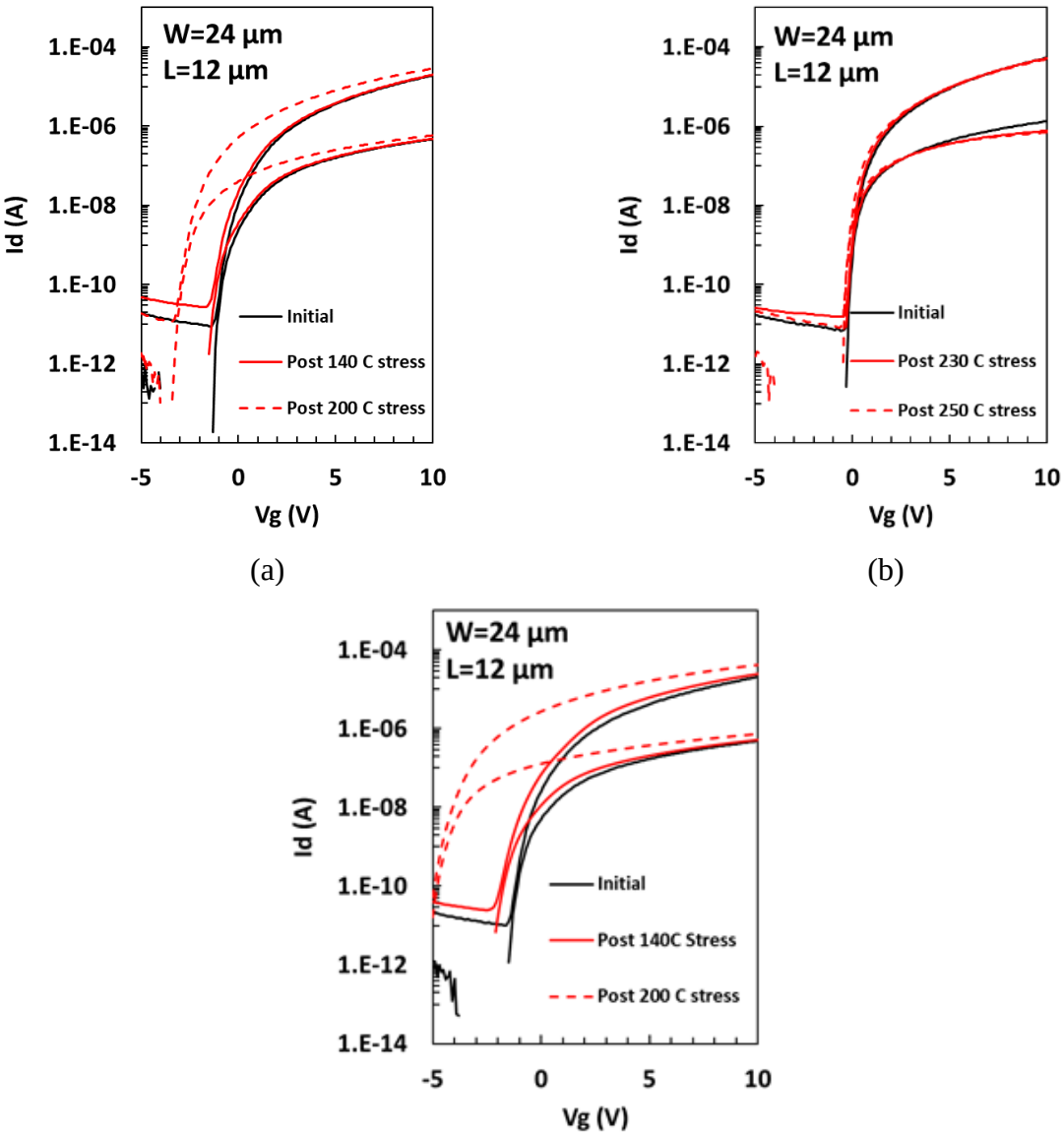
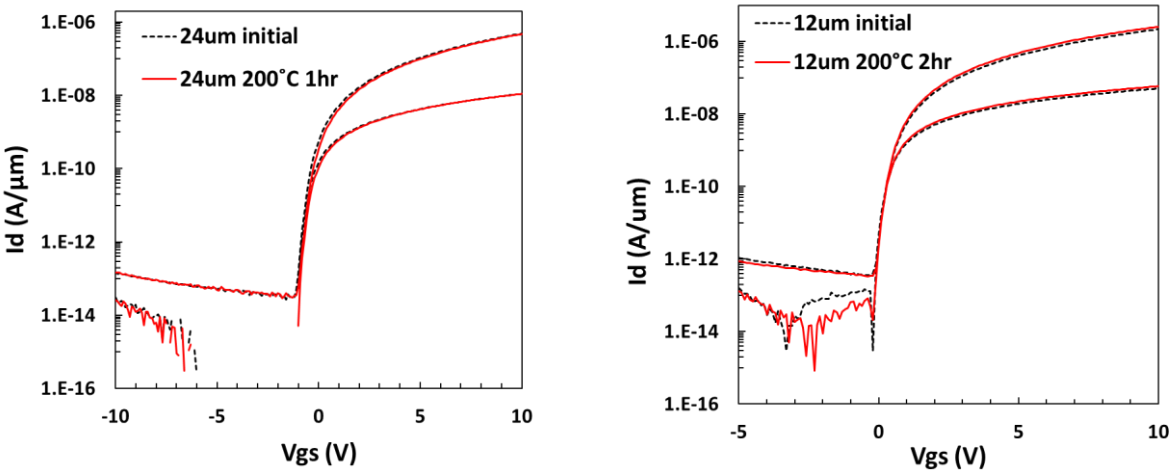


Figure 3.12: BG devices with ALD Al_2O_3 capping layer deposited at (a) 150 °C, (b) 200 °C & (c) 250 °C, with channel lengths and 1 hour sequential thermal stress treatment temperatures as indicated. The 200 °C ALD temperature maintains good thermal stability at temperature up to 250 °C [58].

The thermal stability of capped BG devices was found to depend upon the deposition temperature of the ALD process. Figure 3.12 shows a comparison of BG devices with ALD films deposited at different temperatures, with electrical characteristics measured following 1 hr thermal stress hotplate treatments performed sequentially at indicated temperatures. The standard temperature for dehydration bake during HMDS vapor prime used in photoresist processing is

140 °C and the ALD process is typically done at 200 °C. Thus, the fabricated devices were thermally stressed with three cycles at 140 °C and two cycles at 200 °C for an hour each. All devices were electrically tested before and after each hot plate treatment.

The lower ALD temperature was not adequate in supporting thermal stability on 12 µm channel length devices stressed at 200 °C. It is likely that the lower temperature ALD process results in an alumina film with significant hydrogen or H_2O content, and thus may act as a source of these contaminants under subsequent thermal stress conditions. The same devices processed at 200 °C ALD temperature maintained thermal stability up to 250 °C. At a higher ALD process temperature T = 250 °C, the devices again exhibited shifted characteristics with thermal stress. This is likely due to the vacuum anneal resulting in a formation of back-channel defects (e.g. V_O) during the thermal stabilization at the beginning of the ALD process. These defects may then be susceptible to interactions with H_2O and hydrogen, even at low concentrations. Neither of these scenarios are operative at the 200 °C ALD process temperature. Also note that the initial characteristics shown in Figure 3.12a and Figure 3.12c are approximately 1 V left-shifted in comparison to Figure 3.12b, indicating the onset of thermal instability during the ALD process itself. Figure 3.13 shows transfer characteristics of an L = 24 µm BG device and an L = 12 µm DG device with no shift from treatments at 200 °C, reinforcing the effectiveness of the ALD capping layer deposited at 200 °C in promoting thermal stability of IGZO TFTs.



(a) (b)

Figure 3.13: Representative characteristics of (a) BG and (b) DG devices with a 10 nm ALD Al_2O_3 capping layer deposited at 200 ℃ above the back-channel passivation/gate oxide. Channel length values are indicated [13].

3.3.3 Channel-Length Dependent Behavior

Within these successive thermal treatments, the alumina-capped BG devices were extremely resistant to thermal degradation, showing no apparent relationship to channel length. However, there was a clear channel length trend observed on DG device behavior. Failures were statistical, with some devices being able to withstand more thermal cycles than others.

Long channel IGZO TFTs (L = 48 µm) appeared to degrade consistently when subjected to thermal hot plate treatments (1-2 hours) at or above 140 °C. Some short channel devices (12 µm, 24 µm) showed degradation, but in general were able to withstand higher levels of thermal stress. Figure 3.14 shows the channel length dependence, with longer channel devices being more susceptible to degradation. No channel width (and thus area) dependence has been observed. The origin of channel length dependent degradation observed on the DG TFT is presumed to again be related to H_2O through direct interaction with the back-channel region, or through hydrogen liberation as described. The BG TFTs did not exhibit this dependence. It is expected that hydrogen generated by the water-metal reaction is primarily responsible since any remaining water molecule

distribution within the passivation oxide after the 400 °C passivation anneal is independent of the gate electrode configuration.

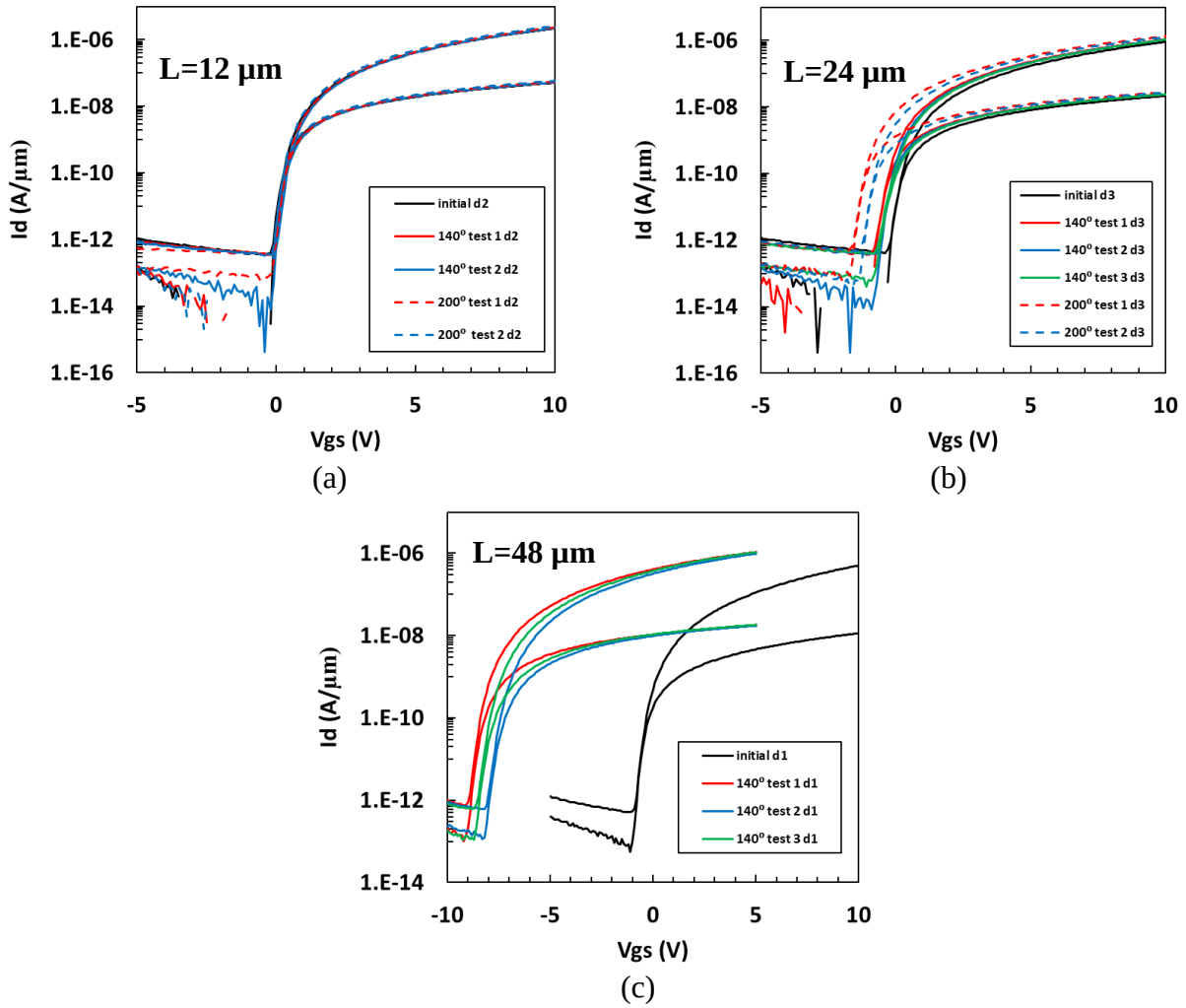


Figure 3.14: Channel length dependent behavior of ALD Al_2O_3 capped DG devices with (a) L=12 µm, (b) 24 µm, and (c) 48 µm [13].

An extension of the thermal instability hypothesis that may explain the channel length dependence is the molybdenum source/drain contact regions acting as gettering sites for H_2O molecules during the 400 °C annealing process. The removal of H_2O from the back-channel region is a two-dimensional process limited by the diffusivity and/or transport along the back-channel interface of H_2O molecules, with the process being more complete in short channel devices. In

shorter channel devices, H_2O molecules that reach the metal regions would be effectively removed from the system. In longer channel devices, the H_2O molecules that are not gettered remain available and can migrate during thermal stress treatments, establishing complete coverage on devices that experience degradation. Figure 3.15 shows a cartoon illustration of the proposed mechanism.

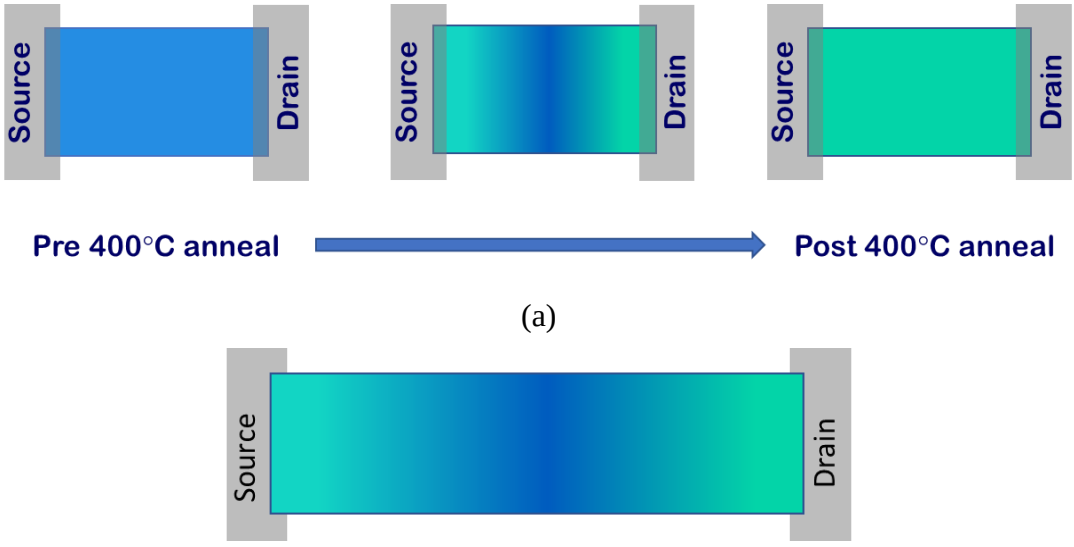


Figure 3.15: (a) Water segregation from channel due to source/drain electrodes acting as a getter. Blue regions indicate the presence of H2O molecules. (b) In longer channel devices the water is not effectively gettered during subsequent anneal.

The source/drain metal is proposed to act as a getter to water during the 400 °C passivation anneal, thus removing water molecules from within the back-channel passivation oxide nearby these regions. In shorter channel devices ($L \leq 24\mu m$) this water evacuation process is complete, whereas in longer channel devices the water molecules away from these regions remains significant. During subsequent thermal stress at 140-200 °C, any remaining water molecules can migrate and may segregate to the back-channel interface. In DG devices, a reaction of water with the top-gate metal may liberate monatomic hydrogen (similar mechanism as the getter process)

which may influence the entire back-channel region. Note that the liberation of hydrogen that may be occurring during the 400 °C anneal, and during the 200 °C ALD process following the anneal, does not appear to have a negative impact on device operation.

3.4 BIAS STRESS INSTABILITY

It is important to perform bias-induced instability tests on TFTs as the application of this technology in flat panel display products requires prolonged on/off states. Devices are subjected to positive bias stress (PBS) and negative bias stress (NBS) tests which involved setting the gate voltage to +10 V and -10 V, respectively, with source & drain electrodes at reference ground. Measurements were taken at various intervals over an accumulated time of 10,000 seconds or as mentioned otherwise. A characteristic shift in response to bias stress can be attributed to defect state changes either in the dielectric region, the IGZO/SiO_2 interfaces, or the bulk IGZO material. Charge trapped in a dielectric or interface region that remains fixed would induce a lateral characteristic shift, whereas changes in interface traps would tend to cause differences in characteristic distortion and spreading.

3.4.1 Response to Positive Bias Stress

BG devices show little or no response to PBS as seen in Figure 3.16. Although most devices in literature [9], [11], [59] depict a positive shift in threshold voltage for PBS, it is important to note that devices fabricated at RIT did not show any significant shift.

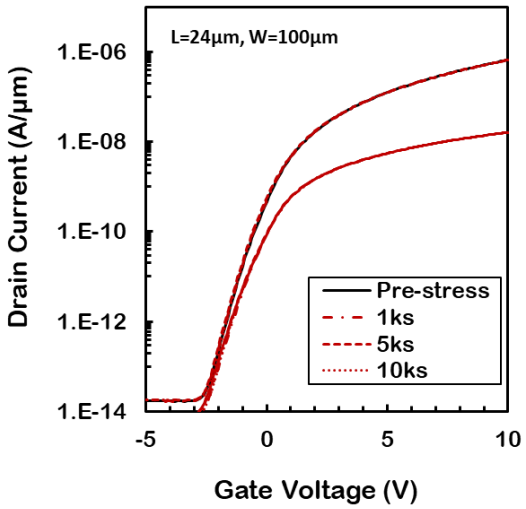


Figure 3.16: BG device under the influence of PBS showing no effect on device characteristics [40].

Figure 3.17 shows ATLAS simulations of electron concentration in IGZO TFTs. The device was simulated to be in PBS (b) compared to un-biased state (a). The TFT is in accumulation mode under positive-stress and the voltage drop occurs in the oxide where we see minimal back-channel effect. Interaction with the front-channel is said to have no effect on our devices since this behavior is attributed to the high quality of our gate oxide that significantly minimizes the effect of front-channel interface defects on device performance.

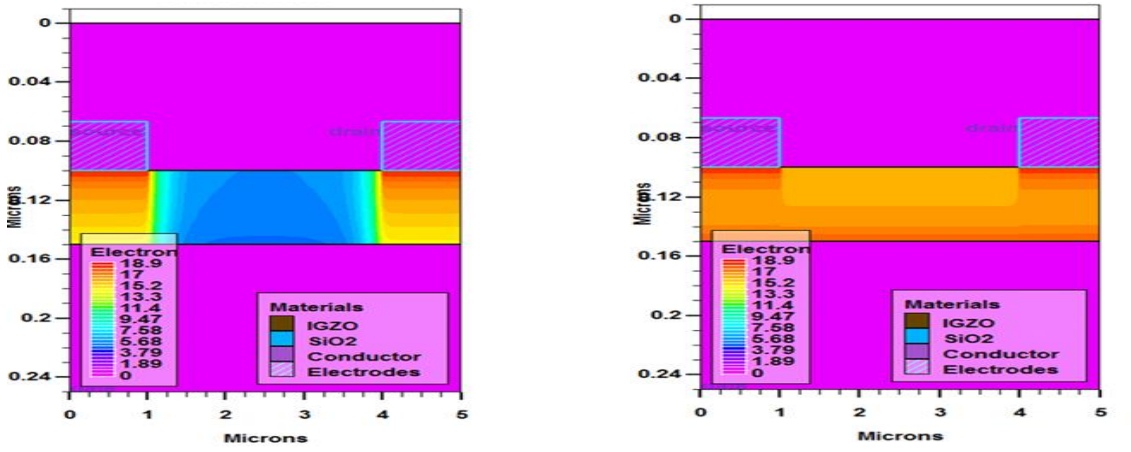


Figure 3.17: ATLAS simulation showing electron concentration of BG TFTs in (a) un-biased state and in (b) positive-stress [60].

3.4.2 Response to Negative Bias Stress

NBS resulted in significant left-shifting (shift ~ -1.5 V) and subthreshold steepening as shown in Figure 3.18. The starting characteristic has a shallow subthreshold slope, indicating poor gate control over interface traps. Time under NBS appears to convert some of these donor-like traps into positive charge that remains fixed during transfer characteristic measurements [61]. This attracts a negative charge in the channel making it abundant in electrons which turns on the transistor at relatively lower V_G, thus explaining the left shift.

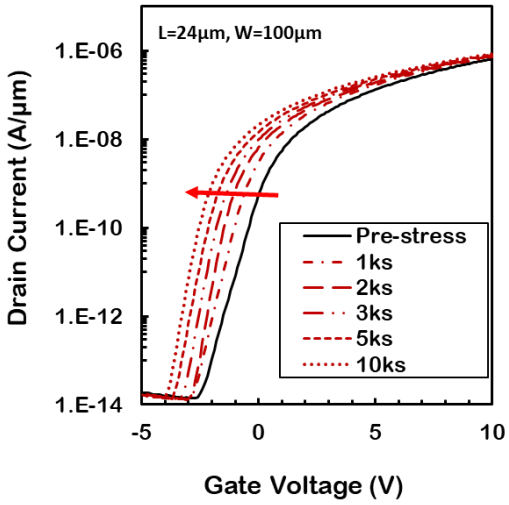


Figure 3.18: I-V characteristics of L/W=24/100 µm device showing a significant left shift in V_T under NBS [40].

Upon investigating TFTs that were bias stressed, the devices exhibited relaxation or recovery back to their original profiles. As discussed, PBS has an insignificant effect on the threshold voltage shift of bottom gate TFTs and hence the corresponding recovery mechanism was not apparent in this case.

3.4.3 Proposed Model for Bias Stress and Relaxation

Analogous to dopant atoms in semiconductor materials, oxygen vacancy defects in IGZO behave as donors which when ionized provide free electron carriers. However, these defects may exist in various charge states, specifically in a neutral V_O, singly ionized, V_O^+, and doubly ionized, V_O^{2+}, state. Under NBS the channel region is completely void of free electrons, and the Fermi Energy (E_F) drops below the energy of the double-donor V_O^{2+} state, as portrayed in Figure 3.19, thus supporting ionization.

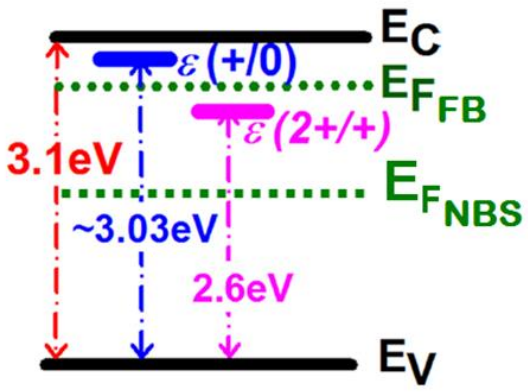


Figure 3.19: IGZO energy band diagram, showing single-donor (V_O^+) and double-donor (V_O^{2+}) oxygen vacancy defect states within the bandgap. The Fermi Energy (E_F) is approximated at flatband and NBS conditions. Using the indicated energy differences referenced to E_V, the energy levels for the V_O^+ and V_O^{2+} states are calculated to be 70 meV and 500 meV below E_C, respectively. Figure adapted from Chowdhury et al. [62].

A model proposed to explain the temperature dependence of NBS under illumination (NBIS) and relaxation has been presented by Chowdhury et al. [62] and has been the primary reference towards the interpretation of NBS results in this investigation without illumination. NBIS using a UV light source (λ = 365nm) resulted in the creation of V_O^{2+} donor states that left-shifted the I_D-V_{GS} transfer characteristic (Figure 3.20) with a forward activation energy of 1.06 eV. The relaxation process resulted in neutralization of the donor states and a characteristic right-shift with an activation energy of 1.25 eV.

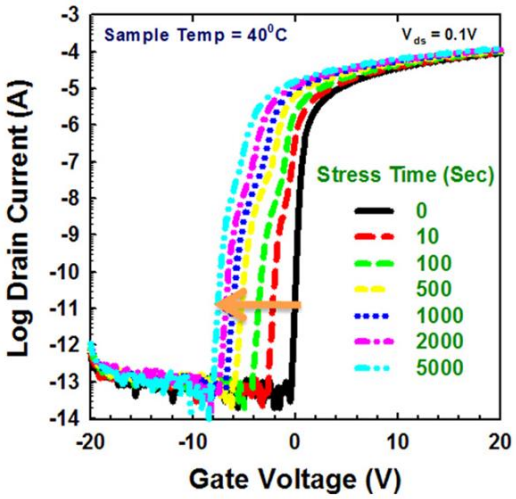


Figure 3.20: Representative response to NBIS [62].

Note that the characteristic left-shift is consistent with a certain level of V_O^{2+} existing in quasi steady-state, appearing like fixed charge. However, the distinct hump formation is likely due to back-channel interface traps also related to oxygen vacancy defects. The stated activation energies are shown in the following potential energy – configuration coordinate diagram in Figure 3.21 that represents the formation and relaxation of the operative V_O^{2+} defect state.

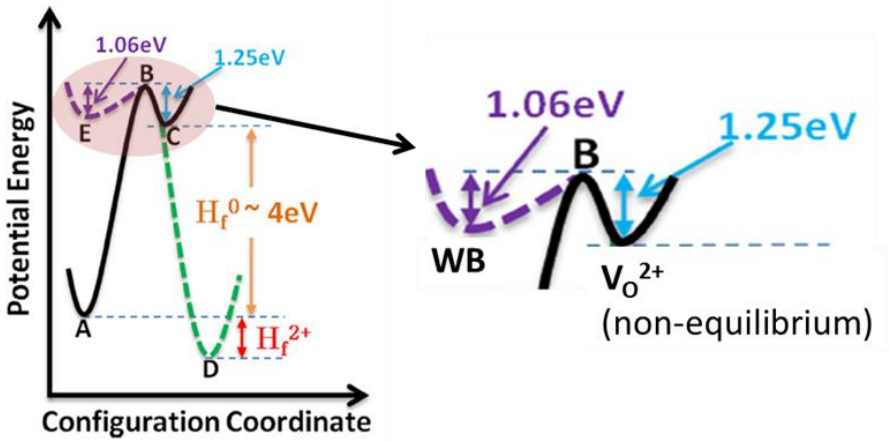


Figure 3.21: Proposed Configuration coordinate diagram by Chowdhury et al. [62] for the creation and relaxation of NBIS defects; NBS instability presumed to be of similar origin. State definitions are described in the corresponding narrative. The zoomed-in region identifies the state transitions and associated activation energies, both forward and reverse, between a "weak bond" neutral defect (WB) and the double-donor V_O^{2+} defect created during NBS which is not in thermal equilibrium once NBS is removed.

The states in Figure 3.21 are defined as follows: “A” is a reference ground state (no defect); “B” is a saddle point (i.e., energy barrier); “C” is a neutral oxygen vacancy state; “D” is a double-ionized oxygen vacancy state; “E” is a weak bond state. A detailed discussion can be found by Chowdhury et al. [62]. Application of NBS, along with thermal energy and time, will enable a transition from “E” (or WB) to another state over the barrier represented by “B”. As E_F is below the double-ionized donor state energy during NBS (Figure 3.19), the neutral oxygen vacancy defect state “C” is not favorable. This results in the creation of a V_O^{2+} defect state “D” which is in thermal equilibrium only during NBS. Once NBS is removed the double-donor defect is no longer in thermal equilibrium and should recapture electrons and relax back to the neutral V_O state “C”, however experimental results show that the energy barrier for the forward transition is immediately reestablished. Thus, the relaxation process involves a transition from the non-equilibrium V_O^{2+} state to WB, with a barrier appearing as if it were returning from state “C”. Overcoming the relaxation energy barrier and the recapture of electrons can be considered simultaneous events.

3.5 SUMMARY

A hypothesis on the origin of TABL was presented based on inhomogeneity at the topside IGZO interface, resulting in donor-rich defect regions separated by low-charge gaps. The ripening process passivates these defect states through interaction with room air and suppresses the TABL over time. A refined IGZO model for TCAD simulation provided insight on the progression of TABL behavior similar to real scenario during ripening.

An investigation has been presented on the thermal stability of IGZO TFTs fabricated using SiO_2 dielectric layers in BG and DG configurations. Without any capping layer on top of the back-

channel passivation oxide, the devices continuously degraded during applied thermal stress. This was more pronounced on DG devices, and led to the proposed mechanisms for thermal instability, involving H_2O and the liberation of monatomic hydrogen. Investigations on both silicon MOSCAPs and IGZO TFTs demonstrated that an ALD Al_2O_3 capping layer was effective at reducing the influence of thermal treatments at 140 °C and 200 °C, suggesting that the capping layer suppressed H_2O incorporation and reaction with the top-gate metal. An observed channel length dependence on the thermal degradation of DG devices led to a hypothesis involving the gettering of water from the back-channel material during the passivation anneal. Process techniques which minimize the incorporation of water in the passivation oxide, and the application of an effective capping layer such as ALD alumina which immediately follows an optimized passivation anneal are all key elements towards achieving thermally stable IGZO TFTs.

IGZO with bottom gate and double gate configurations were used to study the response of bias stress stability. Positive bias stress (PBS) and negative bias stress (NBS) tests involved setting the gate voltage to +10 V and -10 V, respectively, with source & drain at reference ground. Measurements were taken at various intervals over an accumulated time of 10,000 seconds. A characteristic shift in response to bias stress can be attributed to defect state changes either in the dielectric region, the IGZO/SiO_2 interfaces, or the bulk IGZO material. Passivated BG devices showed slightly degraded transfer characteristics due to interface traps that originated during passivation. BG devices under PBS were found to be fairly stable with few devices showing a slight left shift along with a hump-like distortion in I-V characteristics. This stability is due to the high quality of front-channel SiO_2-IGZO interface. BG devices under NBS showed a significant left shift in I-V characteristics leading to a ~2V shift in V_T. The starting characteristic has a shallow subthreshold slope, indicating poor gate control over interface traps. Time under NBS appears to

convert some of these donor-like traps into positive charge that remains fixed during transfer characteristic measurements [62]. This attracts a negative charge in the channel making it abundant in electrons which causes transistor to turn on at relatively lower V_G, thus explaining the left shift. The transfer characteristics for BG TFTs were found to return to their original "pre-stress" profiles without subjecting the device to any treatment in room temperature. The right shifting "relaxation" phenomenon in these devices began as soon as the application of stress was withdrawn.

Chapter 4. TCAD MODEL REFINEMENT

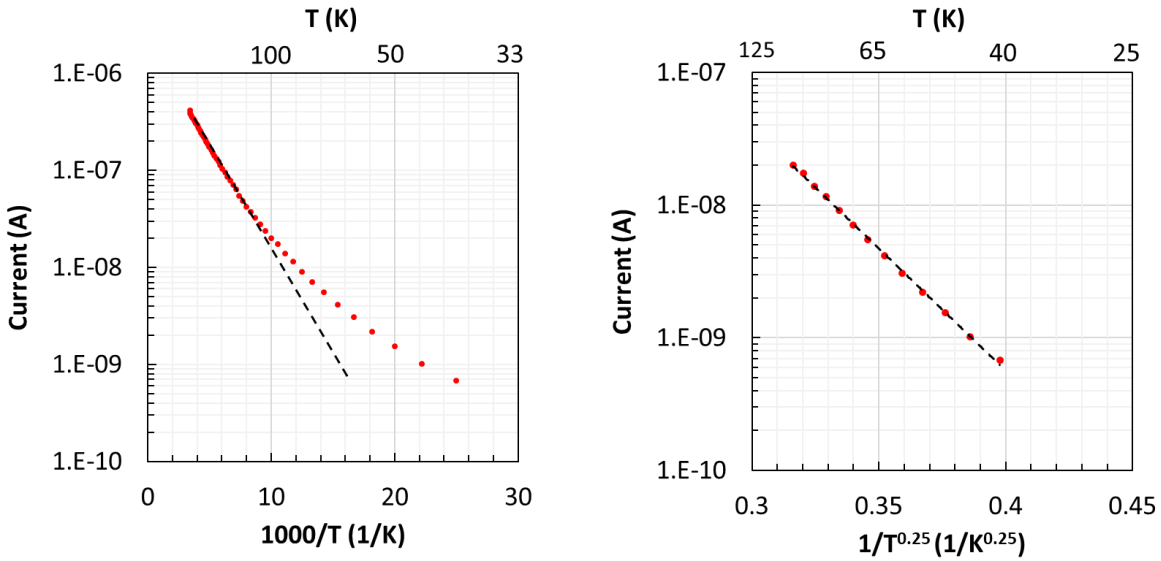
In this chapter, *I-V* measurements taken at different temperature on TFTs is presented. The IGZO material model is presented, with details on the density of states (DOS) distribution within the energy bandgap. The Silvaco® Atlas™ TCAD device simulator has been used for simulation. The bulk defect material model is refined using the I-V characteristics of passivated devices with further modification and the inclusion of interface states needed to represent the operation of passivated TFTs at different temperatures.

The conduction mechanism in IGZO material has been studied through low temperature measurements taken on TFTs. In previous work [25], IGZO TFTs without any back-channel passivation material were initially used to avoid the influence of interface defect states at the IGZO/passivation material interface. However, discrepancies in the measurements were observed most likely due to water adsorption on the exposed back-channel during the measurement. This hypothesis was supported by the fact that working TFTs after cryogenic measurements showed a transfer characteristic shift of -8 V [25]. IGZO TFTs with effective back-channel passivation such as the device structure described in section 3.3.2 should prevent such behavior and avoid questionable interpretation.

4.1 CHARGE TRANSPORT IN IGZO

Passivated BG TFTs were tested in Lakeshore cryogenic probe station, with transfer characteristic measurements taken from room temperature to as low as 40 K using liquid helium. The following

analysis of transport behavior and extraction of the defect density-of-states (DOS) follows the work of Chowdhury & Jang et al. [63]. This work is based on the premise that states which enable localized-state hopping transport at very low temperature (i.e. T < 100 K) are responsible for extended-state conduction behavior above a mobility edge at high temperature (i.e. T > 100 K) and is given in details in [64]. In Figure 4.1a, it can be seen that the current follows an Arrhenius relationship at high temperature, with the characteristic becoming more shallow as the temperature approaches 100 K, reflecting different transport behavior.



(a) (b)

Figure 4.1: (a) Drain current versus 1000/T shown for the full temperature (40K-290K) regime, it can be seen that at lower temperatures the current no longer follows a linear relationship with reciprocal temperature & (b) The linear dependence of log(ID) on $1/T^{0.25}$ over temperature (40K- 100K) indicates variable range hopping as the carrier transport mechanism at low temperature (T<100K). Here, V_{DS}=0.1 V and V_{GS}=5 V.

4.1.1 Low-Temperature Range (40 K to 100 K)

Below 100 K, current shows a weak thermal dependence and follows Mott's law [65] which describes variable range carrier hopping in amorphous materials [63],

$$I_D = I_{D0} \exp\left(-\frac{B}{T^{\frac{1}{4}}}\right) \quad 4.1$$

where I_{D0} is a drain current prefactor, B depends on the material properties. The drain current (I_D) values are plotted against the temperature ($1/T^{0.25}$) at V_{DS}=0.1 V and V_{GS}=5 V in Figure 4.1b. The characteristic fit supports carrier hopping as the dominant transport mechanism in the low temperature range.

The value of *B* in equation 4.1 can be extracted from the slope of ln(I_D) *vs* $1/T^{0.25}$ plot. The theoretical value of *B* is related to the density of states at E_F as given in equation 4.2 [63] [66]:

$$B(E_F) = 2\left(\frac{\alpha^3}{k_b\, N(E_F)}\right)^{\frac{1}{4}} \quad 4.2$$

where α is the inverse of Bohr radius (a) that is related to the overlap of wave functions of two localized states and can be calculated from:

$$a = \frac{a_0 \varepsilon_r}{m_e^*/m_0} \quad 4.3$$

where a_0 is the Bohr radius of hydrogen atom (0.53 Å), ε_r is the relative permittivity of IGZO (11.5) [67], m_e* is the effective mass of electron in IGZO ($0.34m_0$) [8], and m_0 is the physical electron mass. From equation 4.3, a is approximately 17.9 Å. N(E_F) values can be calculated using equation 4.4, with $B(E_F)$ values obtained over a series of gate voltages:

$$N(E_F) = 16\left(\frac{a^3}{k_b\,(B(E_F))^4}\right) \quad 4.4$$

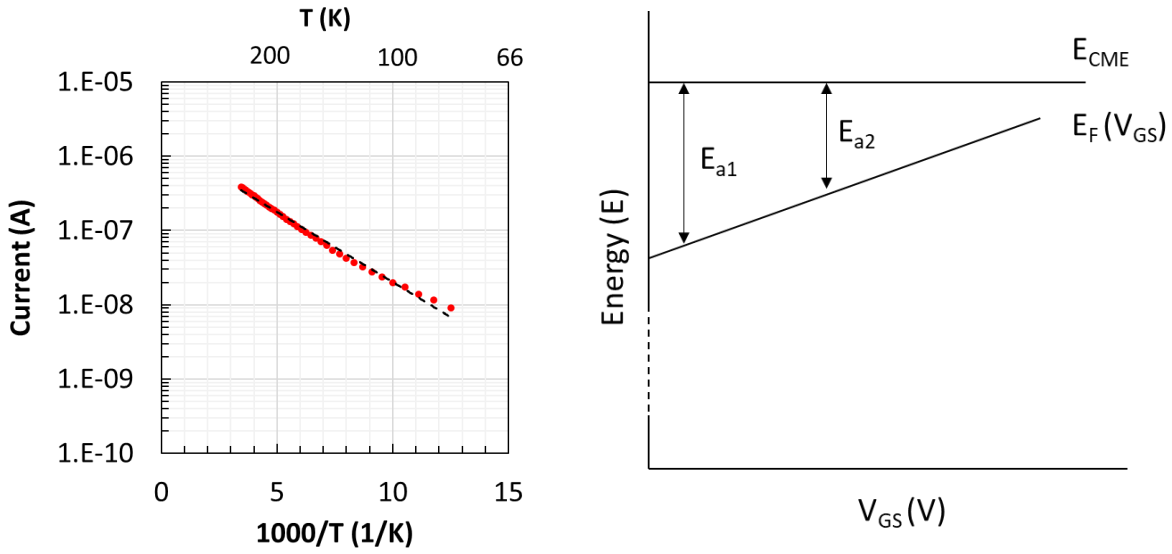
4.1.2 High-Temperature Range (T > 100 K)

At T >100 K, the current vs temperature response follows Arrhenius behavior [68],

$$I_D = I_{D0}\exp\left(-\frac{E_a}{k_b T}\right) \quad 4.5$$

where E_a is the activation energy taken to be the energy difference between the conduction band mobility edge (E_{CME}) energy and Fermi energy, i.e. $E_a = (E_{CME} - E_F)$ [63], I_{D0} is a drain current prefactor, and k_b is the Boltzmann constant. The activation energy is gate voltage dependent and decreases with increase in V_{GS} [69].

The Arrhenius fit in Figure 4.2a infers that charge transport in IGZO from 100K to room temperature, follows a thermally activated process which corresponds to the promotion of electrons from band-tail states to the mobility edge. As V_{GS} increases, E_F moves closer to the E_{CME} and therefore the value of activation energy E_a decreases as shown in Figure 4.2b. The extracted range of activation energy is 20-80 meV for V_{GS} values from 10 V to 1 V, respectively.



(a) (b)

Figure 4.2: (a) Drain current versus temperature plot at V_{DS}=0.1 V and V_{GS}=5 V. Charge transport follows Arrhenius behavior for T >100 K, indicating thermally activated band conduction as the charge transport mechanism. (b) Conceptual representation of energy versus gate voltage. Increasing gate voltage causes E_F to approach the conduction band mobility edge.

Now, E_a can be extracted from I_D vs 1/T plot (Figure 4.2a) using equation 4.5. Thus $N(E_F)$ is extracted over a series of V_{GS} values from the low temperature regime, and E_a is extracted at the same gate voltage series from high temperature regime characteristics. Finally, $N(E_F)$ and E_a values found at common V_{GS} are plotted in Figure 4.3, with the data fit to equation 4.6:

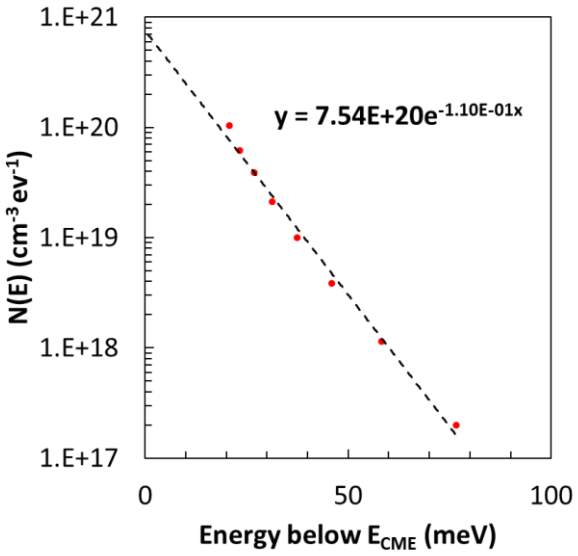


Figure 4.3: Extracted DOS (N(E)) versus energy below the conduction band mobility edge.

$$N(E) = \mathrm{N_{TA}} \exp\left(\frac{E - E_{CME}}{W_{TA}}\right) \qquad 4.6$$

Where N_{TA} is the peak density of band-tail acceptor states at E_{CME}, and W_{TA} is the Urbach energy which characterizes the band-tail slope. The parameter values extracted from Figure 4.3 are $N_{TA}=7.54\times10^{20}$ $cm^{-3}eV^{-1}$ and $W_{TA}=9.1$ meV. Note that the data in Figure 4.3 is arguably not well-characterized by a single Urbach energy, which leads to uncertainty in values; this becomes especially important as E_F becomes closer to E_C at higher V_{GS} values. The value of N_{TA} is almost 5x higher compared to the N_{TA} used in the IGZO default material model for TCAD simulation (see section 2.2), with additional noted inconsistency in W_{TA} (default is 13 meV). The discrepancy in these extracted parameters is even more pronounced in the analysis by Chowdhury & Jang et al. which yielded values $W_{TA}=5.73$ meV and $N_{TA}=3.01\times10^{21}$ $cm^{-3}eV^{-1}$ [63]. This common inconsistency suggests that while elegant, the DOS extraction methodology presented lacks the consideration of additional defect states and/or potential barriers present that result in the observed

temperature dependence. This calls into question the interpretation of cryogenic measurements and reveals the lack of comprehension in temperature-dependent behavior. Furthermore, there exists an additional inconsistency in the continuity of the DOS at the mobility edge, which will now be deliberated.

4.2 CONTINUITY OF DENSITY OF STATES

Band-tail states (BTS) are localized electronic states existing just below conduction band minima or above valence band maxima. In IGZO a high density of band-tail states exists due to incomplete bonding, random arrangements of atoms and variations in bonding angle [31]. The DOS continuity for amorphous oxide semiconductors has been nicely presented by Wager [70]. For a smooth transition across the mobility edge from localized to extended conduction band states, it is required that the density of states (DOS) be continuous as shown in Figure 4.4 [70]. DOS continuity at E_{CME} is represented by equation 4.7:

$$g_{TA}(E_{CME}) = g_{C}(E_{CME}) \tag{4.7}$$

Using equation 4.7 and the relationships given in Figure 4.4 leads to equation 4.8:

$$N_{TA} = \frac{1}{2\pi^2}\left(\frac{2m_e^*}{h^2}\right)^{\frac{3}{2}}\sqrt{E_{CME} - E_C} \tag{4.8}$$

It should be noted that E_C is the conduction band minima which is positioned at a lower energy than E_{CME} and established the onset of $g_C(E)$ DOSgiven by equation 4.8. Additionally, the DOS

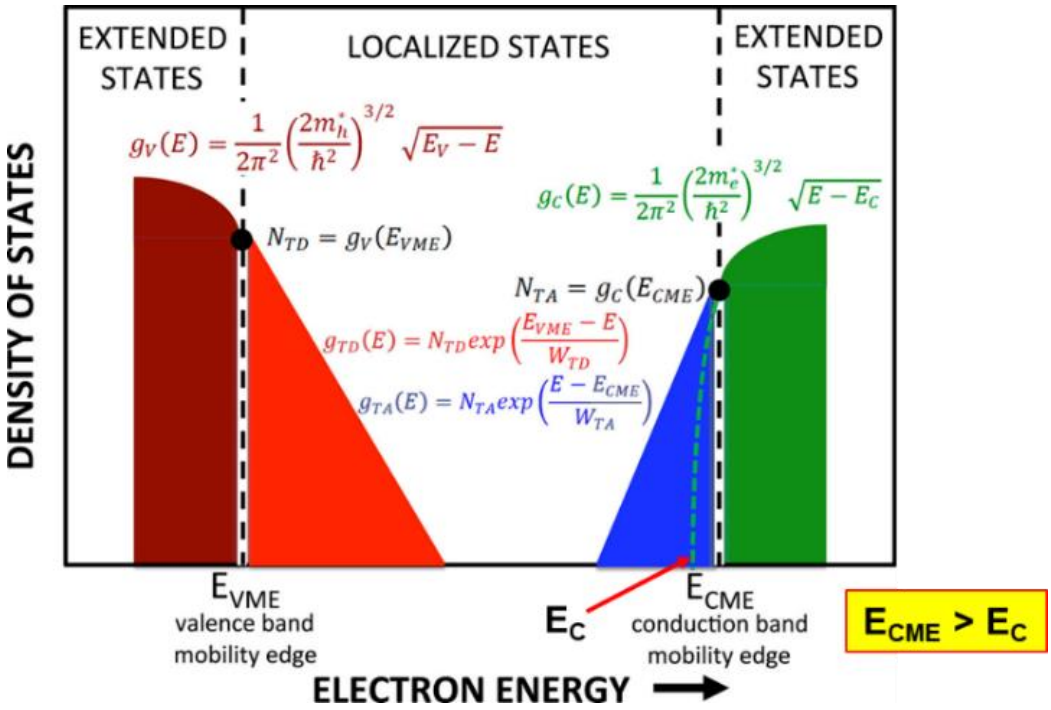


Figure 4.4: Density of states model illustrating localized and extended state densities for both valence and conduction band [70]. Here the original figure is modified to show E_C below E_{CME}.

derivative with respect to energy should also be continuous across the mobility edge. Using these constraints results in,

$$\frac{dg_{TA}}{dE} = \frac{dg_C}{dE}$$

$$\frac{N_{TA}}{W_{TA}} = \frac{1}{2\pi^2}\left(\frac{2m_e^*}{h^2}\right)^{\frac{3}{2}}\frac{1}{2\sqrt{E_{CME} - E_C}} \qquad 4.9$$

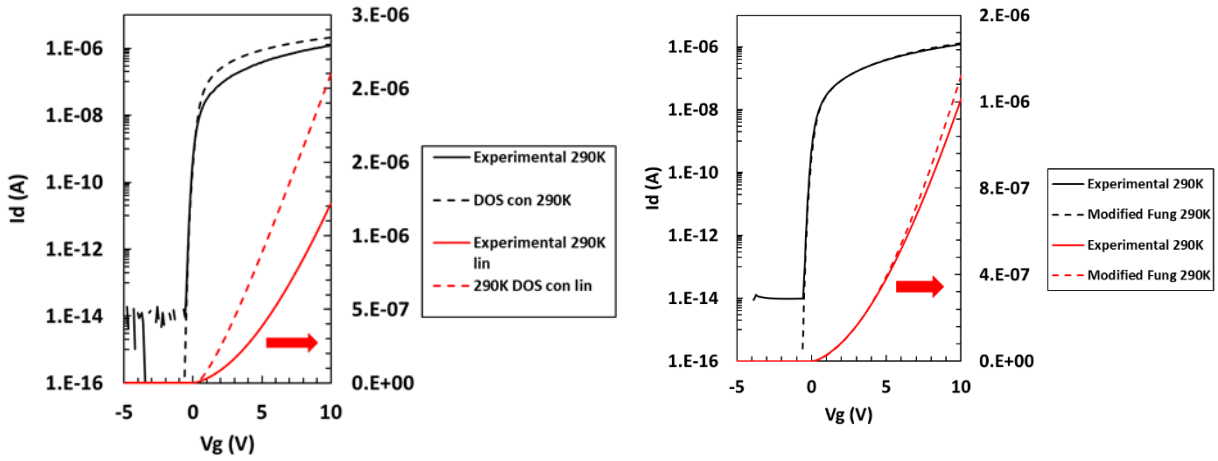
Using equations 4.8 and 4.9 leads to

$$E_{CME} - E_C = \frac{W_{TA}}{2} \qquad 4.10$$

Now substituting this value in equation 4.8

$$N_{TA} = \frac{1}{2\pi^2}\left(\frac{2m_e^*}{h^2}\right)^{\frac{3}{2}}\sqrt{\frac{W_{TA}}{2}} = 4.9\times10^{21}\sqrt{\frac{W_{TA}}{2}}\left(\frac{m_e^*}{m_0}\right)^{\frac{3}{2}}\ (\mathrm{cm^{-3}eV^{-1}}) \qquad 4.11$$

According to the equation 4.11 N_{TA} is dependent on W_{TA} and the effective mass of electron. Using m_e^*=0.34m0 [8] for IGZO and W_{TA}=13meV [32], the calculated band-tail state density peak $N_{TA}=1.1\times10^{20}\mathrm{cm^{-3}eV^{-1}}$, which is lower than the Atlas default value reported by Fung [32]. As shown earlier in section 2.3, the passivated device TCAD model listed in Table 2-III has modified N_{TA} and W_{TA} values which show an excellent match to room temperature behavior, yet do not conform to DOS continuity constraints. It should be noted that, in this work room temperature refers to 290 K and hereafter will be used interchangeably. Figure 4.5 shows a comparison of room temperature model characteristics with and without meeting the DOS continuity criteria, which essentially decouples the band-tail disorder from the effective mass characterizing the extended band states. While this goes against a key outcome emphasized in Wager's discussion [70], the model match to the experimental data is markedly better when the DOS continuity criteria is relaxed. This topic will be revisited in further model refinement needed to account for temperature dependent behavior.

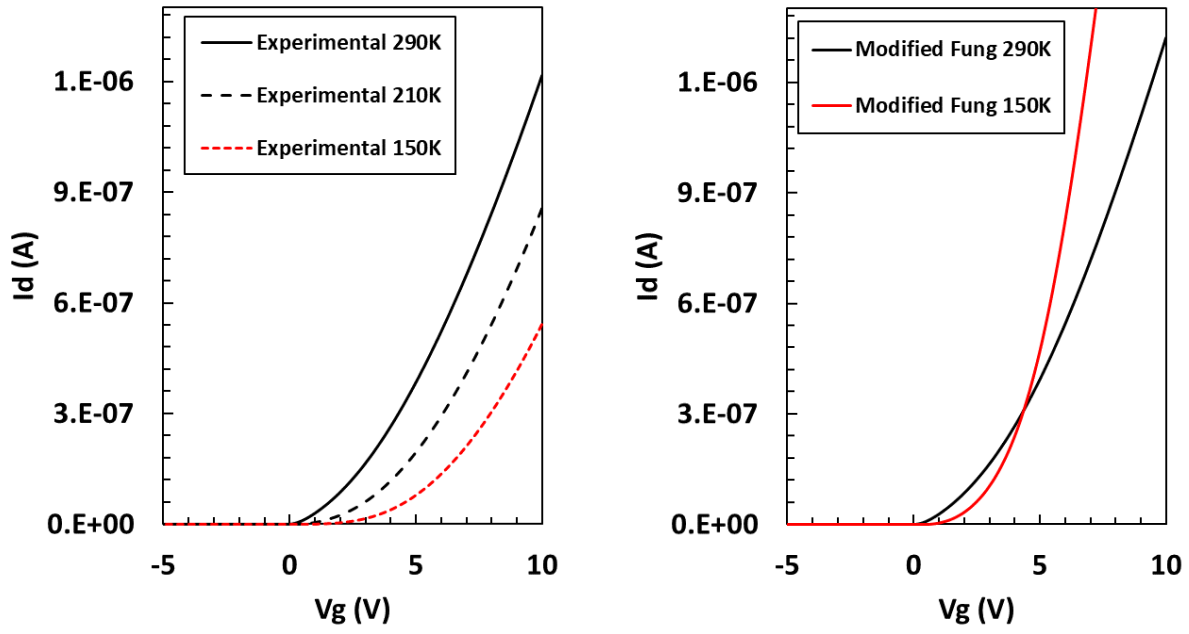


(a) (b)

Figure 4.5: (a) DOS continuity with W_{TA}=13meV at RT (b) without DOS continuity using W_{TA}=13meV at RT (reproduction of Figure 2.10).

4.3 TEMPERATURE DEPENDENT MODEL REFINEMENT

While room-temperature transfer characteristics are well represented in Figure 4.5(b), the simulated characteristic at lower temperature exhibits a significant departure from the experimental data, as shown in Figure 4.6. The simulated current level at T = 150 K exceeds that at T = 290 K, which can be explained by the default mobility model which has remnants of that used for silicon that are used completely out of context. This identifies the absence of a comprehensive TCAD model which accurately reflects temperature-dependent behavior. The development of such a model is now presented, with the details of an investigative approach utilizing various carrier transport models within Silvaco Atlas TCAD simulation.



(a) (b)

Figure 4.6: (a) Experimental transfer characteristics at different temperatures, (b) Simulated I-V characteristics using modified passivated paramters and default (Fung) mobility model.

4.3.1 Temperature Independent Mobility

IGZO TFTs shows increasing current with increasing temperature as shown by the experimental results in Figure 4.6a. If the channel mobility is dominated by lattice scattering then the scattering theory states that to first order,

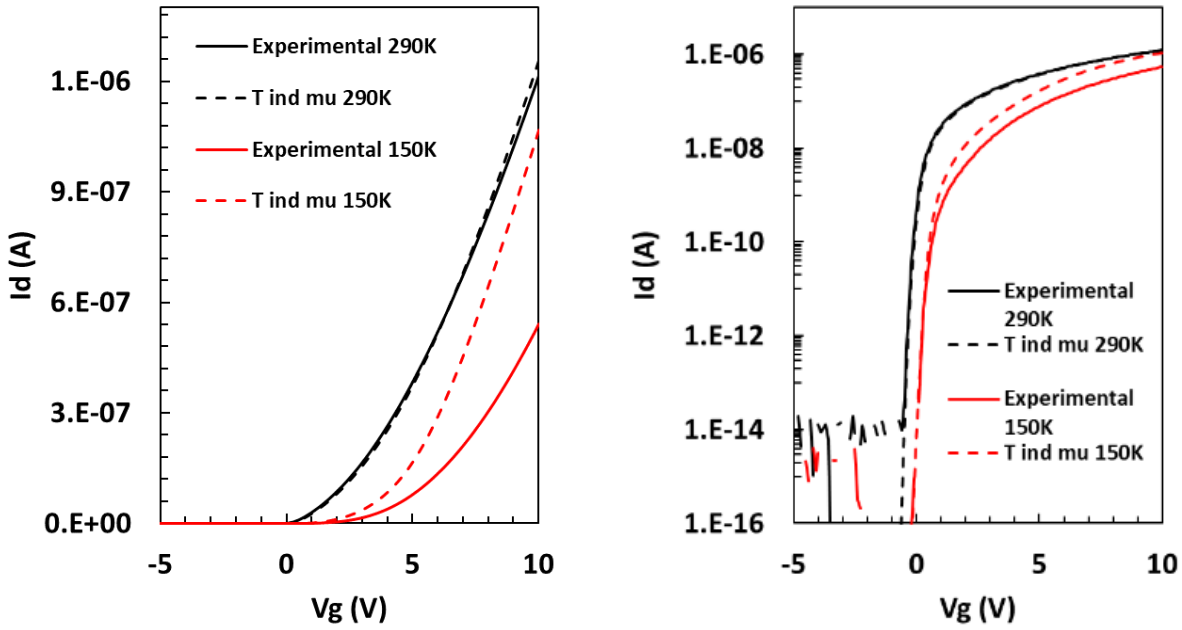
$$\mu_L \propto T^{\frac{-3}{2}} \qquad 4.12$$

which may represent the simulated behavior in Figure 4.6b. At lower temperature the probability of a scattering event decreases, thus increasing mobility [71]. A competing mechanism is ion scattering where impurity atoms, or defect states in the case of IGZO, are ionized resulting in coulombic attraction/repulsion between the electrons and the ionized defects. If ion scattering

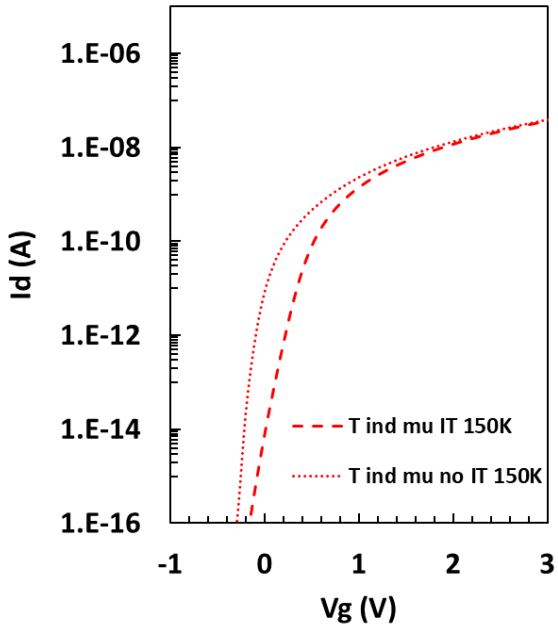
dominates then to first order,

$$\mu_L \propto \frac{T^{+\frac{3}{2}}}{N} \qquad 4.13$$

where, N is the total ion concentration in the semiconductor [71]. Thus, the mobility increases with increasing temperature which may represent the experimental data in Figure 4.6a. Note that the temperature dependent influence of band-tail states and interface traps complicates the situation significantly. A necessary starting point prior to temperature dependent model refinement was the elimination of the dependence of temperature on the carrier mobility. A temperature-independent mobility model was implemented, with initial characteristics shown in Figure 4.7a & b. The lower temperature characteristics at T=150 K has lower current than the higher temperature characteristics at T=290 K throughout the full V_G sweep, attributed entirely to the role of defect states. At this point the device model parameters are as reported in Chapter 2, Table 2-III(column 3). The acceptor-like IT states defined as $NTA_{IT}=5\times10^{13}$ $cm^{-2}eV^{-1}$ and $WTA_{IT}=0.07$ eV were key to match subthreshold behavior. These trap states are responsible for the shallower slope and right-shifted characteristic observed at lower temperature, as the capture of electrons becomes more significant. Figure 4.7c shows the importance of the IT distribution in matching the subthreshold response. Unfortunately, the device model does not adequately represent the on-state behavior of the experimental data. Further refinement of the device structure and/or model parameters is required to address the mismatch in current observed at T = 150 K. A primary candidate considered for this observed temperature dependence was the nature of the source/drain contact, which was well characterized as ohmic at room temperature (RT). The introduction of non-ohmic contacts was the next part of this investigation on temperature-dependent operation.



(a) (b)



(c)

Figure 4.7: Temp independent mobility 290k vs 150k, where the mobility μ=19cm^2/Vs in (a)linear scale, (b)log scale &(c) Simulated I-V with or without IT at T=150K.

4.3.2 Schottky Contact

Ohmic contact behavior was originally established in the device model by setting the source/drain contact workfunction to 4.13 eV. While the workfunction of molybdenum is commonly reported as $q\Phi M = 4.53$ eV, and the electron affinity in IGZO is taken to be $q\chi = 4.16$ eV, the expected barrier at the metal/semiconductor interface does not appear to be operative [72]. An increase in the source/drain contact workfunction to 4.53 eV limits the electron injection and results in a significant discrepancy in room temperature characteristics, as seen in Figure 4.8. Since the 4.13 eV workfunction setting maintains ohmic behavior at low temperature simulations, the workfunction was marginally increased to 4.35 eV to establish a M-S Schottky barrier to the IGZO channel. An increase in the intrinsic mobility from 19 to 23 cm^2/Vs was employed to match the room temperature characteristic as shown in Figure 4.9a. The lower temperature operation is shown in Figure 4.9b, where thermionic emission at the reverse-bias source-channel M-S junction remains significantly limited and appears to dominate the behavior. The inclusion of a tunneling mechanism referred to as the Universal Schottky Tunneling (UST) model was used to elevate the level of source injection into the channel. The simulated device structure and both thermionic emission and barrier tunneling mechanisms operative at the source M-S junction are illustrated in Figure 4.10.

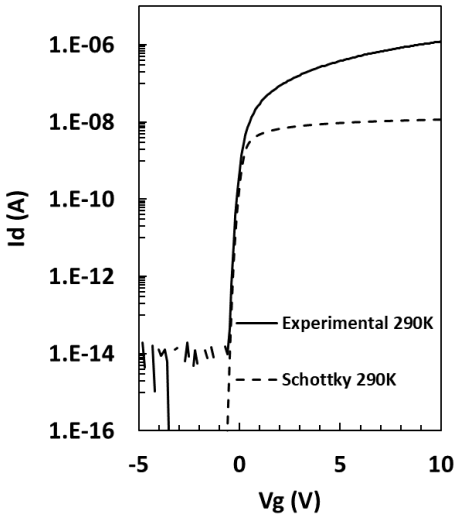
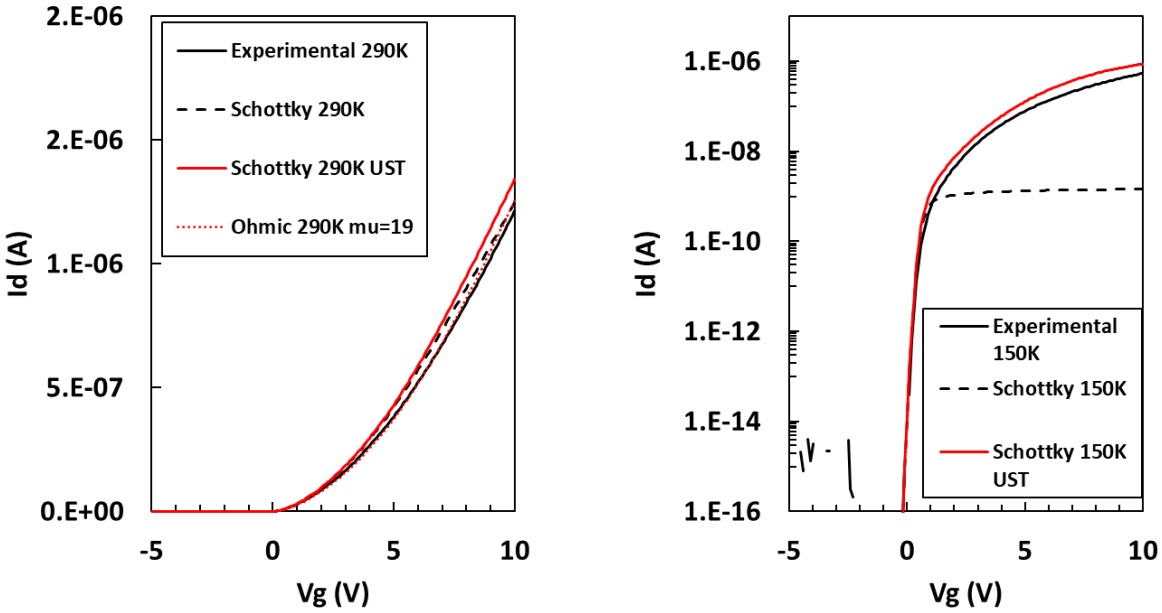
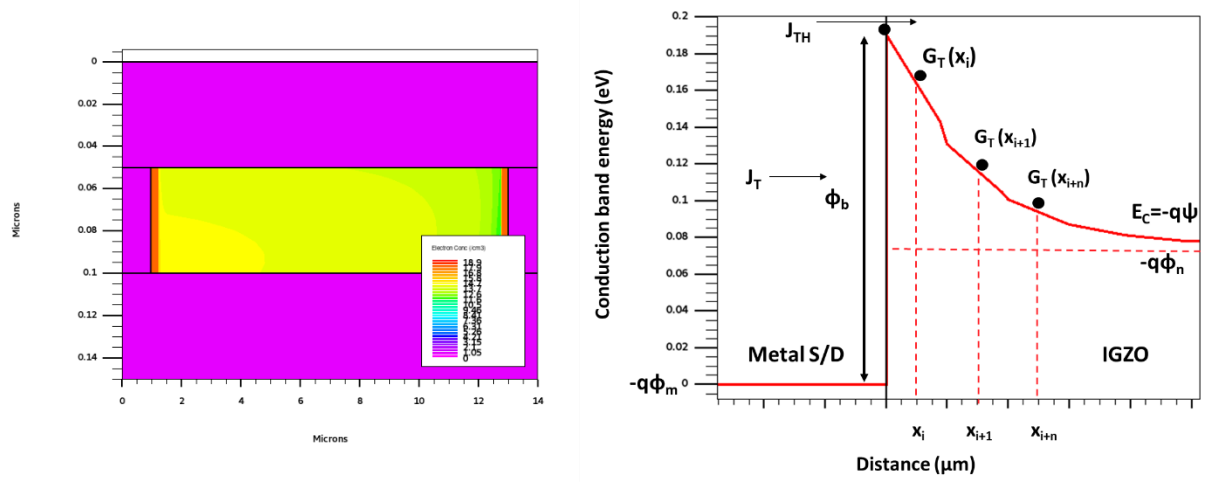


Figure 4.8: Workfunction=4.53 used for S/D contact shows Schottky contact and the simulated I-V shows contact limited behavior at room temperature.



(a) (b)

Figure 4.9: Measured and simulated transfer characteristics at (a) T = 290 K and (b) T = 150 K, with V_{DS} = 0.1 V and indicated parameter treatment combinations for Schottky barrier ($q\Phi_M$ = 4.35 eV), Ohmic ($q\Phi_M$ = 4.13 eV), with and without UST, and intrinsic channel mobility (µch) adjusted to 23cm^2/Vs unless indicated otherwise.



(a) (b)

Figure 4.10: (a) BG TFT with edge-defined contact regions for barrier simulation, here V_D=1V and V_G=0V, (b) Conduction band energy showing tunneling and thermionic emission, here V_D=1V, V_G=3V and $q\Phi_M$ = 4.35 eV.

The room temperature characteristics shown in Figure 4.9a exhibit relatively small differences, in contrast to the low temperature characteristics shown in Figure 4.9b. At T = 150 K, thermionic emission alone results in a clipped characteristic, whereas the inclusion of barrier tunneling results in a significant overshoot in current simulation. An alternative tunneling model was investigated to facilitate source injection through barrier tunneling, seeking appropriate temperature sensitivity to match the temperature dependence of measured characteristics.

Pipinys et al. analyzed the temperature dependence of reverse-bias leakage current in GaN Schottky diode as a consequence of phonon-assisted tunneling (PhAT) [122]. The electrons emitted from local levels in the metal-semiconductor interface dominate the leakage current in the diode and the current density can be given by equation 4.14,

$$J = qN_S W \tag{4.14}$$

Here, q is the electron charge, N_S is the occupied state density near the interface and W is the rate of phonon-assisted tunneling of electrons from localized states into the conduction band. The rate of PhAT is given by equation 4.15 [74],

$$W = \frac{eE}{8m_e^*\varepsilon_T}\left[(1+\gamma^2)^{1/2} - \gamma\right]^{1/2}[1+\gamma^2]^{-1/4} \times \exp\{\frac{-4}{3}\frac{(2m^*)^{1/2}}{eE\hbar}\varepsilon_T^{3/2}\left[(1+\gamma^2)^{1/2} - \gamma\right]^2 \times [(1+\gamma^2)^{1/2} + \frac{1}{2}\gamma]\} \quad 4.15$$

Where,

$$\gamma = \frac{2m_e^{*1/2}\Gamma^2}{8eE\hbar\varepsilon_T^{1/2}} \quad 4.16$$

Here, Γ^2 is the width of the center absorption band caused mainly by interaction with optical phonons and is given by equation 4.17, E is the electrical field, and ε_T is the trap depth,.

$$\Gamma^2 = \Gamma_0^2(2n+1) = 8\alpha(\hbar\omega)^2(2n+1) \quad 4.17$$

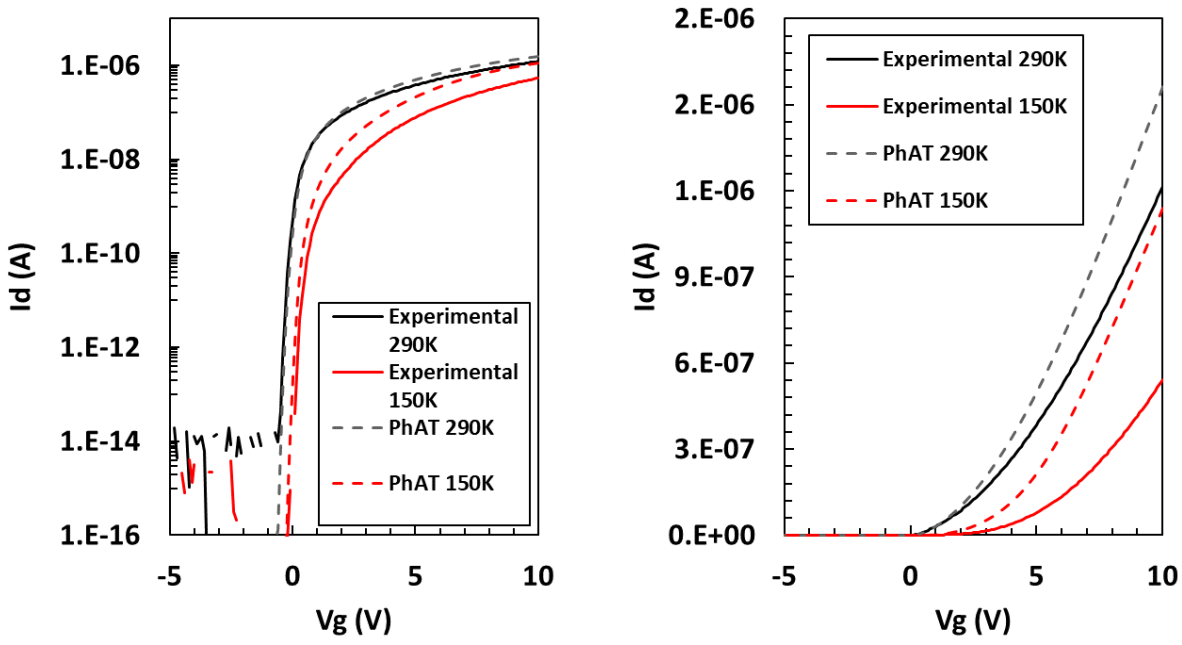
Now, α is the electron-phonon interaction constant, n is given by equation 4.18, and $\hbar\omega$ is the phonon energy. The PhAT model parameter values used in Atlas are listed below in Table 4-I.

$$n = [\exp\left(\hbar\omega/k_BT\right) - 1]^{-1} \quad 4.18$$

Table 4-I: Phonon assisted tunneling (PhAT) parameters used in Atlas

Parameter	Meaning	Value
m_e^*	Effective mass	0.34
$\hbar\omega$	Phonon energy	0.02 eV
α	Electron-phonon interaction constant	1.5
ε_T	Trap depth	0.15 eV
N_S	Occupied state density near the interface	1×10^{11} cm^{-2}

The parameter values were arrived at through iterative simulation trials, with the goal to reflect the actual temperature dependent behavior. With the degrees of freedom available, a single transfer characteristic at one temperature can be well matched; unfortunately, complex interactions rendered parameter optimization a futile exercise. The characteristics in Figure 4.11 show a relatively poor on-state fit while prioritizing the off-state behavior. The failure of the Schottky/UST and PhAT models to properly represent the experimental data directed efforts away from the contact behavior and towards a new focus on channel mobility.



(a) (b)

Figure 4.11: PhAT model 290K & 150K simulated vs experimental data.

4.3.3 Tokyo Mobility Model

Issues surrounding the temperature dependence of the default mobility model in the IGZO material definition in Atlas have been discussed (Figure 4.6), and thus led to removing the temperature dependence entirely. However as is the case for most semiconductor materials, the IGZO channel

mobility is likely to possess temperature dependence. Abe & Hosono et al. proposed a mobility model for amorphous IGZO TFT that is dependent on both temperature and carrier density [123]. The mobility dependence on carrier density is completely separated from the role of band-tail states, and all charge induced by field-effect contribute to electrical conduction (i.e. free carriers). The drift mobility (μ_d) is given by equation 4.19,

$$\mu_d = \mu_0 (1+\gamma)(\frac{n_e}{n_{CR}})^{\frac{\gamma}{2}} \quad 4.19$$

where, μ_0 is the intrinsic mobility, n_e is the carrier density, n_{CR} is the critical density, and γ is the index parameter whose temperature dependence is expressed by equation 4.20,

$$\gamma = \frac{T_\gamma}{T} + \gamma_0 \quad 4.20$$

Here, T is the temperature, T_γ and γ_0 are the model parameters. The parameters of μ_0, n_{CR}, T_γ and γ_0, are determined from TFT characteristics as described in [76]. This model has been incorporated as an optional mobility model in Silvaco Atlas TCAD, referred to as “IGZO.tokyo”. The model dependence of drift mobility on free electron concentration at different temperatures is obtained from Atlas and shown in Figure 4.12. Note that while the assumed mechanism of carrier dependence is expressly stated to be distinctly different than band-tail states, there is no alternative mechanism provided.

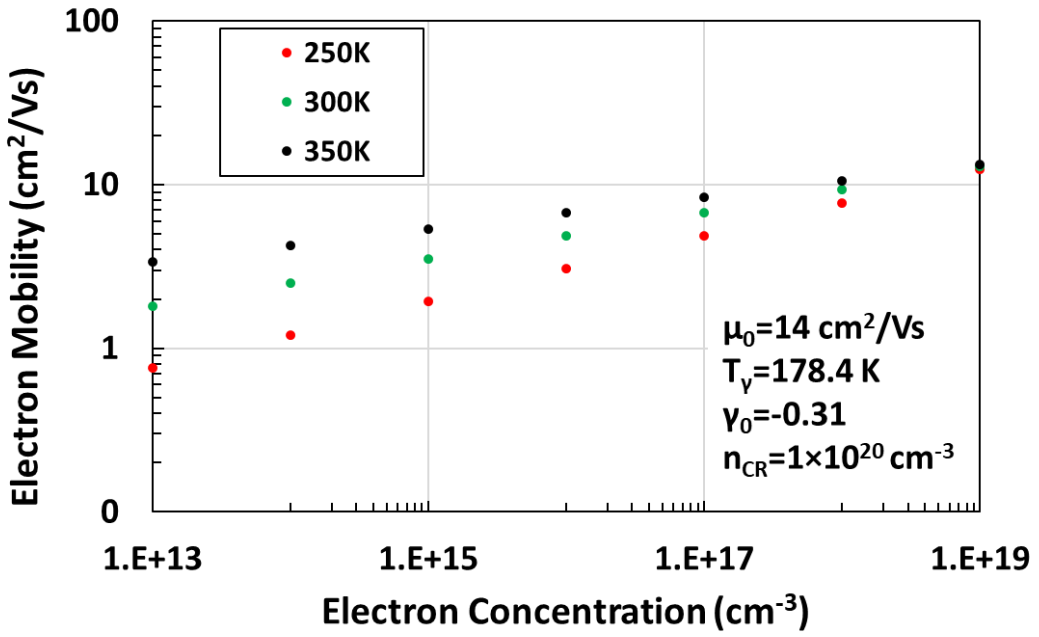
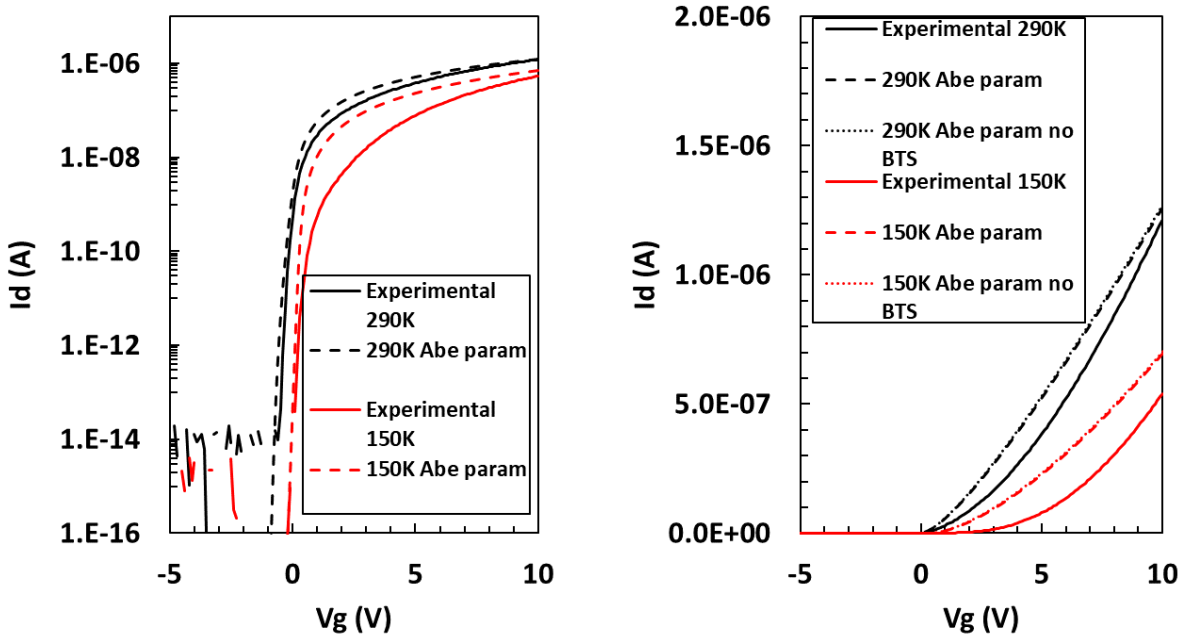


Figure 4.12: Mobility vs concentration at varied temperature using equation 4.19 and 4.20.

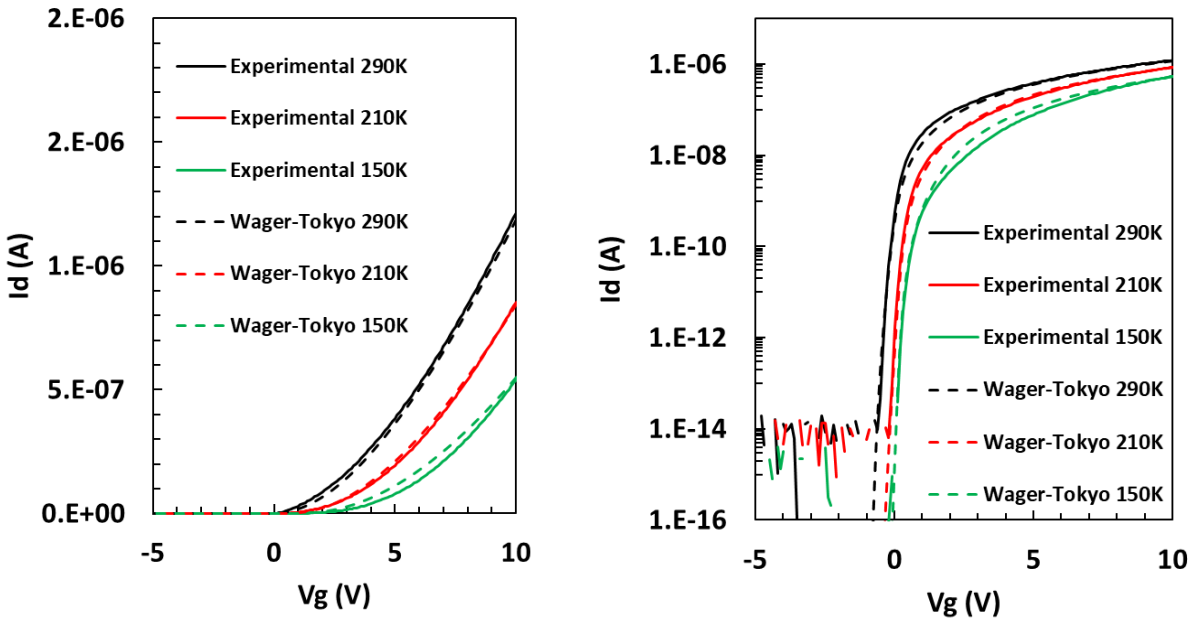


(a) (b)

Figure 4.13: (a) Experimental results with simulated I-V using Abe's parameters (Table 4-II, column 2), (b) Simulated I-V with or without Abe's BTS values showing no effect on the device behavior.

An initial evaluation of simulated characteristics using the IGZO.tokyo mobility model with temperature at T = 290K and 150 K is shown in Figure 4.13a. The mobility and other IGZO material parameters used were consistent with [75], and a summary of parameter values is provided in Table 4-II, column 2. An intrinsic mobility setting of μ_o = 14 cm^2/Vs provided appropriate current levels for comparison. Both temperature and carrier concentration dependence are managed entirely through the mobility relationship; the parameter values entered for BTS that describe the defect DOS distribution are completely insignificant and have no impact on device simulation results. The mobility dependence on carrier concentration completely overwhelms the role of BTS, as confirmed in Figure 4.13b which shows linear-scale simulation results from models with and without the defined acceptor tail states (i.e. N_{TA} & W_{TA}). Both on-state and off-state behavior shown have a dependence on gate voltage that cannot be represented by the IGZO.Tokyo drift mobility model due to the diminished role of BTS.

With the inclusion of BTS that have a significant influence on free charge, the parameter extraction method presented in [75] no longer applies. A hybrid model includes the carrier concentration and temperature dependence on channel mobility through IGZO.Tokyo, with the addition of BTS that provides a reasonable match to on-state and off-state characteristics. The defect DOS distribution used is that presented by Wager [70], which is fully consistent with defect/conduction DOS continuity and maintain the associated constraints on the relationships between N_C, m_e*, N_{TA}, and W_{TA} (see section 4.2). The mobility model parameters were arrived at iteratively through extensive TCAD simulation, with transfer characteristics shown in Figure 4.14. A summary of parameter values is provided in Table 4-II, column 3.



(a) (b)

Figure 4.14: Hybrid BTS-IGZO.Tokyo model results with adjusted parameters (Table 4-II, column 3)

As demonstrated, the hybrid BTS-Tokyo model represents the temperature dependent behavior of transfer characteristics from 150 K to 290 K reasonably well. The influence of both temperature and carrier concentration on the transfer characteristic behavior has contributions from both BTS and the mobility model. While perhaps empirically applicable, the physical basis of the IGZO.Tokyo mobility model is questionable. The intrinsic mobility value applied (μ_o = 24 cm^2/Vs) appears exaggerated to compensate for the increased role of BTS, rather than a full assignment to the mobility model. The defined BTS parameters maintain consistency with DOS continuity, however there is noted mismatch in the on/off transition region which is particularly dependent on the BTS distribution. In addition, the mobility model presents a complicated interaction between temperature and carrier concentration shown in Figure 4.12, with no proposed alternative to BTS for describing dependence on the latter. A simplified temperature-dependent mobility model that is independent of carrier concentration was pursued, with BTS defined to provide the appropriate influence on free channel charge.

4.3.4 Non-Fermi Mobility Model

A carrier concentration independent mobility model, referred to as "non-Fermi" (IGZO.NF) was implemented to isolate the effect of temperature and associated interactions with BTS and interface traps. The established BTS and interface trap parameters provided in Table 2-III (column 3) were applied to extract channel mobility values at different temperatures by matching TCAD simulated transfer characteristics to the experimental data. The defect state parameters along with the room temperature intrinsic channel mobility are listed in Table 4-II for comparison to other IGZO models discussed.

Table 4-II: Parameter values for various IGZO material (mobility) models; values with an asterisk indicate they were applied for model-fit compairsons.

Parameters	**Fung** [32] **(Atlas default)**	**Abe** [75] **(IGZO.Tokyo)**	**Hybrid w/BTS (BTS-Tokyo)**	**This work (IGZO.NF)**
N_C (cm^{-3})	5×10^{18}	5×10^{18}	5×10^{18}	5×10^{18}
m_e*	0.34	0.34	0.34	0.34
N_{TA} ($cm^{-3}eV^{-1}$)	1.55×10^{20}	1×10^{19}	1.11×10^{20}	3.25×10^{20}
W_{TA} (eV)	0.013	0.008	0.013	0.02
DOS continuity	NO	NO	YES	NO
μ_o (cm^2/Vs)	15 (RT)	14	24*	19 (RT)
T_γ (K)	NA	178.4	230*	NA
γ_0		-0.31	-0.10*	
n_{CR} (cm^{-3})		1×10^{20}	1×10^{20}	
NTA_{IT} ($cm^{-2}eV^{-1}$)	0	5×10^{13}*		
WTA_{IT} (eV)	0	0.007*		

A remarkable fit to experimental data at temperature range 150 K to 290 K was realized using a constant mobility at each temperature, as shown in Figure 4.15. The functional dependence of mobility on temperature is revealed in Figure 4.16. Using the channel mobility values found via TCAD simulation match at T ≤ 250 K, the resulting power-law fit resembles $\mu \sim T^{+3/2}$ behavior that is consistent with ionized defect scattering. The mobility model is expressly independent of carrier concentration, without dependence on the applied gate bias.

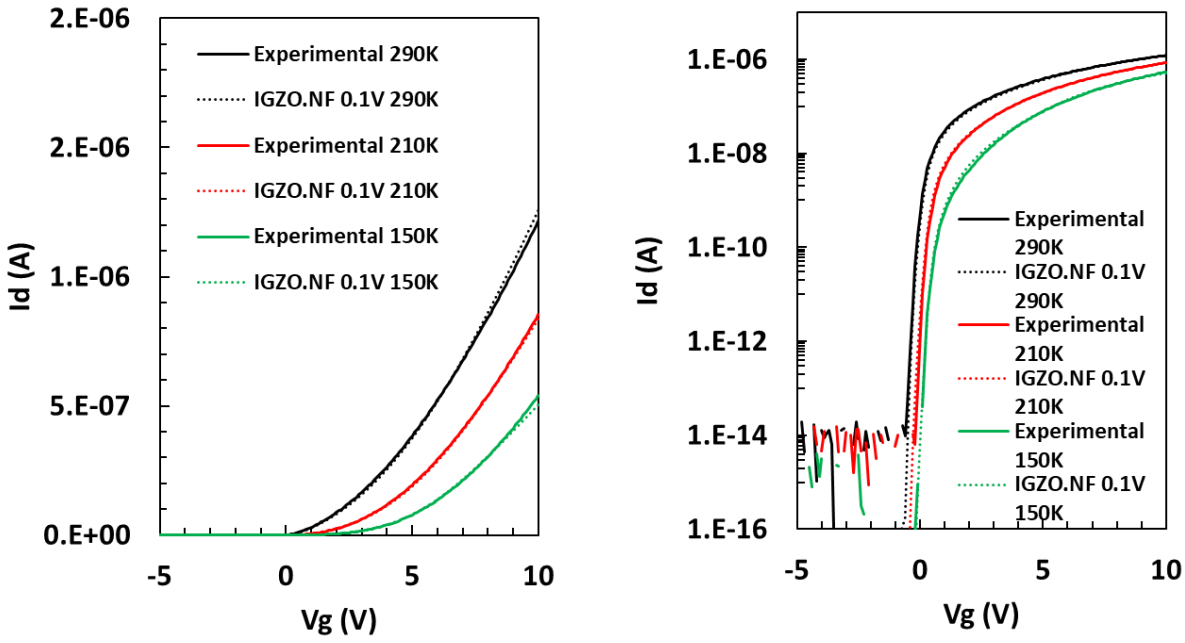


Figure 4.15: Non-Fermi mobility model with mobility as a function of temperature with V_D=0.1V.

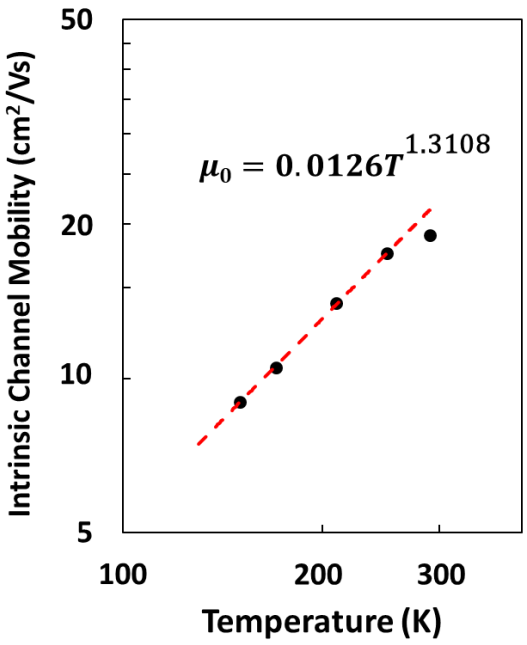
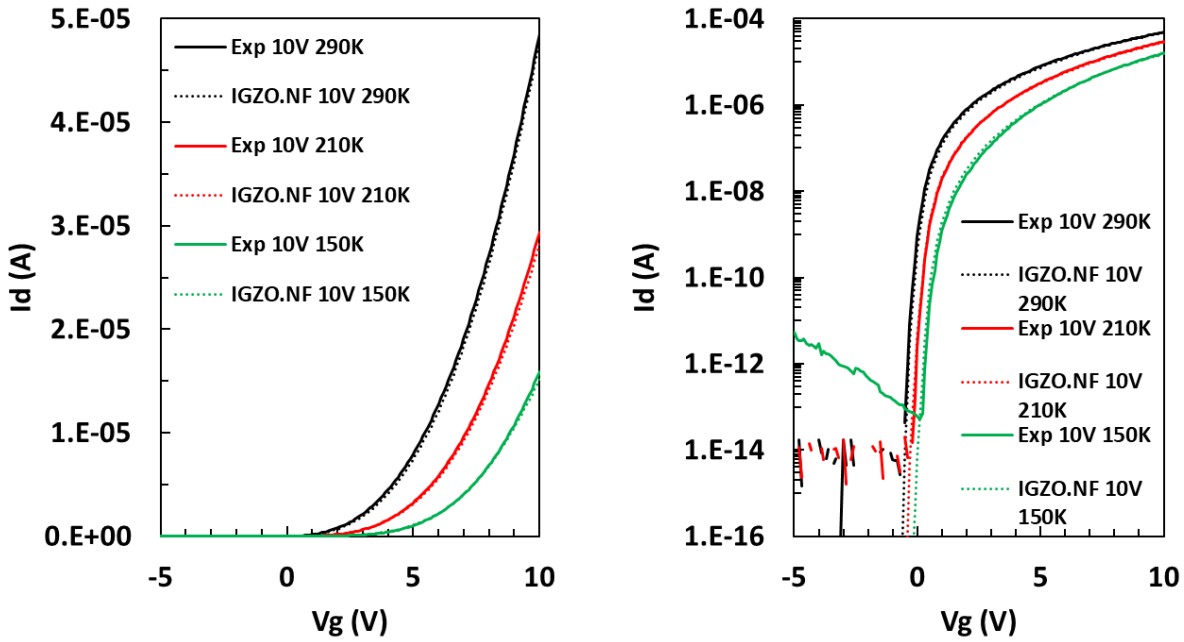


Figure 4.16: Power law fit of mobility extracted from IGZO.NF model as a function of temperature, at room temperature μ_o=19cm^2/Vs and at 150K μ_o=9cm^2/Vs.

At temperature above 250 K there is a deviation from the low-temperature trend which reflects a contribution from phonon scattering. While phonon scattering governs mobility behavior in lightly doped crystalline semiconductors such as silicon, the ion scattering mechanism appears to dominate the mobility behavior in IGZO, even approaching room temperature operation. The ionized states that are responsible for this proposed mechanism remain in question. These states are not presently defined in the TCAD model, and the electron mobility has no specified dependence on ion concentration. The Vo^+ donor states have an integrated concentration [Vo] ~ 5x10^{15} cm^{-3} which is relatively low, and become neutral at low temperature and thus do not participate in coulombic scattering events. The defined BTS are acceptor-like, and integrate to a relatively high concentration, N_{BTS} = 6.5x10^{18}cm^{-3}. However, the significant involvement of BTS in coulombic scattering would necessarily result in Fermi level dependence, i.e. $\mu_o = f(E_F)$. The

defined interface traps are also acceptor-like, however the integrated trap density N_{IT} = 3.5x10^{11} cm^{-2} is very low and these states are assumed to be physically located at the back-channel which does not present scattering sites for the majority of channel charge. In addition, a scattering mechanism involving acceptor-like interface traps would also necessarily result in a channel mobility with Fermi level dependence. This suggests that there are both positive and negative fixed ionic states in the IGZO structure which are responsible for the observed scattering behavior, yet present no net space charge and thus have no additional influence on device operation.



(a) (b)

Figure 4.17: Non-Fermi mobility model with mobility as a function of temperature with V_D=10V.

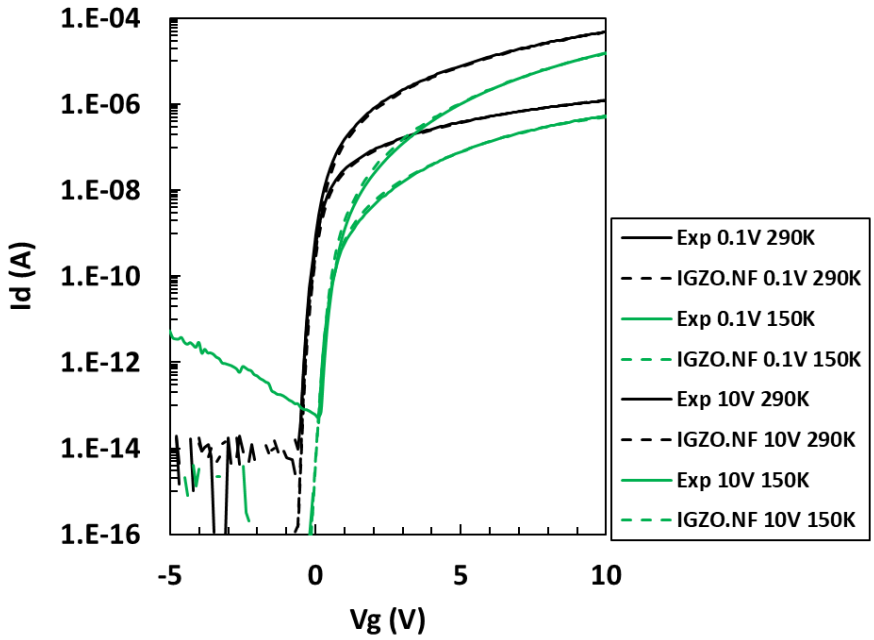
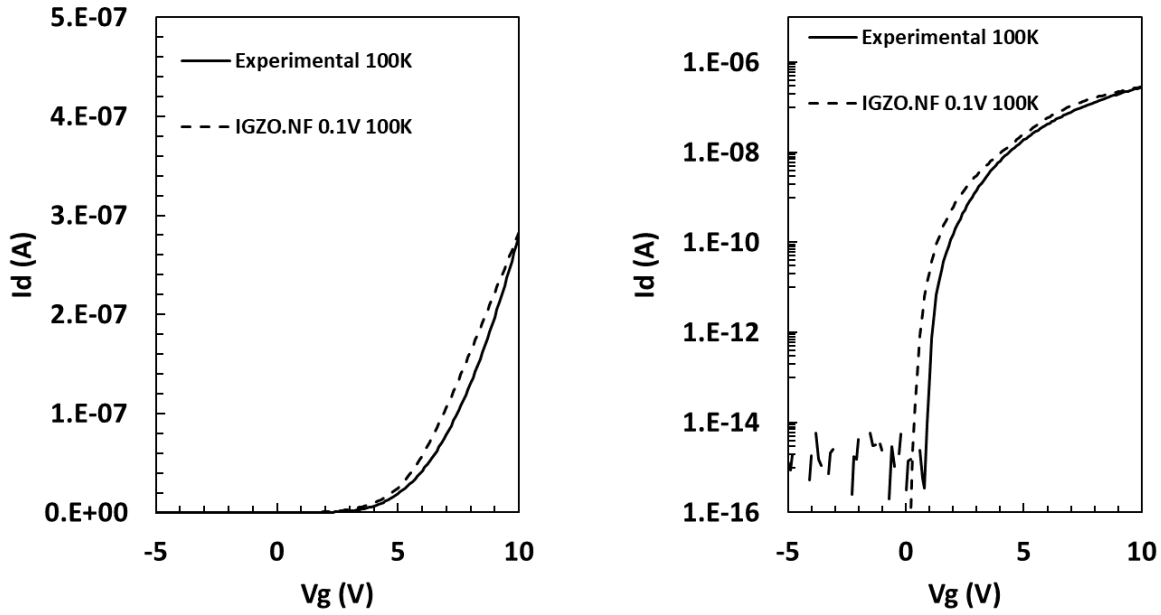


Figure 4.18: Low drain & high drain for 290K and 150K using IGZO.NF model with mobility as a function of temperature.

Furthermore, an excellent match to high drain (V_{DS} = 10V) characteristics is observed when using the same mobility values without adjustment, as shown in Figure 4.17. Pairs of transfer characteristics measured at room temperature and 150 K are shown in Figure 4.18 with simulated characteristics using the established mobility values, validating both temperature dependence and Fermi level (i.e. carrier concentration) independence. This result also validates the on-state compact model discussed in section 5.4, which uses a channel mobility that is independent of carrier concentration, with BTS serving the role of regulating the level of free charge as dependent on both gate bias and drain bias conditions. At 100 K (low-temperature regime) the intrinsic mobility based on the model in Figure 4.16 is μ_o = 5.3 cm^2/Vs, which seems to predict the on-state current reasonably well as shown in Figure 4.19. However, the model starts to deviate from the

experimental behavior which can be attributed to a transition from band conduction to localized state hopping transport discussed in section 4.1.1.



(a) (b)

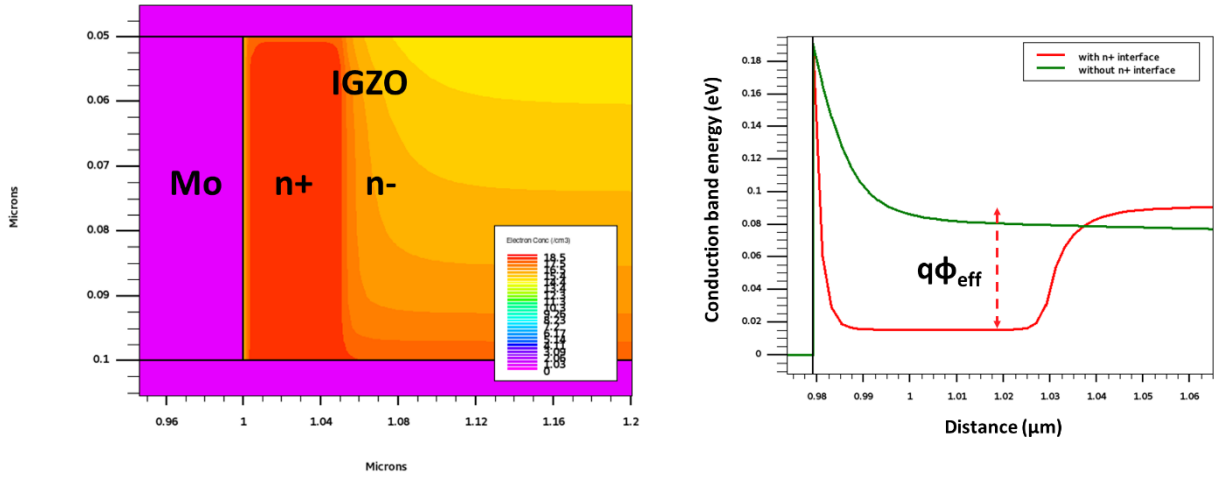
Figure 4.19: IGZO.NF model with mobility as a function of temperature at 100K in (a)linear scale and (b) Log-scale

4.3.5 Revisiting the Contact Model

The mechanism of source injection has been modeled as ohmic through a decrease in the contact metal workfunction to a low enough value (i.e. 4.13 eV) such that the metal-semiconductor barrier remains negligible, even at low temperature. Modification of the device structure to include a submicron n+ interface region adjacent to the S/D contacts that is assumed to have a higher electron concentration promotes source injection through enhanced electron tunneling using the UST model.

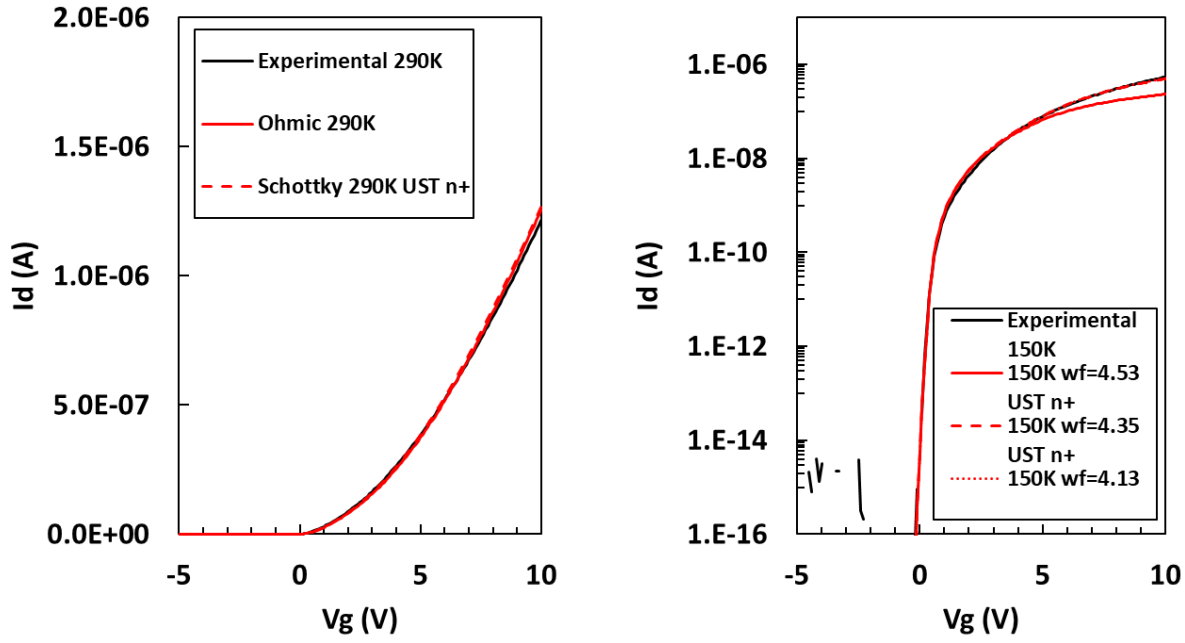
Due to the physical sputtering process, the IGZO in direct contact with the S/D metal may have a higher level of V_O which assists the injection of electrons into the channel. The structure shown

in Figure 4.20a includes a thin (50 nm) n+ interface region with the oxygen-vacancy donor concentration increased to $N_{OV}=10^{20}$ $cm^{-3}eV^{-1}$. The n+ interface modification narrows the tunneling barrier and presents lower energy states available for source injection, which is observed in Figure 4.20b. Comparisons of IGZO TFT simulation using different contact definitions at room temperature and T = 150 K are shown in Figure 4.21a&b respectively. With the contact workfunction set to $q\Phi_M$ = 4.35 eV, the UST model matched ohmic behavior at both RT and 150 K. However, with the contact workfunction set to the generally accepted value for molybdenum ($q\Phi_M$ = 4.53 eV), the simulated characteristic at T = 150 K remained clipped. This suggests that there is a departure from the ideal Mo/IGZO Schottky barrier, which promotes barrier lowering and/or further enhances electron tunneling at the M-S interface, thus supporting ohmic contact behavior at low temperature.



(a) (b)

Figure 4.20: (a) n+ interface region (50 nm) at the source end with the oxygen-vacancy donor concentration increased to $N_{OV}=10^{20}$ $cm^{-3}eV^{-1}$, (b) n+ interface region near the source narrows the tunneling barrier and effectively reduces the barrier height ($q\phi_{eff}$) for source injection.



(a) (b)

Figure 4.21: (a) Schottky contact with UST & n+ interface and Ohmic contact show perfect match with experimental results at room temperature, here μ_0=19 cm^2/Vs, (b) At 150 K, wf=4.13 eV shows an almost perfect overlay with experimental results and simulated I-V using higher workfunctions with UST & n+interface here μ_0=9 cm^2/Vs.

4.4 SUMMARY

While consistency with DOS continuity was considered a desirable property of the hybrid BTS-Tokyo model described, the improved characteristic match to experimental data using the much simpler IGZO.NF mobility model must be recognized. The defect DOS definition allows both N_{TA} and W_{TA} parameters to be independent adjusted for an improved model fit, relaxing the continuity constraint. As discussed in section 4.2, this allowance decouples the band-tail disorder from the effective mass characterizing the extended band states. While the continuity criteria remains insightful for an ideal portrayal of the DOS distribution, such constraints are perhaps unrealistic considering the extensive variation of the influence of defect states on IGZO TFT operation presented in the literature. Relaxation of DOS continuity is not validated by widespread acceptance

or general practice, however strict adherence results in a significant compromise in model accuracy. It may be considered unreasonable to hold a device model for a non-ideal semiconductor material such as amorphous IGZO accountable to the expectations of an ideal mathematical derivation.

Chapter 5. SCALED IGZO TFTS

An established process for the fabrication of IGZO TFTs exhibits excellent electrical characteristics in both bottom-gate (BG) and double-gate (DG) configurations [40]. The channel length is defined by the source/drain (S/D) metal liftoff process, with approximately zero process bias as shown in Figure 5.1. This ensures a precise channel definition which is needed to approach the lithographic limit. However, limitations of the device electrostatics begin to give way to short channel behavior as the devices are scaled to channel lengths shorter than those shown in Figure 5.2. With the same IGZO and gate dielectric (SiO_2) thickness the DG device shows superior current drive and subthreshold operation, with associated tradeoffs in process complexity. To maintain long-channel operation on scaled devices the dielectrics used for the gate and back-channel regions are typically adjusted to overcome short-channel effects as lateral dimensions are reduced. In addition, the IGZO thickness can also be reduced. TCAD simulation results listed in Table 5-I shows how these parameters and gate electrode configuration influences drain-induced barrier lowering (DIBL), with the subthreshold voltage offset (ΔV) between low and high drain bias as a measure of short-channel behavior.

Table 5-I: TCAD simulation of short-channel response to TFT structure and film thicknesses

	Thickness (nm)		Gate	Lin/Sat
***L* (µm)**	**IGZO**	**Gox**	**Electrode**	**ΔV**
2.0	50	100	BG	0.02
1.0	50	100	BG	0.3
1.0	***50***	***50***	***BG***	***0.01***
0.5	50	50	BG	0.4
0.5	20	50	BG	0.2
0.5	50	50	DG	0.1

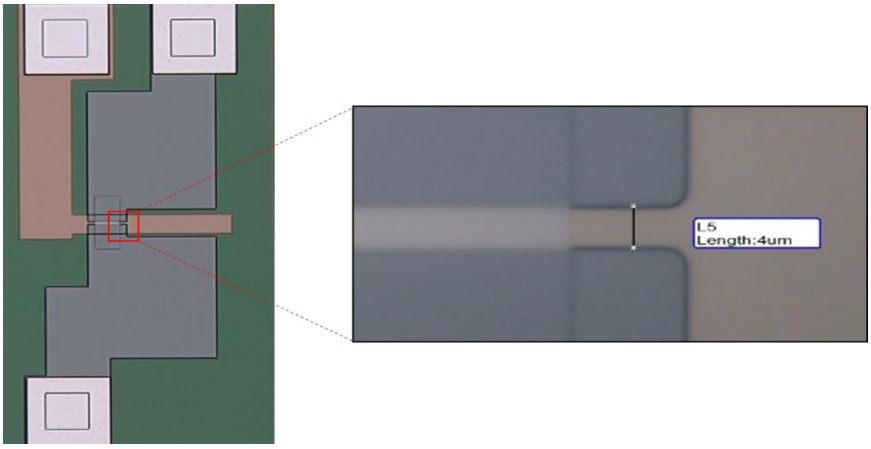
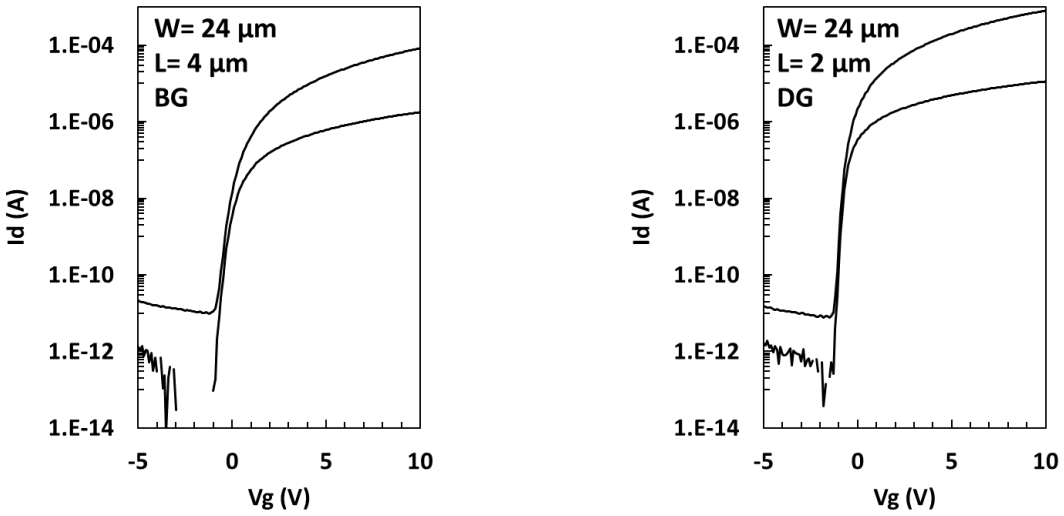


Figure 5.1: BG IGZO TFT with channel length L = 4 µm as defined by the S/D lift-off metallurgy using negative photoresist (Futurrex NR9g-1500PY) with almost negligible offset from the mask definition (i.e. ΔL ~ 0) [58].



(a) (b)

Figure 5.2: Transfer characteristics of IGZO TFTs with 100 nm SiO_2 gate/passivation dielectric. Drain bias conditions are 0.1V and 10V, (a) BG configuration with L = 4 µm. (b) DG configuration with L = 2 µm [58].

5.1 PRELIMINARY STUDY FOR SCALED TFTS

The options for scaling are clear; thinner gate dielectric, thinner IGZO, and DG configuration. However, the choice among these options must consider process tolerances and interaction effects, and impact on device reliability. The BG device with the established process supports a 2 µm channel length with long-channel operation, however the gate dielectric (PECVD SiO_2) thickness must be reduced for a 1 µm channel length device. For an L = 0.5 µm device, the DG configuration suppresses short-channel behavior without the need to thin the gate dielectric or the IGZO below 50 nm. Thus, the initial focus was on the DG device configuration. Thinning the BG dielectric was considered straightforward, however thinning the top-gate oxide required adjustment of the O_2 passivation anneal used to establish the IGZO semiconductor properties. The passivation anneal was reduced significantly to 3-hour O_2 anneal from 8 hour at 400 °C and keeping 2 hour-controlled ramp-down in O_2 ambient the same as before. This modified process was verified on the BG device operation with electrical results shown in Figure 5.3, demonstrating consistency with Figure 5.2a.

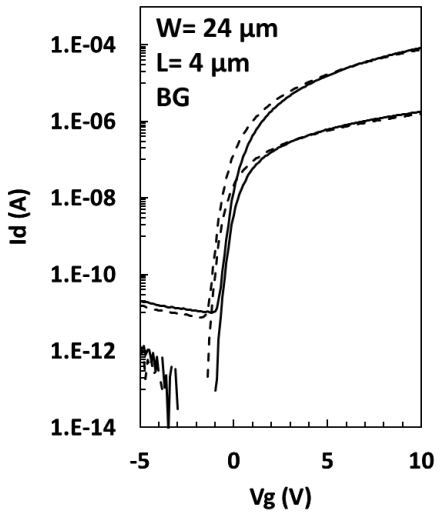


Figure 5.3: Transfer characteristics of an intermediate stage (gate oxide thickness remained at 100 nm and the passivation oxide thickness was reduced to 50 nm) BG device shown here in dashed line compared with device with gate oxide thickness and the passivation oxide thickness at 100 nm where each has W = 24 µm and L = 4 µm [58].

At this intermediate stage, the device demonstrated characteristics that were consistent with the previously established process. Arriving at the optimal O_2 passivation anneal process recipe required a significant engineering effort, yet appears deceptively trivial in hindsight. At this point the focus shifted towards reducing the gate oxide thickness and evaluating the revised process flow on scaled BG devices. The exposure system used for the lithographic processes was limited to an image resolution of approximately 1 µm, and thus submicron DG devices were not realized. The bold treatment listed in Table 5-I indicates that a reduction in gate dielectric thickness to 50 yield long-channel operation at length down to L = 1 µm. The details of the revised process flow with select treatment comparisons are described in the following section 5.2.

5.2 REVISED PROCESS CONDITIONS

To fabricate scaled BG TFT a 50 nm SiO_2 gate dielectric is deposited by PECVD (TEOS precursor, 390 °C) on the molybdenum gate electrode. The SiO_2 was densified for 2 hours in N_2 at 600 °C in a furnace. A second 50 nm PECVD SiO_2 passivation layer followed the IGZO mesa definition. A 3-hour O_2 passivation anneal at 400 °C with a 2-hour controlled ramp-down in O_2 ambient was performed, and was immediately followed by an HMDS vapor treatment at 140 °C to avoid water adsorption. The devices were then capped with 10 nm Al_2O_3 film using atomic layer deposition (ALD) at 200 °C.

5.3 SCALED IGZO TFTS

BG devices using the revised process displayed excellent electrical performance, with representative transfer characteristics shown above in Figure 5.4. The improvement over the characteristic shown in Figure 5.3 appears even more than what should be realized by the gate

oxide thickness reduction alone. In addition to a steeper subthreshold region, there is a notable right-shift in the characteristic that supports enhancement-mode operation and suppresses off-state leakage. This behavior was demonstrated on device samples which had the ALD Al_2O_3 layer applied immediately after the HMDS vapor treatment, which immediately followed the 400 °C O_2 passivation anneal. The application of an ALD capping layer as a water barrier has been previously reported with associated benefits in thermal stability [13]. While all samples received the HMDS vapor treatment, the time delay before the ALD capping layer was applied typically varied from 0 to 2 hours. This fortunate improvement in subthreshold and enhancement-mode operation seems to be associated with back-channel passivation that is absolutely free from adsorbed water molecules, indicating the difference is due to procedure rather than process definition.

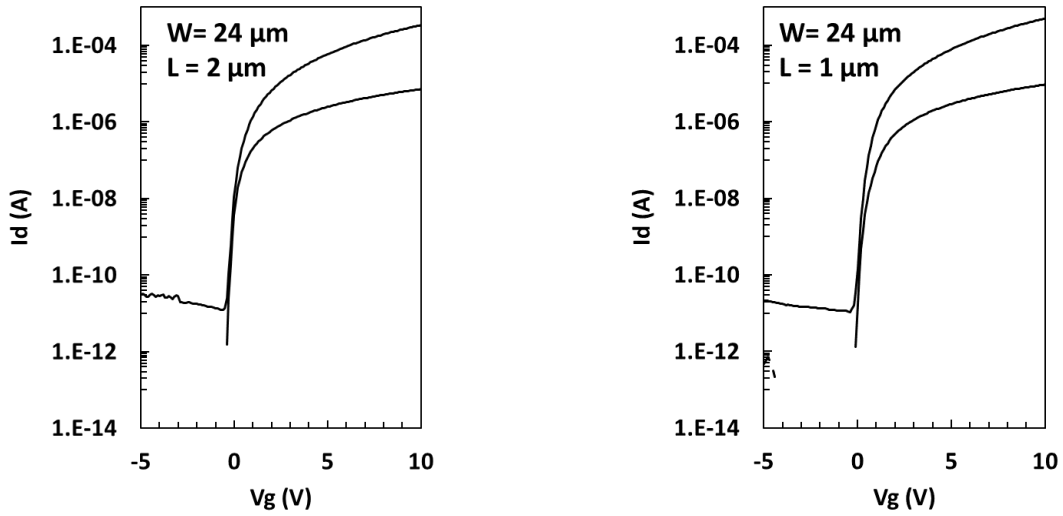
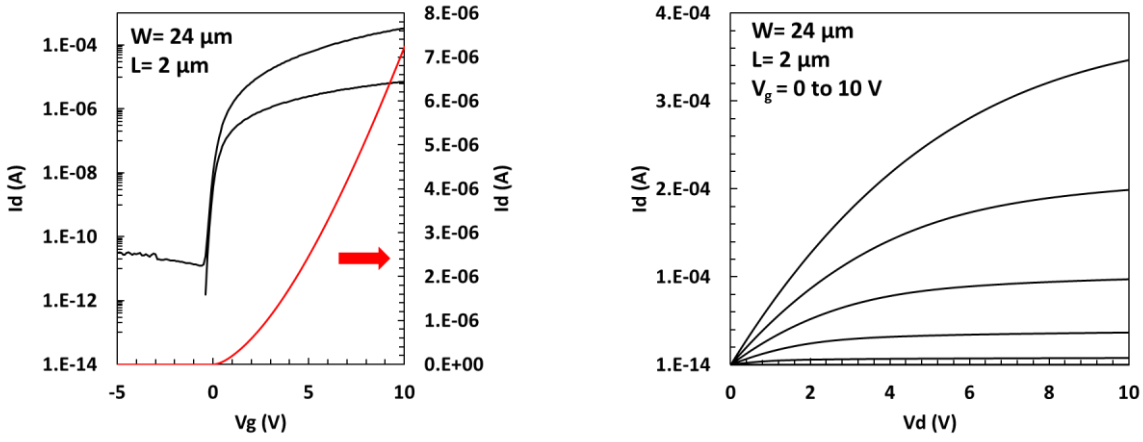


Figure 5.4: Transfer characteristics from BG devices fabricated with the revised process which included gate oxide thickness reduction to 50 nm. Excellent performance is demonstrated at 2 µm and 1 µm channel lengths, as suggested by Table 5-I [26].

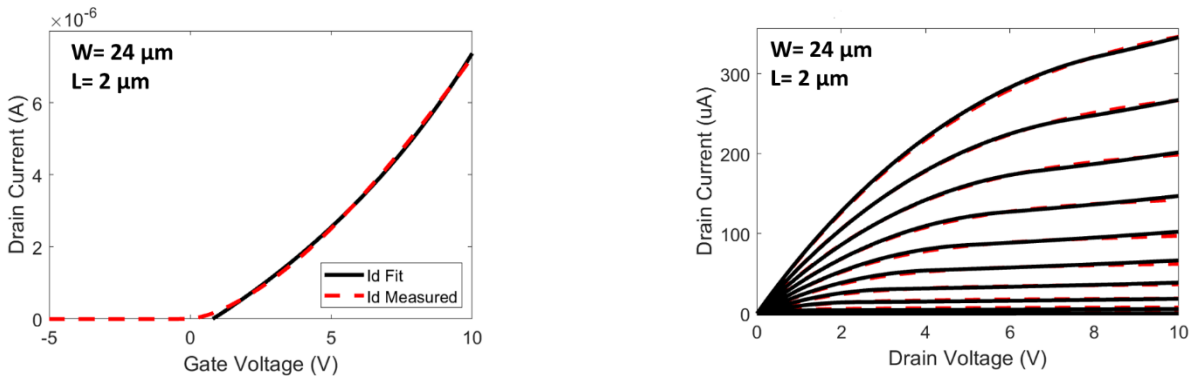
5.4 DEVICE MODELING OF SCALED IGZO TFTS

The 2 µm channel length device transfer characteristics shown in Figure 5.4 are also shown in Figure 5.5 next to the I_D-V_{DS} output characteristics. The linear-scale transfer characteristic shown demonstrates the typical concave-up characteristic associated with band-tail states (BTS). The influence of BTS is dependent upon both the gate and drain bias conditions, and renders traditional methods of parameters extraction not applicable. A new device model referred to as BTS2D has been recently developed that accounts for the bias-dependent level of trapped charge and free channel charge; complete details are described in [73]. Extraction of the redefined threshold voltage (V_T) as well as other operational parameters that represent the on-state transfer and output characteristics, and account for BTS and short-channel effects (SCE), was performed using nonlinear least-squares regression analysis in MathWorks® MATLAB®. The BTS2D model provides an excellent match to device measurements, as shown in Figure 5.6.



(a) (b)

Figure 5.5: Transfer characteristics (a) and output characteristics (b) of a representative BG device with 2 µm channel length. The Y2 axis in (a) shows the low-drain bias measurement on a linear-scale, demonstrating the influence of band-tail states on electrical behavior [58].



(a) (b)

Figure 5.6: BTS2D device model representing the on-state operation of a BG device with 2 µm channel length, showing an excellent fit to the linear-mode transfer characteristic (low drain bias) and output characteristic family of curves [58].

Table 5-II shows the mean ± standard deviation of the subthreshold swing (SS) and BTS2D model extracted V_T for 4 µm and 2 µm channel length devices with N = 10 sample size. The variation in V_T is relatively small and can be explained primarily by thickness variation in the PECVD SiO_2 gate dielectric. However, the same device dies were measured for each device size, thus the difference in V_T cannot be attributed to differences in sampling or process non-uniformity, neither random nor systematic. This length-dependent characteristic shift is counter to short-channel behavior and, although subtle, appears to extend to the 1 µm channel length device seen in Figure 5.4.

Table 5-II: Extracted Device Parameters (N=10).

***L* (µm)**	**V_T (V)**	**SS (mv/dec)**
4	0.79 ± 0.18	202.82 ± 31.23
2	1.07 ± 0.17	191.42 ± 27.78

5.5 THERMAL STRESS STABILITY OF SCALED IGZO TFTS

As mentioned previously in section 3.3.2, the application of the ALD Al_2O_3 capping layer as a water barrier has been associated with good thermal stability, which is a standard requirement for product integration. Thermal degradation at temperatures $T \leq 200$ °C typically cause a characteristic left shift and is also reported to be a more pronounced issue on long channel devices [13]. The scaled devices (L=2 µm) processed with ALD maintained thermal stability up to 250 °C (Figure 5.7).

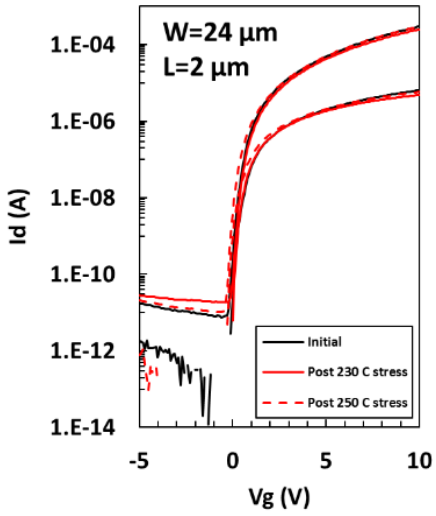
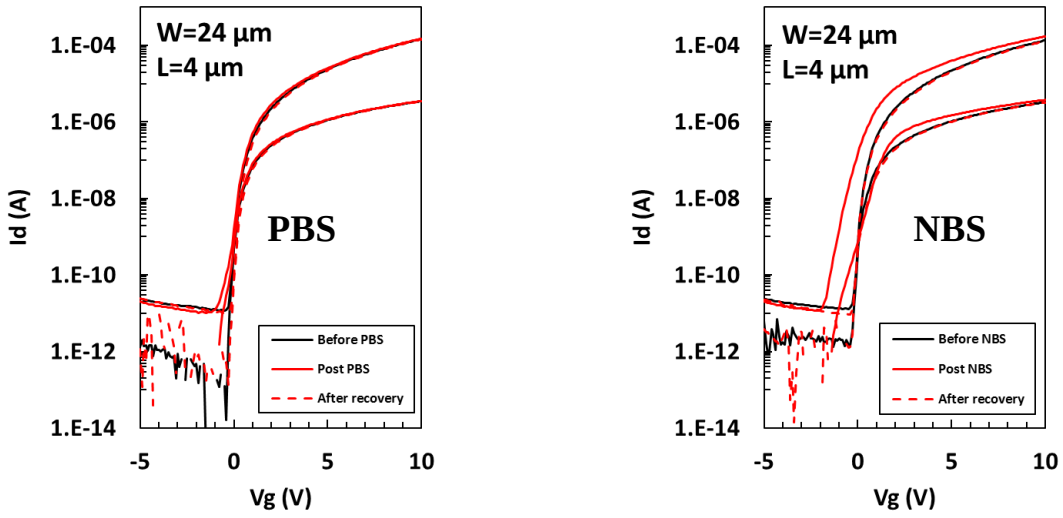


Figure 5.7: BG devices with ALD Al_2O_3 capping layer deposited at 200 °C with scaled channel lengths and 1-hour sequential thermal stress treatment temperatures as indicated [26].

5.6 BIAS STRESS STABILITY OF SCALED IGZO TFTS

The BG devices were also subjected to gate bias-stress conditions performed at room temperature to evaluate the resistance to the degradation of electrical characteristics. Positive bias-stress (PBS) and negative bias-stress (NBS) tests involved setting the gate voltage to ±10 V with S/D at reference ground. Devices used for bias-stress testing had a channel length of 4 µm, however the

applied stress conditions did not present significant lateral electric fields, and thus the response would not have a strong dependence on channel length. Transfer characteristics were measured immediately following 1 hour applied stress, with results shown in Figure 5.8. Both PBS and NBS induced an observable response that was completely reversible following 4 - 5 hours of relaxation time. The PBS response was very slight at picoampere current levels; negligible by most standards.



(a) (b)

Figure 5.8: Two separate BG devices showing effects of (a) PBS and (b) NBS applied at V_G = ±10 V with S/D at reference ground. The post-stress measurements were taken immediately following 1 hour stress duration. The PBS effect is virtually negligible, whereas the NBS effect indicates the influence of carrier traps. Both PBS and NBS effects were completely reversible [58].

The NBS response demonstrated distortion and spreading which indicates an influence of carrier traps. The NBS depletion of channel electrons has the opportunity to interact with the entire IGZO layer and associated interface regions. A negligible effect of NBS in the absence of illumination has been claimed [45], [74], although the applied NBS E-field in this work (2 MV/cm) is higher than these reports. A model presented in [63] proposes a weak-bond neutral oxygen vacancy defect state that is susceptible to reconfiguration as a double-donor oxygen vacancy defect (V_O^{2+}) during NBS with above-bandgap illumination, or NBIS as discussed in 3.4.3. This or a similar mechanism may be operative even without illumination due to the high E-field present.

Note that in this work the degree of lateral left-shift is relatively small; the transfer characteristic separation is not due to SCE, but rather is attributed to the inhomogeneity of donor-like trap states [40].

5.7 IGZO TFTs ON GLASS SUBSTRATE

Most of the TFT applications will require fabrication on glass substrate. In our previous studies the devices were fabricated on thick oxide on Si wafer. To ensure the compatibility of our TFT process on glass substrates the scaled devices were fabricated on Corning NXT glass wafers. In this process the devices were fabricated with the revised process flow described in section 5.2, with both 100 nm and 50 nm gate oxide. As shown in Figure 5.9, the TFTs showed excellent transfer characteristics in long ($L \geq 4$ µm) and short channel devices. The short channel devices exhibited steeper subthreshold slope.

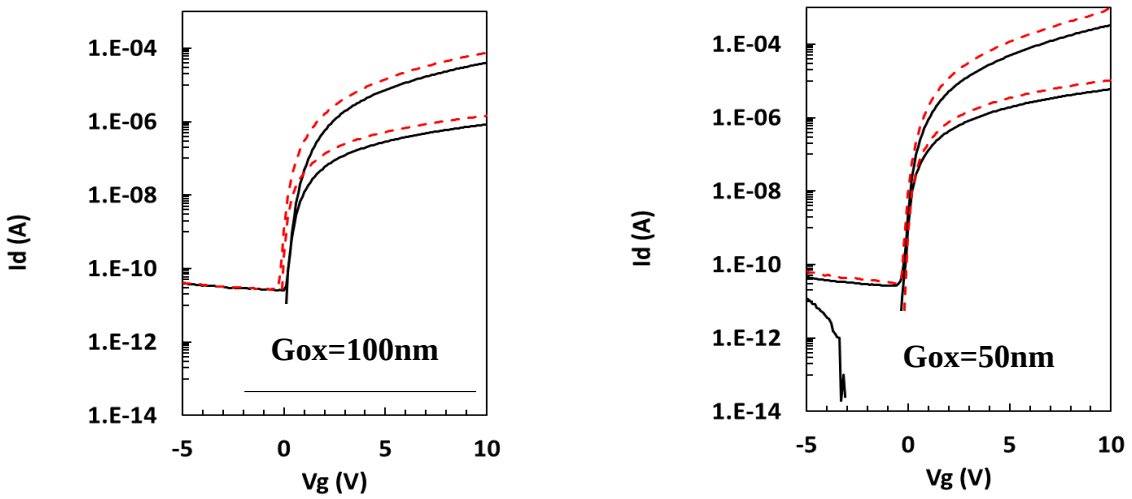


Figure 5.9: Devices fabricated on Corning NXT glass substrate with (a) 100 nm and (b) 50 nm gate oxide respectively. In (a) solid line represents L=6 µm and dashed line L=4 µm and in (b) solid line represents L=2 µm and dashed line L=1 µm.

5.8 SUMMARY

Scaled BG devices with a reduction in gate oxide thickness to 50 nm demonstrated excellent electrical characteristics at channel lengths as small as L = 1 μm. Thickness adjustment of the PECVD SiO_2 passivation layer required re-engineering the O_2 passivation anneal. While this change at the backchannel was not needed for improved electrostatic control on the BG device, it presents an optimized process for a scaled top-gate dielectric on a DG device structure. The specific details of the ALD Al_2O_3 capping layer, both process and procedure, where shown to be important in supporting enhancement-mode BG device operation with steep subthreshold characteristics and excellent thermal stability. The scaled process also maintained good stability when subjected to PBS and NBS, with complete recovery to initial characteristics.

Both the BG dielectric and the IGZO thickness could be reduced further to enable shorter channel length, however the DG device structure presents a conservative approach towards submicron dimensions that supports low variation and reliability. Unfortunately, DG devices with channel length below 1 μm were not realized due to limitations in the S/D patterning and metal lift-off processes. While such techniques can be used for nanoscale devices, the lift-off defined channel region with lithographic alignment tolerances to ensure gate-S/D overlap presents significant scaling challenges. A self-aligned gate process scheme utilizing ion-implanted S/D regions will be discussed in Chapter 6 that would support scaling trends similar to silicon device technology.

Chapter 6. SELF-ALIGNED IGZO TFTS

Self-aligned (SA) channel regions in thin-film transistors have advantages in reduced parasitic capacitance and stage delay, and a reduction in overhead real estate. A common method used to fabricate self-aligned a-Si:H TFTs is to utilize a through-glass exposure of photoresist which is blocked by the opaque metal bottom-gate electrode [79], [80]. This process does not require an additional photomask or lithographic alignment, and thus supports low production cost. Sputtered IGZO has been introduced into flat panel display product manufacturing, exhibiting a channel mobility of approximately an order of magnitude higher than a-Si:H. The working source/drain (S/D) electrodes in IGZO TFTs can be direct metal contact regions to the IGZO, without the need for additional processes such as doping to render the IGZO conductive. Proper metallurgy and annealing processes can provide ohmic behavior with minimal series resistance [72], however this usually requires several microns of gate-to-S/D overlap in order to ensure such behavior. Various self-aligned channel strategies have been demonstrated that either utilize a TG structure or a through-glass exposure for BG configurations [81], [82]. The SA-TG or associated SA-BG feature must protect the channel region during S/D formation.

Various techniques that have been used to selectively form conductive IGZO regions include hydrogen diffusion [83], hydrogen plasma treatment [84]–[86], argon plasma [87], and arsenic implantation [88]. In the current work the activation of IGZO S/D regions by O_2 plasma and ion implantation using $^{31}P^+$, $^{19}F^+$, $^{40}Ar^+$, and $^{11}B^+$ has been investigated on different gate-electrode configurations. Activation behavior due to $^{40}Ar^+$ implant would be associated with ionized defect states, such as oxygen vacancies [89], [90] whereas activation behavior due to the other implanted

ions would be associated with either ionized defect states and/or the implanted element serving as an electrically active species. Annealing was done both before and after the S/D implant treatment to explore the possibility of enhanced activation and/or thermal instability. SA-TG devices with $^{11}B^{+}$ and $^{40}Ar^{+}$ implanted regions demonstrated ohmic contact behavior with TFT results showing DC operation comparable to metal-overlapped devices. SA-BG devices were also fabricated using backside flood exposure on glass substrate.

6.1 LITERATURE REVIEW

Different TFT electrode configurations (BG, TG and DG) have been utilized, with selection depending on the specific application. Scaling the channel length ($L \leq 2$ μm) and integrating the devices on glass or flexible substrates would have major impact on the display industry. To achieve submicron IGZO TFTs, self-aligned (SA) strategies have been explored where the channel length is not defined by the S/D metal separation, but rather by the gate dimension. It offers the ability to scale down to smaller channel lengths without the associated limitations of a channel length defined by the S/D contact regions. Non-SA TG coplanar TFTs typically exhibit inferior performance due to high parasitic capacitance induced by the overlap between gate and source/drain electrodes (RC delay). Also, a decrease in gate capacitance at the edges of the channel adjacent to the S/D is observed in such structure as shown in Figure 6.1a. SA-TG coplanar TFTs exhibit superior performance because overlap between gate and source/drain electrodes can be eliminated which reduces the parasitic capacitance as shown in Figure 6.1b.

(a) (b)

Figure 6.1: Cross sectional image of (a) non-SA TG TFT and (b) SA-TG TFT (The patterned region indicates the ion-implanted mesa).

A self-aligned structure has other advantages, such as enhanced channel length scalability, and process integration options over the standard non-SA structure making it especially desirable for high-resolution applications [91]. Fabrication of self-aligned IGZO TFTs requires the formation of a homojunction between the highly conductive IGZO serving as the S/D regions and the semiconducting IGZO serving as the channel region. Among the several different of ways to form such a highly conductive IGZO layer, DUV irradiation [92], plasma treatments [51], [85], [89], [93], [94] and ion implantation [95], [96] are methods that have been reported which will be discussed briefly in the next few sections.

6.1.1 Deep UV Irradiation

This technique uses deep ultraviolet (DUV) irradiation to define the source/drain (S/D) region of SA coplanar IGZO TFTs. Here, the gate mask pattern acted as a DUV shield layer to define the source/drain regions for selective DUV irradiation at wavelengths of 185 nm and 254 nm and an energy of 30 J/cm^2 as shown in Figure 6.2.

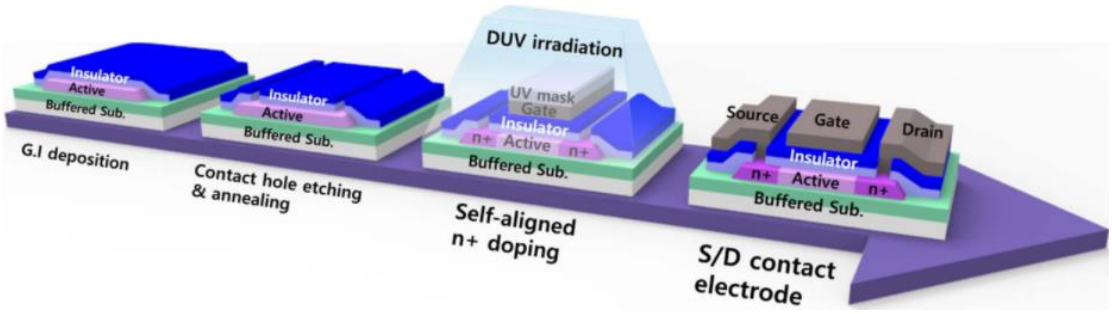
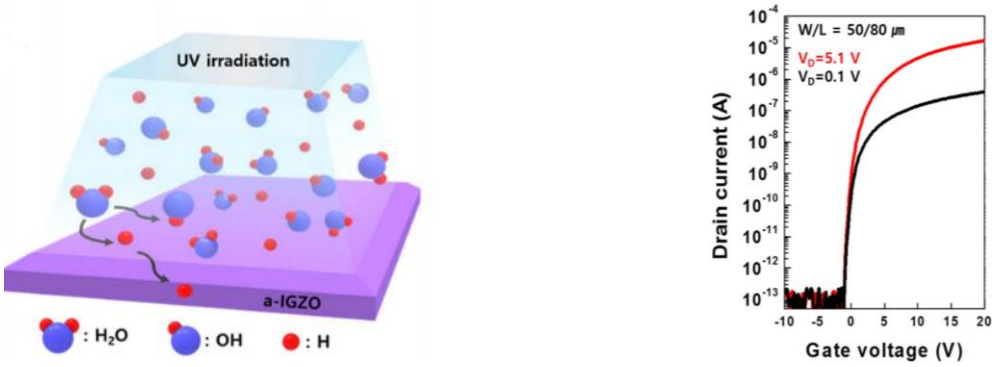


Figure 6.2: Schematic process flowchart for a coplanar SA-TG IGZO TFT with S/D regions formed by DUV irradiation energy of 30 J/cm^2 . Adapted from [92].

DUV irradiation-induced increase in oxygen deficiencies and dissociation of water molecules in IGZO thin film indicates an increase in carrier concentration in the film. The water molecule bond dissociation energy is 497.1 kJ/mol or 5.1 eV [97]. The energies of DUV light of 185 nm and 254 nm wavelength are 6.7 eV and 4.9 eV, respectively. Therefore, 185 nm wavelength DUV is likely to decompose the water molecules into H and OH radicals through photochemical water dissociation as shown in Figure 6.3a. As a result, the hydrogen can donate electrons in the IGZO thin film increasing the conductivity of the film [20].



(a) (b)

Figure 6.3: (a) Scheme of photochemical dissociation caused by DUV irradiation and (b) transfer characteristics of self-aligned coplanar IGZO TFT with DUV irradiation energy of 30 J/cm^2. The channel width (W) and length (L) were 50 and 80 μm, respectively. Adapted from [92].

The electrical properties of the device are shown in Figure 6.3b, with a field-effect mobility μ_{FE} = 13.2 cm^2/Vs, subthreshold swing SS = 0.32 V/decade, and threshold voltage V_T = 3.2 V [92]. However, this technique would be a challenge for SA-BG devices. Also, hydrogen incorporation during DUV irradiation may lead to degraded thermal stress stability as hydrogen can rapidly diffuse and may extend across the entire IGZO channel region as discussed in section 3.3.

6.1.2 Plasma Treatment

Plasma treatment using H_2, O_2, Ar can be an effective method to decrease the resistance of IGZO. However, hydrogen can rapidly diffuse out of the S/D region into the IGZO thin films at a temperature above 200 °C leading towards large series resistance in S/D regions of the device and poor device performance as shown in Figure 6.4. The oxygen vacancies in the S/D regions created by argon plasma treatment decrease after thermal annealing, which increase the sheet resistance of the S/D regions. Thus, thermal stability becomes the main concern for IGZO TFTs with S/D regions formed by argon or hydrogen plasma treatments [95].

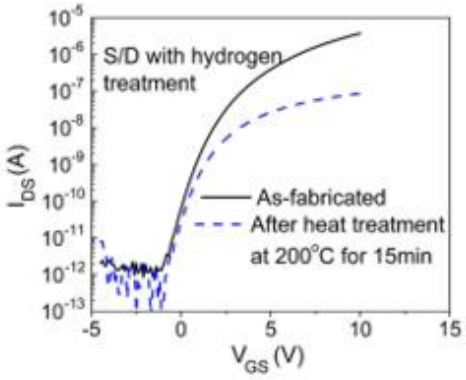
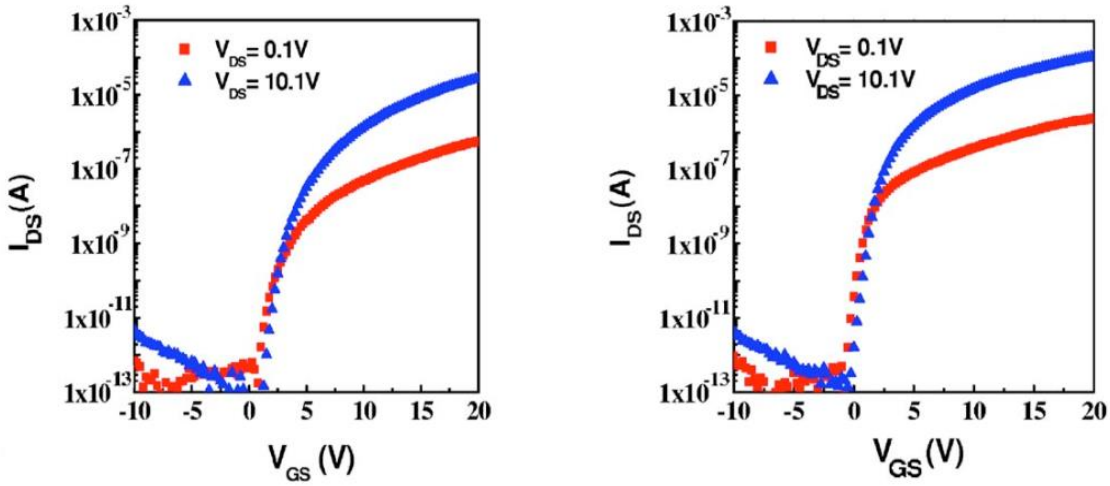


Figure 6.4: Transfer characteristics of the IGZO TFTs with S/D regions treated with hydrogen plasma under heat reatment at 200 °C. Adapted from [95].

Energetic Ar ion bombardment during plasma treatment induces the preferential sputtering of the relatively light atoms from the surfaces of II-VI or III-V group semiconductors as a result of the physical momentum transfer between the ions in the plasma and the atoms on the material surface [90]. Therefore, the oxygen on the IGZO film surface is preferentially dissociated by the Ar ion bombardment and increases the net electron concentration by the formation of an oxygen deficient surface layer as compared to the bulk IGZO film. The transfer characteristics of non-SA IGZO TFT with and without Ar^+ plasma treatment is shown in Figure 6.5. An excellent SS of 0.19 V/decade, I_{on}/I_{off} ratio of 10^8 and μ_{FE} of 9.1 cm^2/Vs were achieved for the IGZO TFTs with Ar^+ plasma treatment. The improvements were attributed to the reduction of the contact resistance between the source/drain electrodes and IGZO semiconductor. It should be noted that the Ar^+ plasma treatment is carried out before depositing the S/D metal with no additional anneal treatment.



(a) (b)

Figure 6.5: Representative transfer characteristics (W/L=50/4 µm) of IGZO TFTs (a) without and (b) with Ar plasma treatment before depositing the source/drain electrode. Adapted from [90].

6.1.3 Ion Implantation

Ion implantation has also been used as an effective technique to decrease the resistance of IGZO film. The development of a SA IGZO TFT with good performance and high stability is necessary. Successful reports on SA IGZO TFTs with S/D regions doped by implanted arsenic [88] or phosphorus [96] show good electrical performance and high thermal stability.

The SA S/D regions were implanted with $^{31}P^{+}$ at a dose of 5×10^{15} cm^{-2} and energy of 45 keV using the gate electrode Indium Tin Oxide (ITO) pattern as a mask as shown in Figure 6.6 [96]. The implanted phosphorus dopant was activated by annealing at 500 °C for 25 min in O_2 ambient. Results exhibited good transfer TFT characteristics at a drain-to-source voltage (V_{DS}) = 0.2 V, with μ_{FE} of 5 cm^2/Vs, V_T of 5.6 V, an SS of 0.5 V/dec, and an I_{ON}/I_{OFF} ratio of 6×10^7 [96]. The proposed IGZO TFT shows much better thermal stability as shown in Figure 6.7 compared to the S/D regions formed by plasma treatment as shown in Figure 6.5.

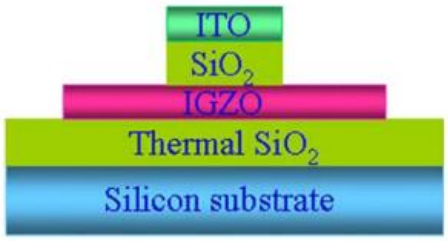
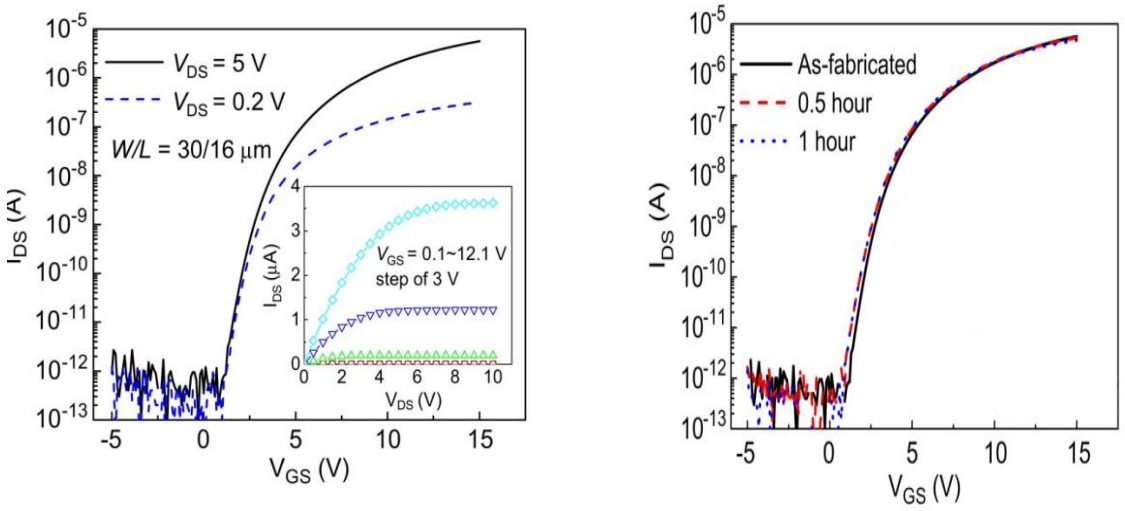


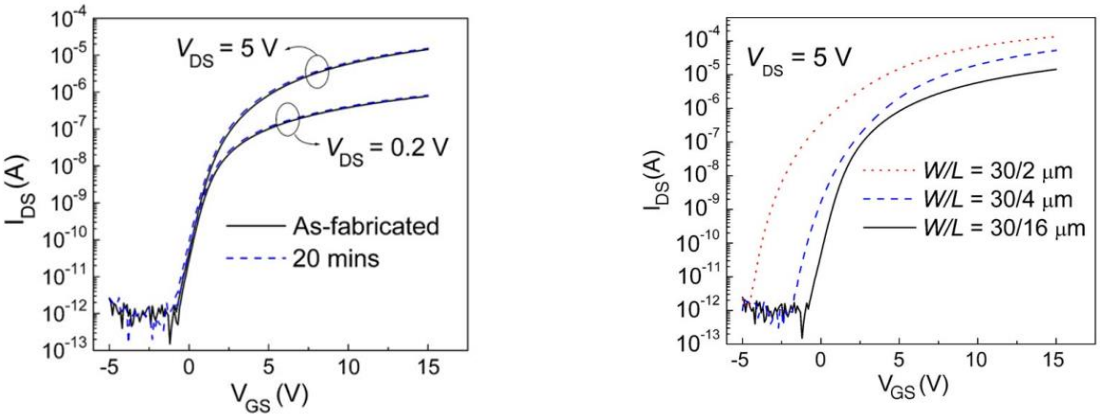
Figure 6.6: Cross-sectional schematic of the proposed IGZO TFT with SA-TG structure. Adapted from [96].



(a) (b)

Figure 6.7: (a) Transfer and output characteristics (shown in the inset) of the self-aligned top-gate IGZO TFTs with phosphorus doped S/D regions and (b) transfer characteristics under thermal stress treatments at 200 °C. Adapted from [96].

In this report [98], the SA S/D regions were masked using gate-electrode ITO pattern and implanted with arsenic at a dose of 5×10^{15} cm^{-2} and energy of 100 keV. To activate the implanted arsenic dopant, an annealing process at 525 °C for 30 min in O_2 ambient was performed. The proposed mechanism suggested arsenic substitution on the zinc site introducing a donor state, however, a potential alternative mechanism could be the defect associated with the presence of arsenic or displacements (i.e., oxygen vacancy). Also, oxygen vacancies in the S/D region decreased after the thermal annealing following the implant which increased the sheet resistance of the S/D region.



(a) (b)

Figure 6.8: (a) Transfer characteristics of the IGZO TFTs with arsenic doped S/D regions under thermal stress treatment for 20 min at 200 °C (W/L=30/16) and (b) transfer characteristics of the IGZO TFTs with the same channel width but different channel lengths. Adapted from [98].

The IGZO TFTs showed good transfer characteristics at V_{DS} = 0.2 V, with μ_{FE} of 12 cm^2/Vs, V_T of 3.5 V, SS of 0.5 V/dec, and I_{ON}/I_{OFF} ratio of 9×10^7. The gate leakage current for the TFTs was ~10 pA. In SA-TG devices the edges of the gate-dielectric could be damaged by ion-implantation due to lateral scattering which is not an issue in SA-BG. The devices were also thermally stable as seen from Figure 6.8a. However, channel length dependence was. The TFTs scaled down nicely to channel lengths of $L \geq 4$ μm with a small change of the threshold voltage and little degradation of subthreshold swing as seen from Figure 6.8b. For L = 2 μm channel length devices, the threshold voltage shifted largely to the left which might be due to the lateral diffusion of the arsenic dopant into the channel region. Investigations of SA devices using plasma and ion-implantation technique is detailed in the subsequent sections.

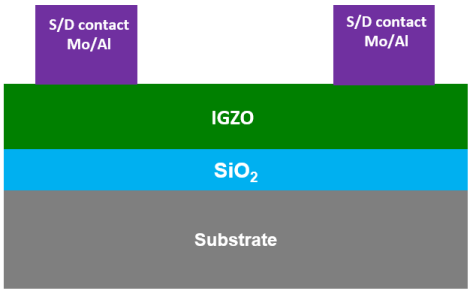
6.2 SA-TG CO-PLANAR TFT

The SA-TG process shown in Figure 6.9 began with a thick isolation oxide (~500 nm SiO_2) thermally grown on a silicon wafer as the starting substrate. A 50 nm IGZO layer was sputtered

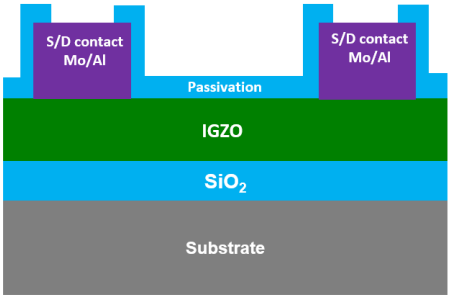
using an $InGaZnO_4$ (1:1:1:4) target in an argon ambient with 7% oxygen, and then patterned and etched using dilute HCl.

(a) Thick oxide growth

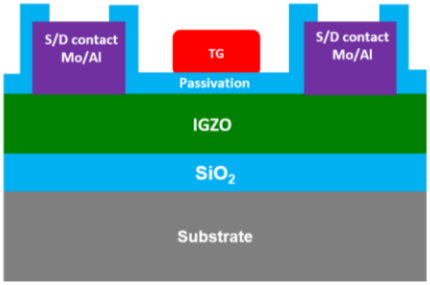
(b) IGZO MESA definition



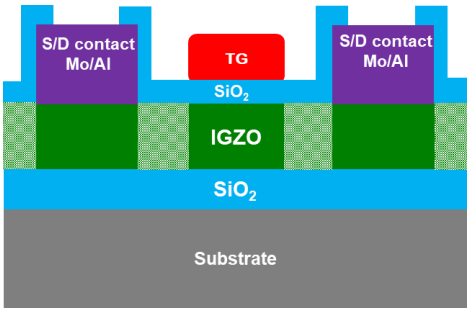
(c) S/D contact metal (Mo/Al sputter)



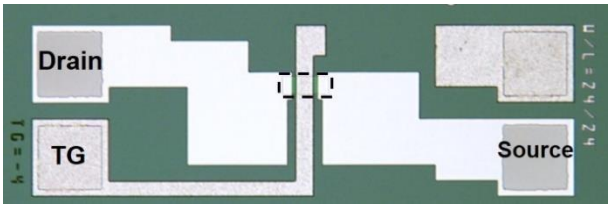
(d) Passivation & anneal/Passivation open



(e) TG (Flash Al)



(f) IGZO S/D treatment



(g) Top-down view of a fabricated SA-TG IGZO TFT

Figure 6.9: (a-f) Step by step cross-sectional schematic of SA-TG (Type-TL (Treatment Last)) device, where the textured and non-textured IGZO represents implanted and non-implanted regions, respectively. Note that in this process scheme (type-TL) the implant is blocked in both channel and S/D metal contact regions and (g) top-down view of a fabricated SA-TG IGZO TFT.

The S/D contact metal (100 nm Mo/Al bilayer) was sputtered and patterned using a lift-off process. A 50 nm PECVD SiO_2 layer was then deposited as the gate dielectric. This was followed by 3 hr O_2 anneal at 400 °C with 2 hr controlled ramp-down in O_2 ambient. The devices were then capped with 10 nm Al_2O_3 film using ALD at 200 °C. The S/D contact regions were opened using 10:1 buffered HF. The TG electrode was then defined using evaporated Al with a lift-off process. Finally, the active S/D regions of the samples were then treated using ion-implantation or O_2 plasma. Figure 6.9g shows an image of a fabricated SA-TG device with S/D gaps of 4 µm visible over the outlined mesa region between the TG and the S/D metal contacts.

6.2.1 Oxygen Plasma Treatment

It is known that oxygen vacancies (V_o) act as donors in the IGZO film [15], thus it is crucial to optimize the channel region to achieve ideal characteristics. In this work, O_2 plasma was used to treat the underlapped IGZO regions in a similar fashion as previously investigated using argon plasma which attributed enhanced conductivity to the preferential dissociation of oxygen on the IGZO film surface by the $^{40}Ar^+$ ion bombardment due to its relatively high sputtering yield [90].

The parameter settings of power and exposure time were 0.3 kW and 1, 2, and 5 minutes, respectively. The insight gained by showing the "non-activated" device operation is the lateral position of the characteristic in comparison to the "activated" device as shown in Figure 6.10a. The device characteristics are left shifted from standard TG device, with the amount of V_T shift (at $I_d = 10^{-10}$ A) and the low-V_{DS} drain current (at $V_g = 10$ V) increasing with immersion time as shown in Figure 4.2b. The devices showed increased current with plasma immersion time which clearly indicates improvement in channel charge injection. Unfortunately, the associated shift in V_T progressively worsened. The V_T shift might be recoverable by O_2 anneal which could be

counterproductive to maintain high carrier concentration. Note that this technique is not directly compatible with SA-BG devices if photoresist is used for back-channel protection, since it would be etched by the O_2 plasma. Plasma treated IGZO TFTs also suffer from thermal stability issues [83]. Hence, an alternative strategy using ion implanted S/D activation is discussed in the following section.

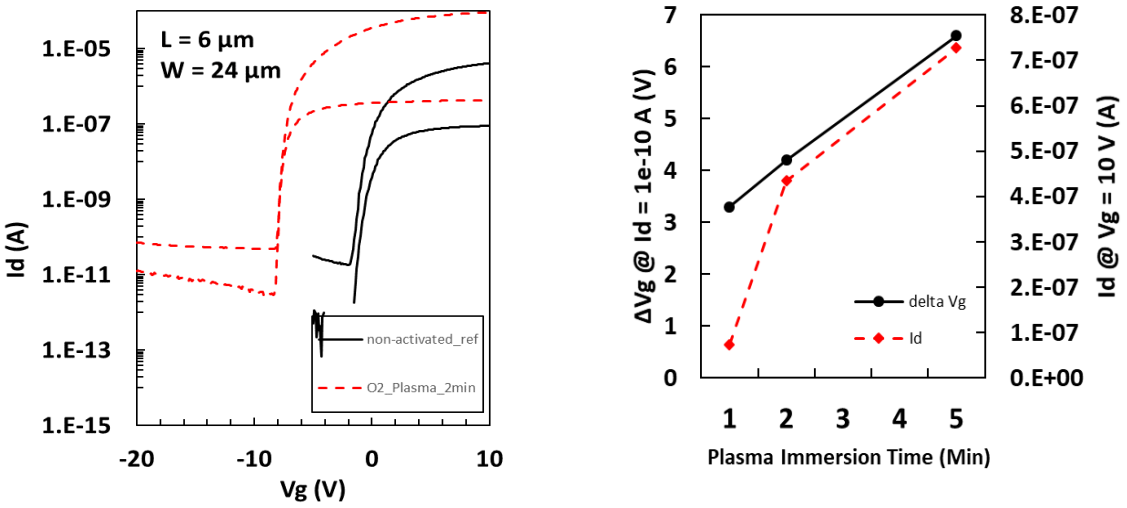


Figure 6.10: O_2 plasma treated self-aligned TG device response with L = 6 µm and W =24 µm, with 4 µm underlap between TG and S/D contact metal. (a) Transfer characteristics measured before (solid line) and after (dashed line) the treatment with t = 2 min and and 0.3 kW power and (b) the amount of V_T shift at $I_d = 10^{-10}$ A and the increase in I_d at V_{GS} = 10 V and V_{DS} = 0.1 V observed based on the plasma immersion time.

6.2.2 Ion Implantation

In this study, SA-TG and BG co-planar TFTs has been fabricated using ion implantation to selectively form conductive IGZO regions, with the channel region masked by the gate electrode. Several different species have been explored as shown in Table 6-I. Implant energies were chosen to ensure that a significant fraction of the dose resides in the IGZO film. Only implantation of boron and argon ions have been demonstrated to successfully "activate" IGZO. In this context, the

term “activate” refers to the formation of conductive IGZO regions through the implantation process without annealing.

Table 6-I: Design of experiments for ion-implantation treatment to realize SA-TG TFTs.

Species	Energy (keV)	Dose (cm^{-2})	Beam Current (μA)
$^{31}P^{+}$	80	4×10^{15}	100
$^{19}F^{+}$	60	2×10^{15}	30
$^{11}B^{+}$	35	4×10^{15}	50
$^{40}Ar^{+}$	80	2×10^{15} 4×10^{15}	80

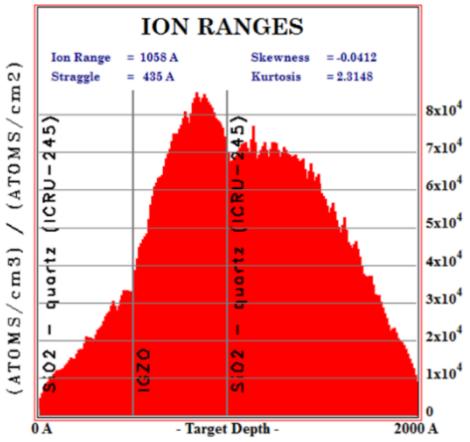


Figure 6.11: Representative SRIM analysis of $^{11}B^{+}$ implanted with energy E = 35 keV into IGZO beneath a 50 nm screen SiO_2 layer. The simulation shows that approximately 40 percent of the implanted dose resides within the IGZO film, which translates to an average boron concentration of approximately 3.2×10^{20} cm^{-3} [99].

The implant profiles were simulated using SRIM ion-matter interaction software [100], with a simulated distribution example shown in Figure 6.11. The 50 nm screen oxide represents the gate dielectric above the IGZO. The IGZO material model was specified to have a compositional ratio of In:Ga:Zn:O = 1:1:1:4 and density of 6.1 g/cm^3 [101].

6.2.2.1 Phosphorus and Fluorine Implantation

SA-TG TFTs were implanted using $^{31}P^{+}$ and $^{19}F^{+}$ ions to activate the IGZO S/D regions. In both cases following the high-dose implants the device characteristics were shifted and distorted, with current levels below the initial non-implanted condition. The fluorine implanted devices no longer demonstrated transistor operation. The phosphorus implanted devices did not show any S/D activation and ~10 V left shifted transfer characteristics from standard TG devices was observed as shown in Figure 6.12a. It was initially hypothesized that this may be due to the devices being subjected to thermal stress during ion-implantation, however further results suggest a different origin that will be discussed.

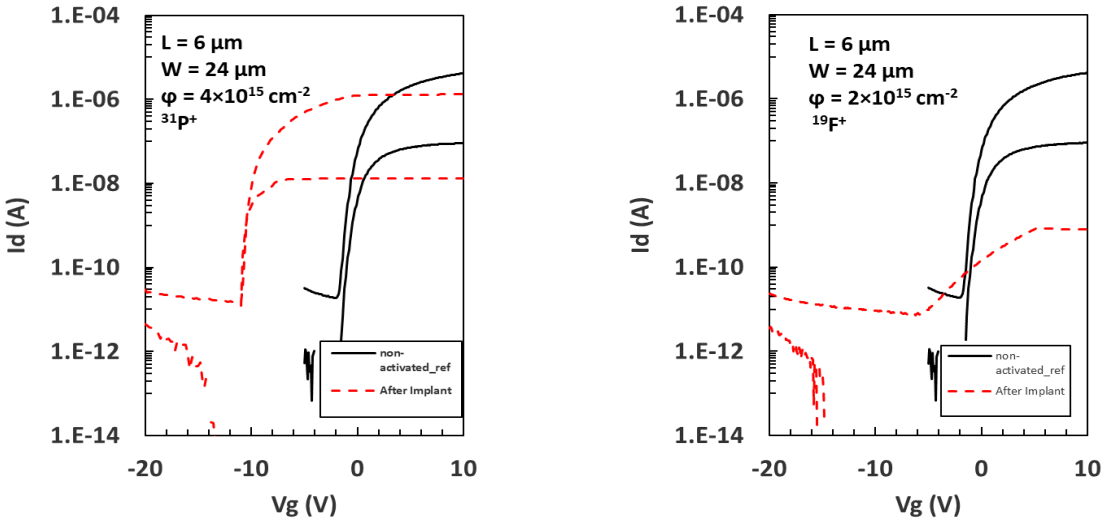
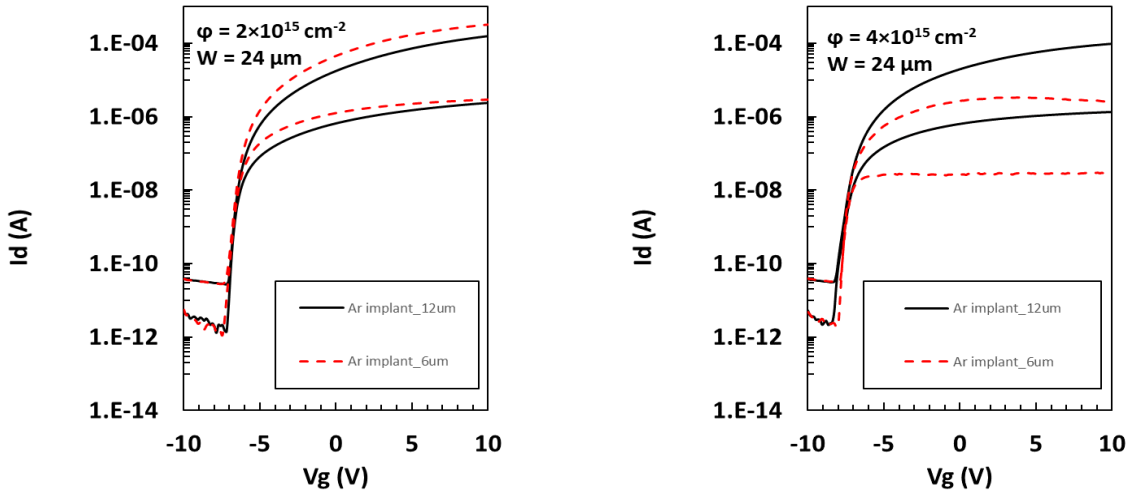


Figure 6.12: Comparison of SA-TG device characteristics for L = 6 µm with before (solid lines) and after (dashed lines) (a) $^{31}P^{+}$ implant with energy E = 80 keV and dose $\phi = 4\times10^{15}$ cm^{-2} and (b) $^{19}F^{+}$ implant with energy E = 60 keV and dose $\phi = 2\times10^{15}$ cm^{-2}. Here, the device width is 24 µm and the Vd is 0.1 V and 10 V respectively with 4 µm underlap between TG and S/D contact metal.

6.2.2.2 Argon Ion-Implantation

While argon plasma has been used to form selectively conductive IGZO regions, at the time of this investigation no work had been published with $^{40}Ar^{+}$ ion implantation into IGZO to make SA devices. In this work, $^{40}Ar^{+}$ ions have been implanted in the SA-TG devices at the very last step with two different doses. The activated S/D region became markedly conductive from the $\phi = 2\times10^{15}\,cm^{-2}$ implant, as shown in Figure 6.13a, albeit with a significant left shift. The electrical characteristic degradation at the higher dose ($\phi = 4\times10^{15}\,cm^{-2}$) shown in Figure 6.13b happens to be more pronounced at the shorter channel length devices. A degradation in source injection results in current saturation and translates to poor current modulation in the transfer characteristics.



(a) (b)

Figure 6.13: Comparison of $^{40}Ar^{+}$ implanted SA-TG device characteristics with L = 6 (red dashed line) and L = 12 µm (black solid line) with (a) $\phi = 2\times10^{15}\,cm^{-2}$ and (b) $\phi = 4\times10^{15}\,cm^{-2}$ and energy E = 80 keV. Here, the device width is 24 µm and the V_d is 0.1 and 10 V respectively with 4 µm underlap between TG and S/D contact metal.

Terada-Muta (T-M) analysis was done on $^{40}Ar^{+}$ implanted SA-TG devices with $\phi = 2\times10^{15}\,cm^{-2}$ [102], with the T-M plot shown in Figure 6.14. The common intersection of extrapolated characteristics occurs at $\Delta L \sim 1.67$ µm and a series resistance $R_{SD} \sim 0.68$ kΩ. The

amount of series resistance equates to approximately one-fourth the measured sheet resistance of 2.75 kΩ/sq, which is close to the one-third estimation based on the device structure layout. The origin of free electrons is not certain yet and there was no annealing following the implant process. Previous work in [90] suggests that the oxygen in the IGZO film surface is preferentially dissociated by the $^{40}Ar^{+}$ ion bombardment due to its relatively high sputtering yield. Hence, the carrier concentration increases most likely due to the formation of oxygen vacancies in IGZO film.

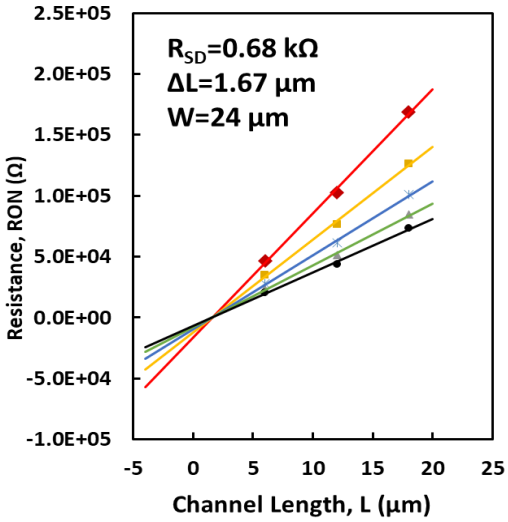


Figure 6.14: T-M analysis for $^{40}Ar^{+}$ implanted SA-TG devices using channel length of 6, 12, 18 µm devices. The resistance is calculated at Vg = 2, 4, 6, 8, 10 V with drain voltage at 0.1 V. The extracted parameters are ΔL = 1.67 µm and R_{SD} = 0.68 kΩ for 24 µm wide device.

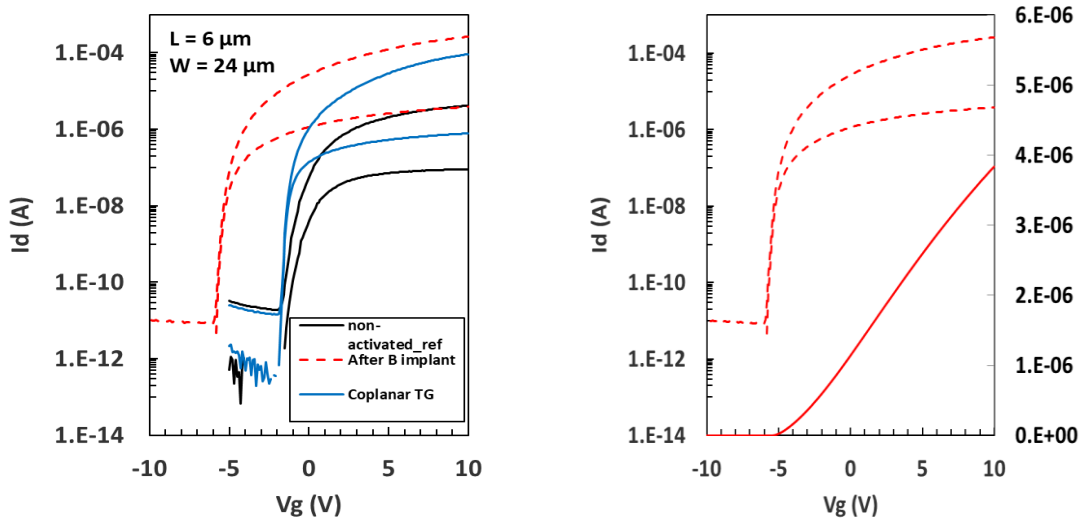
6.2.2.3 Boron Ion-Implantation

Boron-doped ZnO has been studied as a potential candidate in solar cell and solid state lighting as a transparent conductive electrode [103]–[105]. The ZnO:B film has low resistivity, high transparency and broad-band photoluminescence [103]. However, the doped regions were not formed selectively; no transistor characteristics were shown in these studies. Compared to polycrystalline ZnO, IGZO has better uniformity and stability due to its amorphous nature. This

work is the first report of SA IGZO TFTs that have had selectively doped S/D regions formed via boron ion implantation [99]. The high-dose ($\phi = 4\times10^{15}$ cm^{-2}) $^{11}B^{+}$ implant was done at 35 keV which is the lower energy limit of the ion implanter used. The boron implanted IGZO had a measured sheet resistance Rs ~ 9 kΩ/sq, which assuming an electron mobility $\mu_n = 10$ cm^2/Vs translates to an electron concentration of n ~ 1.4×10^{19} cm^{-3}. This suggests an activation level of approximately 4% of the boron atoms present if in fact the mechanism involves boron behaving as an electrically active species, although the level of electrical activation is most likely higher considering mobility degradation due to implant damage and/or the presence of dopant ions. Note that there was no annealing following the implant process, and the relationship between boron and free electrons is not yet certain. However, results strongly suggest that boron is participating as an electrically active species, as will be discussed further in later portions of this chapter.

The I_D-V_{GS} transfer characteristics of the SA-TG TFT both before and after the boron implant are shown in Figure 6.15a, along with a comparison to a standard TG coplanar non-SA device. The SA-TG TFT prior to implant has significant series resistance which severely limits current flow. The boron implant increases the on-state current by more than two orders of magnitude and supports ohmic contact behavior and steep subthreshold operation.

The SA-TG characteristic exhibits a shift of approximately -4 V in comparison to the standard TG device with metal electrode overlaps, as shown in Figure 6.15a. The magnitude of shift is somewhat less in comparison to the results of other ion species; the origin of which remained uncertain. A similar left-shift was observed on implanted TG coplanar devices with metal blocking all IGZO regions, thus it is related to the implant process and not the presence of implanted boron atoms.

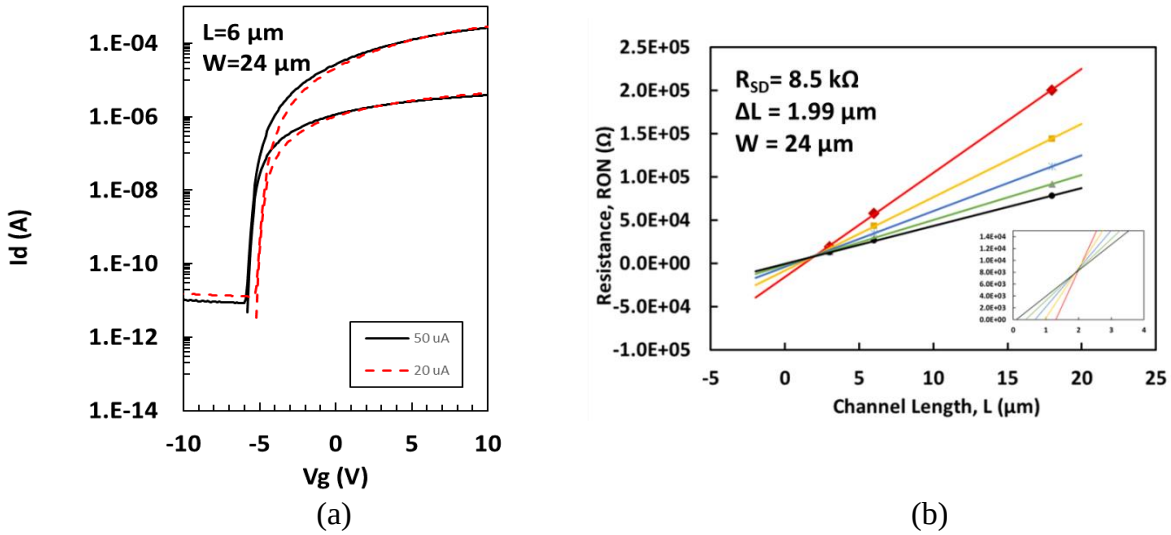


(a) (b)

Figure 6.15: (a) Comparison of TG device characteristics, SA $^{11}B^{+}$ implanted ($\phi = 4\times10^{15}$ cm^{-2}) TG device with L = 6 µm (dashed lines) and standard co-planar L= 4 µm (solid line) TG device with 4 µm underlap between TG and S/D contact metal. Here, the device width is 24 µm and the V_d is 0.1 V and 10 V respectively. After $^{11}B^{+}$ implant, the I-V curves are showing improved although left shifted characteristics. (b) SA-TG device characteristics with L= 6 µm after $^{11}B^{+}$ implant ($\phi = 4\times10^{15}$ cm^{-2}) in log scale (dashed line) and linear scale (solid line) [99].

To analyze the influence of generated heat during ion-implantation, $^{11}B^{+}$ was implanted using two different beam currents. From Figure 6.16a, it can be seen that the implant with relatively low beam current (20 µA) is left-shifted slightly less in comparison to the higher beam current (50 µA) implant; nonetheless the lower beam did not resolve the issue.

T-M analysis was done on SA-TG devices [102], with the T-M plot shown in Figure 6.16b. The common intersection of extrapolated characteristics occurs at ΔL ~2 µm and a series resistance R_{SD} ~ 8.5 kΩ. The lateral straggle from the boron implant has a negligible influence on the effective channel length, however the ΔL value incorporates process biases that are unique to the gate-defined channel length of the SA-TG device. The amount of series resistance equates to approximately "one square" of sheet resistance, which is higher than the device layout would suggest. Regardless, the contact behavior is ohmic and has a minor influence on device behavior as shown in Figure 6.15b.



(a) (b)

Figure 6.16: (a) Comparison of SA-TG device characteristics for L = 6 µm $^{11}B^{+}$ implanted ($\phi = 4\times10^{15}$ cm^{-2}) device with 20 µA (solid line) and 50 µA (dashed line) beam current. (b) T-M analysis for $^{11}B^{+}$ doped ($\phi = 4\times10^{15}$ cm^{-2}) SA-TG devices using channel length of 3, 6, 18 µm devices. For T-M analysis, the resistance is calculated at Vg = 2, 4, 6, 8, 10 V with drain voltage at 0.1 V. The device width is 24 µm and the V_d is 0.1 V and 10 V respectively with 4 µm underlap between TG and S/D contact metal. The extracted parameters are ΔL = 1.99 µm and R_{SD} = 8.5 kΩ.

In addition to the SA-TG devices demonstrating left shifted characteristics, they also suffered from thermal instability during subsequent hotplate treatments, causing further shifting and distortion. This is presumably due to residual water reacting with the top metal gate during any

successive high temperature steps [13]. These topics were further investigated on the BG self-aligned structure that does not include a top-gate metal feature that is likely operative in these noted issues.

6.3 SA-BG STAGGERED TFT

Traditional BG staggered TFT configuration has also been explored which utilizes back-side through-glass exposure. Boron and argon ion species have been explored as well to make IGZO selectively conductive as shown in Table 6-II. Both $^{11}B^{+}$ and $^{40}Ar^{+}$ ion implantation demonstrated good TFT transfer characteristics. Here, the dose values were chosen based on previous SA-TG device results including a higher dose (2x) value for $^{11}B^{+}$.

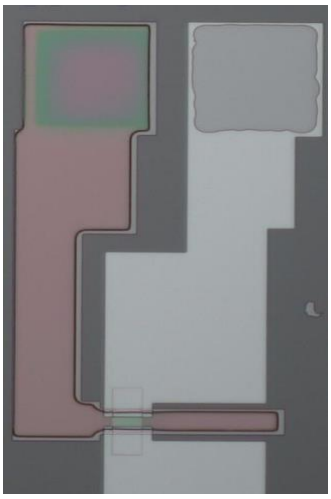
Table 6-II: Design of experiments for ion-implantation treatment to realize SA-BG TFTs.

Species	Energy (keV)	Dose (cm^{-2})	Beam Current (µA)
$^{11}B^{+}$	35	4×10^{15}	50
		8×10^{15}	85
$^{40}Ar^{+}$	80	2×10^{15}	100

6.3.1 Pseudo-SA BG Lithographic Process

The SA-BG process was initially investigated using a "pseudo" self-aligned process. It is not truly self-aligned; rather it mimics a self-aligned device concept where the channel was protected from ion implant by using a BG photoresist pattern with special attention to overlay. The process flow had several steps common to the standard staggered BG process, with top-side exposure using BG

mask to protect the channel region from S/D activation techniques on silicon wafers. This is done to ensure that the SA-BG strategy will work with the implanted species. A 50 nm Mo gate electrode was sputtered and patterned on a thick isolation oxide (~650 nm SiO_2) thermally grown on silicon wafers, followed by a 50 nm SiO_2 gate dielectric deposited by PECVD (TEOS precursor, 390 °C). The SiO_2 was densified for 2 hours in N_2 at 600 °C in a furnace. A 50 nm IGZO layer was sputter deposited using an $InGaZnO_4$ (1:1:1:4) target in an argon ambient with 7% oxygen, followed by mesa pattern and etch using dilute HCl. The S/D contact metal (100 nm Mo-Al bilayer) was then sputtered and defined by lift-off technique using Futurrex NR9g-1500PY negative photoresist. A second 50 nm PECVD SiO_2 layer was then deposited as the passivation material. A 3-hour O_2 passivation anneal at 400 °C with a 2-hour controlled ramp-down in O_2 ambient was performed, and immediately followed by an HMDS vapor treatment at 140 °C to avoid water adsorption. The devices were then immediately capped with 10 nm Al_2O_3 film using ALD at 200 °C after annealing to minimize exposure to air ambient. The wafer was coated with AZ MIR 701 positive resist following an HMDS vapor prime at 140 °C and over-exposed for 5 sec using BG mask which left resist on top of BG polygon with careful attention to overlay, thereby protecting the IGZO channel region. The alignment of the BG polygon is critical for the appropriate activation of the underlapped S/D region. Note that the overexposure ensures the resist polygon is slightly inside the original gate definition. After exposure, the resist was developed for 45 sec in Microposit MF CD-26 developer solution and hotplate baked for 60 s at 140 °C. The wafer was then ion implanted for S/D activation and resist was removed after the ion implantation. Finally, the gate and S/D contact windows were patterned and etched using 10:1 buffered HF solution. Figure 6.17 shows the cross-section schematic and top-down view of the pseudo SA-BG device.



(a) (b)

Figure 6.17: (a) Cross-sectional schematic and (b) top-down view of pseudo-SA BG device, where the textured and non-textured IGZO represents implanted and non-implanted regions, respectively. Note that in this process scheme, the implant is blocked in the channel region only and the alignment of the BG pattern is critical.

The device characteristics shown in Figure 6.18 represents a $^{11}B^{+}$ implanted pseudo-SA BG device with E = 35 keV and $\phi = 4\times10^{15}$ cm^{-2}. The characteristics do not experience the pronounced left-shift demonstrated by SA-TG devices. This implies that the origin of the left-shift was due to metal electrode charging during the implant, subjecting the gate dielectric to electrical stress and inducing positive bulk oxide charge. The pseudo-SA BG characteristics are left shifted compared to the standard non-SA BG device characteristics shown in Figure 5.5a, however the shift is relatively minor ($\Delta V \sim 1$ V).

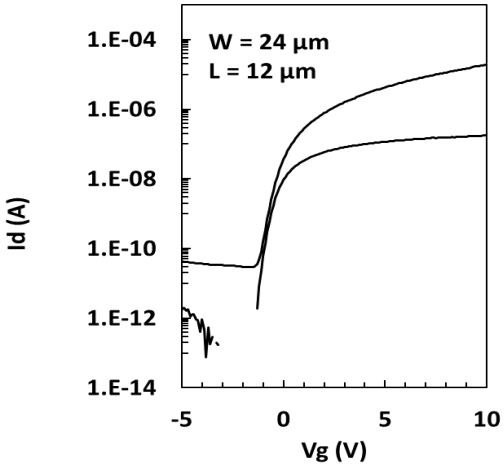


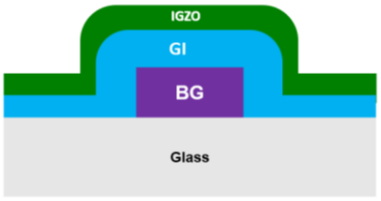
Figure 6.18: $^{11}B^{+}$ implanted ($\phi = 4\times10^{15}\,cm^{-2}$) pseudo-SA BG device characteristics with L = 12 µm. The device width is 24 µm and the V_d is 0.1 and 10 V respectively with 4 µm underlap between BG and S/D contact metal.

6.3.2 SA-BG Lithographic Process Using Backside Flood Exposure

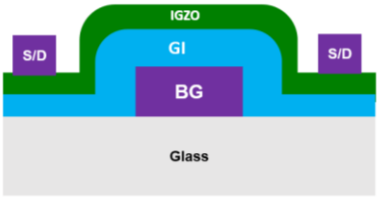
The SA-BG process investigated had several steps common to the SA-TG process flow, using back-side flood exposure through the glass substrate to pattern the photoresist implant mask. Figure 6.19 shows cross-sectional schematics of the SA-BG lithographic process. Using a glass substrate, a 50 nm thick Mo gate electrode was sputtered and patterned, followed by a PECVD SiO_2 gate dielectric which was densified for 2 hours at 600 °C in N_2. A 50 nm IGZO layer was sputtered using an $InGaZnO_4$ (1:1:1:4) target in an argon ambient with 7% oxygen, and then patterned and etched using dilute HCl.

(a) BG definition

(b) BG dielectric (TEOS)

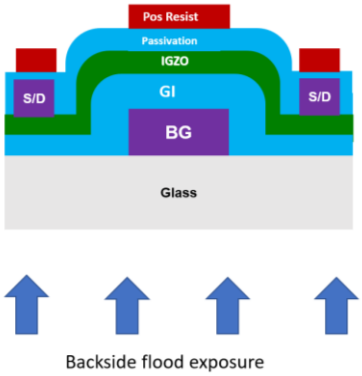


(c) IGZO MESA definition

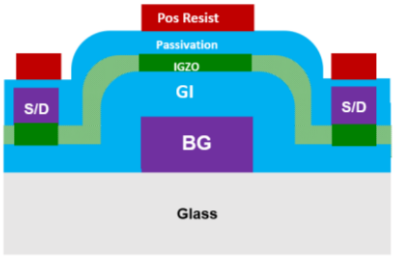


(d) S/D contact metal (Sputter Mo/Al)

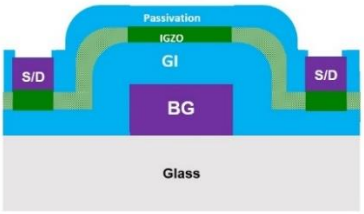
(e) Passivation oxide/ Passivation anneal



(f) Positive resist & back side flood exposure



(g) S/D treatment on IGZO

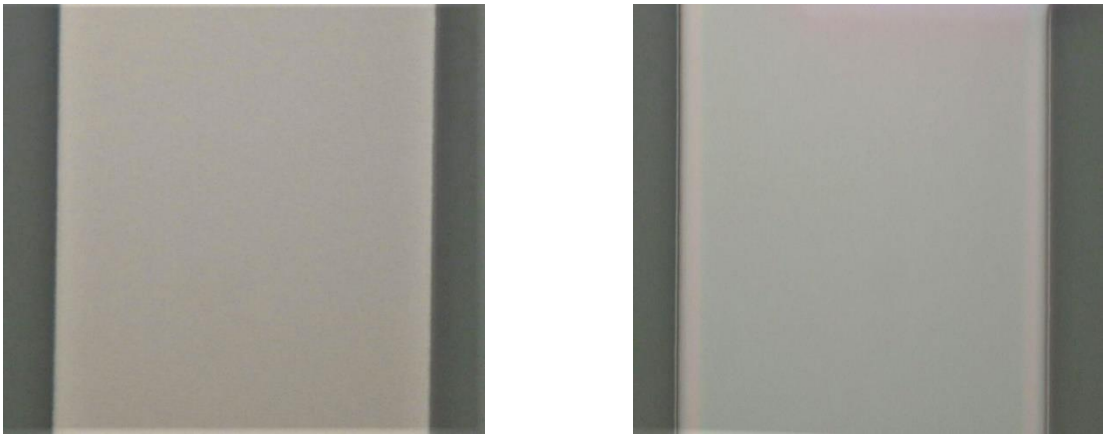


(h) Resist removal/Passivation Open

Figure 6.19: Step by step cross-sectional schematic of SA-BG device, where the textured and non-textured IGZO represents implanted and non-implanted regions, respectively. Note that in this process scheme the implant is blocked in both channel and S/D metal contact regions.

The S/D contact metal (100 nm Mo/Al bilayer) was then sputtered and patterned using a lift-off process. For implant-last device strategy, a 50 nm PECVD SiO_2 passivation oxide was then deposited, followed by the O_2 anneal and Al_2O_3 capping layers described previously. The wafer

was then coated with AZ MIR 701 positive resist following an HMDS vapor prime at 140 °C. Back-side illumination with broadband spectrum was done using Suss MA150 Contact Aligner and a black absorbing layer was used to avoid reflections. After exposure, the resist was developed for 45 sec in Microposit MF CD-26 developer solution and hotplate baked for 60 s at 140 °C. The samples were then ion implanted for S/D activation. Finally, the implant blcoking resist was removed. For anneal-last devices the passivation anneal is done at this stage prior to the subsequent ALD capping layer. The S/D contact regions were opened using 10:1 buffered HF. Figure 6.20 shows the resist profile with and without backside flood exposure. Resist was remaining everywhere without the backside flood exposure whereas resist was only remaining on top of BG polygon with the backside flood exposure.



(a) (b)

Figure 6.20: BG pattern (a) without backside flood exposure and (b) with backside flood exposure. Note that, resist is remaining everywhere without the backside flood exposure whereas resist is only remaining on top of BG polygon with the backside flood exposure.

6.3.2.1 Boron Ion-Implantation

In this experiment, $^{11}B^{+}$ was implanted with 35 keV energy at two different doses (4×10^{15} cm^{-2} and 8×10^{15} cm^{-2}). The initial results were similar to the characteristics of pseudo-SA-BG devices.

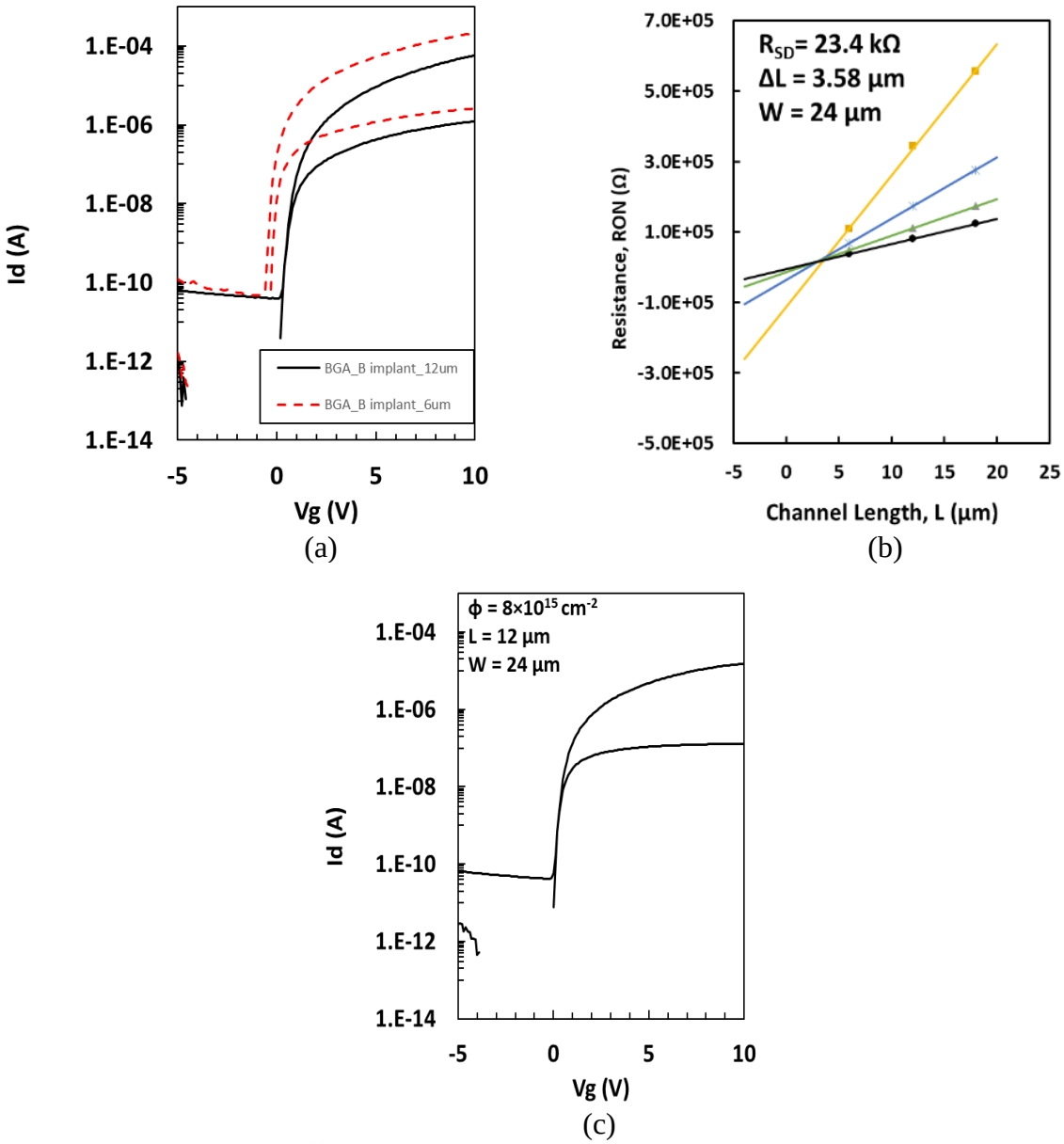
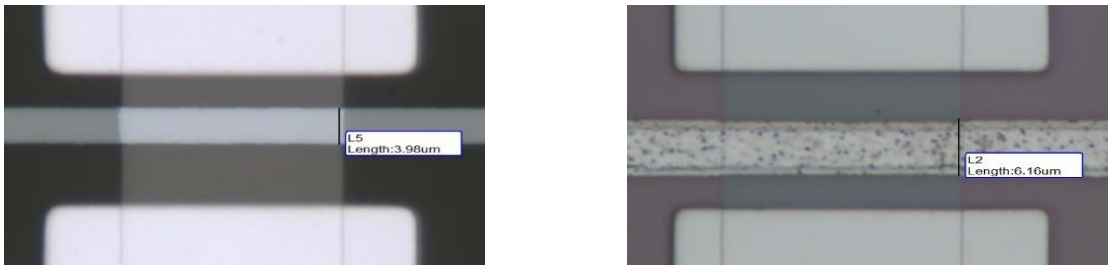


Figure 6.21: (a) Comparison of $^{11}B^{+}$ implanted SA-BG device characteristics with L = 6 µm (dashed line) and L = 12 µm (solid line) with $\phi = 4\times10^{15}$ cm^{-2} into 4 µm underlap regions between resist mask and source-drain metal. The device width is 24 µm and V_{DS} is 0.1 and 10 V and (b) T-M analysis for $^{11}B^{+}$ implanted SA-BG devices using channel lengths of 6, 12, 18 µm devices. The resistance is calculated at V_g = 4, 6, 8, 10 V with drain voltage at 0.1 V. The extracted parameters are ΔL = 3.58 µm and R_{SD} = 23.4 kΩ. (c) L = 12 µm device with a 2x dose increase ($2\phi = 8\times10^{15}$ cm^{-2}) demonstrating a degradation in charge injection that is pronounced at the lower drain [106].

From the transfer characteristics for SA-BG $^{11}B^{+}$ implanted (4×10^{15} cm^{-2} dose) device shown in Figure 6.21a, it was observed that there is a left shift in the characteristics for 6 µm device compared to the 12 µm device. From the T-M analysis, R_{SD} is ~ 23 kΩ and ΔL is 3.6 µm as shown

in Figure 6.21b. Thus, the effective channel length for a 6 µm device is only ~2.5 µm, however the origin of the left shift in the transfer characteristics is still in question and will be discussed further. When the dose was doubled to 8×10^{15} cm^{-2}, the transfer characteristics degraded as shown in Figure 6.21c. This suggests that 4×10^{15} cm^{-2} dose was already at or above the limit of B solid solubility in IGZO and additional B doping (8×10^{15} cm^{-2}) created interstitial point defects in the underlapped region. The devices exhibited degradation in charge injection from source to the channel that is pronounced at low drain bias (0.1 V) as shown in Figure 6.21c. It should be reinforced that the channel was not implanted; this was only an effect of the additional implant in the S/D region.

The large ΔL is mainly due to the subtractive wet-etch for the bottom gate patterning. As seen from microscope images of the SA-BG devices in Figure 6.22a, the gate pattern has ~2 µm offset from the mask defined gate length. The SA-TG devices as shown in Figure 6.22b do not have any offset since the TG is patterned by lift-off using NR9g-1500PY negative resist with almost no offset as shown previously in Figure 5.1.



(a) (b)

Figure 6.22: (a) SA-BG IGZO TFT with channel length L = 6 µm with effective channel length of L = 4 µm as defined by the subtractive wet etching using positive photoresist with 2 µm offset from the mask definition (i.e. ΔL ~ 2 µm) and (b) SA-TG IGZO TFT with channel length L = 6 µm as defined by the S/D lift-off metallurgy using negative photoresist (Futurrex NR9g-1500PY) with almost negligible offset from the mask definition (i.e. ΔL ~ 0).

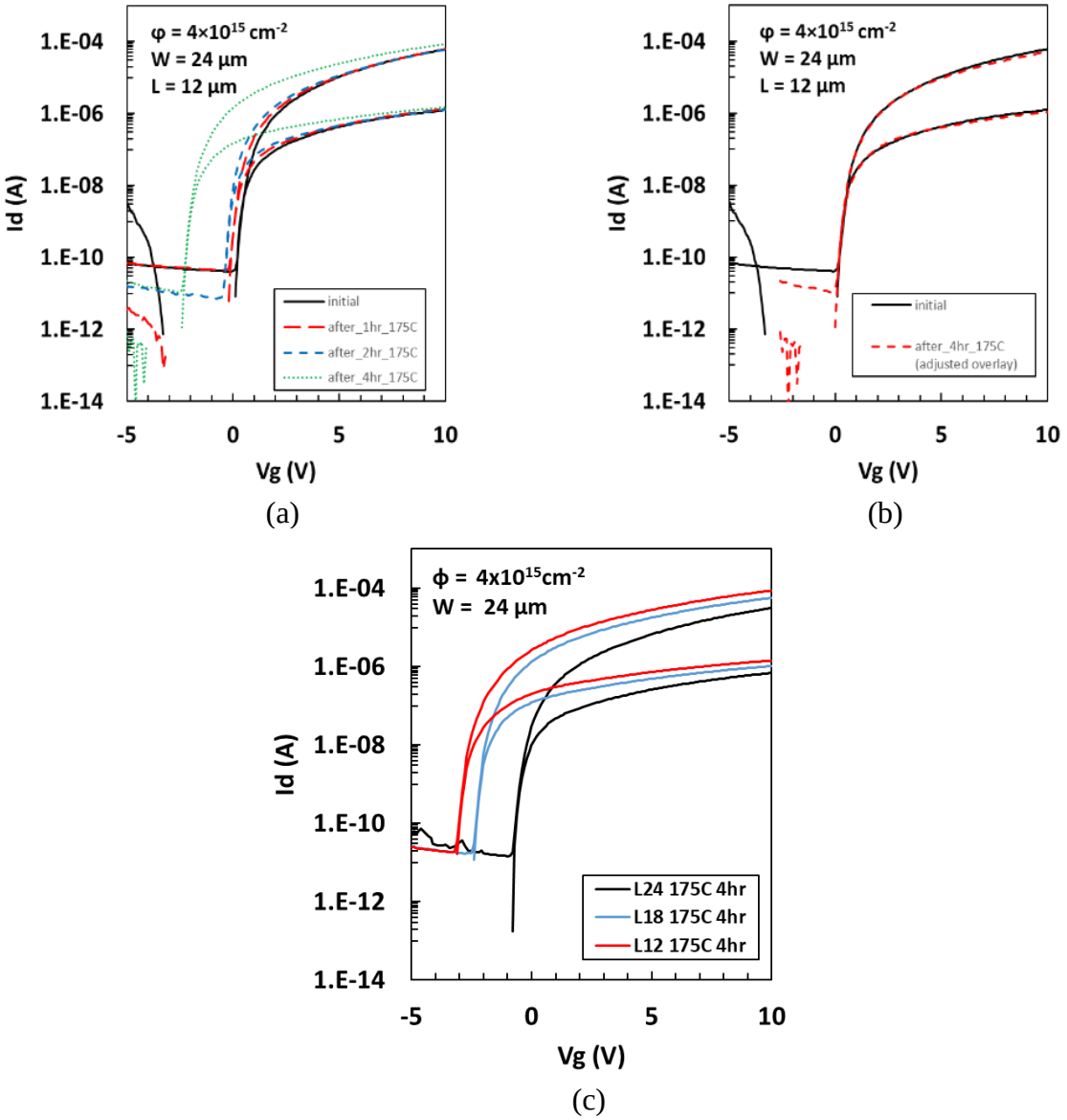


Figure 6.23: (a) Comparison of $^{11}B^{+}$ implanted SA-BG device characteristics with (a) L = 12 µm and $\phi = 4\times10^{15}$ cm^{-2} before (solid line) and after (dashed lines) successive 175 °C bakes, (b) adjusted overlay of the original and 4 hour hot-plate bake characteristics and (c) L = 12 µm with $\phi = 8\times10^{15}$ cm^{-2}. The device width is 24 µm and the V_d is 0.1 and 10 V respectively with 4 µm underlap between BG and S/D contact metal. (c) channel-length dependence of shift induced by the 4-hour hotplate bake treatment [106].

After subjecting the devices to 175 °C hot-plate bake for an hour, there was a slight shift in the transfer characteristics of the 12 µm long device as shown in Figure 6.23a, which became significant as the cumulative time was increased to 2 hours and finally 4 hours. The standard non-

SA devices fabricated on the same substrate did not exhibit any left shift upon thermal stability testing. This “active” species appears to be stable at 175 °C, however the balance of boron interstitials appears to be exceedingly mobile and diffuses throughout the channel region. As interstitial boron enters the channel region, a fraction becomes electrically active and shifts the transfer characteristics to the left as shown in Figure 6.23a. Note that the effective channel length is not changed as shown by the overlay plot in Figure 6.23b, confirming the stability of the active donor species which is at a much higher concentration in the implanted S/D regions in comparison to the amount which eventually becomes active in the channel. This proposed mechanism is diffusion limited, and thus the degree of shift is channel length dependent as shown in Figure 6.23c. This may also be the origin of the left-shifted characteristics of the L = 6 µm device shown in Figure 3a, which has a much shorter effective channel length and could experience thermal diffusion during the implant due to heat generated.

6.3.2.2 Threshold Voltage Adjustment

Here, the entire IGZO mesa (IGZO channel and conductive IGZO S/D with 4×10^{15} cm^{-2} dose) was subjected to a low dose (2×10^{12} cm^{-2}) ion implant at E = 35 keV in order to intentionally adjust the V_T. All devices regardless of channel length exhibited $\Delta V_T > 5V$ left shifted characteristics as shown in Figure 6.24. This degree of shift is more than that supported by the presence of any electrically active boron species in the channel region, inferring the additional participation of defects formed during the implant process.

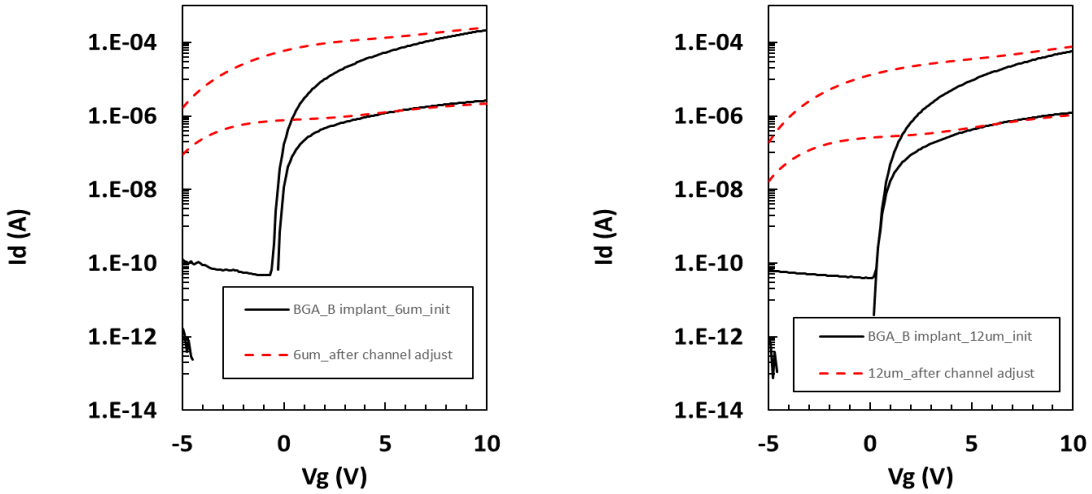


Figure 6.24: Comparison of low dose (ϕ = 2×10^{12} cm^{-2}) $^{11}B^+$ implant on ϕ = 4×10^{15} cm^{-2} $^{11}B^+$ implanted SA-BG device characteristics for V_T adjust with (a) L = 6 µm and (b) L = 12 µm. The device width is 24 µm and the V_d is 0.1 and 10 V respectively with 4 µm underlap between BG and S/D contact metal.

6.3.2.3 Argon Ion-Implantation

Argon ($^{40}Ar^+$) was implanted to realize SA-BG devices with 80 keV energy and 2×10^{15} cm^{-2} dose, with transfer characteristics shown in Figure 6.25. As in the case of boron-implanted SA-BG devices, the transfer characteristics do not show the left shift associated with SA-TG devices. The initial characteristics after implant exhibited a slight crossover effect, which is attributed to localized defects in the transition between the active S/D regions and the channel. This cross-over was not apparent on SA-TG devices due to the large amount of gate oxide induced charge which dominated the electrical behavior. It was also not present on boron implanted SA-BG devices.

After the 175 °C hot-plate bake for an hour, the characteristics degraded as shown Figure 6.25. The current degradation suggests "deactivation" due to instability of the argon-induced activation mechanism. The Gate Induced Drain Leakage (GIDL) behavior is pronounced after thermal stress, suggesting the creation of secondary defects. There is no characteristic left-shift associated with

the argon implanted SA-BG devices, which is consistent with a defect-induced activation mechanism rather than an electrically active argon species. These remaining defect effects would have to be eliminated for argon implant to be used in a self-aligned device strategy.

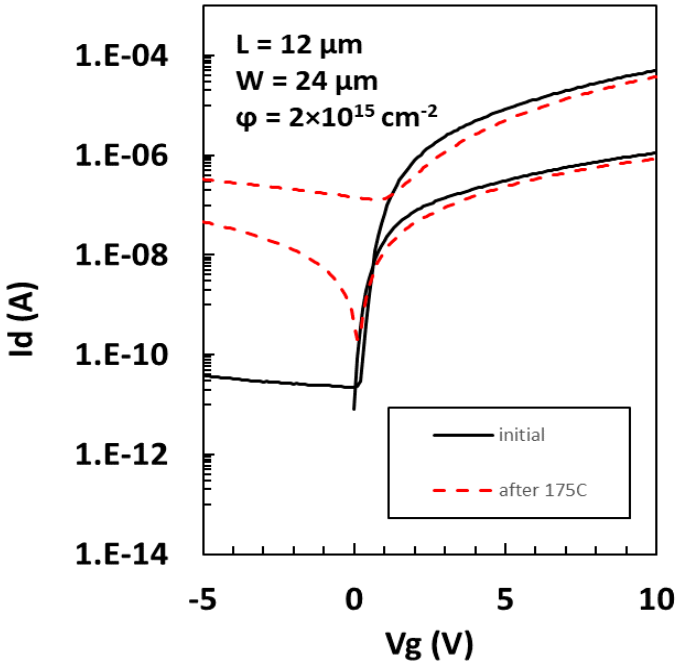


Figure 6.25: Comparison of $^{40}Ar^{+}$ implanted SA-BG device characteristics with L = 12 µm, E = 80 keV and $\phi = 2\times10^{15}$ cm^{-2} before (solid line) and after (dashed line) 175 °C bake for an hour [106].

6.3.3 SA-BG with Anneal-Last Strategy

Boron devices fabricated with an anneal-last strategy had exceedingly low current drive, with an overlay comparison of transfer characteristics from boron and argon anneal-last SA-BG TFTs along with a reference non-SA BG TFT shown in Figure 6.26. The results of the boron implanted SA-BG TFTs using anneal-last approach shows an extensive loss of electrical activity, indicating a nearly complete elimination of the donor species as shown in Figure 6.26. The passivation anneal is performed for 3 hours at 400 °C, which may allow boron to join the amorphous oxide matrix with a different bonding arrangement which does not support donor-like behavior.

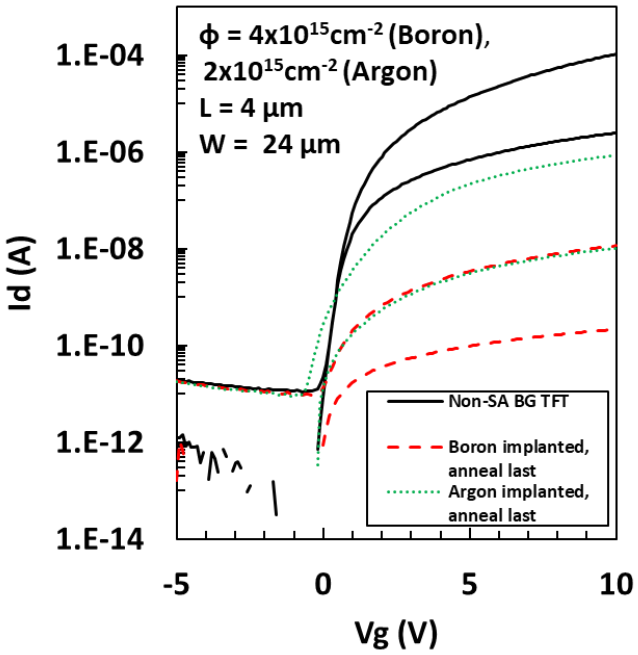
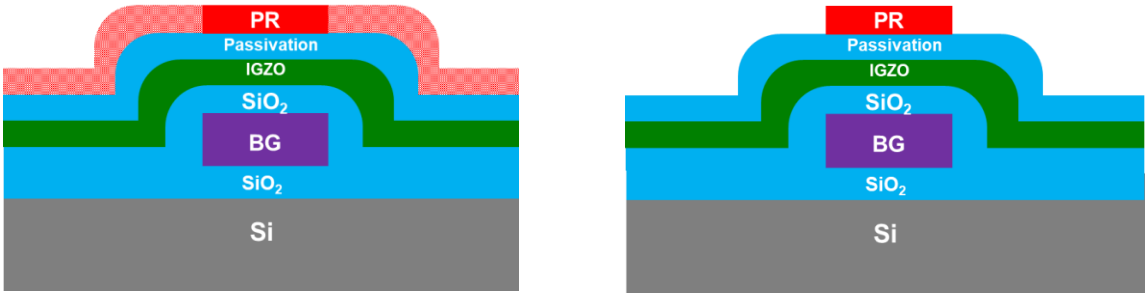


Figure 6.26: Characteristic overlay of an anneal-last SA-BG device with boron and argon doping and a non-SA-BG TFT with the same channel dimensions as indicated [106].

6.3.3.1 SA-BG Lithographic Process Using Topside Flood Exposure

A preliminary indication of the feasibility of the "reflection gate" process was observed during the IGZO mesa lithographic process, which under standard exposure conditions resulted in underexposure over the BG electrode outside of the mesa region while the field area was completely cleared of photoresist. This was then recognized as a potential method for integration into a SA-BG process using a topside flood exposure under optimal exposure conditions. Because of the involvement of interface reflections and thin-film interference the process was found to be extremely sensitive to differences in film thickness and optical properties. For this process to work correctly, the photoresist must mirror the BG polygons with complete coverage.

The SA-BG with topside flood exposure investigated had several steps common to the SA-BG with backside flood exposure process flow, with a top-side flood exposure and optical thin-film interference used to produce a "reflection gate" electrode to serve as an implant mask. The potential advantages of this strategy in comparison to the one discussed before in 6.3.2 were to avoid a complex through-substrate exposure, use of opaque substrates, better substrate handling. Using the same oxidized silicon substrate described previously, a 50 nm thick Mo gate electrode was sputtered and patterned, followed by a PECVD SiO_2 gate dielectric which was densified for 2 hours at 600 °C in N_2. A 50 nm IGZO layer was sputtered using an $InGaZnO_4$ (1:1:1:4) target in an argon ambient with 7% oxygen, and then patterned and etched using dilute HCl. A 50 nm PECVD SiO_2 passivation oxide was then deposited, followed by the O_2 anneal and Al_2O_3 capping layers described previously.

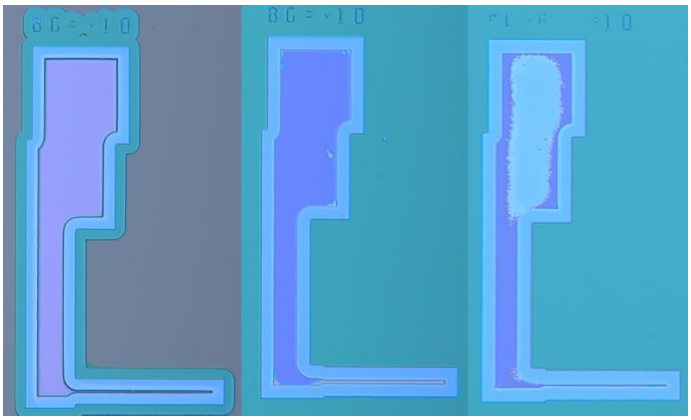


(a) (b)

Figure 6.27: Cross-sectional schematic of a SA-BG lithographic process (a) after exposure and (b) after develop [99].

The wafer was then coated with AZ MIR 701 positive resist following an HMDS vapor prime at 140 °C. Top-side illumination at g-line (λ = 436 nm) with an irradiance of ~ 100 mW/cm^2 was done using an exposure array to determine the resulting contrast between photoresist lying above the field and gate regions. After exposure, the resist was developed for 45 sec in Microposit MF CD-26 developer solution and hotplate baked for 60 sec at 140 °C. Figure 6.27 shows cross-sectional schematics of the SA-BG lithographic process.

An exposure array with short time increments (Δt = 0.03 s) was used for open field exposures on resist-coated BG structures in search of settings that would yield acceptable image contrast with minimal edge exclusion. Select results are shown in Figure 6.28, along with the exposure times used on the projection stepper system.



(1) t = 2.29 s (2) t = 2.41 s (3) t = 2.65 s

Figure 6.28. Photoresist-coated BG structures that were flood exposed for times indicated; all samples exhibit significant edge exclusion. The short exposure time of sample#1 did not clear the field region, whereas the long exposure time of sample #3 resulted in partial clearing of photoresist over the planar BG region [99].

The results shown in Figure 6.28 suggest that an exposure time of ~ 2.4 sec may clear the field of photoresist while maintaining the self-aligned BG image, shown by sample # 2. However, all samples exhibited an edge exclusion, which would result in a significant change in channel length dimension and large gate-S/D overlaps. In addition, the photoresist thickness loss in areas where it did remain may not provide an adequate implant masking layer. The BG image integrity over the mesa is the only region of importance for S/D implant blocking. Unfortunately, a suitable process window was not identified within the experimental conditions used. More experiments which investigate other parameters such as the develop process conditions (e.g. time, concentration) are required.

6.4 SUMMARY

Investigation on new techniques towards the realization of SA IGZO TFTs has been presented in this chapter. This work realized the first report of the use of IGZO:B for the source drain regions

formed selectively via ion implantation The interpretation of donor activation in SA-BG IGZO TFTs with ion-implantation of boron ($^{11}B^{+}$) and argon ($^{40}Ar^{+}$) species as the source/drain treatment has been presented. The analysis focused on experimental observations of electrical characteristics, with a detailed discussion that developed supporting arguments. The claim of a defect-induced mechanism associated with argon implantation is not surprising, as it is a chemically inert species. However, the interpretation on the behavior of boron in IGZO is unique and certainly not obvious. Results suggest there are at least three distinct states in which boron can exist; two which involve chemical bonding and one as an electrically inactive interstitial atom. Of the two states that involve chemical bonding, only one is proposed to behave as an electrically active donor species. The interstitial diffusivity of boron in IGZO is proposed to be very high, where it appears to move several microns within an hour at 175 °C. In contrast, the electrically active donor state is thermally stable and does not appear to diffuse at such a low temperature. There also appears to be a condition of equilibrium in the ratio of electrically active to inactive species, estimated to be less than 10 percent.

Chapter 7. NEXT-GEN AOS TFTS

Since the first ever report of IGZO as a channel material by Nomura et al. [15], it has been widely studied for TFT application. Higher mobility, low-temperature compatibility, higher transparency and large-area scalability are some key attributes that make amorphous oxide semiconductor (AOS) a preferred candidate over conventional a-Si:H. However, Ga_2O_3 and ZnO components of IGZO are sensitive to wet etch process [107]. Thus, it is necessary to explore any alternative material (i.e. IWO) without the acid-soluble components. The WO_3 component in IWO is insoluble in acid except for hydrogen fluoride solutions.

AOS are an attractive option to integrate on flexible substrates such as polyethylene napthalate (PEN) or polyethylene terephthalate (PET) instead of rigid glass. However, the AOS require high temperature annealing in order to activate their electrical properties and reduce defect density that may act as charge traps. Incompatibility of the most researched AOS i.e. IGZO with flexible substrates is a major bottleneck in achieving high performing TFTs on polymers. The indium tin oxide (ITO) system is an attractive alternative since the In & Sn cations with $[Kr]4d^{10}5s^{0}$ electronic configuration offers large spatial overlap between the 5s orbital and render high conductive paths to electron carriers, hence higher electron mobility [108]. It is also necessary to reduce the free carrier density in the channel material to achieve an enhancement-mode device. It is known that Ga cations acts as a carrier suppressor in IGZO as it forms strong bonds with oxygen anions and reduce the possibility of having oxygen vacancies which acts as carriers in AOS [109]. Therefore, Ga doped ITO i.e. ITGO is an ideal AOS candidate for flexible substrates.

7.1 IWO TFTs

InOx-based metal oxide semiconductors have been widely investigated as a channel material in TFT since they show high electron mobility owing to their edge-sharing polyhedral structure [20]. It is known that higher mobility improves electrical conductivity without the cost of optical transparency in the visible light range, but also provides high operation speed in transparent electronic devices [110].

IWO achieved by doping In_2O_3 with very small amount of WO_3 (<5%) has been widely studied as a channel material [111], [112]. It is believed that the presence of a very small amount of WO_3 prevents crystallization of In_2O_3 film and provides a very smooth surface [107]. This will lead to reduction in carrier mobility degradation since surface roughness greatly reduces charge transport. For a-IWO, the thickness of the film can be scaled down without increasing surface roughness. Since the channel thickness affects the absolute number of free carriers, switching behavior can be enhanced by using thinner channel [113]. This cannot be achieved in polycrystalline-based (i.e. ZnO) TFTs due to the damage in back-channel.

Free electrons arise from the oxygen vacancies or the activated W^{6+} ions on substituting sites of In^{3+} ions in n-type IWO semiconductor film [114]. In ITO, complexes of Sn^{4+} substituting for In^{3+} are associated with interstitial O^{2-} (equation 7.1). According to the complex theory, in IWO, W^{6+} would create one carrier when it associates with one interstitial O^{2-} (equation 7.2). Here, O_i'' is interstitial oxygen with negative charge given by the ($'$) and $A_{\dot{B}}$ represents ion A substituting ion B with positive charge given by the ($\cdot$). This will create fewer electrical neutral complexes, fewer impurities and weaker neutral complex scattering, such that the mobility increases with increasing O_2/Ar ratio [115]. But with increasing oxygen, oxygen vacancies can be filled and the substituted

W^{6+} ions can be deactivated by forming W-O complexes [116]. Therefore, the optimization of the O_2/Ar ratio is the key to obtaining a suitable film for TFT channel.

$$2In_{In} + 2SnO_2 \rightarrow (2Sn_{\dot{In}})O_i'' + In_2O_3 \quad 7.1$$

$$In_{In} + WO_3 \rightarrow W_{\ddot{In}}O_i'' + \frac{1}{2}In_2O_3 + \frac{1}{2}O_2 + \acute{e} \quad 7.2$$

The optical transmittance also enhances with increasing O_2/Ar ratio within the visible and NIR region. Lu et al. showed that the average transmittance of the IWO film increases from 81.88% to 84.89% in the visible region and from 90.87% to 93.33% in the NIR region with increasing O_2/Ar ratio from 11% to 17% [111] as shown in Figure 7.1.

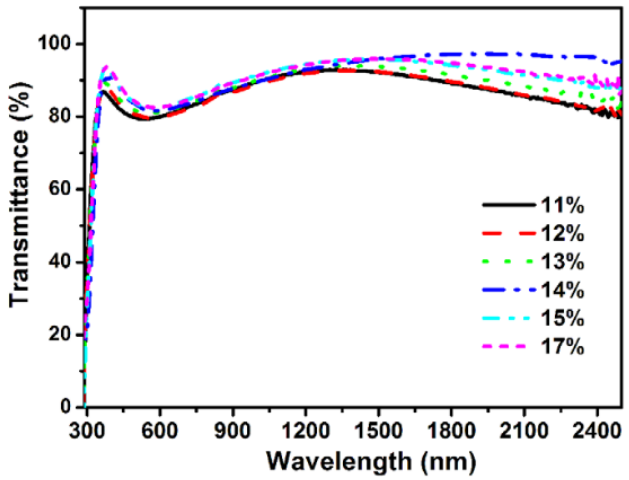


Figure 7.1: Optical transmittance spectra of IWO films with different O_2/Ar ratios [111]

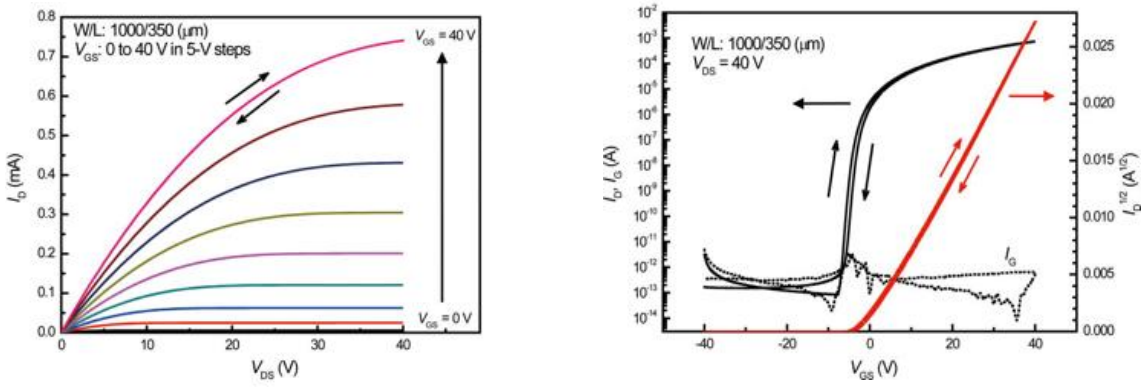
To reduce V_O, Ga and/or Zn can be replaced with other high bonding-dissociation energy which improves the retention of oxygen atoms. In IWO, WO_3 has high oxygen bond-dissociation energy of W (720 kJ/mol) than In (346 kJ/mol) [117]. Zhang et al. proposed an empirical relation which shows the effect of ionic radii (r) and effective charge (Z) of the dopant and defined a function to measure the Lewis acid strength (L) given in equation 7.3, where χ_z is metal ion

electronegativity [118]. A stronger Lewis acid will accept electrons more easily than a weaker one. Also, a high L dopant can polarize the charge carriers away from the oxygen 2p valence band which results in charge screening and reduces scattering thus increasing mobility. Since W^{6+} has a large L value (~3.16), incorporating it into In_2O_3 will be effective in reducing the excess carriers in the film and increase the μ_{FE}.

$$L = {}^{Z}/_{r^2} - 7.7\chi_z + 8.0 \qquad 7.3$$

Subthreshold swing (SS) performance improves with tungsten content which is mainly attributed to the decrease in electron concentration and sub-gap states in the vicinity of the Fermi-level [119]. Due to high bond-dissociation energy of W-O (720 kJ/mol) it is expected to suppress the formation of excess oxygen vacancies. So, the trap states originated from the oxygen vacancies decreases with the incorporation of WO_3.

The first ever a-IWO TFTs were reported by Aikawa et al. where they have demonstrated high performing TFT using IWO channel deposited by DC magnetron sputtering. The TFTs exhibited encouraging electrical characteristics as shown in Figure 7.2 [107]. From Figure 7.2b it can be seen that there is noticeable hysteresis in the transfer curves which indicates the presence of interface traps. In addition, the V_T is negative due to relatively high number of carriers.



(a) (b)

Figure 7.2: IWO TFT (a) family of curves and (b) transfer curves, with μ_{FE} = 19.3cm^2/V·s, I_{ON}/I_{OFF} = 8.9x10^9, and SS = 0.47V/decade [107]

Liu et al. showed that the bias stress stability can be enhanced by decreasing the oxygen partial pressure during IWO sputtering [112]. Due to improved mobility and SS values as seen in Table 7-I, it can be implied that the oxygen partial pressure is a critical factor in controlling the charge trapping defects in the IWO channel and/or channel/dielectric interface. It should be noted that the improvement in SS, mobility and hysteresis comes with a tradeoff in V_T where the devices become depletion-type. The volume trap density and area trap density both considerably decreased with decreasing P_{O2} which can be attributed to the improvement in positive bias stress (PBS) stability.

Table 7-I: Device parameter comparison for a-IWO TFTs [112]

P_{O2} (%)	**V_T (V)**	**SS (V/decade)**	**Mobility (cm^2/Vs)**	**Hysteresis (V)**
7	-3.4	0.39	36.7	0.06
10	4.2	0.42	26.2	0.11
13	8.4	0.55	22.4	0.29

Liu et al. also investigated a bi-layer structure and passivation layer [120]. In this experiment two different channel layers were employed where one was a 30nm thick IWO with P_{O2}=7% (Sample A) and another stacked channel with 10nm thick IWO with P_{O2}=7% and 20nm thick IWO with P_{O2}=13% (Sample B). The TFTs were also passivated using 100nm thick PECVD SiO_2.

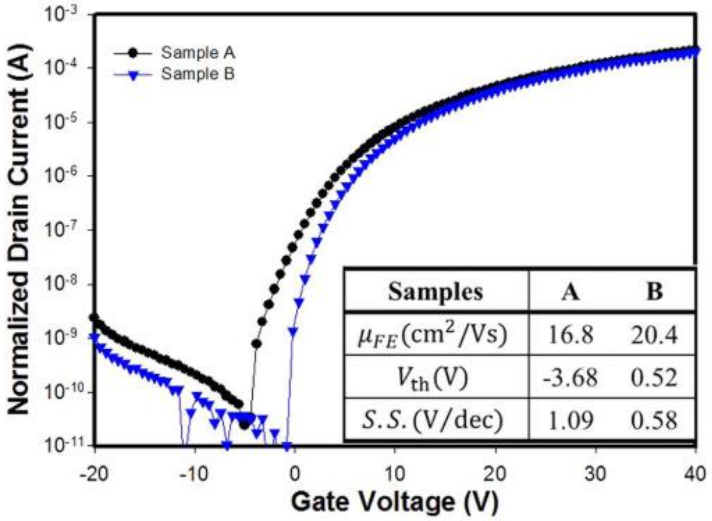


Figure 7.3: Transfer curves of a-IWO TFTs: samples A and B, at V_{DS}=10V. The Inset shows the electrical parameters, including carrier mobility, threshold voltage and substhreshold swing [120].

The relatively higher performance of sample B as seen in Figure 7.3 is attributed to the oxygen rich IWO layer which can reduce the damage to the back channel induced by plasma during the passivation deposition. Additionally, the oxygen rich IWO later can provide oxygen to passivate the oxygen deficiencies during the annealing process which leads to the improvement in the electrical characteristics. SIMS depth profile of the films also showed that sample A has a relatively higher ion intensity of hydrogen in the IWO channel layer. This is attributed to the diffusion of H^+ into the IWO channel of sample A during the PECVD SiO_2 passivation deposition, while the prevalence of oxygen effectively blocks the hydrogen diffusion. Incorporation of hydrogen with oxygen bonding would generate excess electron as shown in the following reaction in 7.4 [121].

$$H^0(from\ outside) + O^{2-}(in\ a\text{-}IWO) \rightarrow OH^-(in\ a\text{-}IWO) + e^- \quad 7.4$$

7.1.1 IWO TFT Fabrication

Experiments on the process development of IWO devices can be performed by varying the oxygen percentage in the sputter ambient, the anneal time and the anneal duration. Devices were fabricated on silicon wafers with bottom gate staggered configuration on a thick thermally grown isolation SiO_2, of a thickness of approximately 650nm. A 150 nm Molybdenum gate electrode was sputtered and patterned, followed by a 50 nm SiO_2 gate dielectric deposited by PECVD (TEOS precursor, 390 °C). The SiO_2 was densified for 2 hours in N_2 ambient at 600 °C in a furnace.

The IWO mesa was patterned using negative lift-off lithography. The mesa was patterned and defined by the lift-off technique which uses Futurrex NR9g-1500PY as the negative photoresist. The composition of the 4-inch IWO ceramic target consists of indium oxide to tungsten oxide at a 98:2 ratio respectively. IWO was sputtered for a dep rate of ~2 nm/min at 7mT pressure, power of 50W, with a gas ambient ratio of $Ar:O_2$ being varied, delivering a mesa of specified thickness. The sputter voltage and current were observed to remain at 320V and 0.15A. The sputter system used was a CVC601 DC sputter machine with rotating platen for substrates. Figure 7.4 shows the 4-inch IWO target installed as a sputter target with added shields on top to achieve improved sputter uniformity. It should be noted that a 30-minute argon only pre-sputter should be performed prior to any device deposition to remove any surface residue and sub-oxide films.

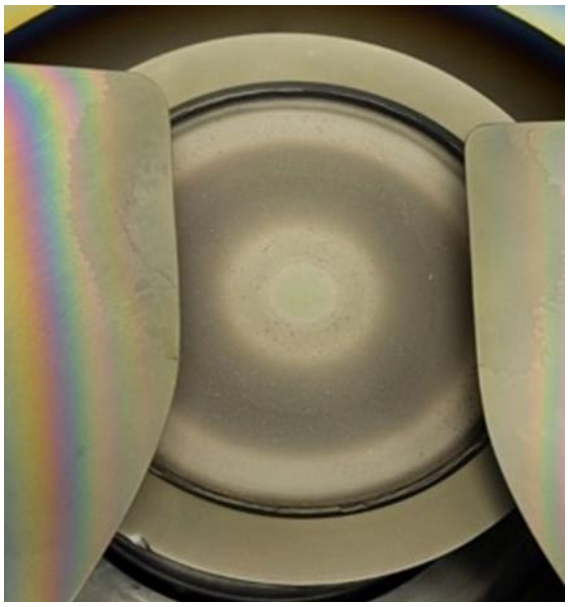


Figure 7.4: IWO target installed in CVC601 sputter machine with added shields for improved sputter uniformity.

The S/D contact metal composed of a Mo-Al bilayer, with thickness of 50nm Mo and 75nm Al, was then sputtered and defined by lift-off technique using Futurrex NR9g-1500PY negative photoresist. The wafer was then broken into four quarters and each quarter was subjected to different design of experiment conditions. After annealing, the gate and S/D contact windows on each quarter were patterned lithographically and finally etched, to open contact to the gate, using 10:1 buffered HF solution.

7.1.2 Annealing on IWO Films

In an experiment by Qu et al., RF magnetron sputtering is used where the target was In_2O_3:WO_3=98:2 wt% and Ar & O_2 are used as the ambient gas [122]. The effect of annealing ambient is explored by using N_2, O_2 and air for 30min at 100°C as shown in Figure 7.5.

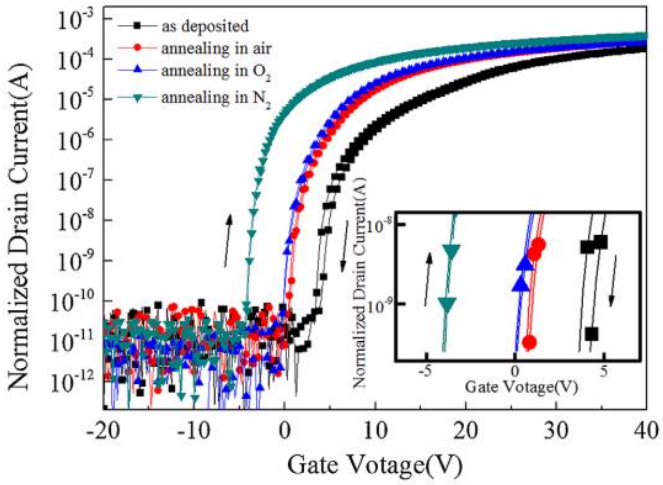


Figure 7.5: Transfer characteristic curves of a-IWO TFTs under different annealing ambient conditions [122]

The V_T of O_2-annealed and air-annealed devices is more positive than N_2-annealed devices. This is attributed to the O_2 in the annealing ambient which can diffuse into a-IWO channel layer and fill excess oxygen vacancies. The hysteresis is related to the electron capture in the channel layers, gate insulator/channel interface [123] and the charge trapping by the adsorbed water on the semiconductor surface [124]. Highest hysteresis is shown with air annealing than O_2 and N_2 annealed devices since it contains H_2O. In addition, O_2 annealed devices showed better PBS and NBS stability which is attributed to the reduction of oxygen desorption and improvement of the interface between the channel and dielectric layer. Since oxygen vacancies in oxide semiconductors are the main source of free electrons, the conductivity of the film can be regulated by controlling the oxygen vacancy content in the film during annealing [125]. Oxygen annealing is thus effective for controlling the carrier concentration of the active layer, decreasing electron traps, and enhancing TFT performance [126].

In IWO TFT literature, annealing performed at temperature as low as 100ºC has produced enhancement-mode devices [107], [112]. Most anneal experiments have been performed at or below 300ºC to avoid crystallization that may occur at higher temperatures. However, IWO

sputtered at RIT with P_{O2}=1.2% and annealed at 400°C for 2 hours in O_2 showed no crystallization as seen in Figure 7.6. Since low temperature processing was not a primary focus of this work, most experiments were done using furnace annealing in O_2 at 300ºC.

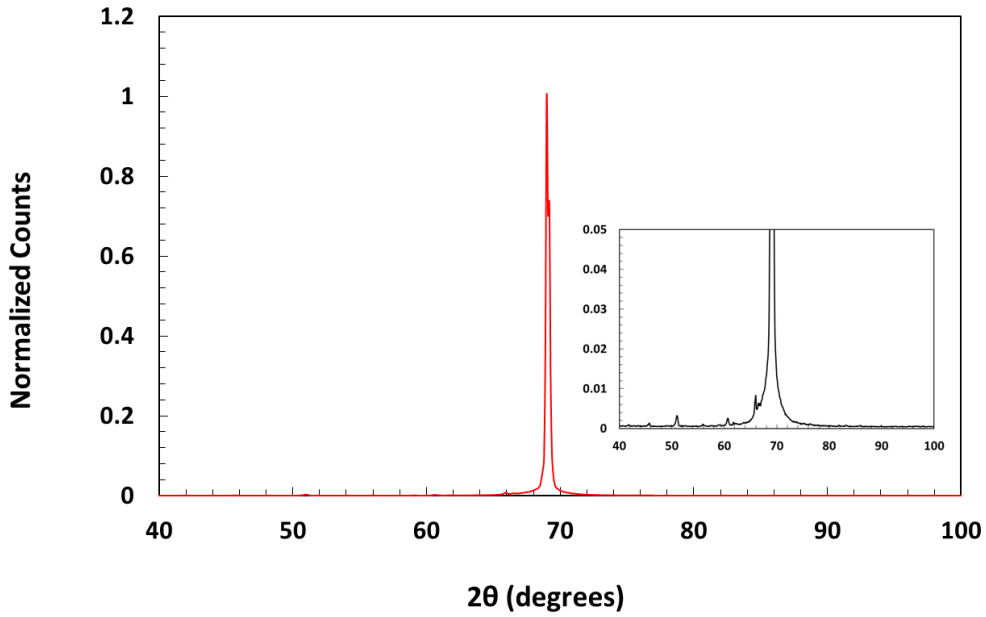


Figure 7.6: XRD spectrum of annealed IWO film for 2hr in O_2 at 400°C on a silicon wafer. The peak at ~70° is from the Si wafer used as substrate, absence of any additional peak confirms the amorphous nature of the annealed films. The inset is a zoomed plot to show the noise margin.

7.1.3 Influence of P_{O2}

The impact of annealing for films sputtered at different oxygen content (0%, 1.2%, 1.75%, 10%) was studied. As standard practice, the run had a half hour argon only pre-sputter, and half an hour deposition at 7mT and 50W. The voltage and current during sputter remained at ~320V and ~0.15A. Figure 7.7 shows that the material resistivity, in samples annealed at 300ºC in O_2 for two hours, does increase as the volume percentage of oxygen increases, with $\rho = 0.74\Omega\cdot cm$ at 10%O_2. Note that the pre-anneal resistivity dependence on %O_2 was not as straightforward. For devices sputtered at oxygen ambient < 2%, an increase in %O_2 caused a decrease in resistivity. However,

high %O_2 in the sputter ambient resulted in significant increase in resistivity. The graph shows that for pre-anneal treatments, an increase in O_2 content in the sputter ambient causes a decrease in sheet resistance however, after the anneal, an increase in O_2 content in the sputter ambient causes an increase in sheet resistance. The anneal appears to have an enhanced impact on passivation of oxygen vacancy defects when the sputter ambient includes oxygen, most likely through the incorporation of interstitial oxygen in the sputtered IWO film. While the Van der Pauw structures confirm differences in the electrical properties of the IWO material, the semiconductor behavior (i.e. ability to modulate charge) must be investigated within a TFT device structure.

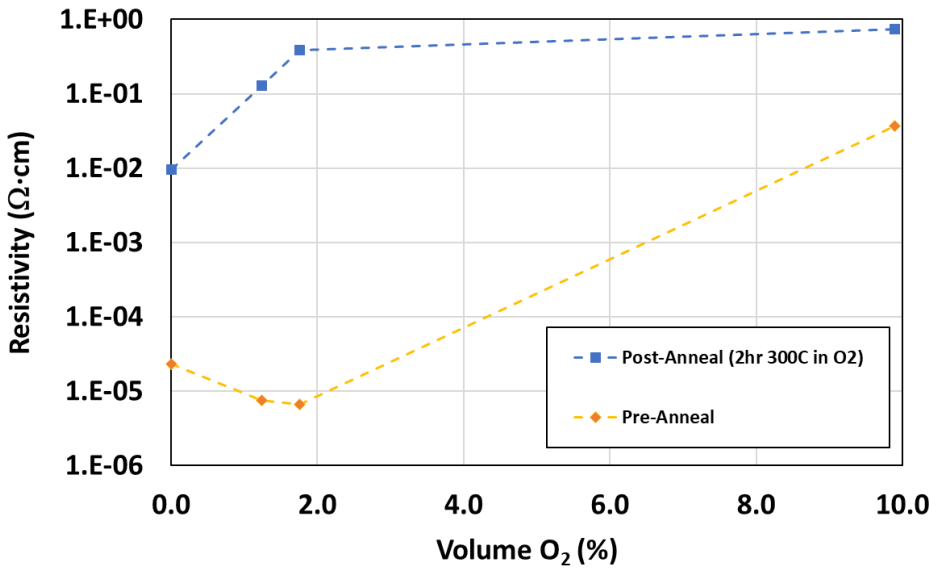


Figure 7.7: Resistivity vs. %O_2, annealed in dry O_2 at 300ºC for 2 hr. Note Rs measurements converted to the material resistivity (Ω·cm).

While the resistivity of the IWO was higher for the 10% O_2 treatment in comparison to the 1.2% O_2 treatment, the TFT characteristics were not as encouraging. The 10% O_2 devices following an 8-10 hours O_2 anneal at 300ºC exhibited semiconductor behavior, however representative transfer curves demonstrated inferior performance. An overlay of the 1.2% and 10%

O_2 characteristics is shown in Figure 7.8. While a high resistivity material is required for proper TFT behavior, this result suggest there are other effects that compromise the device operating characteristics. Apart from the oxygen content in the sputter treatment, both devices underwent similar process conditions. Based on the transfer curves in Figure 7.8, the increasing O_2 content in the ambient does not necessarily result in better enhancement-mode TFTs. These results suggest that excess oxygen may result in charge trapping defects in the IWO channel and/or channel/dielectric interface [107].

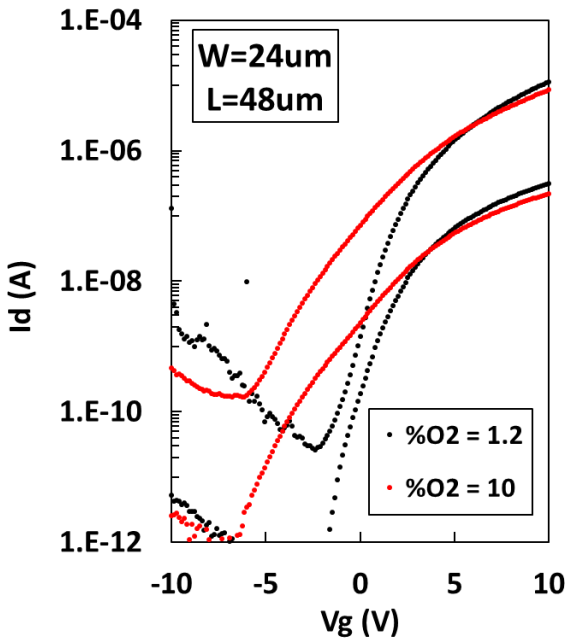


Figure 7.8: Transfer curves for 48um device sputtered in ambient of 1.2% and 10% O_2 per volume and annealed dry O_2 for 10-hour at 300ºC.

Table 7-II: Comparison of various device parameters of 1.2%O_2 vs. 10%O_2 TFTs

Parameter	**1.2 %O_2**	**10 %O_2**
S.S (V/decade)	0.94	1.8
Mobility (cm^2/Vs)	17	9
V_T @ 50pA/μm (@V_{DS}=0.1V)	0.8	-1
ΔV (sat-linear) @ 50pA/μm	0.9	3.4

7.1.4 Impact of Annealing on IWO TFT Behavior

The most successful anneal treatment so far has been the 10-hour 300°C dry O_2 anneal treatment. To avoid polycrystalline material formation, the temperature was initially kept at a consistent 300°C. Eventually higher anneal temperatures were studied for possible improvements in device operation and/or reduction in required anneal time. The temperatures investigated were 350°C and 400°C, with 2 hour anneal time. Figure 7.9 shows transfer curves of 24um devices with 1.2%O_2, with 350°C and 400°C O_2 anneal for 2 hours, and 300°C O_2 anneal for 10 hours.

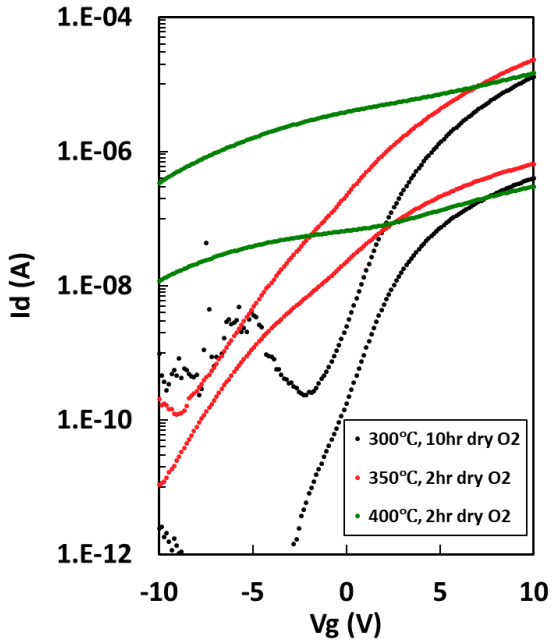


Figure 7.9: Transfer curve of 24um device sputtered in ambient of 1.2%O_2 and annealed at different temperatures.

While the device operation of the sample annealed at 300°C appears superior to the higher temperature samples, the comparison is relative due to the difference in anneal times. However, the 350°C treatment has better semiconductor behavior in comparison to the 400°C treatment, suggesting that the material may have experienced an additional defect mechanism, with compromised device operation as a result when the temperature reaches 400°C.

7.1.5 Further Treatment Comparisons

The first set of TFTs fabricated were sputtered at a 6.7% O_2 ambient at 50W, 7mT for 15 minutes. The target was pre-sputtered for 15 minutes in an argon and oxygen ambient and the TFTs were finally annealed for 2 hours at 300ºC in dry O_2. The transfer characteristics obtained can be seen in Figure 7.10. The preliminary experiments conducted on IWO TFTs produced encouraging results as we observe semiconductor behavior represented on the transfer curves.

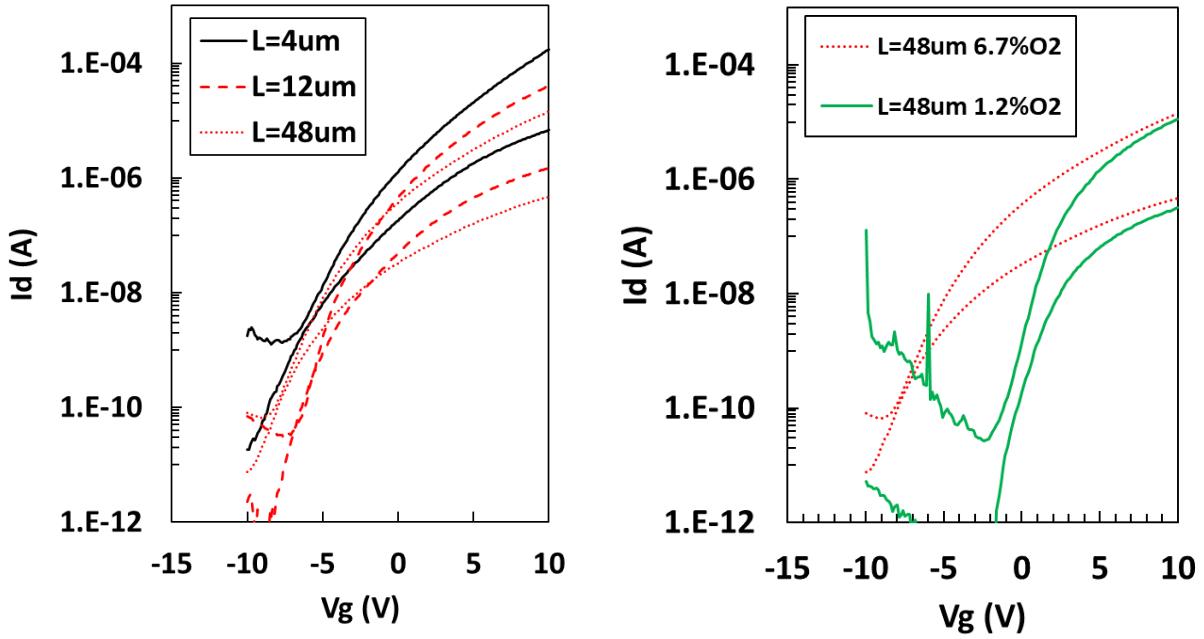


Figure 7.10: (a) Transfer characteristics of IWO TFTs, 6.7% O_2, annealed in O_2 for 2 hours at 300ºC, (b) Comparison of 6.7%O_2 annealed for 2 hours and 1.2%O_2 annealed for 10 hours at 300C in dry O_2

As an attempt to recreate these results a new run was commenced recreating the same conditions as that from before, but by reducing the sputter time by half, the logic behind this being that a thinner mesa would result in less channel conductivity and better gate modulation. However, on doing so the devices tested produced two inconsistencies; firstly, many of the devices were not able to handle large negative voltages applied to the gate and secondly, the few devices that were tolerant, resulted in highly conductive channels with poor current modulation.

A device wafer was processed with 30-minute Argon only pre-sputter and then a 30-minute deposition at an ambient of 1.2%O_2. The devices were then processed as usual and annealed for 2 hours at 300ºC O_2. The devices behaved in a conductive fashion however a slight upward slope. The sample was then once again annealed for additional 8 hours in 300ºC O_2 and tested. The devices clearly demonstrated gate-controlled current modulation as seen in Figure 7.10b. The

electrical parameters of the 48um device extracted from Figure 7.10b was, subthreshold slope of 0.94V/dec, $\mu = 17cm^2/Vs$ and threshold voltage (V_T) = 0.8V taken to be $I_D = 50pA/\mu m$ @ $V_{DS} = 0.1$ V. Van der Pauw test structures were used to find the sheet resistance corresponding to the 1.2%O_2 devices, measured to be Rs ~ 6 MΩ/sq. Note that the semiconductor behavior of the transistors realized after surface reconditioning and 30min argon pre-sputter, was not previously achieved when the plasma current/voltage conditions were different than those specified in the details of TFT fabrication (i.e. 320V, 0.15A). This provided the confirmation necessary to further investigate alternative treatment combinations.

7.1.6 Multilayer IWO TFT

Multi-stacked IWO channel layer was also used by many groups to fabricate devices such as IWO and oxygen rich IWO bi-layer [120], IWO and IWZO double layer [127], IWO and IWO:N double layer [128], multiple combinations of IWO and IWZO [129], IWO and IGZO bi-layer [130] etc. and their properties are summarized in Table 7-III.

Table 7-III: Multi-stacked IWO channel layer TFT parameters

Structure	Anneal condition	μ_{FE} (cm^2/Vs)	V_T (V)	SS (V/dec)	Ref
a-IWO (7% P_{O2})/a-IWO (13% P_{O2}), 100nm SiO2 pass	400°C, O_2, 1hr	20.4	0.52	0.58	[120]
IWO (4% WO_3)/ IWZO (15% WO_3)	NA	21.1	-0.092	0.15	[127]
IWO/ IWO:N	100°C, N_2, 0.5hr	27.2	0.37	0.56	[128]
IWO (4% WO_3)/IWZO (15% WO_3)	150°C, O_2, 20min	26.5	-0.15	0.092	[129]
IWZO (15% WO_3)/IWO (4% WO_3)		22.6	-0.108	0.086	
IWZO (15%WO_3)/IWO (4% WO_3)/IWZO (15% WO_3)		27.9	-0.106	0.079	
a-IWO/IGZO, 100nm SiO_2 pass	200°C, O_2, 2hr	25.54	2.39	0.44	[130]
a-IWO/IGZO, 20nm Al_2O_3 pass		27.92	-1.95	0.58	

In [120], Liu et al. showed that the oxygen-rich IWO layer can provide additional oxygen to passivate the oxygen deficiencies during the annealing process, leading to improvement in the transfer characteristics with the bilayer IWO channel. A similar experiment is done here where a bilayer IWO channel is deposited where the oxygen partial pressure of the first layer is 1.2% and the second layer is 6.7% which are sputtered successively. An improvement is observed as shown in Figure 7.11 in the current drive and the subthreshold behavior of the device characteristics which employed the IWO bilayer.

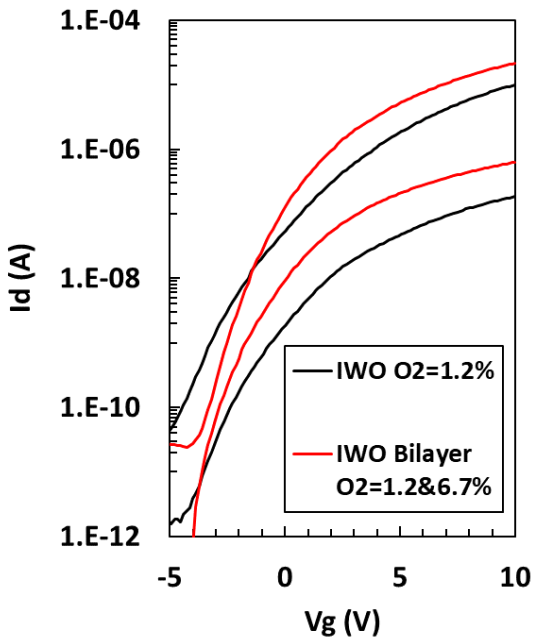


Figure 7.11: IWO TFTs with L=48 um employing bilayer structure of oxygen content in the channel showing improved I-V characteristics over a single layer channel.

7.2 ITGO TFTs

While most of the AOS TFTs are compatible with the thermal constraints of a glass substrate, researchers have been looking for a material compatible with flexible substrates having low glass transition temperature (i.e. T < 250 °C) and relatively high thermal expansion coefficient values.

Flexible substrate materials such as polyethylene naphtholate, polyethylene terephthalate, polyimide, polydimethylsiloxane etc., impose a thermal limit that may be below the typical annealing temperature required to achieve desirable semiconductor properties. Most AOS materials undergo a high temperature (i.e. T > 300 °C) anneal, thus alternative materials must be investigated where alternative methods can be used to achieve the semiconductor properties.

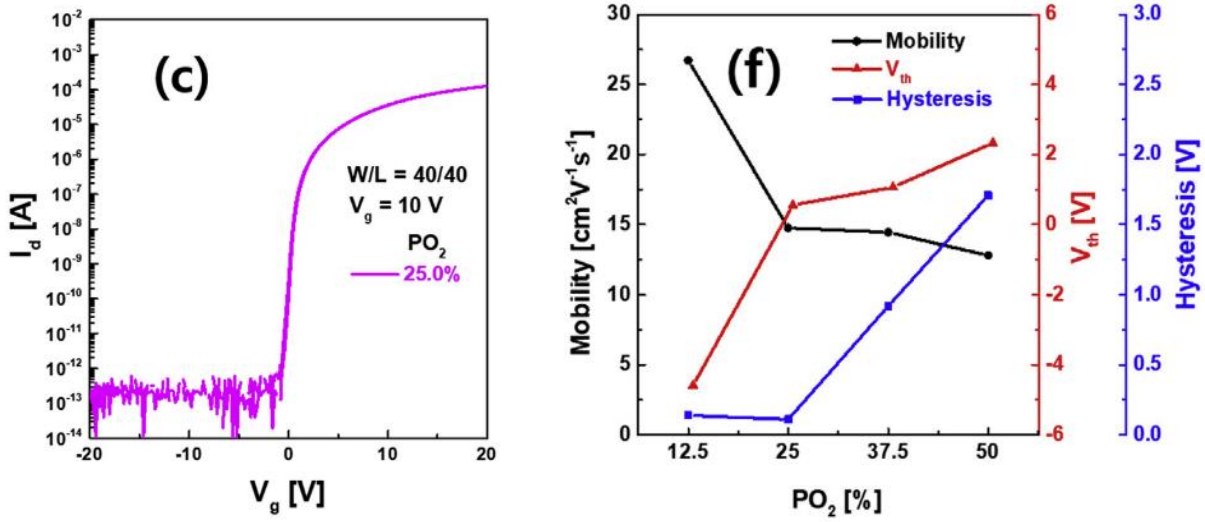
For this reason, Indium Tin Gallium Oxide (ITGO) is an attractive option since In and Sn cations with $[Kr]4d^{0}5s^{0}$ electronic configuration have large spatial overlap between the 5s orbitals and afford highly conductive pathways to electron carriers, thus higher electron mobility. To use this property in a TFT, an applied gate voltage must be able to modulate the free carrier density to provide high on-state drive current and low off-state leakage. The role of Ga cations in IGZO is to suppress excess carriers as it forms strong bonds with oxygen which reduces the number of oxygen vacancy donors that act as sources of free electrons [109].

ITGO TFTs with mobility exceeding 25 cm^2/Vs were achieved by Jeong et al. where they have suggested that oxygen vacancy related defects increase with increasing annealing temperature and results in more pronounced degradation during NBTS [108]. The same group demonstrated ITGO TFTs fabricated at 150 °C with UV-assisted annealing [131]. UV radiation (λ = 254 nm) was used to produce oxygen radicals (UVO treatment), followed by shorter wavelength radiation (λ=186 nm) that generated ozone. The representative device parameters are summarized in Table 7-IV with different activation process.

Table 7-IV: Electrical properties of ITGO films subjected to different activation processes. Adapted from [131].

@60 min	Mobility (cm^2/Vs)	V_T (V)	SS (V/decade)	N_{SS} ($cm^{-3}eV^{-1}$)	D_{IT} ($cm^{-2}eV^{-1}$)
UVO-only	8.21±0.5	0.64±0.82	0.44±0.10	1.55×10^{18}	7.77×10^{12}
UVO-Thermal	21±1.3	0.23±0.53	0.27±0.05	4.77×10^{17}	9.53×10^{11}

In comparison to the UVO treatment at RT, the UVO treatment at 150 °C demonstrated a marked improvement in electron mobility, subthreshold swing (SS), and defect state concentrations. From XPS analysis it is suggested that there is a reduction of oxygen vacancy defects that act as carrier traps, and an increase in hydroxide (OH) bonds that suppresses excess free electrons, resulting in the observed improvement in TFT performance. In previous literature it is shown that UV irradiation increases the field-effect mobility of IGZO TFTs through creation of an -OH rich channel surface [132].



(a) (b)

Figure 7.12: (a) Transfer curves of ITGO TFTs with P_{O2}=25% and (b) field-effect mobility, threshold voltage, and hysteresis of the ITGO TFTs as a function of P_{O2}, adapted from [133].

However, low temperature processing generally involves a high number of defects, nanoscale voids, and unstable dangling bonds, which degrade the channel properties. Processed devices typically exhibit large hysteresis and low channel mobility, and require a high driving voltage range [134]. In [135], the authors suggested that the sputter chamber pressure (P_C) is directly responsible for quality of the channel film. Through deconvolution of the O1s spectra by XPS it was shown that the V_O related peak decreased, and the metal-oxygen lattice peak increased with decreasing P_C, which allowed the channel film to have smoother surface morphology and denser atomic packing. The oxygen partial pressure (P_{O2}) is also a crucial factor in determining the resulting ITGO film characteristics after RF/DC sputter. Oh et al. showed that ITGO TFT with sputter ambient P_{O2} =25% exhibited the best operating characteristics within their experimental range (12.5 - 50%), as shown in Figure 7.12a. The TFT characteristics and stability are strongly dependent on the metal-oxygen surface states rather than the bulk regions of the ITGO films during sputtering. The increase of V_O is attributed to the bombardment of oxygen radicals on the ITGO surface by increasing P_{O2} which generates interface electron trap states of the ITGO TFTs. This results in deteriorating electrical performance (μ_{FE}, SS & hysteresis) and instability of the TFTs during PBS as shown in Figure 7.12b [133]. The increase in V_T from -4.5 to 0.8 V was a benefit from the increase in P_{O2} from 12.5 to 25%, with an unfortunate drop in channel mobility from 27 to 15 cm^2/Vs.

7.2.1 ITGO Process Development

Prior to device fabrication, initial ITGO film properties were characterized on RF sputter deposited samples using the same system applied for IGZO. The RF sputter power density (0.25 W/cm^2) and pressure (~2.3 mT) remained constant, with the partial pressure of oxygen varied from zero to 10% by volume. Energy dispersive X-ray (EDX) composition analysis used in P_{O2}=0% ITGO film revealed the atomic percentages as 56.7, 3.3, 7.3, and 32.7, respectively. The ITGO deposition rate varied significantly as shown in Figure 7.13; ranging from 73 nm/min at P_{O2} = 0 – 1%, down to 50 nm/min at P_{O2} = 10%. There were noted differences in optical constants (n & k), with measurements taken from UV - IR presented in Figure 7.14.

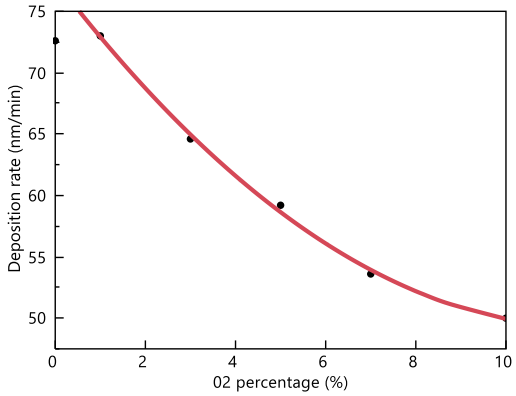
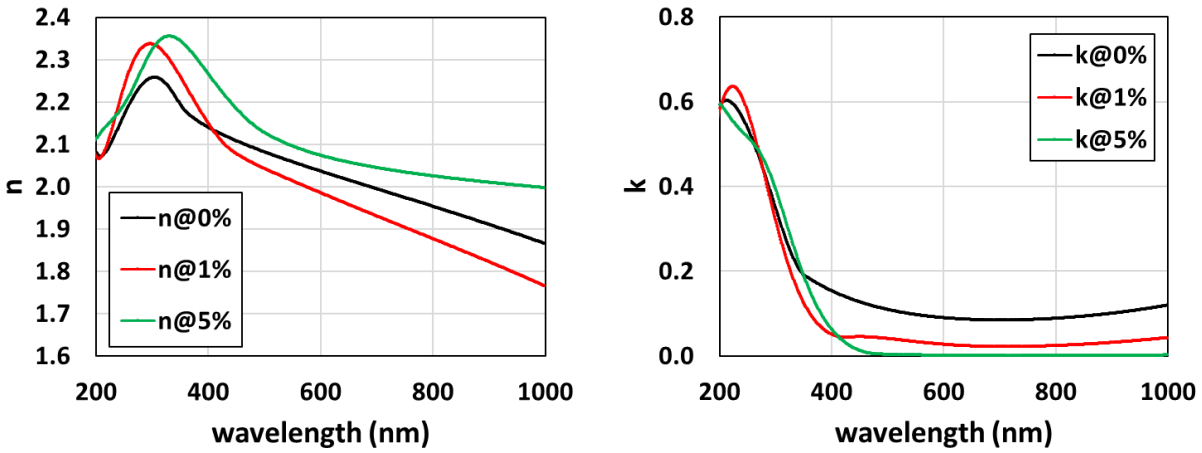


Figure 7.13: ITGO deposition rate with oxygen partial pressure during sputter



(a) (b)

Figure 7.14:Optical constants (a) n & (b) k with varying oxygen partial pressure during ITGO sputter.

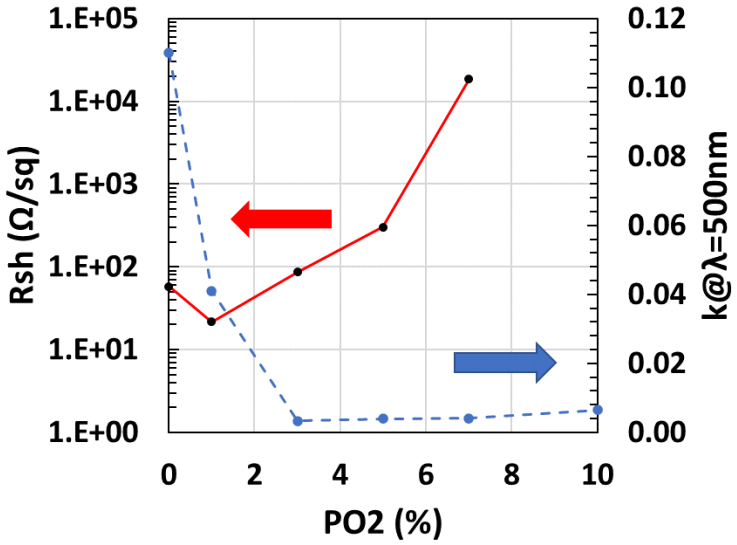
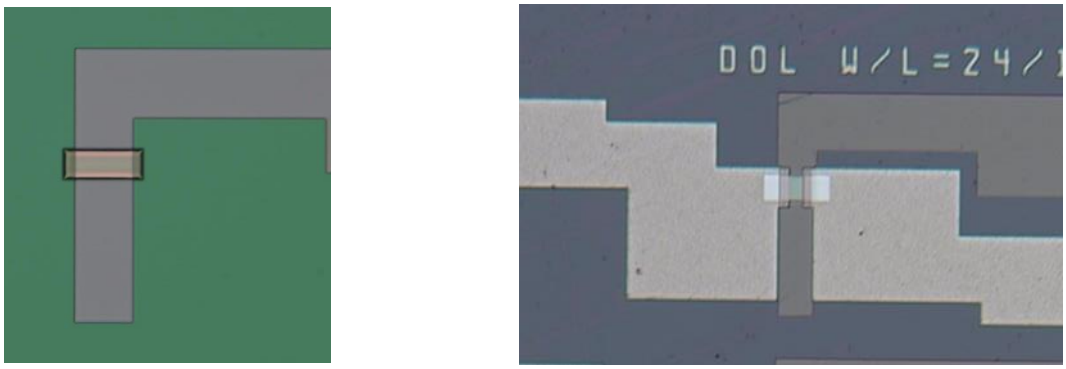


Figure 7.15: Sheet resistance & k@λ=500nm as a function of oxygen partial pressure during sputter of ITGO film, note that for P_{O2}=10% the Rsh was not measureable.

The characteristic changes in the index of refraction (n) appeared somewhat ambiguous, however the behavior of the extinction coefficient (k) revealed a decreasing trend in the absorption of visible light as the P_{O2} setting increased. This appears to go along with the increase in measured Rsh as a function of P_{O2} shown in Figure 7.15, with the exception of the initial change from zero to 1%.

7.2.2 ITGO TFT Fabrication

Experiments on the process development of ITGO devices are performed by varying the oxygen percentage in the sputter ambient and sputter time. Devices were fabricated on silicon wafers with bottom gate staggered configuration on a thick thermally grown isolation SiO_2, of a thickness of approximately 650nm. A 150 nm Molybdenum gate electrode was sputtered and patterned, followed by a 50 nm SiO_2 gate dielectric deposited by PECVD (TEOS precursor, 390 °C). The SiO_2 was densified for 2 hours in N_2 ambient at 600 °C in a furnace. The channel material ITGO was deposited in an Applied Materials Centura RF sputter system in a single wafer, load-locked chamber using ITGO target with a substrate chuck temperature of 200 °C. The deposition pressure was established ~2.4 mT in an argon ambient with 0 to 10% oxygen. The ITGO mesa was patterned by wet etching in dilute HCl as shown in Figure 7.16a.



(a) (b)

Figure 7.16: (a)Wet etched ITGO active region (wet etch rate 20nm/min), (b) Completed BG ITGO TFT showing tranparent channel region.

The S/D contact metal composed of a Mo-Al bilayer, with thickness of 50nm Mo and 75nm Al, was then sputtered and defined by lift-off technique using Futurrex NR9g-1500PY negative photoresist. The wafer was then broken into four quarters and each quarter was subjected to different annealing conditions. After annealing, the gate and S/D contact windows on each quarter were patterned lithographically and finally etched, to open contact to the gate, using 10:1 buffered

HF solution. The devices were then annealed for 2 hours at 300ºC O_2 with a ramp-down in O_2. The devices were then tested, using an Agilent B1500 semiconductor device parameter analyzer, and the I_D-V_G transfer curves were obtained.

7.2.3 ITGO TFT Characteristics

The ITGO TFTs fabricated with P_{O2}<10% during sputter did not show any switching characteristics (not shown here), exhibiting resistor like characteristics. This may be due to extremely high number of oxygen vacancies and defect states.

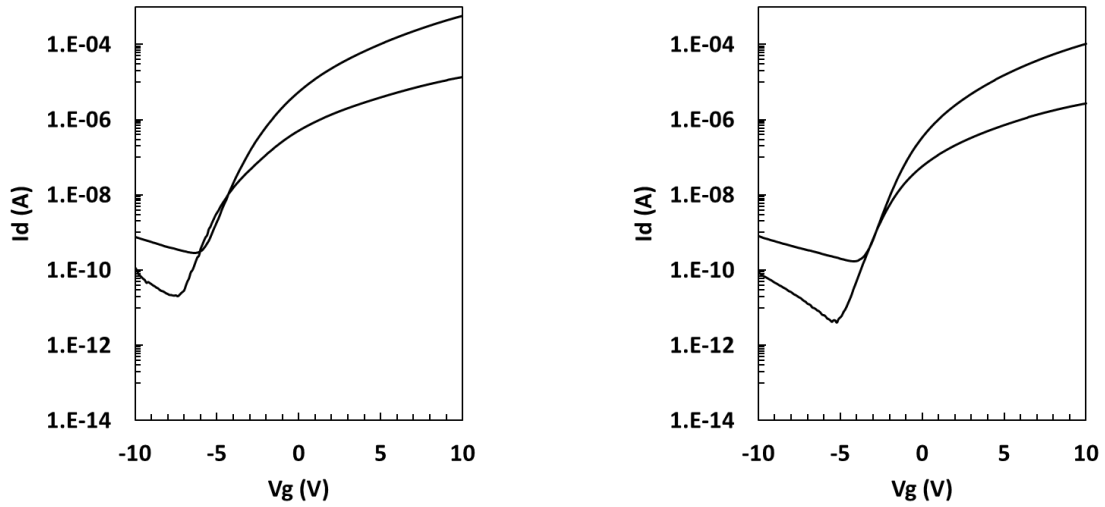


Figure 7.17: ITGO TFT characteristics a) L=12µm and b) L=48µm with t=50nm & P_{O2} =10% and annealed at 300C for 2hr in O_2

The ITGO TFTs fabricated with 50nm channel thickness and P_{O2}=10% showed very promising I-V characteristics as shown in Figure 7.17. The L=12 µm ITGO device has a current higher than 10^{-4}A at V_D=V_G=10V which is usually achieved in L=4 µm IGZO devices. This indicates a very high channel mobility in the ITGO devices where it is ~5x higher mobility than IGZO. However, the SS is relatively shallow and there is also noticeable crossover effect in Figure 7.17a which is

due to interface traps. Further work needs to be done to achieve better electrostatic behavior.

7.3 SUMMARY

Reactive sputter conditions with low O_2 content resulted in electrical behavior that was very different from argon-only sputtering (zero $\%O_2$). Pre-annealed behavior revealed that a low O_2 treatment (i.e. < $2\%O_2$) has a lower sheet resistance than zero-oxygen treatments. The same low O_2 treatments resulted in a post-anneal resistivity $\rho \sim 1\ \Omega\cdot cm$; over an order of magnitude higher than zero-oxygen treatments. These results suggested that annealing at 300°C with O_2 should produce films with high enough resistivity for TFTs. This was indeed the case as demonstrated for IWO TFTs processed with low (1.2%) and high (10%) oxygen content in the sputter ambient, with O_2 annealing at 300°C for 8-10 hr. While the high oxygen treatment material demonstrated a higher post-anneal resistivity, the device operation was inferior to the low oxygen treatment TFT. This was apparent in both on-state and off-state conditions, with the low oxygen treatment exhibiting higher current drive and steeper subthreshold. While the 10 hr O_2 anneal at 300°C demonstrated marked improvement over the 2 hr anneal, it likely represents an upper limit for benefits to the electrical behavior under these conditions and suggests an increase in annealing temperature may be required for additional performance improvement. Increasing the O_2 anneal temperature to 350°C on TFTs with the low $\%O_2$ showed promising results for a 2 hr anneal; a longer anneal time may demonstrate improvement over the 300°C treatment. Raising this temperature to 400°C resulted in reduced gate control and current modulation, suggesting the onset of an additional defect mechanism. Degradation in device operation demonstrated by the high $\%O_2$ material, or by aggressive O_2 annealing at T > 350°C, may have a similar origin.

For ITGO, the sheet resistance (Rsh) and optical constant k have opposite relationship with oxygen partial pressure (P_{O2}) where Rsh increases, and k decreases with increasing P_{O2}. For ITGO film with P_{O2}<10% the Rsh was in measurable range but still did not yield any I-V characteristics with switching behavior. ITGO film with P_{O2}=10% showed very promising I-V behavior where the extracted mobility is ~5X compared to IGZO TFTs. However, further work needs to be done to completely understand the material and I-V behavior.

Materials analysis is needed to determine relationships between $\%O_2$ ambient, O_2 annealing, and the role of oxygen within the next-gen AOS film. The physical content of oxygen may be quantified using secondary ion mass spectroscopy (SIMS). The chemical distinctions of oxygen (e.g. lattice, interstitial) may be characterized by x-ray photoelectron spectroscopy (XPS). Note that the ability to detect such differences in a metal-oxide material presents a significant challenge. Refined experimental designs that considers these findings, followed by materials analysis to quantify treatment combination differences, will provide further understanding and progress towards parameter optimization needed to realize the potential of IWO & ITGO as next-generation AOS candidate for display and other applications.

Chapter 8. CONCLUSIONS

The primary focus of this work was to further the understanding of electronic transport and defects states in IGZO TFTs through the interpretation of measured device behavior and correlation with physical modeling. The goal was attained through the following accomplished objectives:

- Established the relationships between processes associated with IGZO TFT operation including annealing conditions and back-channel passivation that supports device stability when subjected to thermal and bias stress. A hypothesis was proposed to explain the channel length dependence of thermal instability.
- Developed TCAD material and device models using Silvaco Atlas for BG configurations that depict the role of defect states on device operation, as well as provide insight and support of a previously established hypothesis on DIBL-like device behavior explained by trap associated barrier lowering (TABL) linked to back-channel interface trap inhomogeneity.
- Refined TCAD device model which explains device operation over temperatures ranging from T = 150 K to room temperature, over all gate and drain bias conditions ranging from zero to 10 V. This new model accounts for the role of donor-like oxygen vacancy defects, acceptor-like band-tail states, acceptor-like interface traps, and a temperature-dependent intrinsic channel mobility that is not dependent on carrier concentration.
- Presented new scheme of utilizing ion implantation for self-aligned (SA) source/drain regions, which presents a path towards submicron channel length. This strategy offers a reduction in channel length as well as parasitic capacitance, which translates to improvement in RC delay

and associated voltage losses due to charge-sharing. The first ever report of boron-doped SA IGZO TFT is detailed.

- Initial study on IWO and ITGO as next-generation AOS candidates, which identifies the influence of process parameters such as the oxygen percentage in sputter ambient, and annealing conditions.

This chapter provides a summary of the important findings and contributions of this research work, with recommended areas for further study to support the evolution of AOS materials into mainstream manufacturing.

8.1 KEY CONTRIBUTIONS

8.1.1 Defect Passivation and Device Stability

The passivation of back-channel defects through a described "ripening" process was modeled using TCAD in portraying the incremental reduction of trap-state behavior (i.e. TABL) during passivation annealing. Simulation results illustrate a realistic scenario of the gradual progression of defect state passivation. Results emphasize the importance of defect passivation to enable appropriate electrical operation and promote device stability.

An investigation was presented on the thermal stability of IGZO TFTs fabricated using SiO_2 dielectric layers in BG and DG configurations. Without a capping layer above the back-channel passivation oxide, the device characteristics showed continuous degradation (i.e. left-shift, distortion, separation) during applied thermal stress. This was more pronounced on DG devices which led to the proposed mechanisms for thermal instability, involving H_2O and the liberation of

monatomic hydrogen. Investigations on both silicon MOSCAPs and IGZO TFTs demonstrated that an ALD Al_2O_3 capping layer was effective at reducing the influence of thermal treatments at 140 °C and 200 °C, suggesting that the capping layer suppressed H_2O incorporation and reaction with the top-gate metal. An observed channel length dependence on the thermal degradation of DG devices led to a hypothesis involving the gettering of water from the back-channel material during the passivation anneal. Process techniques which minimize the incorporation of water in the passivation oxide, and the application of an effective capping layer such as ALD alumina which immediately follows an optimized passivation anneal are all key elements towards achieving thermally stable IGZO TFTs.

IGZO with bottom gate and double gate configurations were used to study the response of bias stress stability. A characteristic shift in response to bias stress can be attributed to defect state changes either in the dielectric region, the IGZO/SiO_2 interfaces, or the bulk IGZO material. Passivated BG devices exhibit the influence of back-channel interface traps, which slightly degrade subthreshold operation. BG devices under PBS were found to be very stable, with relatively few device characteristics showing any induced distortion. The back-channel region does not experience any significant E-field during PBS; thus the stability is attributed to the high quality of front-channel SiO_2-IGZO interface. BG devices under NBS showed a significant left shift in transfer characteristics, however the initial characteristics had a shallow subthreshold slope, indicating an elevated level of interface traps. Time under NBS appears to convert some of these donor-like traps into positive ions that remain fixed during transfer characteristic measurements. The proposed mechanism involves defect reconfiguration during the transition from a “weak bond” neutral state to a double-donor V_O^{2+} state during NBS. The reversal of this behavior to “pre-stress” conditions is explained by thermal relaxation and return to the original

defect configuration.

8.1.2 Scaled IGZO TFT

Scaled BG devices with a reduction in gate oxide thickness to 50 nm demonstrated excellent electrical characteristics at channel lengths as small as L = 1 μm. Thickness adjustment of the PECVD SiO_2 passivation layer required re-engineering the O_2 passivation anneal. While this change at the backchannel was not needed for improved electrostatic control on the BG device, it presents an optimized process for a scaled top-gate dielectric on a DG device structure. The specific details of the ALD Al_2O_3 capping layer, both process and procedure, where shown to be important in supporting enhancement-mode BG device operation with steep subthreshold characteristics and excellent thermal stability. The scaled process also maintained good stability when subjected to PBS and NBS, with complete recovery to initial characteristics. Both the BG dielectric and the IGZO thickness could be reduced further to enable shorter channel length, however the DG device structure presents a conservative approach towards submicron dimensions that supports low variation and reliability.

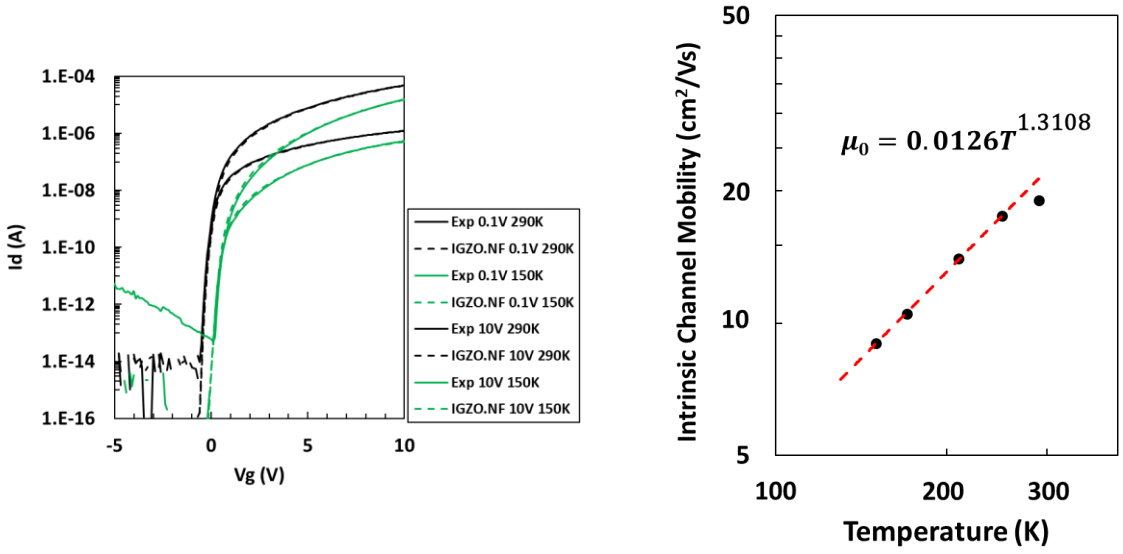
8.1.3 Self-Aligned IGZO TFT

The first ever report of the use of boron-doped IGZO for self-aligned S/D regions formed selectively via ion implantation has been discussed. This technique enables device scaling without the associated limitations of the channel length defined by the metallized S/D contact regions. The interpretation on the activation behavior of boron in IGZO is unique and certainly not obvious. Results suggest there are at least three distinct states in which boron can exist; two which involve chemical bonding and one as an electrically inactive interstitial atom. Of the two states that involve

chemical bonding, only one is proposed to behave as an electrically active donor species. The interstitial diffusivity of boron in IGZO is proposed to be very high, where it appears to move several microns within an hour at 175 °C. In contrast, the electrically active donor state is thermally stable and does not appear to diffuse at such a low temperature. There also appears to be a condition of equilibrium in the ratio of electrically active to inactive species, with the degree of electrical activation estimated to be ~ 10%.

8.1.4 Refined IGZO TCAD Model: Non-Fermi Mobility Model

The development of a refined TCAD model that accounts for temperature dependent behavior over a wide temperature range ($150\ K \leq T \leq 290\ K$) and bias conditions is unprecedented in the literature. Previous models have been plagued with inconsistencies and artifacts which do not resemble the true device physics of operation. The presented model allows the TCAD simulation to account for the behavior of defect states according to their defined energy distributions, thus properly regulating the amount of free channel charge. The channel mobility is considered only a function of temperature as shown in Figure 8.1a, with no dependence on carrier concentration; thus referred to as “non-Fermi” as it is independent of the Fermi energy level. The TCAD model is validated by the demonstrated fit to experimental data shown in Figure 8.1b, which will be a notable contribution to the body of science on AOS materials.



(a) (b)

Figure 8.1: (a) Low drain & high drain for 290K and 150K using IGZO.NF model with mobility as a function of temperature and (b) Power law fit of mobility extracted from IGZO.NF model as a function of temperature, at room temperature μ_o=19cm^2/Vs and at 150K μ_o=9cm^2/Vs.

8.2 FURTHER WORK

A consequence of the breadth of topics and experimental nature of this work are remaining areas that require further investigation. While the IGZO TFT TCAD model development is relatively complete, a complementary assessment from cryogenic multi-frequency CV analysis using interdigitated capacitors would be insightful. A variety of DOS extraction techniques reported in literature such as low-frequency CV [136], multi-frequency CV & GV [137], photonic CV & IV [138], [139], absorption spectroscopy & PL spectroscopy [140], pulse transient spectroscopy [141] can be investigated. The development of a compact model for SPICE circuit simulation is still a work in progress. There has been advancement in extending the previously developed on-state model to include off-state (subthreshold) operation, however additional work must be done to address remaining issues with transitions between regimes of operation. There are also details of process integration which must be considered when integrating devices for display or sensing with

an IGZO TFT backplane, such as temperature constraints and material compatibility; this may require alternative materials and process methods to those used here. The progress towards a self-aligned IGZO TFT using implanted S/D regions is encouraging, however the success of using B^+ ions is limited due to thermal instability which may not be solvable. Investigations on other potential implant species such as phosphorus have also shown promise, with experimental treatments currently in progress. Finally, the investigations on alternative AOS materials to address the requirements of next-generation TFT applications has just begun. While the preliminary studies on IWO and ITGO demonstrate high channel mobility and the potential for superior performance to IGZO, there is an extensive amount of work still needed to optimize processes and realize TFTs with the performance qualities of IGZO.

8.3 CLOSING REMARKS

While IGZO has been introduced into display products for quite some time, advancements in understanding and performance are still relevant research areas and of high interest to a large portion of the scientific community. While there is a particular focus on display applications, IGZO has the potential for device integration onto alternative substrate materials ranging from plastics for flexible electronics, to silicon CMOS for a back-end compatible device technology. It took around 40 years for an alternative semiconductor material to challenge hydrogenated amorphous silicon for large area display applications. While a-Si:H remains as the TFT material in most of the large area active matrix displays, IGZO is gaining market share due to the increasing performance demands of high-definition OLED displays and microLED displays. The development of alternative AOS materials for next-generation display products are likely more than a decade away from mainstream manufacturing, however their advancement will be driven

by the continuous demand for higher performance that is common to all consumer electronics. A remaining gap for AOS materials is the demonstration of a feasible candidate for p-channel devices needed to realize CMOS circuit designs while maintaining low production cost. There has been some recent progress towards this, however LTPS remains the only viable option to deliver PMOS TFTs with acceptable performance. Advancements in AOS materials will continue to be a field of increasing interest for display and other large-area electronics applications.

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APPENDIX

A. Deckbuild input file for IGZO Non-Fermi mobility model in Atlas

```
go atlas simflags="-P 8"

############## passivated BG Id-Vg curve with smart grid

#===========Set Variables=================

#sd workfunction
set workf=4.13

#----set temperature in kelvin
set temp=290

#-----------IGZO Thickness
set T=0.05
#---------Channel Length
set L=12
#---------S/D-gate Overlay
set OL=1
#--------Gate dielectric thickness
set BGI=0.05
#-------- Top gate dielectric thickness
set TGI=0.05



#---------- Gap in the channel where no additional defects (bulk/surface) are defined
#---------- setting this to "0" will make distribution uniform in channel (not below S/D)

set sourcegap=0
```

```
set midgap=0
set draingap=0

set sourcegapIT=0
set midgapIT=0
set draingapIT=0


#----------Conduction band tail slope , acceptor type wta
set cbtw=0.02
#----------Conduction band tail states , acceptor type nta
set cbtn=3.25e20

#----------- Valence band tail states ,donor type  ntd
set vbtn=1.55e20
#----------- Valence band tail slope ,donor type  wtd
set vbtw=0.12

#----------Density of Oxygen Vacancies (OV), donor type ngd
set nov=2e16
#------------Average energy of OV , donor  egd
set eov=2.9
#-----------Std Deviation of OV ,donor   wgd
set wov=0.1

# unpassivated region Vo ITs, acceptor like gaussian interface states
#----------Density of Interface OV, acceptor type nga
set novIT=0
#------------Average energy of Interface OV , acceptor  ega
set eovIT=3.05
#-----------Std Deviation of Interface OV ,acceptor   wga
set wovIT=0.5
```

```
# unpassivated region Vo ITs, donor like gaussian interface states
#----------Density of Interface OV, donor type ngd
set ndvIT=0
#------------Average energy of Interface OV , donor  egd
set edvIT=3.05
#-----------Std Deviation of Interface OV ,donor   wgd
set wdvIT=0.5

#adding acceptor like exp tail states in interface traps
set ntaIT=5e13
set wtaIT=0.07


# passivated gap region Vo ITs

#----------Density of Interface OV, donor type ngd
set gap_nov=1e20
#------------Average energy of Interface OV , donor  egd
set gap_eov=2.9
#-----------Std Deviation of Interface OV ,donor   wgd
set gap_wov=0.1

#----------Density of Interface OV, donor type ngd
set dgap_nov=1e20
#------------Average energy of Interface OV , donor  egd
set dgap_eov=2.9
#-----------Std Deviation of Interface OV ,donor   wgd
set dgap_wov=0.1



#----------Density of Interface OV, donor type ngd
set gap_novIT=0
```

```
#------------Average energy of Interface OV , donor  egd
set gap_eovIT=2.9
#-----------Std Deviation of Interface OV ,donor   wgd
set gap_wovIT=0.1

#---------- Fixed charges
set qf=5e10

#-----------Capture cross-section (default value 1e-15)
set sig=1e-15


## IGZO.TOKYO parameters--------------------
# IGZO.TOKYO mu0 of electron
set mue0=19
# IGZO.TOKYO Tgamma of electron
set tgm=0
# IGZO.TOKYO gamma0 of electron
set gm0=0
# IGZO.TOKYO critical carrier conc. of electron, does not matter since gamma0 and tgamma is
0
set necr=10e19

set nc_f=1.5
set nc=5e18
set mc=0.6


#====================================== mesh outf statement required, otherwise
wont run, specifies the format of output file, smart grid_rev1
mesh width=24 master.out

x.m l=0 s=0.1
```

```
x.m l=$"OL"/2 s=0.005
x.m l=$"OL" s=0.005
x.m l=$"OL"+0.2 s=0.005
#x.m l=$"OL"/2 s=0.0002
#x.m l=$"OL" s=0.0002
#x.m l=$"OL"+0.2 s=0.001
x.m l=1+$"L"/2 s=$"L"/20
x.m l=$"OL"+$"L"-0.2 s=0.005
x.m l=$"OL"+$"L" s=0.005
x.m l=1.5*$"OL"+$"L" s=0.1
x.m l=2*$"OL"+$"L" s=0.1
y.m l=0 s=0.01
y.m l=$"TGI" s=0.005
y.m l=$"TGI"+$"T" s=0.005
y.m l=$"TGI"+$"T"+$"BGI" s=0.01

#================Define IGZO====================
region num=1 material=igzo y.min=$"TGI" y.max=$"TGI"+$"T" x.min=$"OL"
x.max=$"OL"+$"L"
#================================================
region num=2 material=sio2 y.min=$"TGI"+$"T" y.max=$"TGI"+$"T"+$"BGI"
region num=3 material=sio2 y.max=$"TGI"

#elec num=1 name=gate bottom
elec num=1 name=gate y.min=$"TGI"+$"T"+$"BGI" y.max=$"TGI"+$"T"+$"BGI"
elec num=2 name=source y.min=$"TGI" y.max=$"TGI"+$"T" x.min=0.0  x.max=$"OL"
elec num=3 name=drain  y.min=$"TGI" y.max=$"TGI"+$"T" x.min=$"OL"+$"L"
x.max=2*$"OL"+$"L"



#==================Gate====================
```

```
contact num=1 workf=4.53
#============S/D Contacts===========
contact num=2 workf=$"workf"
contact num=3 workf=4.13


#models fermi print temp=$"temp"
models fermi temp=$temp print
output con.band val.band traps.ft

#===========Set IGZO Parameters==============
material region=1 material=igzo user.group=semiconductor user.default=silicon nc300=$nc
eg300=3.05 affinity=4.16 permittivity=10 mc=$mc nc.f=$nc_f

# IGZO parameters
# IGZO.TOKYO mobility model
mobility igzo.tokyo mun=$mue0 mup=0.01 tmun=0 tmup=0 \
                igzo.gamma0=$gm0 igzo.tgamma=$tgm igzo.ncrit=$necr

#====================Defects=========================
################ Bulk defects
defects x.min=$"OL"+$"sourcegap" x.max=$"OL"+$"L"-$"draingap" nta=$"cbtn" wta=$"cbtw"
ntd=$"vbtn" wtd=$"vbtw" \
                nga=0 ega=0 wga=0 ngd=$"nov" egd=$"eov" wgd=$"wov" \
                sigtae=$"sig" sigtah=$"sig" sigtde=$"sig" sigtdh=$"sig" \
                siggae=$"sig" siggah=$"sig" siggde=$"sig" siggdh=$"sig" \
                numa=128 numd=64

#tfile=defects_bulk.dat


# sourcegap defects
```

```
defects x.min=$"OL" x.max=$"OL"+$"sourcegap" nta=$"cbtn" wta=$"cbtw" ntd=$"vbtn" wtd=$"vbtw" \
        nga=0.0 ngd=$"gap_nov" egd=$"gap_eov" wgd=$"gap_wov" \
        sigtae=$"sig" sigtah=$"sig" sigtde=$"sig" sigtdh=$"sig" \
        siggae=$"sig" siggah=$"sig" siggde=$"sig" siggdh=$"sig" \
        numa=64 numd=32

# draingap defects

defects x.min=$"OL"+$"L"-$"draingap" x.max=$"OL"+$"L" nta=$"cbtn" wta=$"cbtw" ntd=$"vbtn" wtd=$"vbtw" \
        nga=0.0 ngd=$"dgap_nov" egd=$"dgap_eov" wgd=$"dgap_wov" \
        sigtae=$"sig" sigtah=$"sig" sigtde=$"sig" sigtdh=$"sig" \
        siggae=$"sig" siggah=$"sig" siggde=$"sig" siggdh=$"sig" \
        numa=64 numd=32

########## Defects at the IGZO/PM interface

intdefects x.min=$"OL" x.max=$"OL"+$"sourcegapIT" nta=0 ntd=0 wta=0.013 wtd=0.12 \
        nga=0.0 ngd=$"gap_novIT" egd=$"gap_eovIT" wgd=$"gap_wovIT" \
        sigtae=$"sig" sigtah=$"sig" sigtde=$"sig" sigtdh=$"sig" \
        siggae=$"sig" siggah=$"sig" siggde=$"sig" siggdh=$"sig" \
        numa=64 numd=32

# From sourcegap to midgap (BT states & Vo ITs)

intdefects y.min=$"TGI" y.max=$"TGI" x.min=$"OL"+$"sourcegapIT" x.max=$"OL"+$"L"/2-$"midgapIT"/2 nta=$"ntaIT" ntd=$"ntdIT" wta=$"wtaIT" wtd=$"wtdIT" \
        ngd=$"ndvIT" egd=$"edvIT" wgd=$"wdvIT"  nga=$"novIT" ega=$"eovIT" wga=$"wovIT" \
        sigtae=$"sig" sigtah=$"sig" sigtde=$"sig" sigtdh=$"sig" \
        siggae=$"sig" siggah=$"sig" siggde=$"sig" siggdh=$"sig" \
        numa=64 numd=32
```

```
# Inside midgap (BT states)

intdefects y.min=$"TGI" y.max=$"TGI" x.min=$"OL"+$"L"/2-$"midgapIT"/2
x.max=$"OL"+$"L"/2+$"midgapIT"/2 nta=0 ntd=0 wta=0.013 wtd=0.12 \
        nga=0.0 ngd=$"gap_novIT" egd=$"gap_eovIT" wgd=$"gap_wovIT" \
        sigtae=$"sig" sigtah=$"sig" sigtde=$"sig" sigtdh=$"sig" \
        siggae=$"sig" siggah=$"sig" siggde=$"sig" siggdh=$"sig" \
        numa=64 numd=32

# From midgap to draingap (BT states & Vo ITs)

intdefects y.min=$"TGI" y.max=$"TGI" x.min=$"OL"+$"L"/2+$"midgapIT"/2
x.max=$"OL"+$"L"-$"draingapIT" nta=$"ntaIT" ntd=$"ntdIT" wta=$"wtaIT" wtd=$"wtdIT" \
        ngd=$"ndvIT" egd=$"edvIT" wgd=$"wdvIT" nga=$"novIT" ega=$"eovIT"
wga=$"wovIT" \
        sigtae=$"sig" sigtah=$"sig" sigtde=$"sig" sigtdh=$"sig" \
        siggae=$"sig" siggah=$"sig" siggde=$"sig" siggdh=$"sig" \
        numa=64 numd=32

# Inside draingap (BT states)

intdefects y.min=$"TGI" y.max=$"TGI" x.min=$"OL"+$"L"-$"draingapIT"
x.max=$"OL"+$"L" nta=0 ntd=0 wta=0.013 wtd=0.12 \
        nga=0.0 ngd=$"gap_novIT" egd=$"gap_eovIT" wgd=$"gap_wovIT" \
        sigtae=$"sig" sigtah=$"sig" sigtde=$"sig" sigtdh=$"sig" \
        siggae=$"sig" siggah=$"sig" siggde=$"sig" siggdh=$"sig" \
        numa=64 numd=32

#tfile=BG-defects_qf=$"qf"_intdef=$"novIT"_$"eovIT"_$"wovIT".dat


#inttrap donor y.min=$"TGI" y.max=$"TGI" x.min=$"OL" x.max=$"OL"+$"L"/2-$"gap"/2
e.level=$"elevelIT" density=$"denIT" degen=1 sign=$"sig" sigp=$"sig"
```

#inttrap donor y.min=$"TGI" y.max=$"TGI" x.min=$"OL"+$"L"/2+$"gap"/2 x.max=$"OL"+$"L" e.level=$"elevelIT" density=$"denIT" degen=1 sign=$"sig" sigp=$"sig"

############ Fixed charge at the GI/IGZO interface presumably created during sputtering, located in the front channel

interface y.min=$"TGI"+$"T" y.max=$"TGI"+$"T" qf=$"qf"

method autonr climit=1e-4 carrier=1 electron

#======================== Id-Vg===========================

solve init

save outfile=BG_Vd=0_Lin_$"L"_$"temp"k_$"workf"_$"cbtn"_$"cbtw"_$"qf"_ae_$"ntaIT"_$"wtaIT"_mu0_$"mue0"_nc_$"nc"_m_$"mc".str

solve vdrain=0.1

save outfile=BG_Vd=0pt1_Lin_$"L"_$"temp"k_$"workf"_$"cbtn"_$"cbtw"_$"qf"_ae_$"ntaIT"_$"wtaIT"_mu0_$"mue0"_nc_$"nc"_m_$"mc".str

solve vgate=0 vstep=0.5 vfinal=10 name=gate

log outf=Lin_$"L"_$"temp"k_$"workf"_$"cbtn"_$"cbtw"_$"qf"_ae_$"ntaIT"_$"wtaIT"_mu0_$"mue0"_nc_$"nc"_m_$"mc".log

solve vgate=10 vstep=-0.1 vfinal=-5 name=gate

log off

solve init

solve vdrain=0.1

solve vdrain=0.2

solve vdrain=1

solve vdrain=2

solve vdrain=3

solve vdrain=5

solve vdrain=10

save outfile=BG-V$"L"_$"temp"k_$"workf"_$"cbtn"_$"cbtw"_$"qf"_$"mue0"_ag_$"novIT"_$"wovIT"_$"eovIT"_ae_$"ntaIT"_$"wtaIT"_dg_$"ndvIT"_$"wdvIT"_$"edvIT"_de_$"ntdIT"_$"wtdIT"_m_$"me"_n_$"nt"_e_$"et"_a_$"acc"_o_$"omega".str

solve vgate=0 vstep=0.5 vfinal=10 name=gate

log outf=BG-Sat-$"L"_$"temp"k_$"workf"_$"cbtn"_$"cbtw"_$"qf"_ag_$"novIT"_$"wovIT"_$"eovIT"_ae_$"ntaIT"_$"wtaIT"_dg_$"ndvIT"_$"wdvIT"_$"edvIT"_de_$"ntdIT"_$"wtdIT"_m_$"me"_n_$"nt"_e_$"et"_a_$"acc"_o_$"omega"_mu_$"mue0".log

solve vgate=10 vstep=-0.1 vfinal=-5 name=gate

log off

quit