Simulation and Tolerance Determination for Lateral DMOS Devices

Matthew Scarpino
Microelectronic Engineering
Rochester Institute of Technology
Rochester, NY 14623

Abstract - SUPREM4 simulation for lateral DMOSFET's are discussed, as well as the Medici simulation of their electrical characteristics. The actual processing parameters of the device simulation are shown, and the theory surrounding device operation is discussed. The three electrical tests – I_D/V_{DS} characteristic, V_T determination, and the breakdown V_{DS} are explained with the testing method used for each. The four process variations – substrate doping, well dose, well drive in temperature, and oxidation temperature are presented as well as their theoretical effects on device performance. Finally, the results of the electrical tests are presented with conclusions regarding the effects of the mentioned process alterations on device performance.

I. INTRODUCTION

The requirement for more reliable power transistors has led to the need for device simulation, and the use of simulation to determine which processing parameters affect device performance the most. This paper discusses the simulation and testing of an example DMOS device for a number of varying process parameters.

The name DMOS refers to the MOSFET processing step in which the source and body contact are diffused simultaneously, yielding a Double-diffused MOSFET. Because they require low on-state voltage, adapt well to higher-level integrated processes, and manifest superior switching capability, they are used in many applications normally attributed to bipolar junction transistors (Efland, 10). Further, these devices can handle large voltages across the drain/source terminals while flowing up to 50 A of current. As a results, DMOSFETs are used in power arrays that form the basis of intelligent power integrated circuits (Marshall, 5). This device technology has found multiple applications in industry, including motor controllers in automobiles, printer heads, and solenoid drivers (Marshall, 7).

SUPREM4 software is used to simulate the DMOS device. Created by Technology Modeling Association, it is used to create a two-dimensional model of a device based on input process steps. This experiment used thirteen different files (regi1.inp to regi13.inp – see Appendix A) to simulate the device. This was done to prevent significant loading of the simulating computer, which has a tendency to shut down if given too many equations at once. These processes begin with a GRID statement, in which the semiconductor region is laid out. SUPREM4 simulates a large region by breaking it up into small regions shaped like triangles. With the GRID statement, it is possible to determine the size of the triangles in a certain area, and therefore the degree of precision of calculation in an area. The grid used in this simulation is shown in Appendix A. Once the grid has been determined and the nature of the original silicon substrate is programmed, a series of standard microelectronic processes such as DIFFUSION, DEPOSITION, IMPLANT, and ETCH are used to detail the fabrication of the device. A cross-section of the final device is shown in Figure 1.

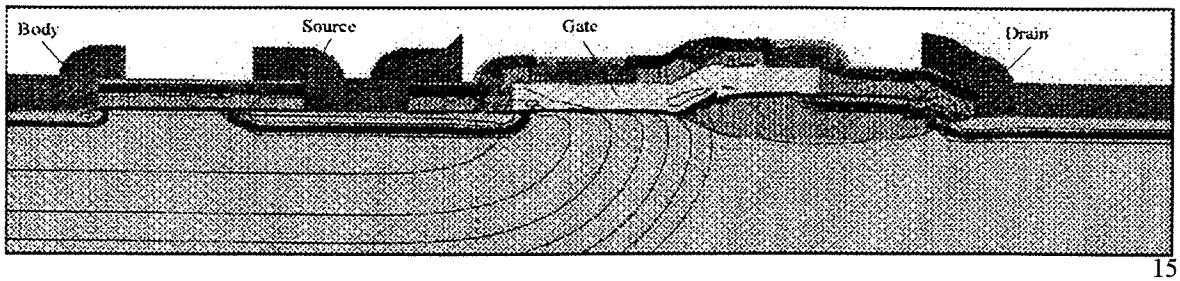


Figure 1: Cross-Section of DMOS Device

Medici, also created by Technology Modeling Association, is used to determine the electrical characteristics of the device simulated in SUPREM4. Similar to the GRID statement in SUPREM4, Medici bases the structure to be tested on a MESH statement. This mesh may be obtained from a file (.med) created by SUPREM4 as long as the electrodes of the device has been determined and programmed. With the mesh created in Medici, it is possible to apply voltages and currents to the electrodes specified in the .med file. Medici uses these electrical inputs and calculates their effects on the various triangles within the region. Medici determines the effects of these triangles on the device's electrodes, and solves for the output electrical performance of the DMOS device.

Specifically, the electrical tests performed by Medici determine characteristics necessary to the understanding of the device's performance. The first characteristic measured by Medici involves the relationship between the drain current and the drain-to-source voltage. This is the most necessary characteristic in nearly any MOSFET, as this determines how the device may be used in a circuit. It is determined in Medici by setting a gate voltage above the threshold value, increasing the drain/source voltage, and measuring the current flowing through the drain. The next test, determining the threshold voltage, allows for an understanding of what gate voltage is necessary to turn on the device, as well as the ability of the drain/source voltage to control current. It is determined by setting a small voltage across the channel, increasing the gate voltage, and calculating the amount of current flowing through the device. The third test involves the breakdown voltage of the DMOS. Breakdown, in this paper, is said to occur when more than 1% of the atoms within the DMOS channel become ionized. Medici determines this by grounding the DMOS gate, increasing the voltage between the drain and source, and calculating the atom ionization within the channel.

II. MODEL AND ANALYSIS

To appreciate the results obtained through the process variations, it is important to understand the theory behind MOSFET operation.

A. Derivation of the Threshold Voltage Equation (Pierret, 44)

The applied gate voltage, $V_G = \phi_s + \phi_{ox}$, (1)
where ϕ_s represents the silicon potential and ϕ_{ox} denotes the oxide potential.

Since the electric field is constant throughout an insulator, $\phi_{ox} = x_0 E_{ox}$ (2)
where x_0 is the oxide thickness and E_{ox} represents the field in the oxide.

Since $E_{ox} = (K_s/K_o)E_S$, substitution into (1) yields
$V_G = \phi_s + (K_s/K_o)x_0 E_S$, (3)
where K_s and K_o represent the dielectric constants for silicon and oxide.

Because $E_{ox} = \sqrt{\frac{2qN_A\phi_s}{K_S\varepsilon_0}}$,

$$V_G = \phi_s + (K_s/K_o)\sqrt{\frac{2qN_A\phi_s}{K_S\varepsilon_0}}\,x_0 \qquad (4)$$

where N_A is the number of donor ions in the well and ε_0 is the permittivity of free space.

Since ϕ_s equals $2\phi_f$ when the device turns on,

$$V_T = 2\phi_f + (K_s/K_o)\sqrt{\frac{4qN_A\phi_f}{K_S\varepsilon_0}}\,x_0 \qquad (5)$$

From (5), we see that the threshold voltage increases with the thickness of the oxide, and with the square root of the well dopant.

While (5) relates the threshold voltage to physical characteristics, a simpler method is used in this experiment. As the gate voltage increases, the current characteristic begins to develop a linear relationship with V_G. For sake of simplicity, the threshold voltage is defined as the voltage at which the current develops linearity. This value is determined by graphical extrapolation, in which a line is drawn from the current characteristic onto the x-axis. As examples, see Figure 2.

B. Derivation of the Current/Voltage Relationship (Pierret, 74)

From the minority carrier diffusion equations, the electron current, $J_N = -q\mu_n nE$ (6)
where μ_n is the electron mobility and n is the electron density.

The drain current may then be found by solving the equation,

$$I_D = -\iint J_N dxdz = -Z\frac{d\phi}{dy}\int \mu_n n dx \qquad (7)$$

where μ_n is the electron mobility and Z is the device width.

Setting Q_N equal to the total charge in the channel,

$$I_D = - Z\mu_n \int_0^{V_d} Q_N d\phi \qquad (8)$$

The total charge in the channel is given by

$$Q_N = - C_0(V_G - V_T), \qquad (9)$$

where C_0 is the capacitance of the oxide.

Replacing (9) into (8) and integrating, the current through the MOSFET is given by

$$I_D = \frac{Z\mu_n C_0}{L}[(V_G - V_T)V_D - \frac{V_D^2}{2}]. \qquad (10)$$

Since μ_n drops with increased doping, (10) shows that the current decreases with increased well doping. Further, since C_0 decreases with increased oxide thickness, the drain current also decreases with increased oxide thickness.

III. RESULTS AND DISCUSSION

A. Process Variation Effect on Current/Voltage Characteristic

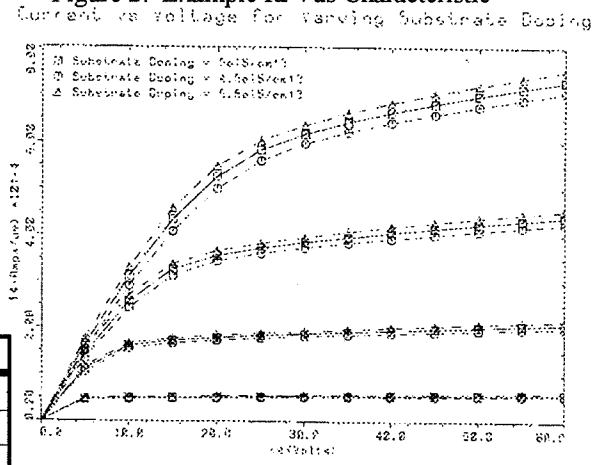
With voltages applied from zero to sixty volts and applied gate voltages of 4,6, 8, and 10 V, the graphs obtained are shown in Appendix B. Table I relates the various process changes to the current with the gate voltage set at 8 V. The "no change" process description refers to the original DMOS device, without process variation. The percentage change is shown to depict the relative difference of each process variation's current from that involving "no change".

Table I: EFFECT OF PROCESS VARIATION ON OUTPUT CURRENT

Process Description	Current - mA/um	% Change
No Change	0.44	--
Sub. Doping - 4.5e13	0.43	2.27%
Sub. Doping - 5.5e13	0.45	2.27%
Well Dose - 4.5e13	0.48	9.09%
Well Dose - 5.5e13	0.44	0.00%
Drive in Temp - 20	0.52	18.18%
Drive in Temp + 20	0.36	18.18%
Oxidation Temp - 20	0.3	31.82%
Oxidation Temp + 20	0.31	29.55%

On average, the process variation with the greatest effect on output current is the oxidation temperature. This agrees with theory, as the temperature determines the thickness of the oxide. Increased oxide thickness, in turn, reduces the effect of gate voltage on the channel, thereby reducing the amount of inversion within the channel. The temperature at which the well dopants are driven in also has a large effect on the output current, as the drive in step changes dopant concentration throughout the channel, thereby altering the channel's conductivity. The amount of the well dose, though, does not affect the current characteristic to the degree that temperature alteration does. However, it is apparent from Table I that reducing the well dose has a much greater effect than increasing the dose. This implies that the relationship between current and well dose is non-linear, and that the reduction in mobility associated with an increase in dose reduces the gain caused by an increased number of charges. Finally, substrate doping has the least effect on output current. This is because the well doping is sufficiently large to reduce the effect of substrate doping on the electrical characteristics of the channel.

Figure 2: Example Id/Vds Characteristic



B. Process Variation Effect on Threshold Voltage

With gate voltages applied from zero to two volts and an applied drain-source voltage of .2 V, the graphs obtained are shown in Appendix B. Table II relates the various process changes to the extrapolated threshold voltages. The "no change" process description refers to the original DMOS device, without process variation. The percentage change is shown to depict the relative difference of each process variation's threshold voltage from that involving "no change".

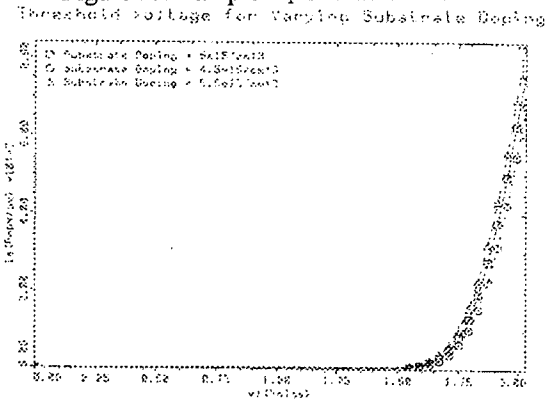
Table II: EFFECT OF PROCESS VARIATION ON THRESHOLD VOLTAGE

Process Description	Vt (V)	% Change
No Change	1.8	--
Sub. Doping - 4.5e13	1.76	2.22%
Sub. Doping - 5.5e13	1.82	1.11%
Well Dose - 4.5e13	1.85	2.78%
Well Dose - 5.5e13	1.92	6.67%
Drive in Temp - 10	1.75	2.78%
Drive in Temp + 10	1.83	1.67%
Oxidation Temp - 10	1.61	10.56%
Oxidation Temp + 10	1.9	5.56%

Similarly to the effects on drain current, variations in oxidation temperature make the greatest difference in altering the performance of the MOSFET. This corresponds to theory, as threshold voltage increases linearly with increases in oxide thickness. The well dose plays the next most important role in determining threshold voltage. This is because the well dose determines N_A, which is present under the radical in the equation for threshold voltage. Similarly, N_A is influenced by the degree to which the applied dose is driven in – a large temperature drive in reduces the well dopants at the surface of the silicon, and makes the channel harder to invert. Finally, the substrate doping makes the least difference in changing the DMOS performance for the same reason that it did not affect the current characteristic significantly – its effect on the channel impurity concentration is negligible in the face of all of the well dopants present.

Another feature worth noting is the lack of linearity throughout the table. In no case do the two sides of a specific parameter variation cause similar deviations from the nominal threshold voltage. Theoretically, this is understandable for the doping, dose, and drive in, but according to (5), there should be something of a linear relationship between threshold voltage and gate thickness. This implies that the imprecise manner of threshold voltage extrapolation does not yield sufficiently accurate results.

Figure 3: Example V_T Characteristic



C. Process Variation Effect on Breakdown Voltage

With drain voltages applied from zero to twenty volts and a grounded gate, the results are shown in Table III. This table relates the various process changes to the breakdown voltages. The "no change" process description refers to the original DMOS device, without process variation. The percentage change is shown to depict the relative difference of each process variation's breakdown voltage from that involving "no change".

Table III: EFFECT OF PROCESS VARIATION ON BREAKDOWN VOLTAGE

Process Description	Vbd (V)	% Change
No Change	17.8	--
Sub. Doping - 4.5e13	16.6	6.74%
Sub. Doping - 5.5e13	19.2	7.87%
Well Dose - 4.5e13	17.2	3.37%
Well Dose - 5.5e13	18	1.12%
Drive in Temp - 20	16.6	6.74%
Drive in Temp + 20	20.8	16.85%
Oxidation Temp - 20	16.8	5.62%
Oxidation Temp + 20	19	6.74%

In this case, the drive in temperature and the substrate doping play the greatest roles in determining the breakdown voltage. This is due to the fact that breakdown voltage is determined by the conductivity of the substrate seen by the drain. This can easily be altered by changes in the substrate doping or the well drive in. It must be kept in mind that the breakdown voltage was determined by finding the drain voltage at which electron ionization rises above 1 percent.

These results are essentially inexplicable. The effect of oxidation temperature should not have a larger effect on breakdown than the well dose. The only explanation involves the possibility that the oxidation step worked as a second drive in step, and that the well profile was significantly altered during oxidation.

IV. CONCLUSIONS

As seen from Figures 2 and 3, the output characteristics obtained from the DMOS device are similar in shape to those obtained from a normal MOSFET. This implies that the device works as a proper transistor, and that the process yields a working device.

The results from the current test correspond essentially to theory. The gate oxidation temperature played the largest role of the parameters varied due to the reduced inversion of the channel. Well drive in played the second largest role, as it changes the mobility and resistivity of the channel. Well dose came in third, due to its secondary ability to change channel mobility and resistivity. Finally, the substrate doping parameter made the least difference in current performance, as its channel effects were inconsequential compared to those of the dose and drive in.

The results from the threshold voltage also agreed with theoretical determinations. Again, gate oxidation temperature affected threshold voltage the most, and the substrate doping affected it least. Both the well dose and the drive in were in-between, as they altered the ability of the gate voltage to invert the underlying channel.

No real explanation can be found for the strange results regarding breakdown voltage. To begin with, the breakdown voltage for a DMOS should be much larger to prevent leaking with smaller drain voltages. While it is understandable that the substrate doping and drive in affected the voltage to the degree that they did, it is nearly inexplicable that the oxidation temperature should affect breakdown voltage more than well dose.

In the future, it would be useful to alter other parameters within the process, such as other oxidations and diffusions. It would also be useful to change the parameters in this experiment to a greater or lesser degree. Finally, it might be informative to use SUPREM4 with a greater number of triangles, and obtain a more accurate sense of the electrical characteristics of the device.

V. REFERENCES

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