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SYSTEM DESIGN OF HYBRID 350W AUDIO RECEIVER AND AMPLIFIER

by

MATTHEW SEGADA

GRADUATE PAPER

Submitted in partial fulfillment
of the requirements for the degree of
MASTER OF SCIENCE
in Electrical Engineering

Approved by:

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ROCHESTER INSTITUTE OF TECHNOLOGY
ROCHESTER, NEW YORK

DECEMBER, 2021

Dedication

I would like to dedicate this to my parents for their outstanding support for me, and my brother and sister for their guidance in my journey through life.

Declaration

I hereby declare that except where specific reference is made to the work of others, that all content of this Graduate Paper are original and have not been submitted in whole or in part for consideration for any other degree or qualification in this, or any other University. This Graduate Project is the result of my own work and includes nothing which is the outcome of work done in collaboration, except where specifically indicated in the text.

Matthew Segada

December, 2021

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Abstract

Music, for thousands of years, has been at the center of social and cultural aspects to convey emotions and stories to a vast audience. In the modern world, the usage of digital audio has been the main method of consuming music; however, the method in which the translation of a digital audio signal to the analog realm is taken for granted. In this paper, a audio receiver was designed to accept a USB audio signal from any digital source and output an audio signal for headphones or speakers. The receiver was designed to output a maximum of 350W into speakers and 7W into headphones.

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Chapter 1

Introduction

1.1 Project Goals

The goal of this project is to emulate the typical design process of an audio amplifier from the design to the working prototype stage. Additionally, the amplifier needs to be safe to use from a typical wall outlet and pose no risk to the user. While modern designs of amplifiers have used completely IC-based analog chains, a look-to-the-past of vacuum tube amplifier design was utilized to bring a retro aspect to a modern design. Some of the aspects needed to complete the design of the amplifier and prototype are as follows:

- Vacuum tube design
- Operational amplifier based filter design
- Knowledge of AC/DC rectification
- Knowledge of high voltage & high current power supplies
- Printed circuit board schematic and layout capture

1.2 Organization

The following is the organization for the rest of the paper:

- Chapter 2: System-Level Architecture - Block level diagram of the entire system and how each piece fits together
- Chapter 3: Digital-to-Analog Converter Overview - Background on how a DAC works and why they are necessary
- Chapter 4: Vacuum Tube Preamplifier - Background on vacuum tubes, how they work, and how to design a preamplifier using them
- Chapter 5: Analog Based Audio Filters - Background on filters and why they are necessary. Additionally, the method of designing such filters will be described for a 60 Hz notch, low pass, and graphic equalizer filters.
- Chapter 6: Amplifier Overview - Background on the operational amplifier and class D amplifiers and design
- Chapter 7: Power Supply Design - Discussion of AC/DC rectification, power supply safety, and design
- Chapter 8: Conclusion

Chapter 2

System-Level Architecture

2.1 Audio Signal Path Top Level Design

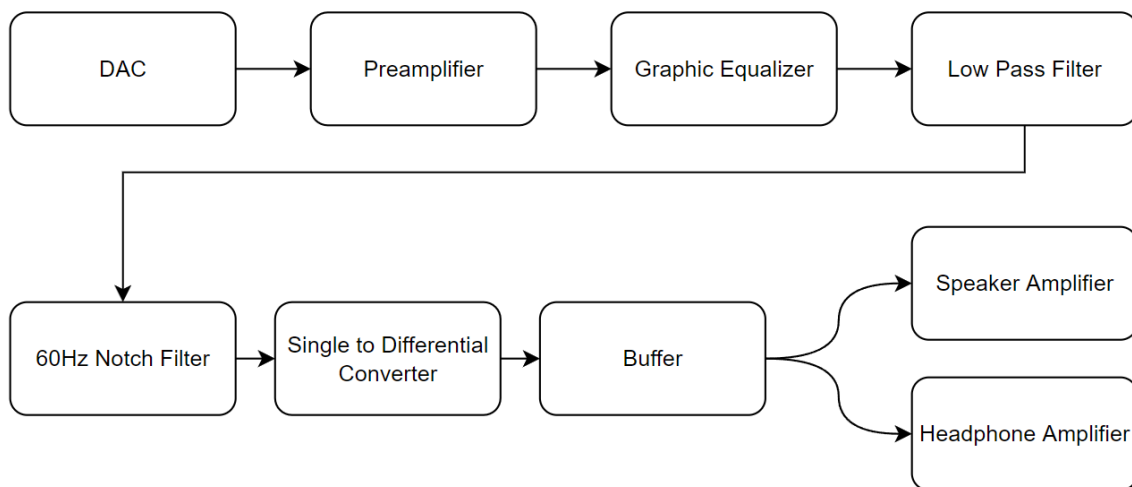


Figure 2.1: Top Level Block Diagram

For the signal flow path of the audio signal, the top-level diagram is shown in Fig. 2.1. The host PC (not pictured) will send a USB 2.0 audio signal to the digital-to-analog converter (DAC). The DAC's purpose is twofold: it is to terminate the USB signal and to convert the

digital signal into an analog one, such that further processing can be completed. In most amplifiers, this is generally done by two integrated circuits (ICs). There is one IC that will take the incoming USB signal and terminate it into, generally, an I2C or SPI to send to the DAC (the other IC). In the case of this design, the PCM2704C from Texas Instruments combines both ICs into one for a convenient solution [13]. The maximum output signal from the DAC, for the left and right channels, is approximately $0.55 V_{CCx}$ (where x is the left or right channel). The nominal voltage of the voltage supply lines are 3.3 V; therefore, the maximum output voltage is calculated to be $0.55 \cdot 3.3 \text{ V} = 1.815 \text{ V}_{PP}$.

After the analog signal comes out of the DAC, the audio signal is fairly low power and is not suitable for outputting directly to speakers. The PCM2704C is able to drive low power headphones; however, it is not suitable for 350W speakers, nor audiophile type headphones. While this signal could directly bypass the preamplifier and go directly into the next stages, vacuum tubes provide a different frequency response that is warmer in tone [14]. The use of such a preamplifier was only due to its affect on the sound. However, by using a preamplifier, there is an associated gain with the stage; as such, the input into the preamplifier must be considered as to not exceed the input voltage limits on the rest of the analog audio chain. To do this, a resistor divider was put at the output of the DAC section and before the input of the preamplifier. This brought down the incoming input signal to a maximum of 113 mV_{PP} . The preamplifier stage that was utilized has a gain of 51 V/V or 34 dB . Which can then be used to calculate the output voltage:

$$\begin{aligned} \text{Gain} &= 20\log_{10}\left(\frac{V}{V_0}\right) \\ 34 &= 20\log_{10}\left(\frac{V}{0.113}\right) \\ 34/20 &= \log_{10}\left(\frac{V}{0.113}\right) \\ 10^{34/20} &= \frac{V}{0.113} \\ V &= 5.663 \end{aligned}$$

Both the speaker and headphone amplifiers can accept this input voltage, so it is an acceptable output voltage for the preamplifier [13, 15]. After the preamplifier, the audio signal is fed into the graphic equalizer, whose purpose is to either provide gain or attenuation for a specific frequency band of the audio signal. In this specific implementation, there are a total of 7 frequency bands to choose from. It is called a graphic equalizer, because the use of sliding potentiometer, or faders, and the position of the faders will give a rough estimate of the frequency response curve. The low pass filter is to attenuate any high frequency content that could cause harmonics to show up in the audible range. Additionally, due to the presence of 120 V_{AC} mains on the board, there will be the presence of 60Hz noise on the board as well. To get rid of this, a notch filter is designed to attenuate any frequency content around 60Hz. These filters are placed before the amplifiers, such that the filters do not have to be able to handle high power (or voltage) inputs.

In the case of the audio amplifiers, both the TPA3251 and TPA6120 utilize a differential input signal (however they can run off of a single ended input). The main reason for the differential input is to reduce any noise picked up from the audio signal path[16]. To reduce any cause for interference between the speaker and headphone amplifiers, they are isolated

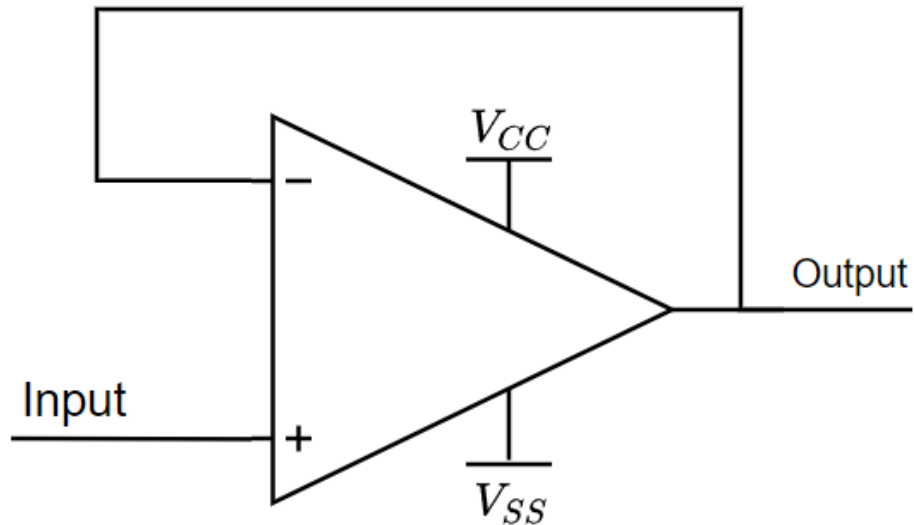


Figure 2.2: Operational Amplifier Voltage Follower Configuration

by a buffer stage. This buffer stage is comprised of 8 operational amplifiers setup in a voltage follower configuration, this is shown in Fig. 2.2. There are 8 total buffers as each amplifier gets its own set of 4 buffers, of which 2 buffers are dedicated for either the left or right channel's differential pair.

As headphones and speakers require different amounts of power, the amplifiers utilized for each output must be different. For the speaker output, the TPA3251, a high power 350W class D amplifier, is used; while for the headphone amplifier, the TPA6120, which is based on an operational amplifier design, is used. The TPA3251 was chosen due to its highly efficient nature, meaning that the amplifier consumes very little power for the amount of output power. In the case of the TPA3251, it can be up to 94% efficient [15]. The TPA6120 was chosen due to it being a headphone based operational amplifier solution, it can drive up to 700mA at ± 15 V. While this is way more than enough power for most headphones and would most likely cause most headphone drivers to explode, more is always better - a common theme of the project.

2.2 Power Supply Top Level Design

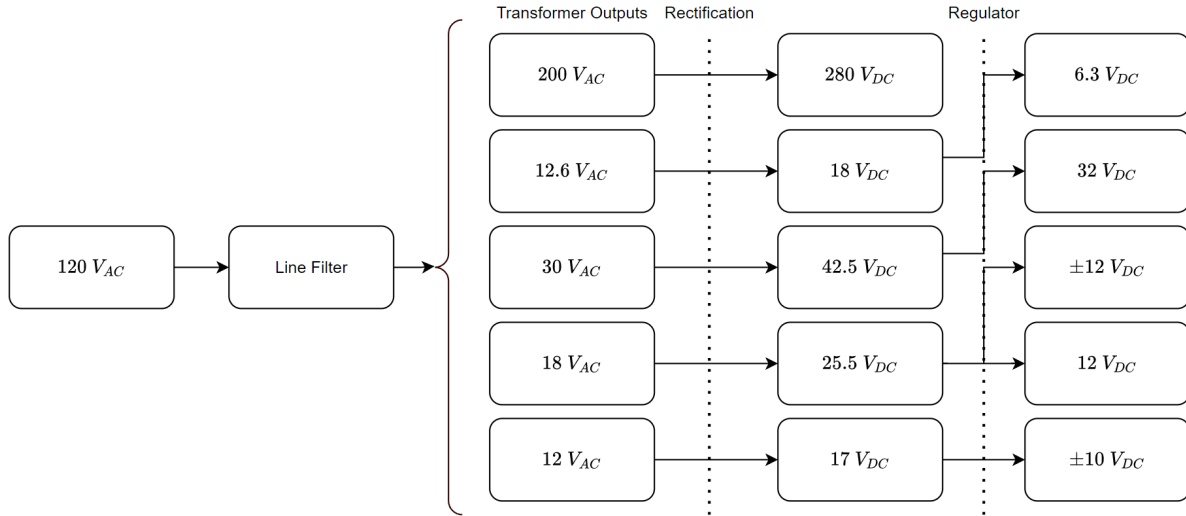


Figure 2.3: Top Level Power Supply

As the amplifier has many different voltage domains with varying current demands, a power delivery system needed to be built to supply each power rail. In the case of this project, it would have probably been easier to buy a commercial-off-the-shelf high power AC/DC converter; however, it was a goal to design the entirety of the power supply. As such, the naturally noisy $120 V_{AC}$ line input needed to be filtered; this is done by a purpose built line filter which eliminates common and differential mode noise [17]. After the line filter, the output is fed into two transformers; one transformer is specifically for vacuum tubes and the other is a high power transformer. The vacuum tube transformer has a total of 4 outputs, two $200 V_{AC}$ outputs and two $6.3 V_{AC}$ outputs. While not necessary, the $200 V_{AC}$ outputs are put into a parallel configuration to give twice the total output current of one secondary winding. However, the $6.3 V_{AC}$ outputs are put into a series configuration to give a total of $12.6 V_{AC}$. The $200 V_{AC}$ output is then rectified, which turns into $280 V_{DC}$. The $12.6 V_{AC}$ after rectification turns into $18 V_{DC}$; which is too high of a voltage to feed into the vacuum tubes. This is then sent through

a series of regulators to bring down the voltage to $6.3 V_{DC}$.

In the case of the high power transformer, there are 3 outputs: $30 V_{AC}$, $18 V_{AC}$, $12 V_{AC}$ - there are 2 $30 V_{AC}$ outputs. These are each rectified and after rectification their respective voltages are as follows, $42.5 V_{DC}$, $25.5 V_{DC}$, $17 V_{DC}$. Each of these outputs are then fed into a series of regulators, the $32 V_{DC}$ is utilized for the TPA3251 speaker amplifier. This output can supply 13 A per $30 V_{AC}$ output but with paralleled outputs, this can supply a maximum of 26 A [18]. The $18 V_{AC}$ output is rectified to $25.5 V_{DC}$ which is then utilized for a low noise $\pm 12 V_{DC}$ for the operational amplifier supplies and a $12 V_{DC}$ output for supplying a potential fan and the digital portion of the TPA3251. The $12 V_{AC}$ is rectified into $17 V_{AC}$, which is regulated to $\pm 10 V_{DC}$ for a high power-low noise output for the headphone amplifier supply.

Chapter 3

Digital-to-Analog Converter Overview

The digital to analog converter is utilized to take the incoming USB 2.0 differential signal from a host device and convert it into an analog audio signal. A PCM2704C was used for this task. The main reason that this specific DAC was used, was that it combined the USB interface into the DAC - something that most other DACs do not offer. This additionally allows the PCM2704C to interface with the host PC and display information about the device. Utilizing an EEPROM, the overall audio receiver can have the make and model displayed to the host device - while it is not a necessary feature, it adds to the overall fit and finish of the receiver. Additionally, the DAC has the ability to have buttons connected such that the user can either increase or decrease the volume, or mute the audio all together.

As the DAC is powered from the USB 5 V bus, there is no negative rail. To get around this, the audio signal is biased to 1.65 V [13] and then passed through a DC blocking capacitor to remove the offset. Additionally, due to the DAC utilizing oversampling, there is the requirement to have an analog low pass filter on the output signal path of the DAC. This allows for any high frequency aliases to be attenuated, so they do not appear in the final output.

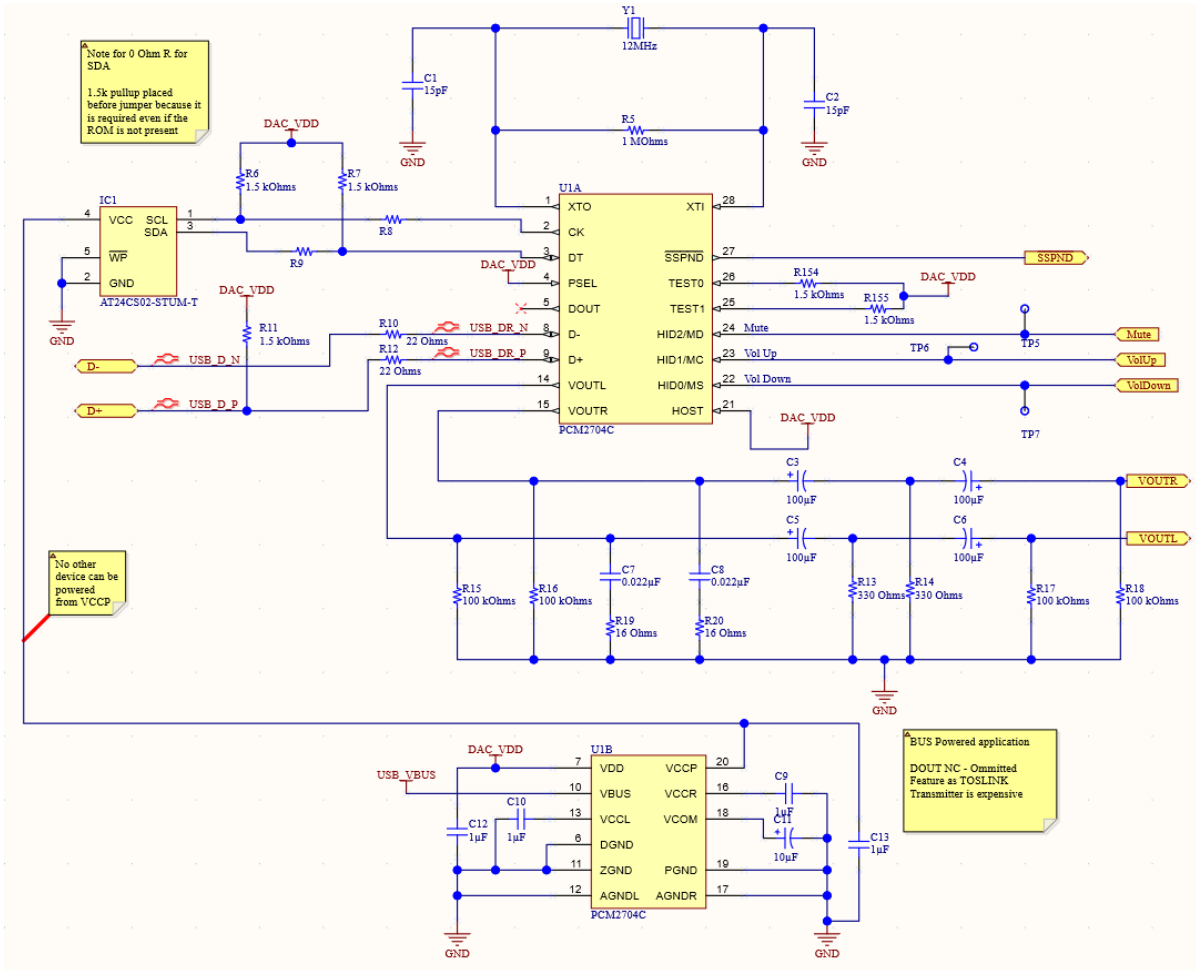


Figure 3.1: Digital to Analog Converter Schematic

Chapter 4

Vacuum Tube Preamplifier

4.1 How does a Vacuum Tube Work?

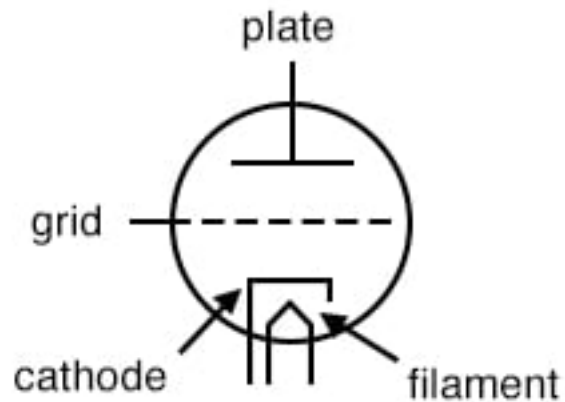


Figure 4.1: Triode Vacuum Tube Symbol [1]

In the specific case of a preamplifier, the vacuum tubes that are being dealt with are specifically called triode tubes. Triode refers to the amount of signal connections the vacuum tube has; in the case of the triode, it has 3 connections. These three connections are the plate

(anode), grid, and cathode. There is an additional connection for the heater filament. These connections are shown in Fig. 4.1. The cathode is the negative terminal of the tube, and as such is the source for electrons. As the heater filament heats up, the cathode “boils” off electrons into vacuum present inside of the tube, hence “vacuum” tube. These electrons are launched towards the positively charged plate; however, the grid can impede the flow of these electrons. The grid, which as it is kept at a voltage below the cathode voltage, will impede the flow of electrons from the cathode to plate, as like charges repel one another. This effectively modulates the grid input onto a larger voltage range, *i.e.* amplifies the signal.

4.2 Vacuum Tube Preamplifier Design

The preamplifier is based off of a 12AX7 tube, specifically the JJ ECC83s vacuum tube, which is a preamp specific tube. The 12AX7 is considered a miniature dual triode tube, which means that it is essentially two tubes in one. It has two different plates, grids, and cathodes - only the heater is shared. The design of the preamplifier is heavily based off of a design from Shine7 [19]. One of the main differences in their implementation and the one presented is the use of a 280 V plate voltage instead of the 300 V presented on the website. This was done primarily because most of the 12AX7 data sheets stated that the maximum voltage allowed on the plate was around 300 V. To be safe, the lower voltage was used.

To first design the preamplifier, the plate characteristic chart must be considered for the appropriate operating point. In Shine7’s design, the destined grid voltage was $U_g = -1$ V. This was picked as it allows for a very linear operating region of the tube. Additionally, the destined value for the plate current (I_a) is 1.4 mA. From these numbers, the load line of the amplifier can be drawn as shown in Fig. 4.2.

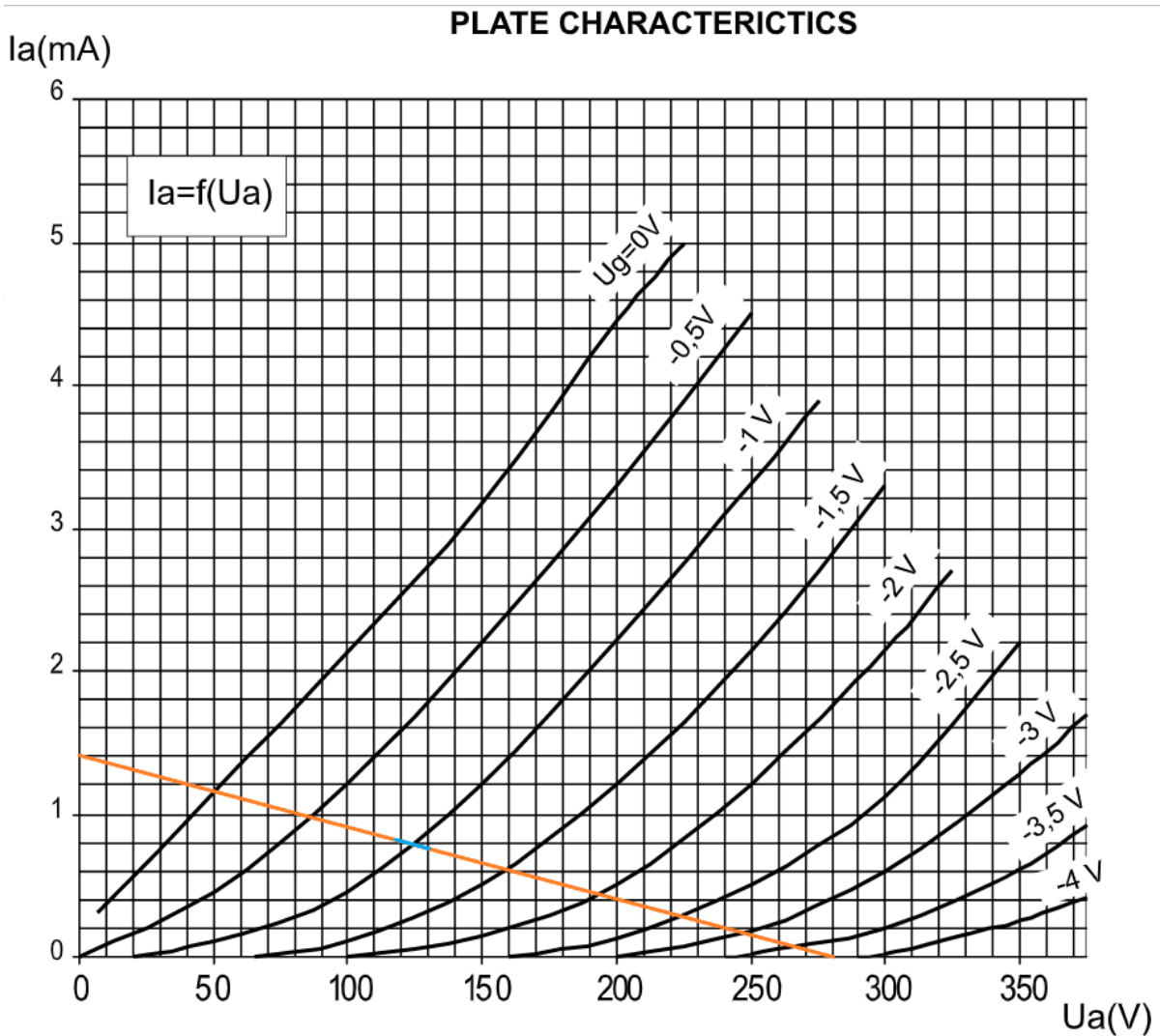


Figure 4.2: ECC83s Load Line [2]

The orange line shown in Fig. 4.2 is considered the load line, while the short blue section is showing the grid voltage while between the maximum and minimum input voltages of approximately 113 mV_{PP} as calculated in Chapter 2.1. To further aid in the analysis of the load line, there are online load line calculators that make interpreting the graphs easier [3]. Using the aforementioned site and the graph, it can be approximately found the the quiescent current is 0.79 mA and the plate voltage at that current will be 122 V . The plate resistor, a resistor

connected from the high voltage (280 V) rail to the plate terminal, allows for the vacuum tube to actually amplify a signal. If the resistor is present, the vacuum tube can modulate the grid voltage to vary the amount of current flowing from the plate to the cathode. In doing so, this will allow a varying amount of current to flow through the resistor, and therefore provide a larger or smaller voltage drop depending on the grid voltage. To calculate the value of the plate resistor, it is assumed that all of the plate voltage is 0 V and therefore, according to Fig. 4.2 the plate current is 1.4 mA. Therefore the plate resistor can be figured out by simple Ohm's Law.

$$V = IR$$

$$280 = 1.4E - 3 * R$$

$$R = 200E3$$

Therefore the plate resistor is found to be 200 k Ω . Given the quiescent current is 0.79 mA, the cathode resistor can be figured out by simple Ohm's Law. This is done by considering the fact that the grid voltage must remain -1 V below the cathode.

$$V = IR$$

$$1 = 0.79E - 3 * R$$

$$R = 1269 \approx 1200$$

The gain equation for this stage is given by Shine⁷ and is as follows: Gain = (Tube Gain x Plate Resistor)/(Plate Resistor + Plate Resistance + ((Tube Gain+1) x Cathode Resistor)) [19].

The calculated value for the overall gain is found to be approximately 51 V/V or 34dB. The output impedance of this stage is too high to drive a load, so there is an additional stage called a cathode follower (essentially a voltage follower op amp configuration) used for reducing the output impedance. The load line for this configuration is as shown in Fig. 4.3.

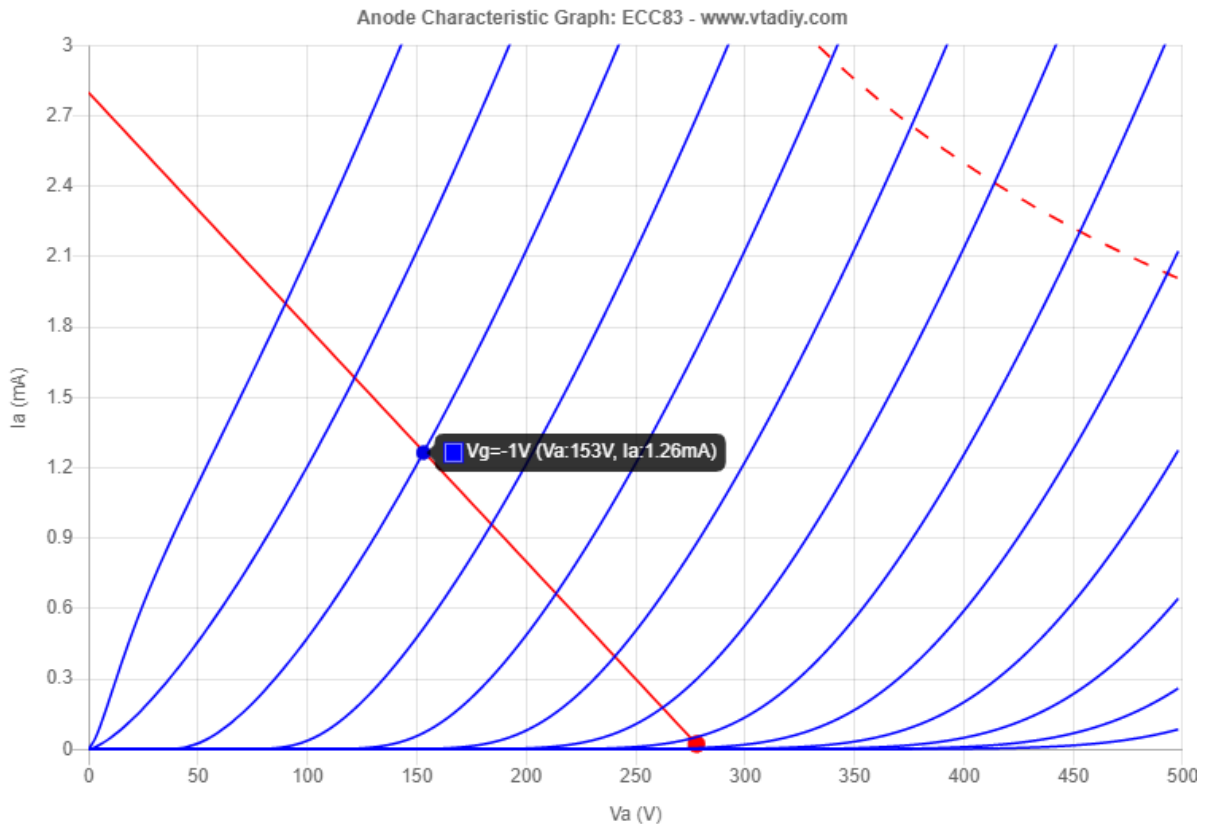


Figure 4.3: Cathode Follower Load Line [3]

Because the cathode follower is designed to drive a load, the output current capabilities of the stage must be increased. Therefore, a 2.8 mA plate current was utilized. Which results in a calculated cathode load resistor of:

$$V = IR$$

$$280 = 2.8E - 3 * R$$

$$R = 100E3$$

To bias the cathode, there must be a resistor in between the cathode load resistor and the cathode, this is called the cathode bias resistor. This is calculated by finding the quiescent current at the grid bias current, using the online tool, it is found to be 1.26mA. This results in the cathode bias resistor:

$$V = IR$$

$$1 = 1.26E - 3 * R$$

$$R = 793 \approx 806$$

The next standard resistor value for the cathode bias resistor is 806Ω. This all results in the schematic as shown in Fig. 4.4

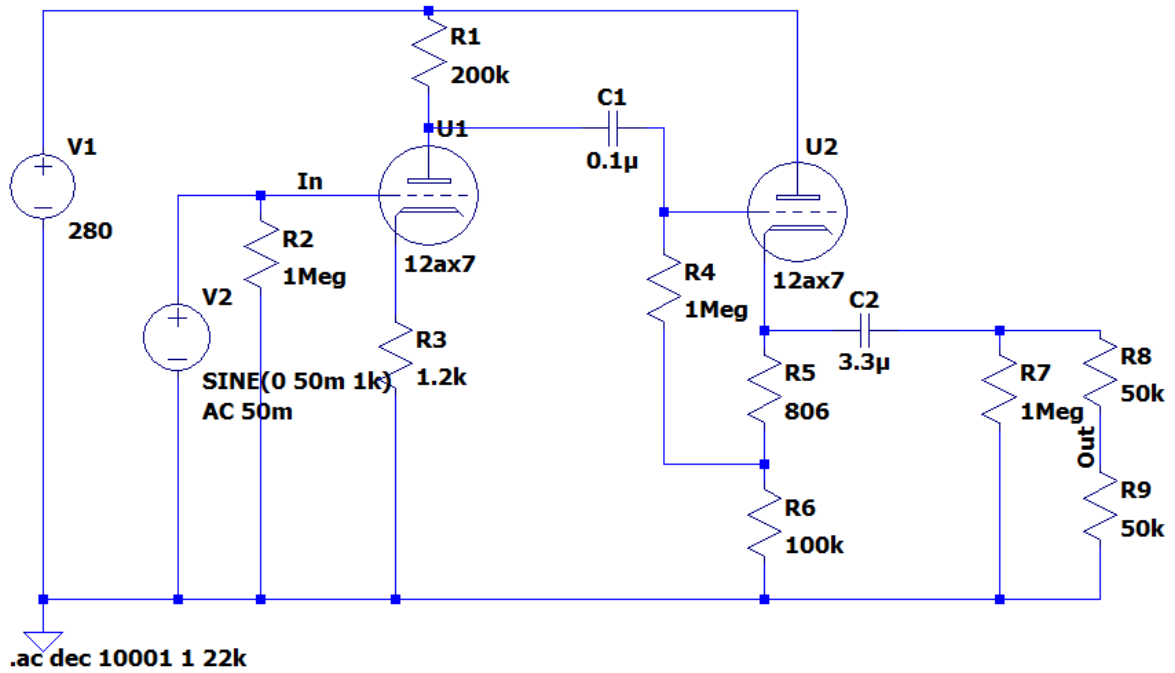


Figure 4.4: LTSpice Schematic of Preamplifier

Capacitors C1 and C2, as shown in Fig. 4.4, were not calculated specifically, but determined to be DC blocking capacitors. The output of the first stage will be DC biased to approximately 122V, which if input directly into the next stage's grid, would blow up the tube. Because of this, a DC blocking capacitor, C1, is utilized. Additionally, this is the same reason that C2 is utilized, to block any DC from the final output of the preamplifier. R7 is utilized to keep the preamplifier output grounded, this would be mainly utilized in case the potentiometer fails so that the capacitor, C2, does not charge to a dangerous level. R8 and R9 are emulating a 100k Ω potentiometer.

4.3 Vacuum Tube Preamplifier Simulation

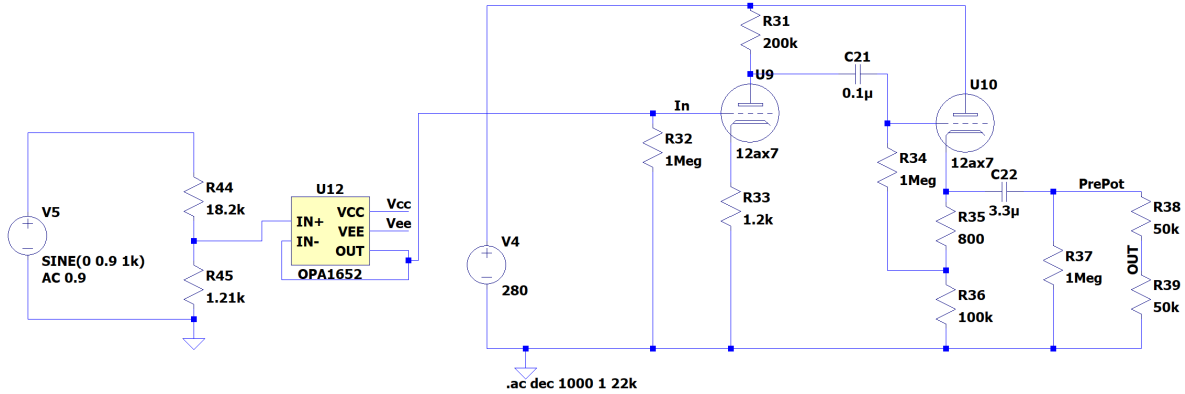


Figure 4.5: DAC Input to Preamplifier Output

As shown in Fig. 4.5, the V5 voltage source is setup for an AC sweep at an amplitude of 0.9V which is half of the input peak to peak calculated in Chapter 2.1. This is fed into a resistor divider to drop the input voltage down to 113mV_{PP} and then into a voltage follower to buffer the DAC and preamplifier. The AC sweep performed will sweep the frequency from 1 Hz to 22kHz in decade increments. There are a total of 1000 points taken per decade for the simulation.

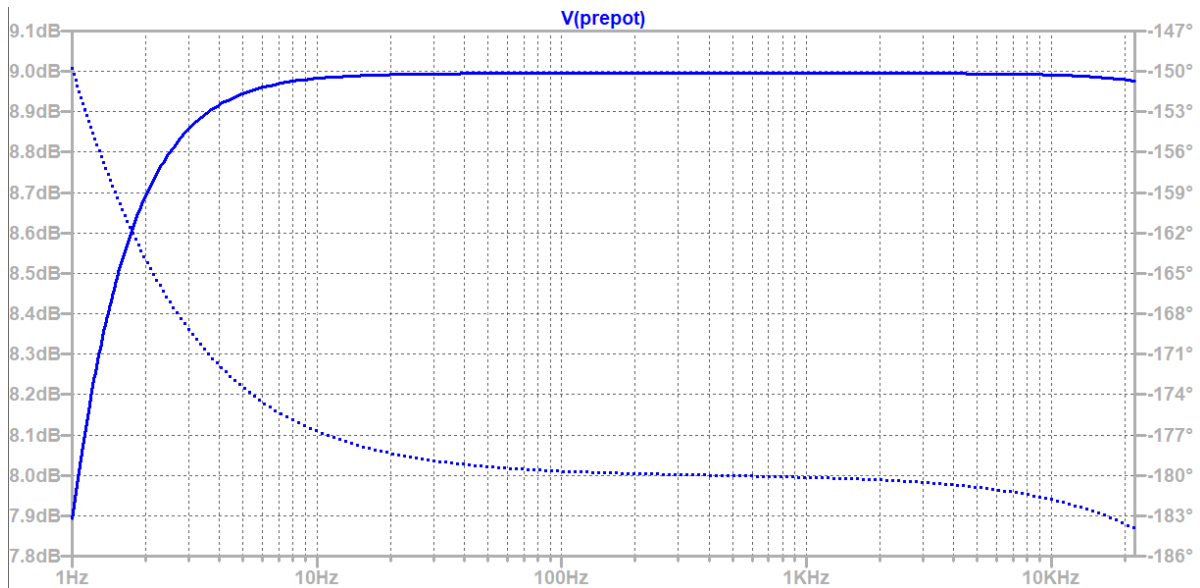


Figure 4.6: Preamplifier Output Pre-Potentiometer

As shown in Fig. 4.6, the frequency response (the solid line) of the preamplifier is very flat within the audible range (between 20Hz to 22kHz). The phase response (the dotted line), is additionally flat within the human hearing range; however, most sources state that the phase response is imperceptible for human hearing through headphones [6]. As such this can largely be ignored.

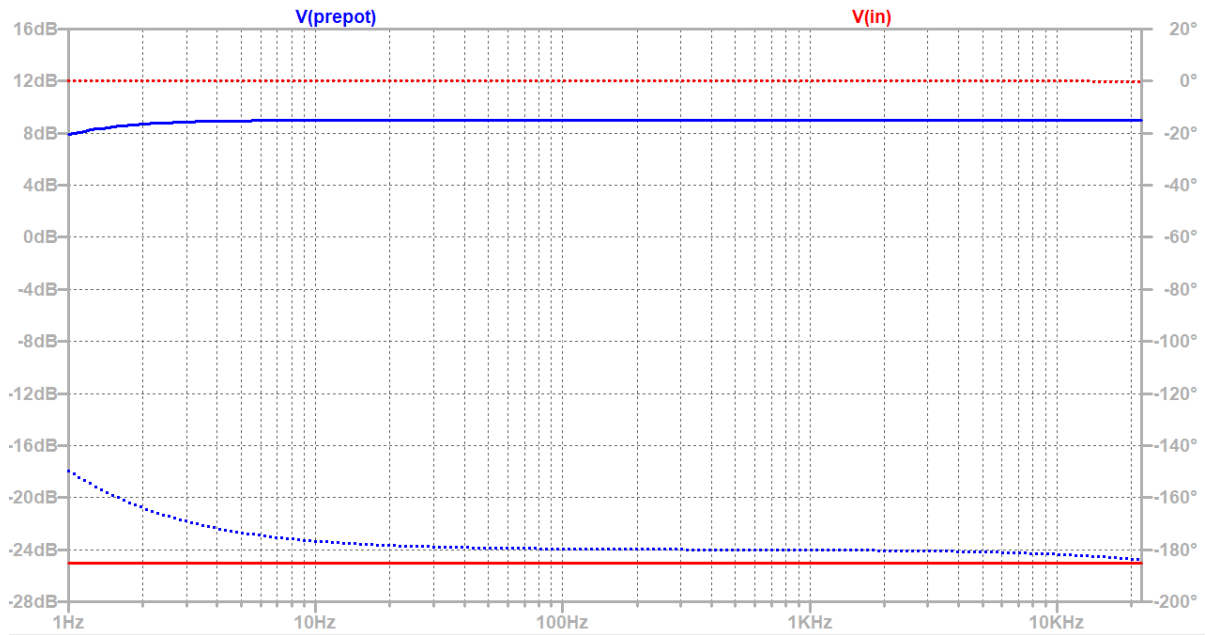


Figure 4.7: Preamplifier Gain

As shown in Fig. 4.7, the approximate gain of the amplifier is found by taking the input signal and subtracting it from the output signal:

$$9 \text{ dB} - -25 \text{ dB} = 34 \text{ dB}$$

This perfectly matches the designed gain of the preamplifier.

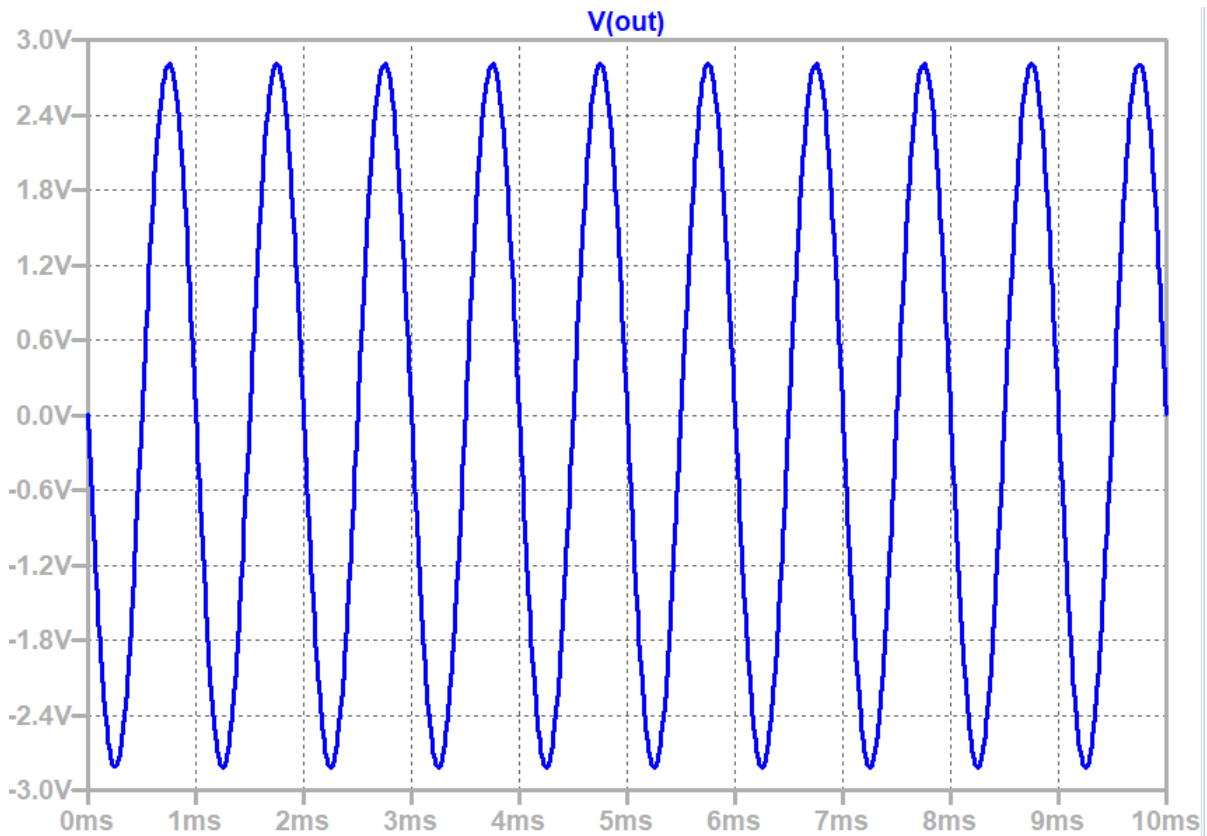


Figure 4.8: Preamplifier Output Voltage

When the volume potentiometer (comprised of R38 and 39 from Fig. 4.5) is set to the maximum output, *i.e.* R38 is reduced to 0Ω and R39 is increased to $100\text{k}\Omega$, the output voltage is approximately 2.8V_{PP} . This is seen in Fig. 4.8 and matches the calculated value in Chapter 2.1.

Chapter 5

Analog Based Audio Filters

5.1 Graphic Equalizer

The graphic equalizer is designed to either attenuate or boost the signal strength in a certain frequency band, determined by the resistance of a linear potentiometer (fader). It is called a “graphic” equalizer due to the positioning of the faders indicates what the frequency response will look like, this is shown in Fig. 5.1.

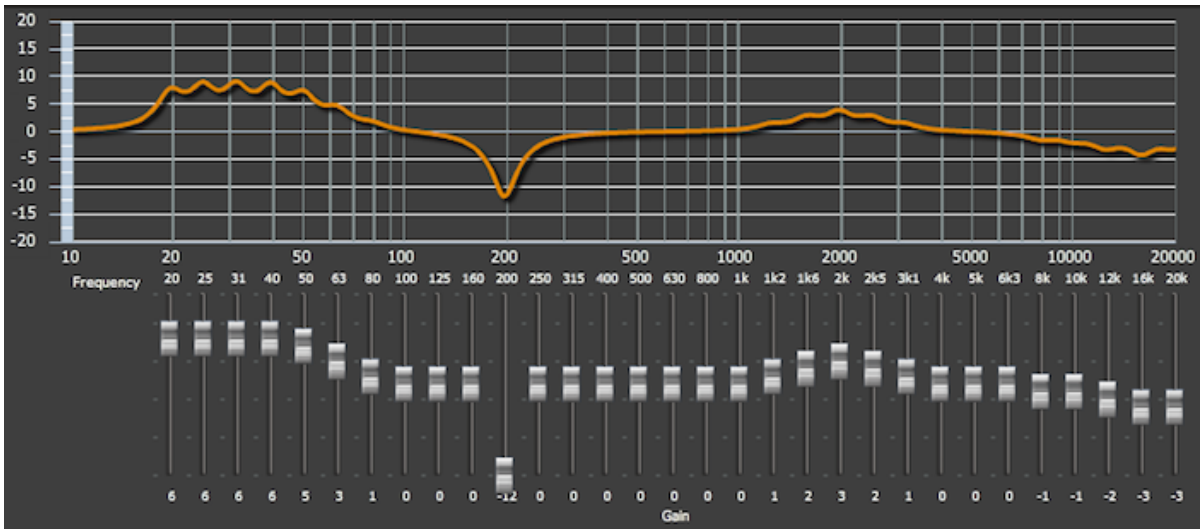


Figure 5.1: Graphic Equalizer Visualization [4]

While most graphic equalizers are implemented in the digital realm, an analog based approach was utilized for this project. A graphic equalizer was implemented from Douglas Self's book: *Small Signal Audio Design* - pg. 446 [6]. The basis for this design is the use of a synthetic inductor or more commonly, a gyrator.

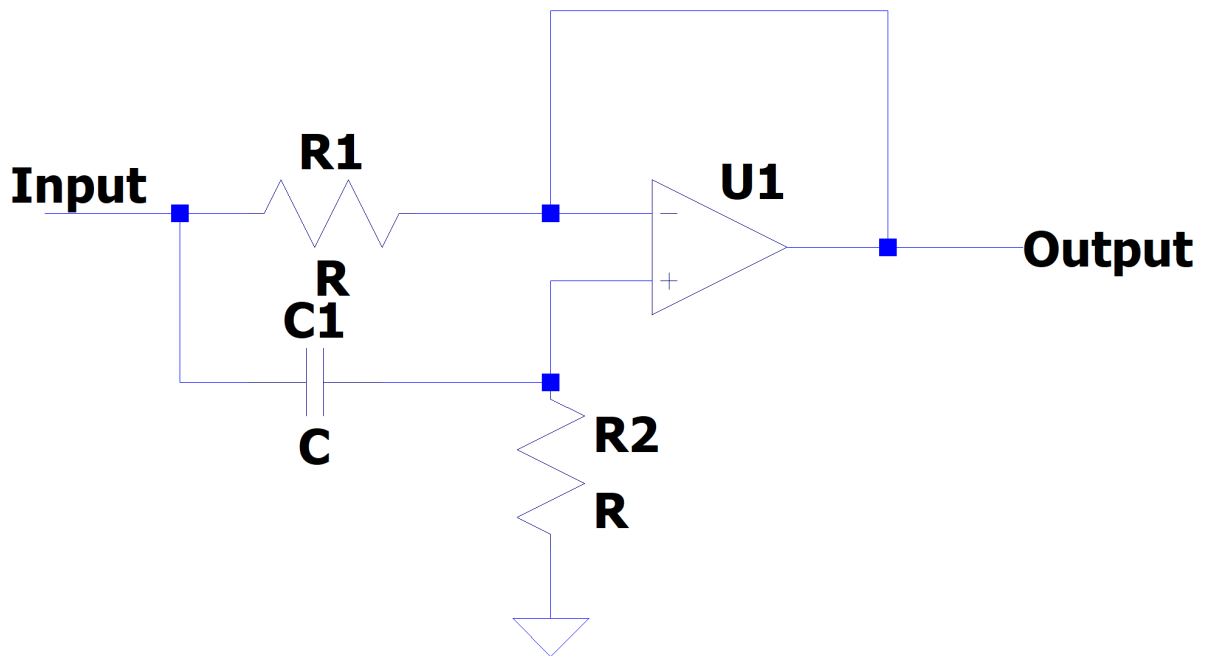


Figure 5.2: Gyrator Circuit

The gyrator works by being an active impedance converter, *i.e.* it would convert a capacitor, $C1$ shown in Fig. 5.2, into an inductor; however if $C1$ was an inductor, the circuit would act as a capacitor. The main reason that gyrators are used over inductors is due to the other parasitic effects that inductors have due to their construction [20]. They intrinsically have a large resistance and a capacitance; the resistance is due to the wire wound construction having an associated resistance with the wire utilized, and the capacitance is due to inter winding capacitance. A gyrator negates these issues, as real capacitors have a very well defined and controlled equivalent series resistance (ESR) and negligible inductance. To determine the inductance of the gyrator, the transfer function must be computed. To calculate this, a nodal equation is written for Fig. 5.2. This is realized, by understanding the operational amplifier is setup in a voltage follower configuration, and the output voltage will follow the positive

terminal of the input.

$$V_o(s) = V_i(s) \frac{R_2}{\frac{1}{sC} + R_2}$$

$$\frac{V_o(s)}{V_i(s)} = \frac{s}{s + \frac{1}{R_2C}}$$

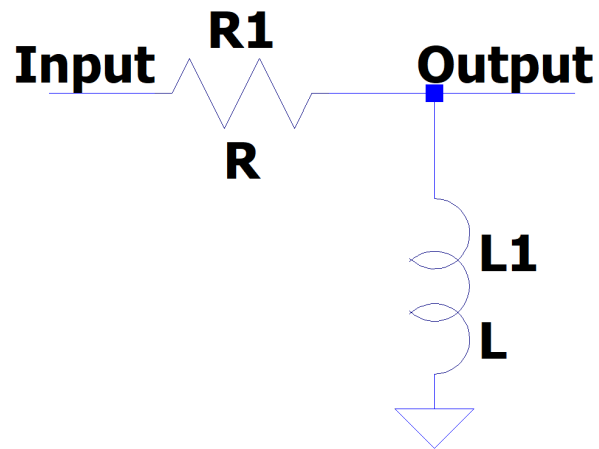


Figure 5.3: Equivalent RL Gyrator Circuit

The equivalent circuit is as shown in Fig. 5.3. Which the transfer function can be computed by implementing a voltage divider equation:

$$V_o(s) = V_i(s) \frac{sL}{sL + R_1}$$

$$\frac{V_o(s)}{V_i(s)} = \frac{s}{s + \frac{R_1}{L}}$$

These two equations for the gyrator and RL circuit can be set equal to one another as they are similar form:

$$\frac{s}{s + \frac{R_1}{L}} = \frac{s}{s + \frac{1}{R_2 C}}$$

$$\frac{R_1}{L} = \frac{1}{R_2 C}$$

$$L = R_1 R_2 C$$

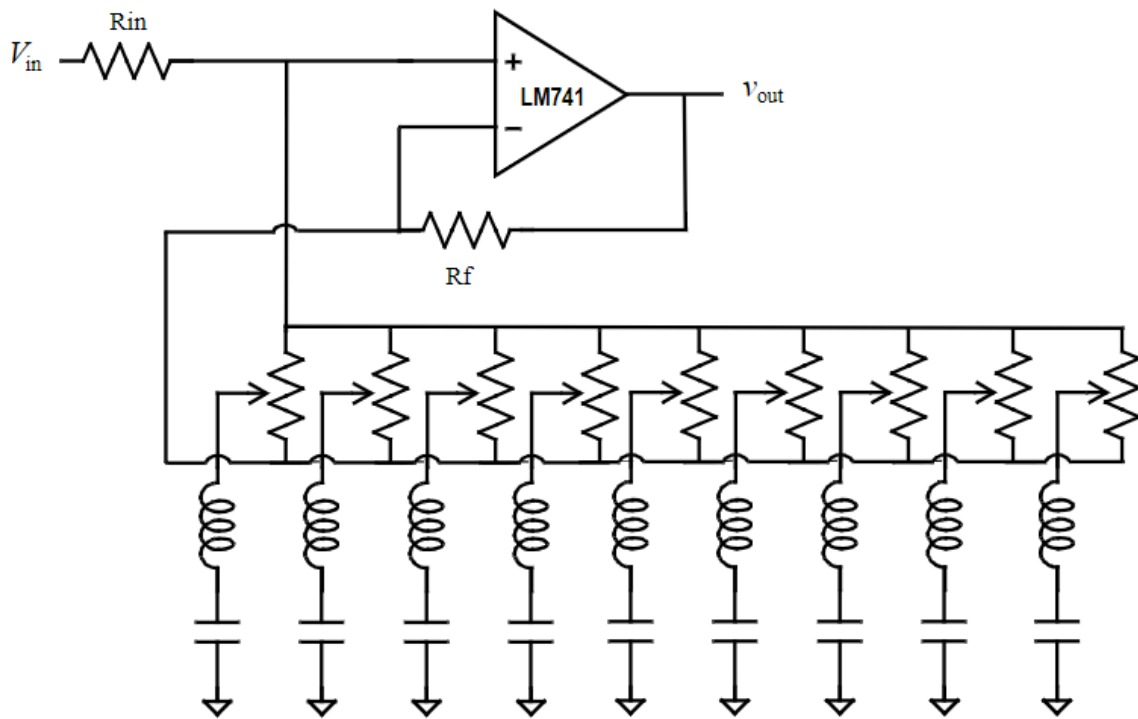


Figure 5.4: LC Based Graphic Equalizer [5]

To further understand the graphic equalizer, an equivalent model utilizing a series LC circuit is shown in Fig. 5.4. The graphic equalizer method of operation is to use several bandpass filters and vary the gain in each stage. The output of each are combined using a summing configuration on an operational amplifier. While, the graphic equalizer implemented in this paper

was based off of a gyrator, it is easier to understand using the LC model. Each LC section has its own resonant frequency, which is calculated in the following manner - it is understood that the resonant frequency, ω_o , is where the impedance's of L and C are equal therefore:

$$\begin{aligned}\omega L &= \frac{1}{\omega C} \\ \omega^2 &= \frac{1}{LC} \\ \omega_o &= \frac{1}{\sqrt{LC}}\end{aligned}$$

While ω is the angular frequency, it is desired to look at the actual frequency, f . Because $\omega = 2\pi f$, it is realized that the resonant frequency, f_o , is $f_o = \frac{1}{2\pi\sqrt{LC}}$. At this frequency, the impedance's are equal and therefore cancel, meaning the circuit would theoretically short the input. Additionally, to view the bandpass nature of the series LC circuit, the input impedance is calculated by the following:

$$\begin{aligned}Z_{in} &= Z_L + Z_C \\ Z_{in}(j\omega) &= j\omega L + \frac{j}{\omega C} \\ Z_{in}(j\omega) &= j\left(\omega L + \frac{1}{\omega C}\right)\end{aligned}$$

It is therefore evident at low frequencies and below the resonant frequency, the circuit is mainly capacitive. While at high frequencies the circuit is largely inductive. Due to the fact that capacitors have a high impedance at low frequencies and low impedance at high frequencies, while inductors are the opposite, it can be understood that a bandpass filter is constructed out of the series combination of the two.

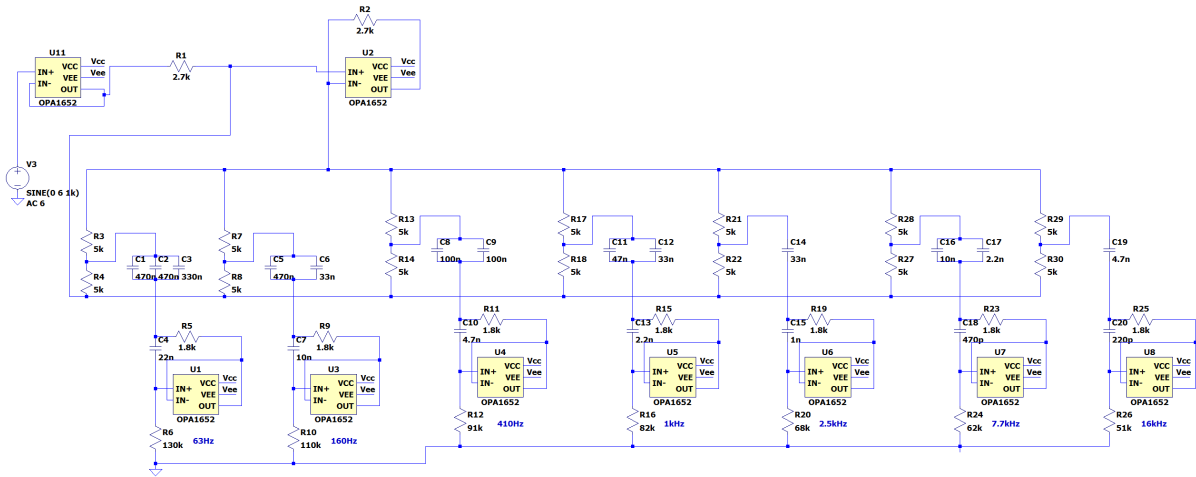


Figure 5.5: Graphic Equalizer with Gyrators [6]

Shown in Fig. 5.5, is the gyrator based equalizer that is from Douglas Self's Small Signal Audio Design. The center frequency of each bandpass is calculated by utilizing the resonant frequency equation for an LC filter. As an example, the 16kHz bandpass is calculated as follows - L is found to be the product of the R_{26} , C_{20} , and R_{25} which is $L = R_{26}C_{20}R_{25} \Rightarrow 1.8E3 \bullet 220E-12 \bullet 51E3 = 0.020196$. From there, the center frequency of the 16kHz bandpass can be calculated:

$$f_o = \frac{1}{2\pi\sqrt{LC}}$$

$$f_o = \frac{1}{2\pi\sqrt{0.020196 \bullet 4.7E-9}}$$

$$f_o = 16374.69$$

Each of the 6 other bandpass sections can be calculated in the same way.

5.1.1 Graphic Equalizer Simulation

To simulate the graphic equalizer, a frequency sweep was combined with a stepped parameter sweep on the 63Hz bandpass's potentiometer - this consisted of R_3 and R_4 from Fig. 5.5. The frequency sweep was performed from 1Hz to 22kHz. The value of the R_3 potentiometer was swept from 1Ω to $9.999\text{k}\Omega$ in 11 steps, while R_4 was the complement *i.e.* $10\text{k}\Omega - R_3$. The result of which is shown in Fig. 5.6.

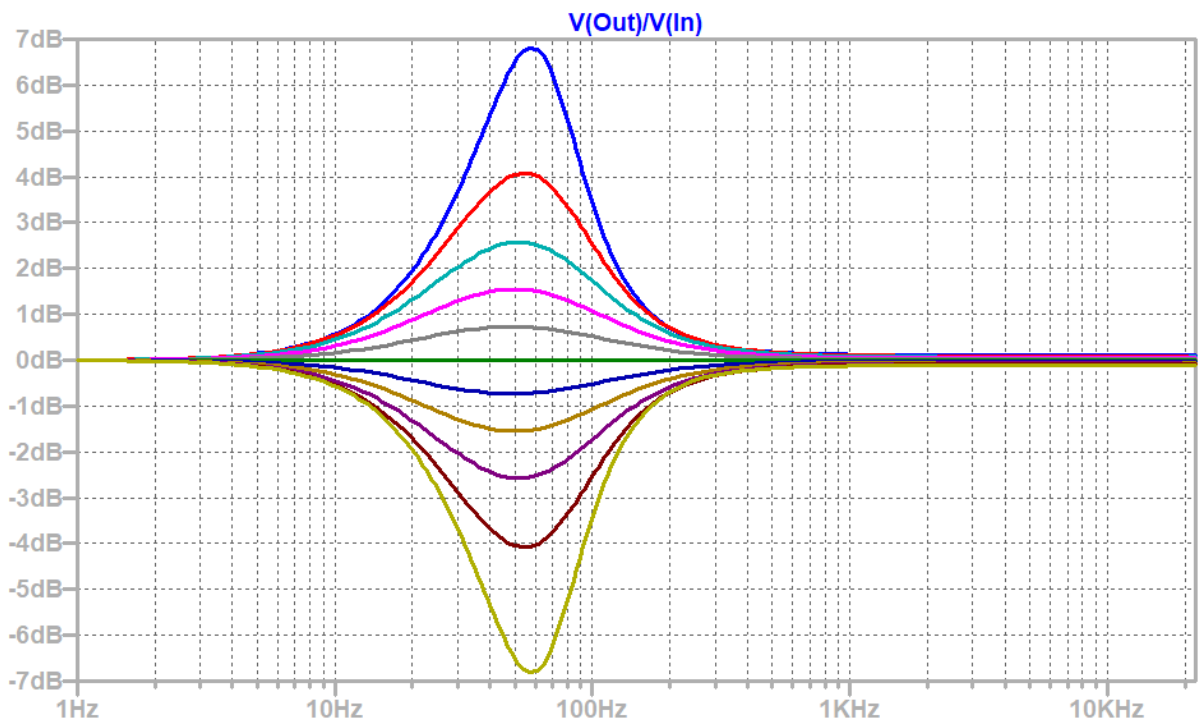


Figure 5.6: Graphic Equalizer Parametric Frequency Sweep

The maximum cut/gain found from the simulation shows approximately $\pm 6.8\text{dB}$, which is slightly lower than the $\pm 8\text{dB}$ as found from the implementation in [6]. Additionally, the Q, or quality factor, of this filter is variable, as shown from the simulation. This is noted by the seeing that the filter becomes more selective as the potentiometer is swept.

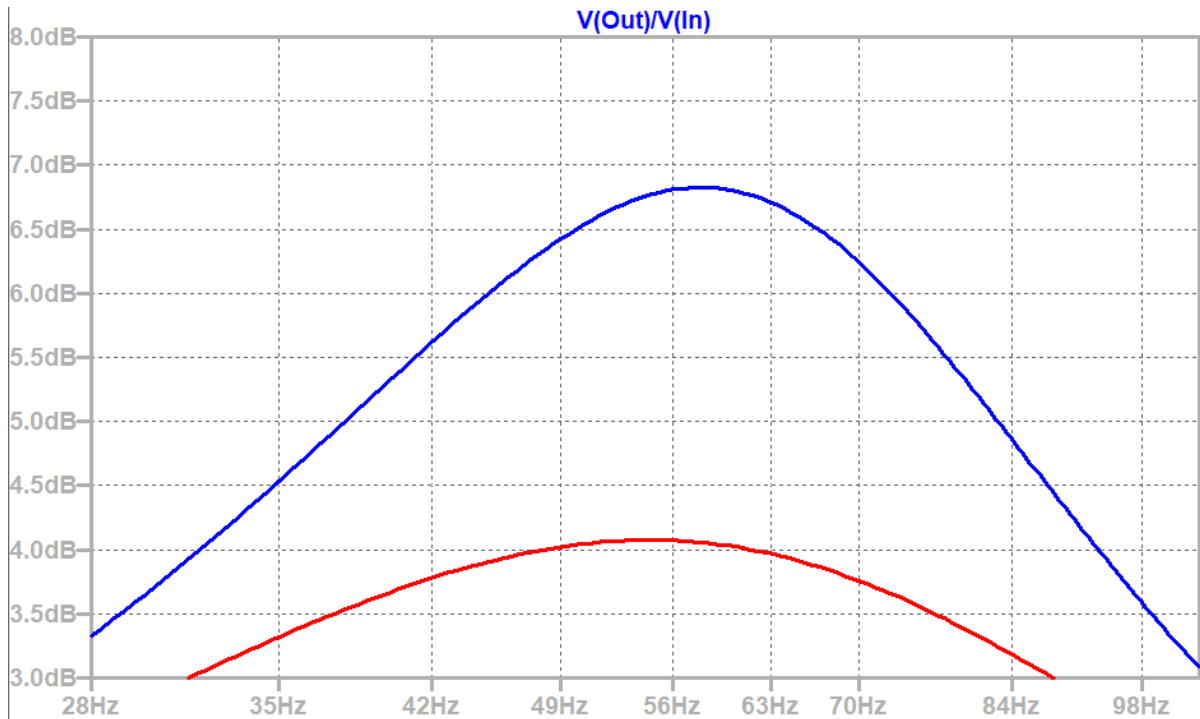


Figure 5.7: Maximum Gain Graph

As the Q factor is variable for this filter, the Q at the maximum gain will be considered. To find the Q factor it is calculated by the following formula [21]:

$$Q = \frac{f_c}{f_1 - f_2} \quad (5.1)$$

The center frequency, f_c , as simulated is approximately 58Hz and the 3 dB points, f_1 and f_2 , of the graph were found at 31 Hz and 94Hz:

$$Q = \frac{58}{94 - 31}$$

$$Q = 0.92$$

[6] gave the Q factor at the maximum gain to be approximately 0.9, so the simulation aligns with what is expected.

5.2 Low Pass Filter

The Low Pass Filter was designed using Analog Devices' Analog Filter Wizard [7]. The specifications given to the wizard was to be a low pass filter with 0dB of gain and a $f_c = 40\text{kHz}$. The stopband setting was automatically set at -30dB at 70kHz , and did not need to be changed. The setting for the "Filter Response" was adjusted until a filter with 4 stages was found, as that's the number of operational amplifiers found within the OPA1654 [22]. This meant that all the operational amplifiers were utilized within each package and would result in the most optimal performance relative to the operational amplifier count. The output of the Analog Filter Wizard can be found in Fig. 5.8.

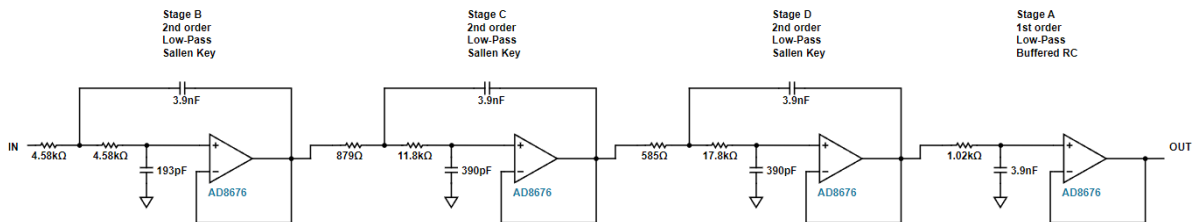


Figure 5.8: 7th Order Butterworth Low Pass Filter from the Analog Filter Wizard [7]

Each stage of the overall circuit shown in Fig. 5.8 can be independently analyzed. Once the transfer function for each stage is found, the overall transfer function is the product of each stage's transfer function.

$$T_{Filter} = T_A T_B T_C T_D$$

One of the main reasons for having a higher order filter, is to increase the roll-off rate of the filter. The roll-off rate is the rate at which the filter's output decreases after the cutoff frequency. For each pole in the overall transfer function, there is a $+20\text{ dB/decade}$ increase. For a 7 pole low pass filter, this would mean the roll-off rate is $+140\text{ dB/decade}$.

5.2.1 Sallen Key Derivation

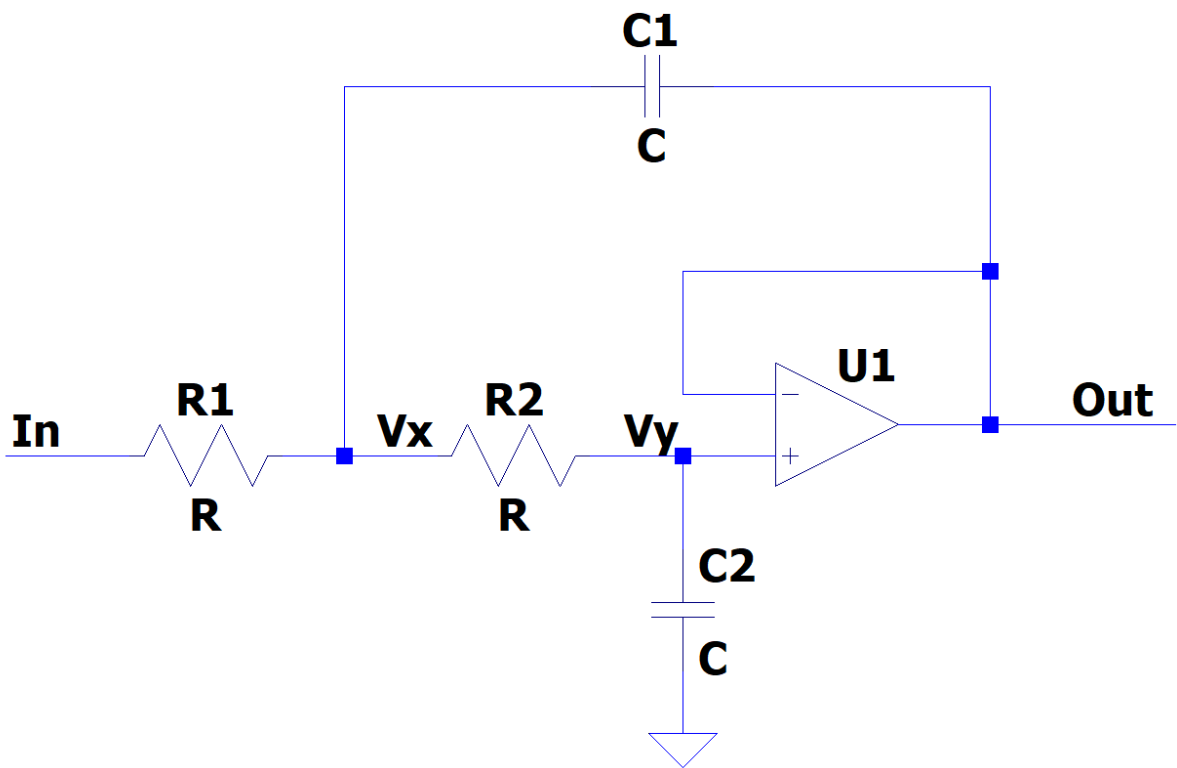


Figure 5.9: Sallen Key Topology for a Low Pass Filter

The Sallen Key low pass topology is shown in Fig. 5.9. To fully understand the circuit, assume a low frequency signal (below the cutoff frequency) is provided at node "In". The low frequency signal will be blocked by C_1 , but will pass onto the positive input to the operational amplifier. Because the input signal is low frequency, C_2 does not have a large effect on it, and

acts as an open circuit. As the operational amplifier is setup as a voltage follow configuration, the output is the same as the input at the positive node. In the case of a high frequency signal (that is above the cutoff frequency), C_2 will act as an open circuit and shunt the signal to ground while C_1 will act as a shunt directly to the output. Because the operational amplifier tries to maintain the same voltage between the positive and negative inputs, any signal present that flowed through C_2 would cause the operational amplifier to output an inverted input signal, and therefore cancel out the high frequency signal. The transfer function of a circuit allows a better understanding of the overall architecture and the circuit's usefulness. To derive the transfer function, a set of nodal equations must be written:

$$\frac{V_x - V_{in}}{R_1} + \frac{V_x - V_{out}}{\frac{1}{sC_1}} + \frac{V_x - V_y}{R_2} = 0 \quad (5.2)$$

$$\frac{V_y - V_x}{R_2} + \frac{V_y - 0}{\frac{1}{sC_2}} = 0 \quad (5.3)$$

It is understood that for an operational amplifier $V_+ = V_-$, since V_- is connected to the output, $V_{out} = V_+ = V_-$. In the case of the derivation, this means that $V_y = V_{out}$. Additionally, for ease of simplification the following substitutions will be made $Z_1 = \frac{1}{sC_1}$ and $Z_2 = \frac{1}{sC_2}$. Equation 5.3 can be therefore simplified to then substitute into Eqn. 5.2.

$$\begin{aligned}\frac{V_y - V_x}{R_2} + \frac{V_y - 0}{\frac{1}{sC_2}} &= 0 \\ \frac{V_{out} - V_x}{R_2} + \frac{V_{out}}{Z_2} &= 0 \\ V_{out}\left(\frac{1}{R_2} + \frac{1}{Z_2}\right) &= \frac{V_x}{R_2} \\ V_{out}\left(1 + \frac{R_2}{Z_2}\right) &= V_x\end{aligned}$$

This equation can then be substituted into Eqn. 5.2 (note: the substitutions $Z_2 = \frac{1}{sC_2}$ and $V_y = V_{out}$ were utilized):

$$\begin{aligned}\frac{V_x - V_{in}}{R_1} + \frac{V_x - V_{out}}{Z_1} + \frac{V_x - V_{out}}{R_2} &= 0 \\ \frac{V_x}{R_1} - \frac{V_{in}}{R_1} + \frac{V_x}{Z_1} - \frac{V_{out}}{Z_1} + \frac{V_x}{R_2} - \frac{V_{out}}{R_2} &= 0 \\ V_x\left(\frac{1}{R_1} + \frac{1}{Z_1} + \frac{1}{R_2}\right) - V_{out}\left(\frac{1}{Z_1} + \frac{1}{R_2}\right) &= \frac{V_{in}}{R_1} \\ V_{out}\left(1 + \frac{R_2}{Z_2}\right)\left(\frac{1}{R_1} + \frac{1}{Z_1} + \frac{1}{R_2}\right) - V_{out}\left(\frac{1}{Z_1} + \frac{1}{R_2}\right) &= \frac{V_{in}}{R_1} \\ V_{out}\left[\left(1 + \frac{R_2}{Z_2}\right)\left(\frac{1}{R_1} + \frac{1}{Z_1} + \frac{1}{R_2}\right) - \left(\frac{1}{Z_1} + \frac{1}{R_2}\right)\right] &= \frac{V_{in}}{R_1} \\ \frac{1}{R_1} \frac{1}{\left[\left(1 + \frac{R_2}{Z_2}\right)\left(\frac{1}{R_1} + \frac{1}{Z_1} + \frac{1}{R_2}\right) - \left(\frac{1}{Z_1} + \frac{1}{R_2}\right)\right]} &= \frac{V_{out}}{V_{in}}\end{aligned}$$

Utilizing MATLAB for further simplification (including back substituting in $Z_1 = \frac{1}{sC_1}$ and $Z_2 = \frac{1}{sC_2}$), the resulting transfer function was found to be:

$$\frac{V_{out}}{V_{in}} = \frac{1}{s^2(R_1R_2C_1C_2) + s(C_2(R_1 + R_2)) + 1} \quad (5.4)$$

The standard form of a second order Butterworth low pass filter is as given by Eqn 5.5 [23].

$$T(s) = \frac{K\omega_o^2}{s^2 + (\frac{\omega_o}{Q})s + \omega_o^2} \quad (5.5)$$

To determine the angular cutoff frequency, ω_o , the transfer function in Eqn. 5.4 must be converted into the form present within Eqn. 5.5:

$$\begin{aligned} \frac{V_{out}}{V_{in}} &= \frac{1}{s^2(R_1R_2C_1C_2) + s(C_2(R_1 + R_2)) + 1} \\ \frac{V_{out}}{V_{in}} &= \frac{1}{R_1R_2C_1C_2} \frac{1}{s^2 + s\frac{C_2(R_1+R_2)}{R_1R_2C_1C_2} + \frac{1}{R_1R_2C_1C_2}} \\ \frac{V_{out}}{V_{in}} &= \frac{1/(R_1R_2C_1C_2)}{s^2 + s\frac{C_2(R_1+R_2)}{R_1R_2C_1C_2} + \frac{1}{R_1R_2C_1C_2}} \end{aligned} \quad (5.6)$$

Equation 5.6 can then be compared against Eqn. 5.5 to determine $\omega_o^2 = \frac{1}{R_1R_2C_1C_2}$, therefore $\omega_o = \frac{1}{\sqrt{R_1R_2C_1C_2}}$, which utilizing $\omega_o = 2\pi f_c$, gives the cutoff frequency:

$$f_c = \frac{1}{2\pi\sqrt{R_1R_2C_1C_2}} \quad (5.7)$$

Additionally, Q can be found by the same methodology:

$$\begin{aligned}
\frac{\omega_o}{Q} &= \frac{C_2(R_1 + R_2)}{R_1 R_2 C_1 C_2} \\
Q &= \frac{\omega_o(R_1 R_2 C_1 C_2)}{C_2(R_1 + R_2)} \\
Q &= \frac{1}{\sqrt{R_1 R_2 C_1 C_2}} \frac{R_1 R_2 C_1}{(R_1 + R_2)} \\
Q &= \frac{1}{\sqrt{R_1 R_2 C_1 C_2}} \frac{\sqrt{R_1 R_2 C_1 C_2}}{\sqrt{R_1 R_2 C_1 C_2}} \frac{R_1 R_2 C_1}{(R_1 + R_2)} \\
Q &= \frac{\sqrt{R_1 R_2 C_1 C_2}}{R_1 R_2 C_1 C_2} \frac{R_1 R_2 C_1}{(R_1 + R_2)} \\
Q &= \frac{\sqrt{R_1 R_2 C_1 C_2}}{C_2(R_1 + R_2)} \tag{5.8}
\end{aligned}$$

5.2.2 Sallen Key Stage Design

Each stage from the Filter Wizard uses $C_1 = 3.9 \text{ pF}$, it will be assumed that this capacitor was picked by the designer and then R_1 , R_2 , and C_2 designed around this value. To determine those values, the easiest way is to setup a system of equations using Eqns. 5.7 and 5.8.

$$\begin{aligned}
f_c &= \frac{1}{2\pi\sqrt{R_1 R_2 C_1 C_2}} \\
Q &= \frac{\sqrt{R_1 R_2 C_1 C_2}}{C_2(R_1 + R_2)}
\end{aligned}$$

An observant reader would notice that in the system of two equations, there are a total of 3 unknowns and therefore it cannot be solved. However, it is generally understood that there is a given scale factor between each resistor and capacitor *i.e.* $R_1 \propto R_2$ and $C_1 \propto C_2$. For Stage B, as shown in Fig. 5.8, it is assumed that $C_1 = 3.9 \text{ pF}$ and C_2 will be $\frac{1}{20}C_1$. This means that 193 pF . It is determined that the cutoff frequency, f_c , will be 40 kHz .

Table 5.1: Butterworth Filter Table [12]

FILTER ORDER	Stage 1		Stage 2		Stage 3		Stage 4		Stage 5	
	FSF	Q	FSF	Q	FSF	Q	FSF	Q	FSF	Q
2	1.000	0.7071								
3	1.000	1.0000	1.000							
4	1.000	0.5412	1.000	1.3065						
5	1.000	0.6180	1.000	1.6181	1.000					
6	1.000	0.5177	1.000	0.7071	1.000	1.9320				
7	1.000	0.5549	1.000	0.8019	1.000	2.2472	1.000			
8	1.000	0.5098	1.000	0.6013	1.000	0.8999	1.000	2.5628		
9	1.000	0.5321	1.000	0.6527	1.000	1.0000	1.000	2.8802	1.000	
10	1.000	0.5062	1.000	0.5612	1.000	0.7071	1.000	1.1013	1.000	3.1969

Table 5.1, gives the value of Q required for each stage, given the order of the filter and the number of stages. In this case, the filter order is 7 and utilizes 4 stages. Usually, when cascading filters, the higher Q stages are left to the end of the filter chain as to not accidentally saturate any stage [12]. However, this is not an issue for this design as this is a unity gain filter. Due to this, the Stage B is utilizing a $Q = 2.2472$. The system of equations are as such:

$$40E3 = \frac{1}{2\pi\sqrt{R_1R_2(3.9E-9)(193E-12)}}$$

$$2.2472 = \frac{\sqrt{R_1R_2(3.9E-9)(193E-12)}}{(193E-12)(R_1+R_2)}$$

This results in the values of $R_1 = 4.67\text{k}\Omega$ and $R_2 = 4.49\text{k}\Omega$. These two resistors are close enough in value that the nearest value of $4.58\text{k}\Omega$ will work for both. Stages C and D are calculated in the same manner as Stage D. However, Stage A is a single pole low pass, so it does not follow the same design methodology. Stage A's operational amplifier is meant to buffer the output of the filter, and as such it is setup in a voltage follower operational amplifier configuration. To minimize the bill of materials, the capacitor for the low pass circuit is the

same 3.9nF capacitor used in the other stages. As this stage does not have a Q , the only consideration is the cutoff frequency. This leads to a simple calculation for the resistance:

$$f_c = \frac{1}{2\pi RC}$$

$$40E3 = \frac{1}{2\pi R(3.9E-9)}$$

$$R = 1020.22$$

5.2.3 Low Pass Filter Simulation

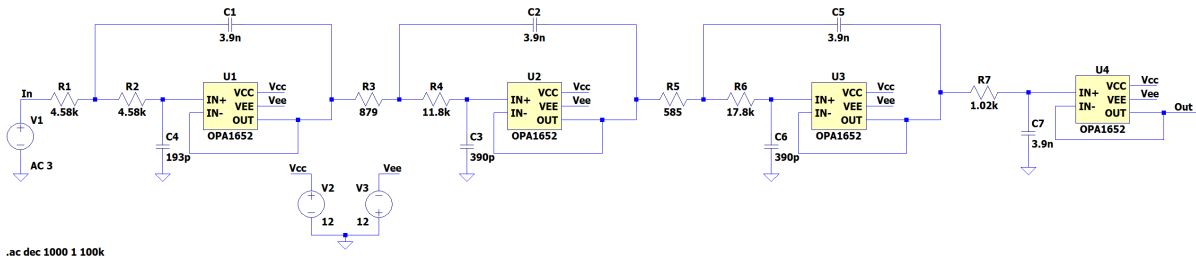


Figure 5.10: LTSpice Schematic of Sallen Key Low Pass Filter

The LTSpice schematic and simulation is shown in Fig. 5.10. The input voltage source is setup to have an amplitude of 3 V as this is approximately the expected input voltage from the preamplifier. As the cutoff frequency of the low pass filter is 40kHz, the simulation sweeps from 1 Hz to 100kHz to view the entire transfer characteristic of the low pass filter. The output of the filter is shown in Fig. 5.11.

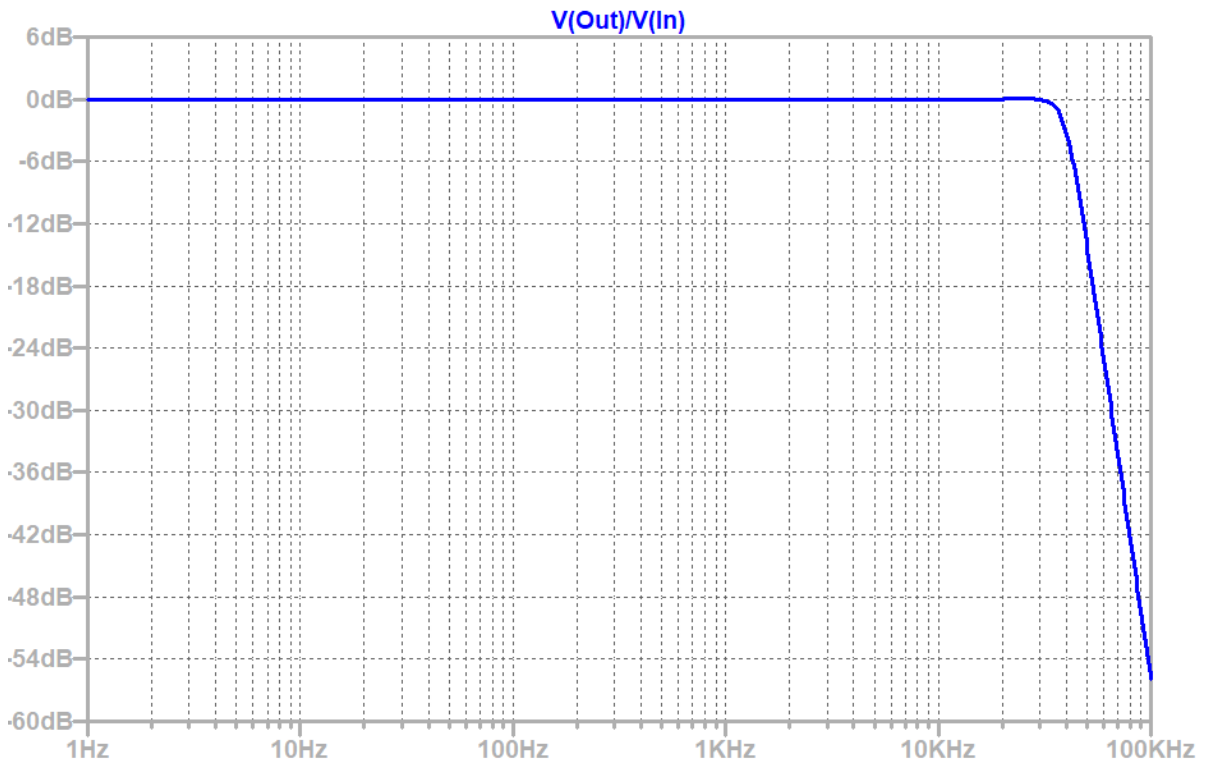


Figure 5.11: Low Pass Filter Bode Plot

The simulation was ran again, but the frequency was swept until 1 MHz to be able to find the roll-off rate. This was found to be 120dB/decade.

5.3 60 Hz Notch Filter

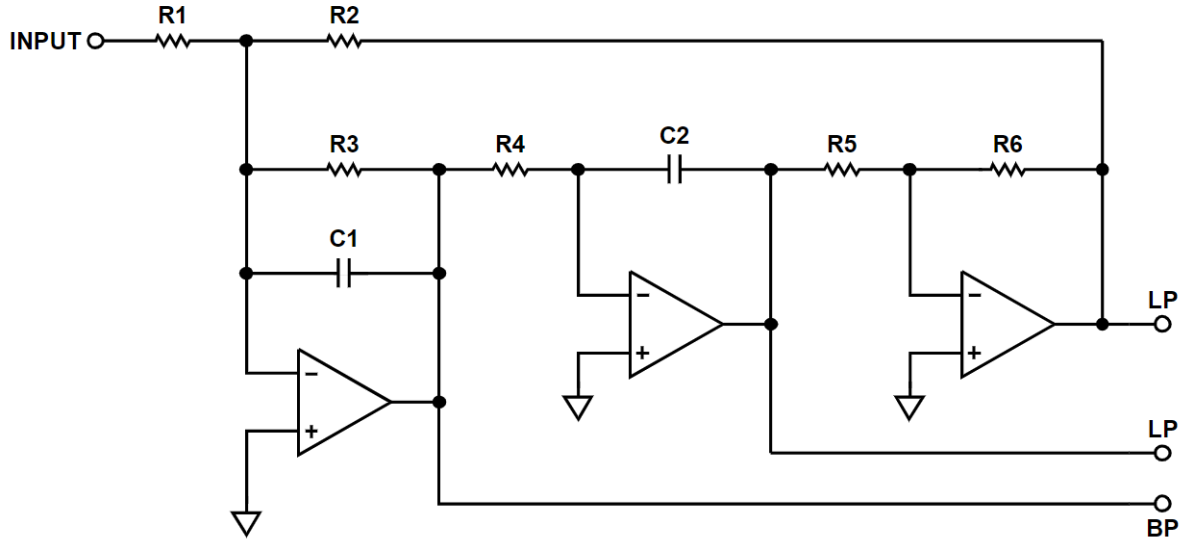


Figure 5.12: Biquadratic Filter [8]

The Tow-Thompson biquadratic (hereby “biquad”) filter is built upon 3 stages of operational amplifiers. It is used to realize three different filters: an inverted (out-of-phase) low pass, (in-phase) low pass, and a bandpass. The 3rd operational amplifier is used to invert the previous stage’s output as it is an out-of-phase version. Additionally, this would mean that if the feedback path was from this out-of-phase output, the feedback would be positive - which would lead to an unstable system.

5.3.1 Tow-Thompson Biquad Derivation

While, the transfer function of a biquad filter is well known, a full derivation of the circuit is almost never given and is generally “hand-waved”. As such, to fully understand the biquad filter, a thorough derivation is as follows (note: for the following derivations, V_w is only used as a placeholder variable, and does not actually lead to any net connections):

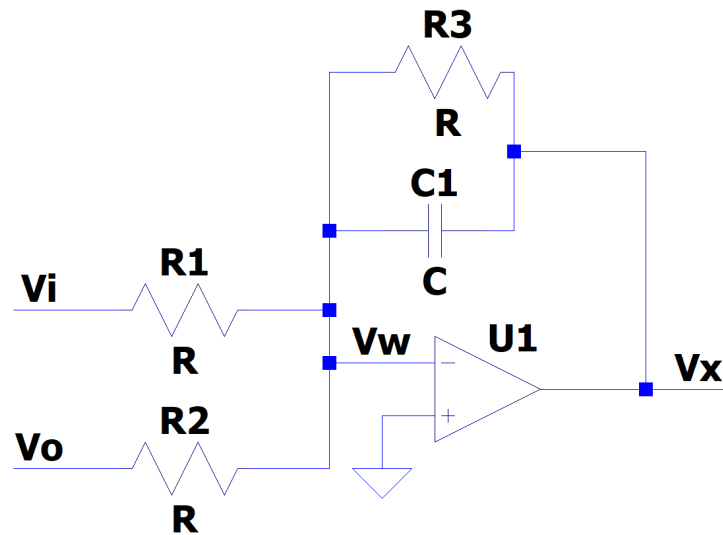


Figure 5.13: Stage One of Biquad Filter

As the biquad can be broken up into four stages, each stage is individually analyzed and then combined to reduce the complexity. Stage one is considered a lossy integrator and adder, which in itself is a low pass filter. However, it is in the feedback path that the output of this stage becomes a bandpass filter. A lossy integrator is utilized instead of a basic integrating topology as it allows for the gain of the pass band to be altered instead of unity gain. The nodal equation for stage 1 is as follows:

$$\frac{V_w - V_i}{R_1} + \frac{V_w - V_x}{Z_1} + \frac{V_w - V_o}{R_2} = 0$$

Additionally, the parallel combination of R_3 and C_1 is combined into Z_1 such that the nodal equation can be written to a more compact form:

$$Z_1 = \frac{R_3 \frac{1}{sC_1}}{R_3 + \frac{1}{sC_1}}$$

$$= \frac{R_3}{sC_1 R_3 + 1}$$

Because the positive and negative inputs of the operational amplifier must be at the same potential it is known that $V_w = 0$.

$$\frac{-V_i}{R_1} + \frac{-V_x}{Z_1} + \frac{-V_o}{R_2} = 0$$

$$\left(\frac{V_i}{R_1} + \frac{V_o}{R_2}\right)(-Z_1) = V_x$$

$$-1 \frac{R_3}{sC_1 R_3 + 1} \left(\frac{V_i}{R_1} + \frac{V_o}{R_2}\right) = V_x \quad (5.9)$$

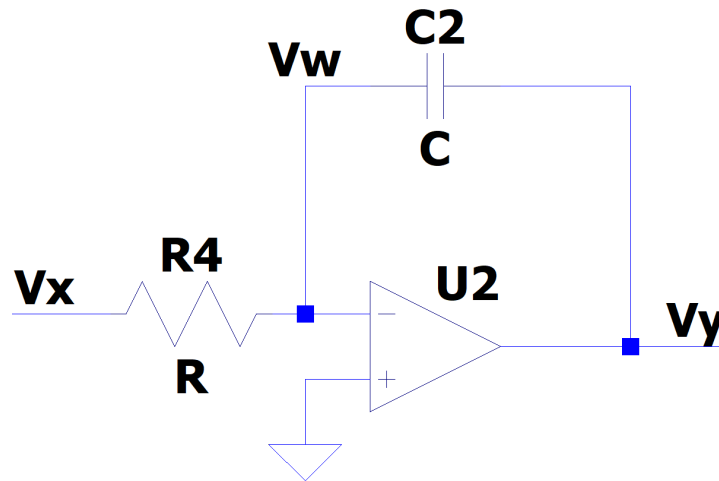


Figure 5.14: Stage Two of Biquad Filter

Stage two is noted to be an integrating topology of an operational amplifier; this also means

that it is a low pass filter. This stage is essentially the same as stage one, 5.13, however this stage does not have the ability to have an adjustable gain. The gain for this stage is fixed at unity. The nodal equation for stage 2 is as follows:

$$\begin{aligned}\frac{V_w - V_x}{R4} + \frac{V_w - V_y}{\frac{1}{sC_2}} &= 0 \\ \frac{-V_x}{R4} + \frac{-V_y}{\frac{1}{sC_2}} &= 0 \\ -V_x \frac{1}{R4C_2s} &= V_y\end{aligned}$$

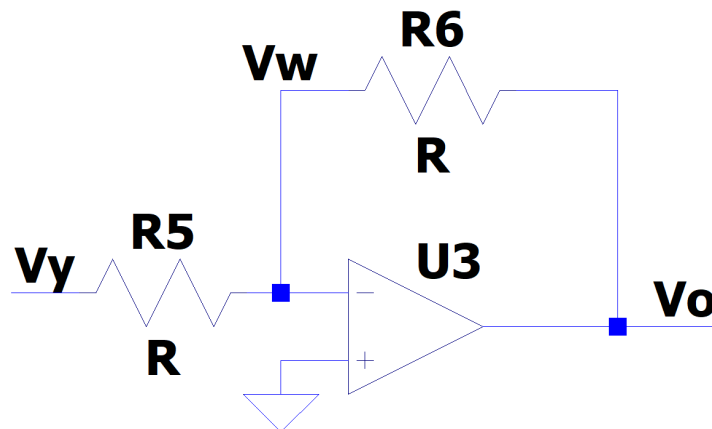


Figure 5.15: Stage Three of Biquad Filter

Stage three is merely used as an inverting, unity gain stage. It is only needed, as previously mentioned, because if this stage was not used, the feedback would be positive, and therefore would create an unstable system. For completeness, the nodal equation for stage 3 is as follows:

$$\frac{V_w - V_y}{R_5} + \frac{V_w - V_o}{R_6} = 0$$

$$-V_y \frac{R_6}{R_5} = V_o$$

Because stages 2 and 3 are fed into one another, the output of stage two can be fed into the input of stage three to find their output:

$$V_o = -\frac{R_6}{R_5} \left(-V_x \frac{1}{R_4 C_2 s} \right)$$

$$= \frac{R_6}{R_5} \frac{V_x}{R_4 C_2 s}$$

Substituting in V_x :

$$V_o = \frac{R_6}{s(R_4 R_5 C_2)} \frac{-R_3}{s C_1 R_3 + 1} \left(\frac{V_i}{R_1} + \frac{V_o}{R_2} \right)$$

$$= \frac{-R_3 R_6}{s^2 (R_3 R_4 R_5 C_1 C_2) + s(R_4 R_5 C_2)} \left(\frac{V_i}{R_1} + \frac{V_o}{R_2} \right)$$

To reduce the complexity of the equation, the following substitution is utilized:: $x =$

$$\frac{-R_3 R_6}{s^2 (R_3 R_4 R_5 C_1 C_2) + s(R_4 R_5 C_2)}, \text{ therefore:}$$

$$\begin{aligned}
 V_o &= x \left(\frac{V_i}{R_1} + \frac{V_o}{R_2} \right) \\
 V_o &= x \frac{V_i}{R_1} + x \frac{V_o}{R_2} \\
 V_o - x \frac{V_o}{R_2} &= x \frac{V_i}{R_1} \\
 V_o \left(1 - \frac{x}{R_2} \right) &= x \frac{V_i}{R_1} \\
 \frac{V_o}{V_i} &= \frac{x}{R_1} \frac{1}{1 - \frac{x}{R_2}} \\
 \frac{V_o}{V_i} &= \frac{xR_2}{R_1(R_2 - x)}
 \end{aligned}$$

To further reduce complexity, the substitution of x is broken up into the numerator portion, x_n , and the denominator portion, x_d .

$$\begin{aligned}
 \frac{V_o}{V_i} &= \frac{\frac{x_n}{x_d} R_2}{R_1 \left(R_2 - \frac{x_n}{x_d} \right)} \\
 &= \frac{x_n R_2}{R_1 (R_2 x_d - x_n)}
 \end{aligned}$$

x_n and x_d are back substituted:

$$\begin{aligned}
\frac{V_o}{V_i} &= \frac{(-R_3R_6)R_2}{R_1(R_2(s^2(R_3R_4R_5C_1C_2) + s(R_4R_5C_2)) - (-R_3R_6))} \\
&= \frac{-R_2R_3R_6}{R_1} \bullet \frac{1}{s^2(R_3R_4R_5C_1C_2) + s(R_4R_5C_2) + R_3R_6} \\
&= \frac{-R_2R_3R_6}{R_1} \bullet \frac{1}{\frac{1}{(R_3R_4R_5C_1C_2)}(s^2 + s\frac{(R_4R_5C_2)}{(R_3R_4R_5C_1C_2)} + \frac{R_3R_6}{(R_3R_4R_5C_1C_2)})} \\
&= -\frac{R_6}{R_1R_4R_5C_1C_2} \bullet \frac{1}{s^2 + s\frac{1}{R_3C_1} - \frac{-R_6}{R_2R_4R_5C_1C_2}}
\end{aligned}$$

Because the final stage is only utilized to invert the output of the second stage, the gain of the final section is always -1 , so $R_5 = R_6$, which means the final form is:

$$\frac{V_o}{V_i} = \frac{-1}{R_1R_4C_1C_2} \bullet \frac{1}{s^2 + s\frac{1}{R_3C_1} + \frac{1}{R_2R_4C_1C_2}} \quad (5.10)$$

This follows the general form of a low pass filter as in Eqn. 5.5. Which, in comparing Eqn. 5.5 and 5.10, the following parameters are found:

$$\begin{aligned}
K &= -1 \\
\omega_o &= \frac{1}{\sqrt{R_1R_4C_1C_2}} \\
f_o &= \frac{1}{2\pi\sqrt{R_1R_4C_1C_2}}
\end{aligned}$$

The quality factor requires some manipulation:

$$\begin{aligned}
 \frac{\omega_o}{Q} &= \frac{1}{R_3 C_1} \\
 Q &= R_3 C_1 \frac{1}{\sqrt{R_1 R_4 C_1 C_2}} \\
 &= R_3 C_1 \frac{1}{\sqrt{R_1 R_4 C_1 C_2}} \bullet \frac{\sqrt{R_1 R_4 C_1 C_2}}{\sqrt{R_1 R_4 C_1 C_2}} \\
 &= R_3 C_1 \frac{\sqrt{R_1 R_4 C_1 C_2}}{R_1 R_4 C_1 C_2} \\
 &= \frac{R_3 \sqrt{R_1 R_4 C_1 C_2}}{R_1 R_4 C_1 C_2}
 \end{aligned}$$

5.3.1.1 Bandpass

Because the overall transfer function of the circuit is known, the feedback path can now be considered. By substituting Eqn. 5.10 into the stage one output Eqn. 5.9, the bandpass section of the biquad may be derived:

$$\begin{aligned}
V_x &= -1 \frac{R_3}{sC_1R_3 + 1} \left(\frac{V_i}{R_1} + \frac{V_o}{R_2} \right) \\
V_x &= \frac{-R_3}{sC_1R_3 + 1} \left(\frac{V_i}{R_1} + \frac{1}{R_2} \cdot \frac{-1}{R_1R_4C_1C_2} \cdot \frac{V_i}{s^2 + s\frac{1}{R_3C_1} + \frac{1}{R_2R_4C_1C_2}} \right) \\
\frac{V_x}{V_i} &= \frac{-R_3}{sC_1R_3 + 1} \left(\frac{1}{R_1} + \frac{-1}{R_1R_2R_4C_1C_2} \cdot \frac{1}{s^2 + s\frac{1}{R_3C_1} + \frac{1}{R_2R_4C_1C_2}} \right) \\
&= \frac{-R_3}{sC_1R_3 + 1} \cdot \left(\frac{R_1R_2R_4C_1C_2(s^2 + s\frac{1}{R_3C_1} + \frac{1}{R_2R_4C_1C_2})}{R_1^2R_2R_4C_1C_2(s^2 + s\frac{1}{R_3C_1} + \frac{1}{R_2R_4C_1C_2})} + \frac{-R_1}{R_1^2R_2R_4C_1C_2} \cdot \frac{1}{s^2 + s\frac{1}{R_3C_1} + \frac{1}{R_2R_4C_1C_2}} \right) \\
&= \frac{-R_3}{sC_1R_3 + 1} \cdot \frac{R_1R_2R_4C_1C_2(s^2 + s\frac{1}{R_3C_1} + \frac{1}{R_2R_4C_1C_2}) - R_1}{R_1^2R_2R_4C_1C_2(s^2 + s\frac{1}{R_3C_1} + \frac{1}{R_2R_4C_1C_2})} \\
&= \frac{-R_3}{sC_1R_3 + 1} \cdot \frac{R_2R_4C_1C_2(s^2 + s\frac{1}{R_3C_1} + \frac{1}{R_2R_4C_1C_2}) - 1}{R_1R_2R_4C_1C_2(s^2 + s\frac{1}{R_3C_1} + \frac{1}{R_2R_4C_1C_2})} \\
&= \frac{-R_3}{sC_1R_3 + 1} \cdot \frac{R_2R_4C_1C_2((s^2 + s\frac{1}{R_3C_1} + \frac{1}{R_2R_4C_1C_2}) - \frac{1}{R_2R_4C_1C_2})}{R_1R_2R_4C_1C_2(s^2 + s\frac{1}{R_3C_1} + \frac{1}{R_2R_4C_1C_2})} \\
&= \frac{-R_3}{sC_1R_3 + 1} \cdot \frac{s^2 + s\frac{1}{R_3C_1} + \frac{1}{R_2R_4C_1C_2} - \frac{1}{R_2R_4C_1C_2}}{R_1(s^2 + s\frac{1}{R_3C_1} + \frac{1}{R_2R_4C_1C_2})} \\
&= \frac{-R_3}{sC_1R_3 + 1} \cdot \frac{s^2 + s\frac{1}{R_3C_1} + \frac{1}{R_2R_4C_1C_2} - \frac{1}{R_2R_4C_1C_2}}{R_1(s^2 + s\frac{1}{R_3C_1} + \frac{1}{R_2R_4C_1C_2})} \\
&= \frac{-R_3}{sC_1R_3 + 1} \cdot \frac{s^2 + s\frac{1}{R_3C_1}}{R_1(s^2 + s\frac{1}{R_3C_1} + \frac{1}{R_2R_4C_1C_2})} \\
&= \frac{-R_3s}{R_3C_1(s + \frac{1}{R_3C_1})} \cdot \frac{s + \frac{1}{R_3C_1}}{R_1(s^2 + s\frac{1}{R_3C_1} + \frac{1}{R_2R_4C_1C_2})} \\
&= \frac{-s}{R_1C_1} \cdot \frac{1}{(s^2 + s\frac{1}{R_3C_1} + \frac{1}{R_2R_4C_1C_2})} \\
&= \frac{s\frac{-1}{R_1C_1}}{s^2 + s\frac{1}{R_3C_1} + \frac{1}{R_2R_4C_1C_2}}
\end{aligned} \tag{5.11}$$

5.3.1.2 Notch Section

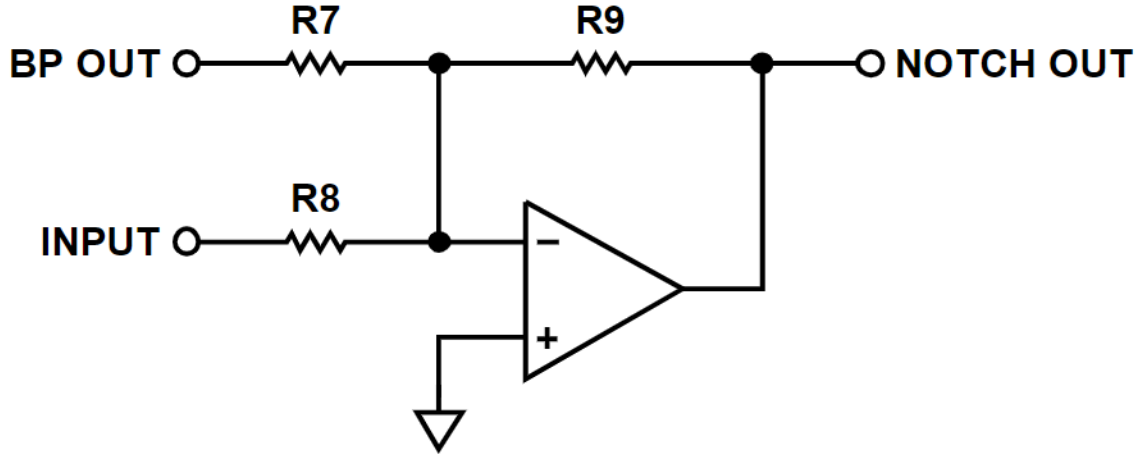


Figure 5.16: Biquad Notch Addition [8]

$$\begin{aligned} \frac{V_x - V_i}{R_7} + \frac{V_x - V_B}{R_8} + \frac{V_x - V_n}{R_9} &= 0 \\ \frac{-V_i}{R_7} + \frac{-V_B}{R_8} + \frac{-V_n}{R_9} &= 0 \\ -R_9 \left(\frac{v_i}{R_7} + \frac{V_B}{R_8} \right) &= V_N \end{aligned}$$

The biquad circuit can be improved by the use of a 4th operational amplifier, in this case a notch filter is required so the configuration shown in Fig. 5.16 is utilized. For the the fourth stage, it is only required to have an inverting summation of the initial input, V_i , and the bandpass output, V_B . Additionally, it is desired that there is unity gain, therefore $R_7 = R_8 = R_9$ can be applied, This results into the following expression:

$$V_N = -(V_i + V_B)$$

Plugging in V_B from Eqn. 5.11 results in:

$$\begin{aligned}
 V_N &= - \left(V_i + V_i \frac{s \frac{1}{R_1 C_1}}{s^2 + s \frac{1}{R_3 C_1} + \frac{1}{R_2 R_4 C_1 C_2}} \right) \\
 \frac{V_N}{V_i} &= \frac{s \frac{1}{R_1 C_1}}{s^2 + s \frac{1}{R_3 C_1} + \frac{1}{R_2 R_4 C_1 C_2}} - 1 \\
 &= \frac{s \frac{1}{R_1 C_1}}{s^2 + s \frac{1}{R_3 C_1} + \frac{1}{R_2 R_4 C_1 C_2}} - \frac{s^2 + s \frac{1}{R_3 C_1} + \frac{1}{R_2 R_4 C_1 C_2}}{s^2 + s \frac{1}{R_3 C_1} + \frac{1}{R_2 R_4 C_1 C_2}} \\
 &= \frac{s \frac{1}{R_1 C_1} - (s^2 + s \frac{1}{R_3 C_1} + \frac{1}{R_2 R_4 C_1 C_2})}{s^2 + s \frac{1}{R_3 C_1} + \frac{1}{R_2 R_4 C_1 C_2}} \\
 &= \frac{-(s^2 + s(\frac{1}{R_3 C_1} - \frac{1}{R_1 C_1}) + \frac{1}{R_2 R_4 C_1 C_2})}{s^2 + s \frac{1}{R_3 C_1} + \frac{1}{R_2 R_4 C_1 C_2}}
 \end{aligned}$$

In the the case that the gain of the overall biquad filter is required to be unity, $R_1 = R_3$ which further simplifies down the equation to:

$$\frac{V_N}{V_i} = \frac{-(s^2 + \frac{1}{R_2 R_4 C_1 C_2})}{s^2 + s \frac{1}{R_3 C_1} + \frac{1}{R_2 R_4 C_1 C_2}} \quad (5.12)$$

In understanding that a notch filter transfer function has the form [23]:

$$T_N = - \frac{s^2 + \omega_o^2}{s^2 + s \frac{\omega_o}{Q} + \omega_o^2} \quad (5.13)$$

Which leads to (from previous manipulation it can be seen that the parameters are of the same form):

$$\begin{aligned}
 K &= -1 \\
 \omega_o &= \frac{1}{\sqrt{R_2 R_4 C_1 C_2}} \\
 f_o &= \frac{1}{2\pi \sqrt{R_2 R_4 C_1 C_2}} \\
 Q &= \frac{\sqrt{R_2 R_4 C_1 C_2}}{R_4 C_1 C_2}
 \end{aligned}
 \tag{5.14}$$

5.3.2 Design of the Biquad Filter

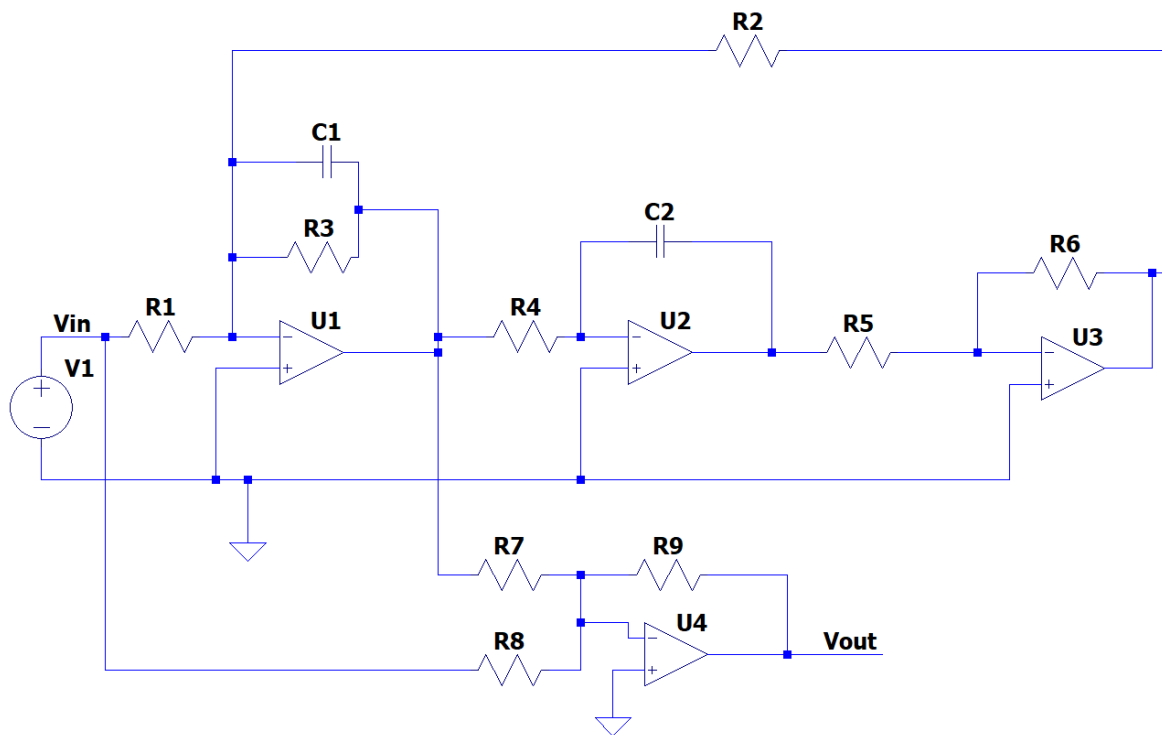


Figure 5.17: Notch Biquad Filter

A biquad circuit can be orthogonally tuned, meaning that certain components can be determined in order without interfering with future component selections inside of the circuit [23].

As in Fig. 5.17, R_2 can be picked to determine the specific cutoff frequency required. R_3 can be adjusted to determine the Q of the filter. Then R_1 is adjusted to determine the overall gain of the filter. Following Example 5.4 in [23], a 60Hz notch filter is required to remove any possible power supply noise within the audio signal. As such $f_o = 60\text{Hz}$. The specified bandwidth of the filter should be 10Hz, as signals outside the range of any 60Hz noise should not be attenuated. Additionally, in the case of this stage and all filters designed in this paper, the gain shall be unity, because the audio signal strength is sufficient for the input into the amplifier section. Due to this, this means that $R_1 = R_3$. It is known that:

$$Q = \frac{\omega_o}{BW} \quad (5.15)$$

Where $BW = \omega_2 - \omega_1$, which are the two 3 dB points of the notch filter. This results in the following value of Q :

$$\begin{aligned} Q &= \frac{\omega_o}{BW} \\ &= \frac{60}{10} \\ &= 6 \end{aligned}$$

R_2 is picked to be 10k Ω for no particular reason, however it will allow for an easy scaling of the other resistors. Given this, and assuming that $R_2 = R_4$ and $C_1 = C_2$, the capacitors can be calculated by using the cutoff frequency Eqn. 5.14:

$$f_o = \frac{1}{2\pi\sqrt{R_2R_4C_1C_2}}$$

$$60 = \frac{1}{2\pi\sqrt{(10E3)(10E3)C_{1,2}^2}}$$

$$60 = \frac{1}{2\pi(10E3)C_{1,2}}$$

$$C_{1,2} = 0.2652E - 6$$

The summation stage has all the same resistors, so this means that $R_7 = R_8 = R_9$ which they are utilized as $10\text{k}\Omega$ resistors to reduce the bill of materials. Additionally, stage 3 is only used as an inversion stage, so $R_5 = R_6$ and these are also $10\text{k}\Omega$ for the aforementioned reason. To determine R_1 and R_3 , it is known from [23] that $R_1 = QR_2$. Therefore, $R_1 = R_3 = 60\text{k}\Omega$. After finding the nearest real component sizes of $C_1 = C_2 = 0.02652\mu\text{F} \approx 0.27\mu\text{F}$ and $R_1 = R_3 = 60\text{k}\Omega \approx 60.4\text{k}\Omega$. The complete 60Hz notch schematic is shown in Fig. 5.18.

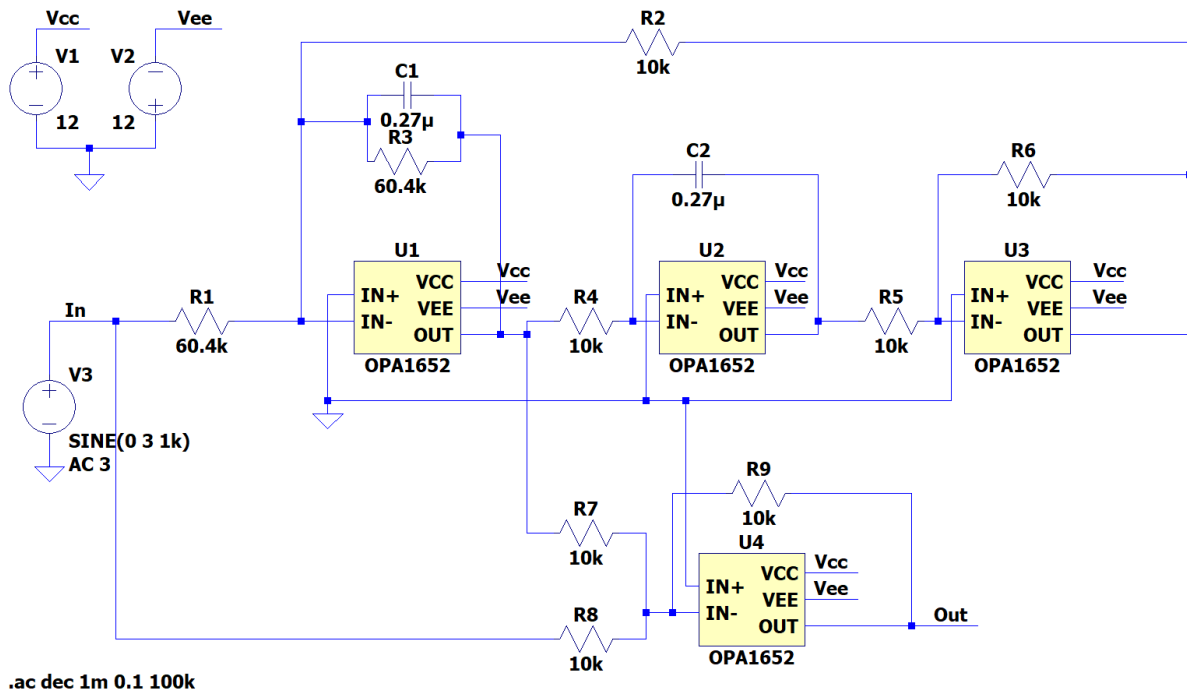


Figure 5.18: LTSpice Notch Schematic

5.3.3 60 Hz Notch Filter Simulation

The circuit in Fig. 5.18, had an AC frequency sweep performed upon it. The output of the sweep is shown in Fig. 5.19.

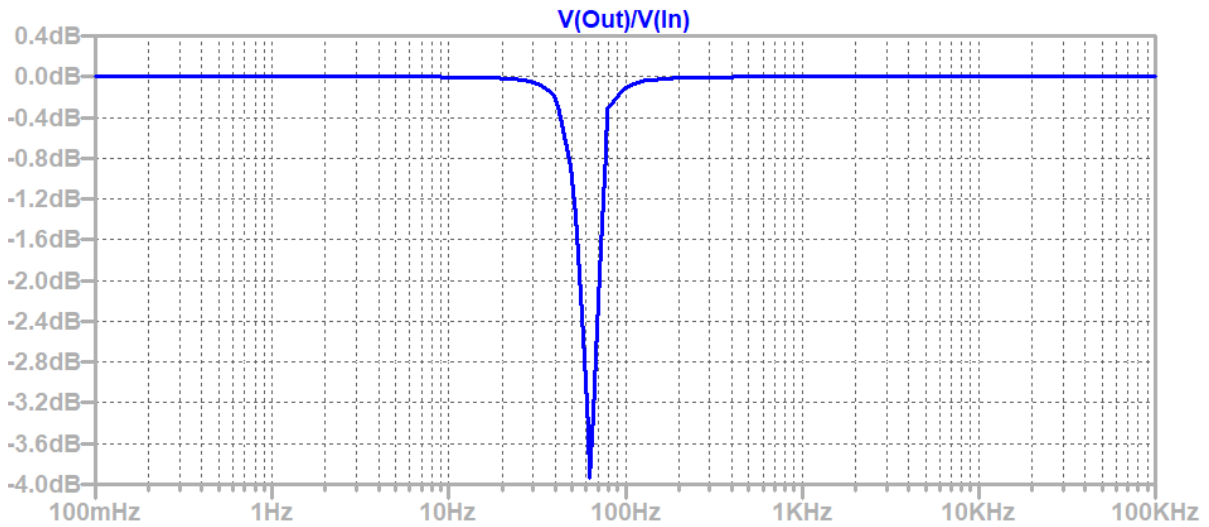


Figure 5.19: 60Hz LTSpice Simulation Output

On closer inspection of the output, the two 3 dB points of the filter were found to be 59.4 Hz and 66.6 Hz. Therefore the bandwidth is calculated to be $BW = 66.6\text{ Hz} - 59.4\text{ Hz} = 7.2\text{ Hz}$. Additionally, the center frequency was found to be 63 Hz. These values are slightly off the theoretical bandwidth of 10 Hz and the center frequency of 60 Hz; however, this is most likely due to the component rounding and the use of non-ideal operational amplifier simulation models.

Chapter 6

Amplifier Overview

There are two different high power audio amplifiers utilized in the project, a speaker amplifier and a headphone amplifier. The two stages are utilized such that either headphones or speakers can be listened to off of the receiver.

6.0.1 Speaker Amplifier

The amplifier utilized in this design was a TPA3251 class D amplifier from Texas Instruments. It was mainly chosen for its high output power and efficiency. Most audio amplifiers are based on a class A or AB transistor amplifier. The traditional amplifier classes (A, B, AB, and C) are all categorized by how long the switching elements are conducting. Class A amplifiers are the most linear amplifier design from the traditional topologies, however they are horribly inefficient [24]. The class B amplifier design is more efficient than class A, but there are non-linearity issues near the zero crossing point of the amplifier due to its push-pull construction. Class AB was designed to be the best of both worlds, with better efficiency and linearity at the zero crossing point. A class AB amplifier is still only 50 – 60% efficient, which if an equivalent output power of the TPA3251 was utilized for a class AB amplifier, it would require

around 500W of total power to get the same 350W output.

6.0.1.1 Class D Amplifier Basics

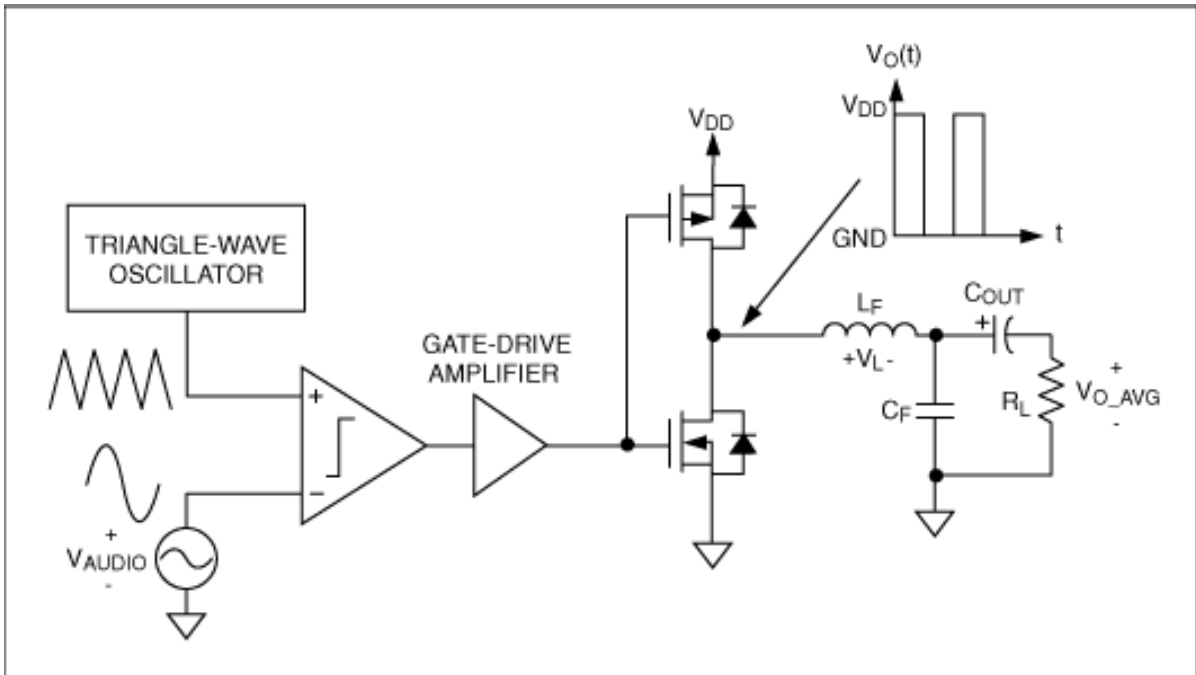


Figure 6.1: Class D Amplifier Overview [9]

The Class D amplifier forms a pulse width modulated (PWM) signal by comparing a triangle wave to the incoming sinusoidal audio signal. This comparison and therefore generation of the PWM can be visualized in Fig. 6.2.

The PWM output is then fed into a CMOS amplifier stage. This stage directly connects the high power input supply to the CMOS stage, meaning that any noise in the power rail will appear on the output signal. There are ways to deal with this issue, however their implementations lead to other issues. To convert the PWM signal back into a sinusoid to output to the speakers, a 2^{nd} order LC filter stage is generally used. As the LC filter is a low pass filter, it removes the high frequency content of the PWM output. From Fourier Analysis, an ideal square

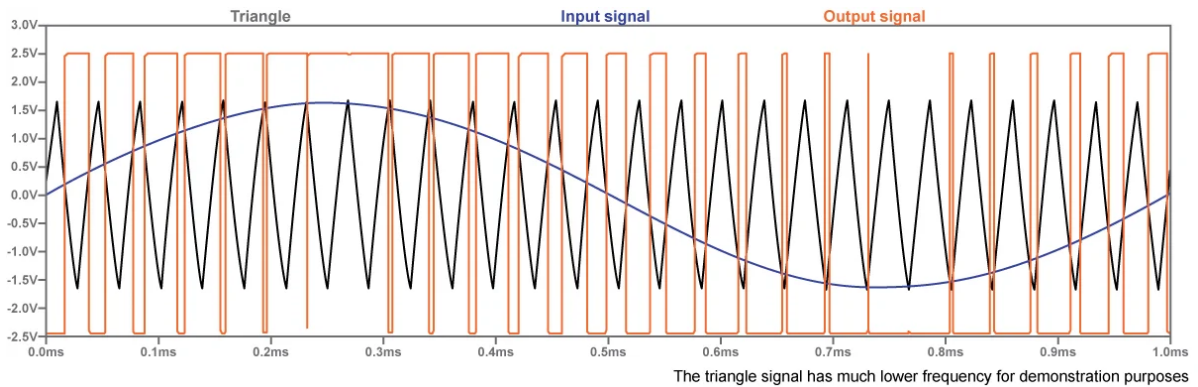


Figure 6.2: PWM Generation for Class D Amplifier [10]

wave is known to be comprised of infinitely many frequencies, with the higher frequency-low amplitude portions comprising most of the sharp edges. The low pass filter will filter out the high frequency components and reduce the square wave to its low frequency, fundamental components.

6.0.1.2 TPA3251 Design Considerations

The main challenge with the TPA3251 is the power supply; however, that will be covered in Section 7.0.2. The other main consideration of the amplifier is the design of the LC filter. The filter design was based off of [25] which included suggestions for the inductor and capacitor values. As an 8Ω output impedance is targeted, a $15\mu\text{H}$ inductor and a $0.47\mu\text{F}$ capacitor were used. This combination was picked due to the components resulting in a $Q = 0.708$, which is very close to the critically damped value of $Q = 0.707$. This combination, and therefore value of Q , allows for maximum passband gain flatness. The entire output filter is shown in Fig. 6.3.

Additionally, to use the output of the TPA3251 in a Bridge Tied Load (BTL) mode, the inputs of the TPA3251 have to be differential and not single ended. As the signal chain in the filter section is single ended, a single to differential converter must be utilized. The single to differential converter as shown in Fig. 6.4, utilizes two inverting operational amplifiers to

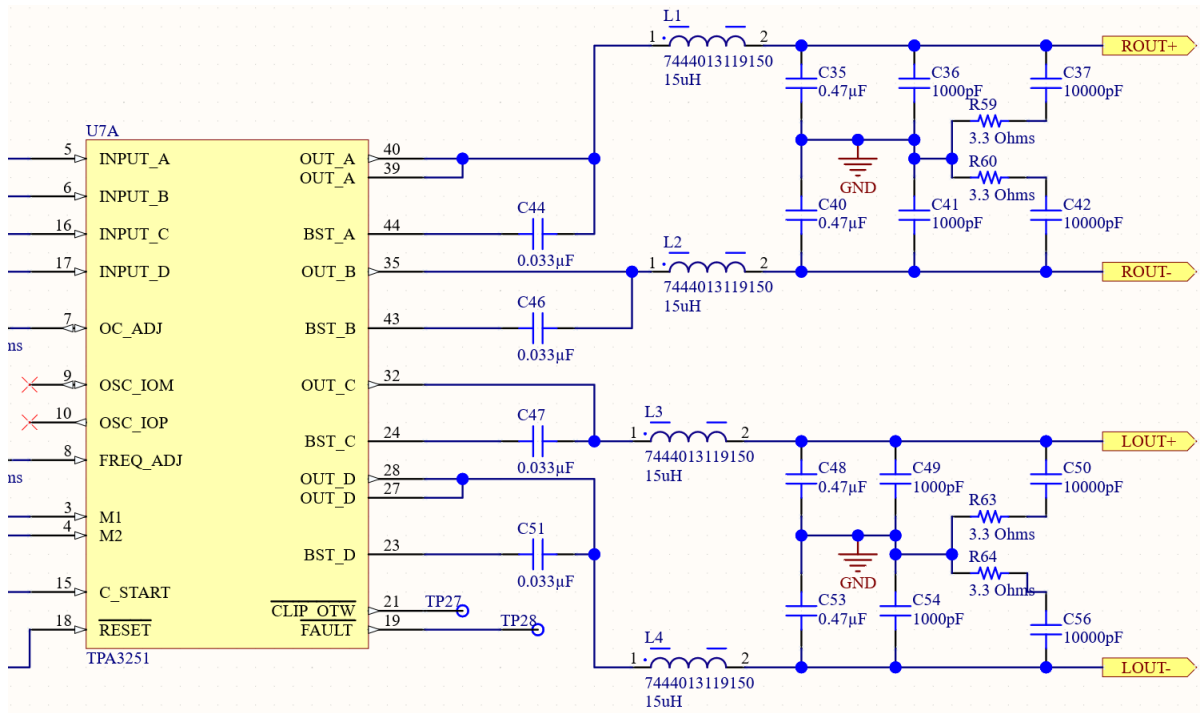


Figure 6.3: Output Filter of TPA3251

negate and buffer the signal. The output of this is then fed into a voltage follower stage of operational amplifiers to isolate the speaker amplifier from the headphone amplifier.

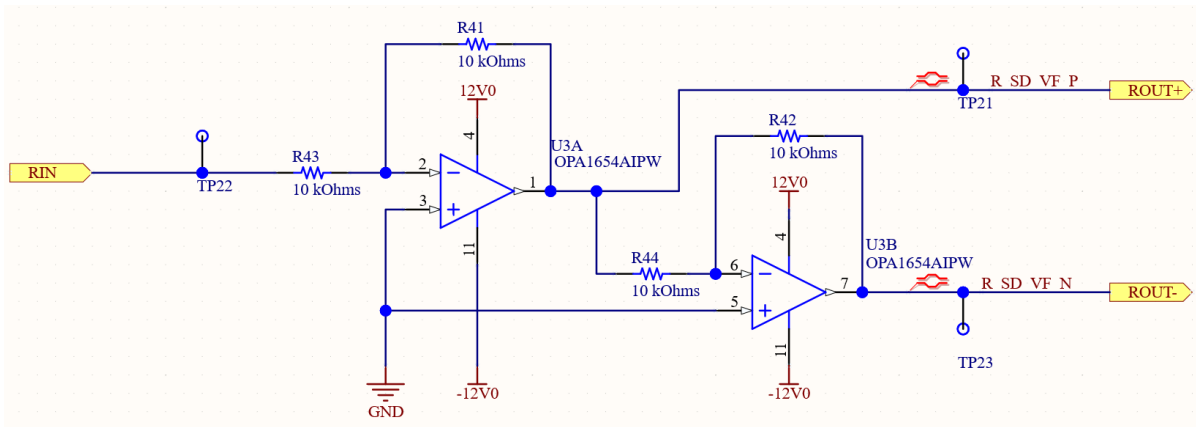


Figure 6.4: Single to Differential Converter

6.0.2 Headphone Amplifier

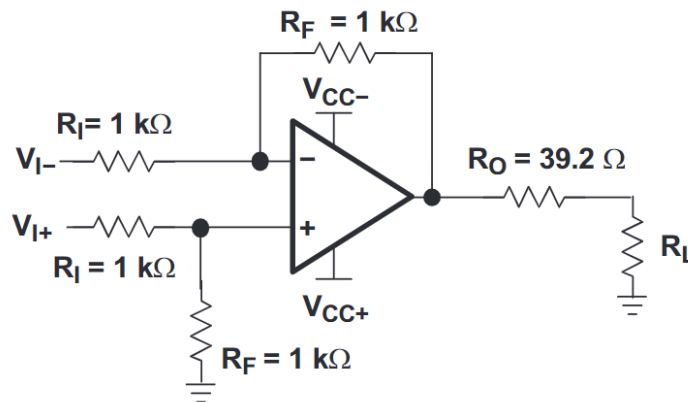


Figure 6.5: TPA6120A2 Schematic (One Channel Shown) [11]

The headphone amplifier used is the TPA6120A2, internally it consists of two high power operational amplifiers. As headphones are generally not high power devices, a traditional switching amplifier is not required. The main design consideration of the TPA6120A2 is the calculation of the input and feedback resistors. The amplifier is generally setup as a differential amplifier. The transfer function of which is known to be $V_o = \frac{R_F}{R_I} (V_{I+} - V_{I-})$. Because the inputs are differential, meaning $V_{I+} = -V_{I-}$, the transfer function can be reduced to $V_o =$

$\frac{R_F}{R_I}(2V_{I+})$. As the power supply for this amplifier stage is only $\pm 12\text{ V}$, the gain must be reduced from the standard 2 V/V . To not saturate the amplifier, the output voltage is set at a maximum of 9.5 V_{PP} and the input is noted to be 5.6 V_{PP} . Additionally, R_I is chosen to be $1\text{ k}\Omega$ due to convenience. As such, the equation to find the feedback resistor is setup:

$$V_o = \frac{R_F}{R_I}(2V_{I+})$$

$$9.5 = 2 \bullet 5.6 \bullet \frac{R_F}{1E3}$$

$$R_F = 848.21$$

The next closest resistor size is 845Ω . The final configuration is shown in Fig. 6.6.

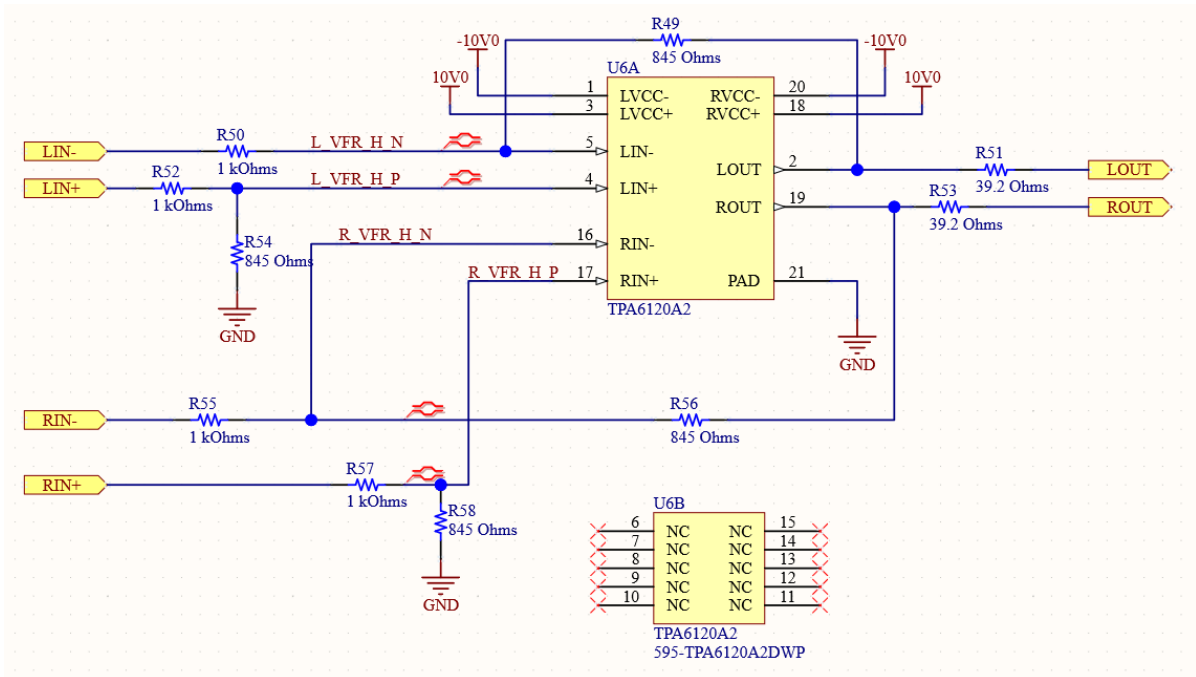


Figure 6.6: Headphone Amplifier Schematic

Chapter 7

Power Supply Design

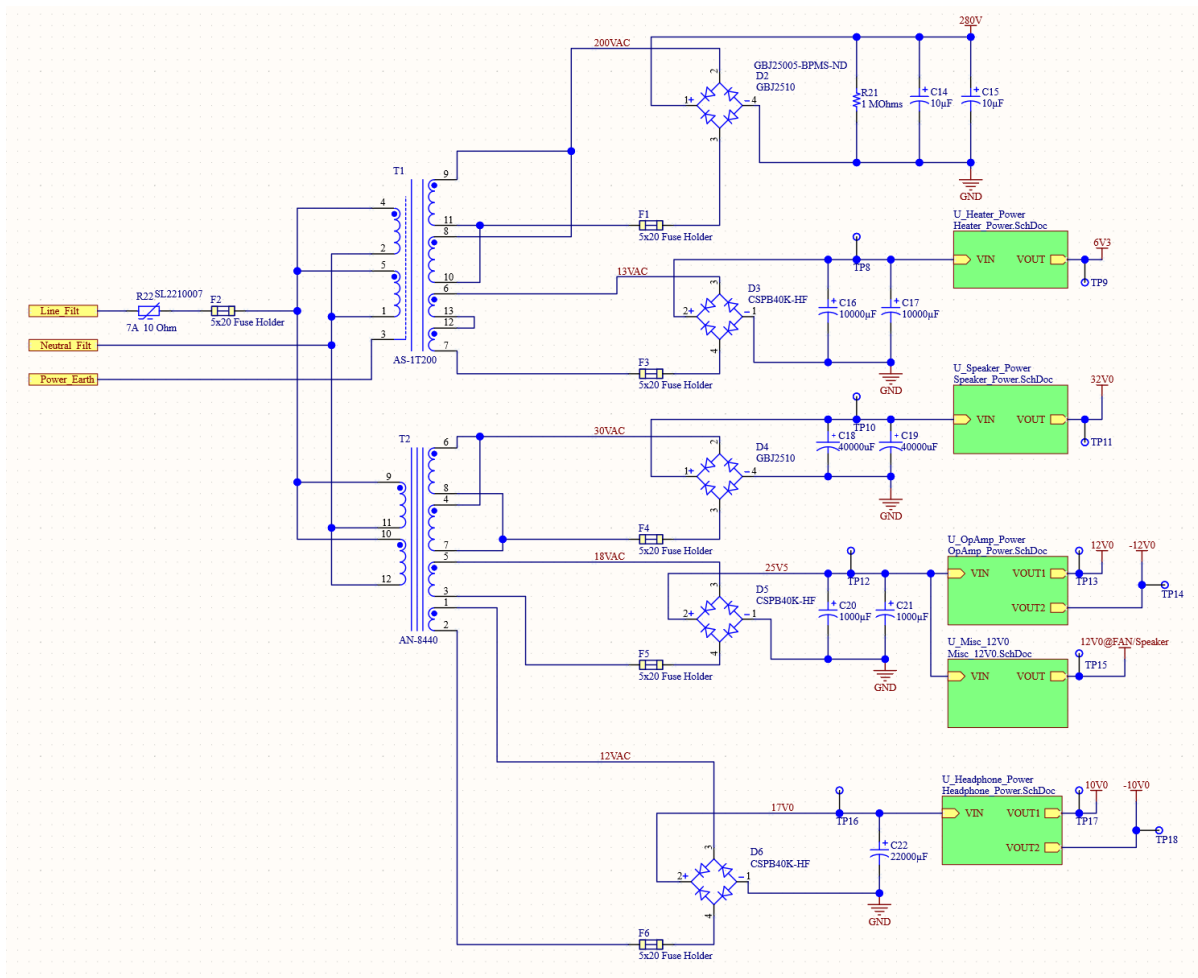


Figure 7.1: Power Supply Top Level Detailed

The power supply is comprised of two transformers which perform vastly different tasks. One transformer is utilized to get the high voltage and heater supplies for the preamplifier vacuum tubes, while the other transformer is utilized for the high power for the TPA3251 and the remainder of the board power. The estimated power draw, assuming 100% efficiency is around 400 W. However, if a worst case efficiency of 80% is utilized the overall worst case power draw is about 500 W. This yields the wall current draw being around 4.2 A. This allows for proper sizing of the main fuse and thermistor. The thermistor is utilized for limiting inrush current due to the 800 VA transformer. Due to the large size of the transformer utilized for the high power section, there is an associated inrush current that can be over 100 A. As plugging this directly into a wall outlet would most certainly cause a breaker to trip, the inrush current must be limited. This is done by a thermistor, which is a negative temperature coefficient resistor. In the case of the thermistor used, the SL22 10007, its resistance upon startup is $10\ \Omega$ and will reduce its resistance to a fraction of that (depending on the load current).

7.0.1 Vacuum Tube Power Supply

The vacuum tube supply is only utilized for the preamplifier section of the board, as such a high voltage-low current supply and low voltage-high current heater supply are required. From Section 4.2, the overall current draw of the preamplifier stage (minus the heater) is $2 \cdot (1.4\ \text{mA} + 2.8\ \text{mA}) = 8.4\ \text{mA}$. The typical heater current draw from the JJ ECC83s is 300 mA from a 6.3 V source [2]. As such, the AnTek AS-1T200 transformer was picked. This transformer is quite over-sized for its intended use case, but for future use cases a higher power transformer was chosen. The transformer has four total outputs, two $200\ \text{V}_{\text{AC}}@250\ \text{mA}$ and two $6.3\ \text{V}_{\text{AC}}@3\ \text{A}$ outputs. The $200\ \text{V}_{\text{AC}}$ transformer was chosen because after rectification, the output voltage is approximately $200\ \text{V}_{\text{AC}} \cdot \sqrt{2} = 282\ \text{V}_{\text{DC}}$. The reservoir capacitors for the

stage can be computed by Eqn. 7.1.

$$C = \frac{I_{Load}}{2 \cdot f \cdot \Delta V} \quad (7.1)$$

Where $f = 60\text{Hz}$ and ΔV is the desired ripple voltage on the power supply rail. The overall ripple voltage for this stage is desired to be 5% of the overall output voltage. The load current, I_{Load} , is designed for a worst case value of 20mA. This yields in a calculation of:

$$\begin{aligned} C &= \frac{20E - 3}{2 \cdot 60 \cdot (280 \cdot 0.05)} \\ &= 11.9E - 6 \end{aligned}$$

This is the minimum capacitance required to yield the requirements of the design, as such two of $10\mu\text{F}$ capacitors are placed in parallel to exceed the design specification.

7.0.1.1 Heater Supply

The heater supply is the more challenging of the two supplies for the preamplifier, as the tube heaters are susceptible to heater hum. This is generally solved in most designs by twisting the two heater supply wires together. However, because this project is to be implemented onto a printed circuit board (PCB), this is unable to happen. The best solution is to convert the AC heater supply into a DC supply, as the regulators will reduce the power supply noise. The parameter for this is called Power Supply Rejection Ratio (PSRR) and is a measure of how well a regulator will reject a ripple on the regulator input.

Because a conversion from AC to DC is required for the heater supply, the output voltage will be approximately $6.3 V_{AC} \cdot \sqrt{2} = 8.9 V_{DC}$. Which, if utilizing a linear regulator and ac-

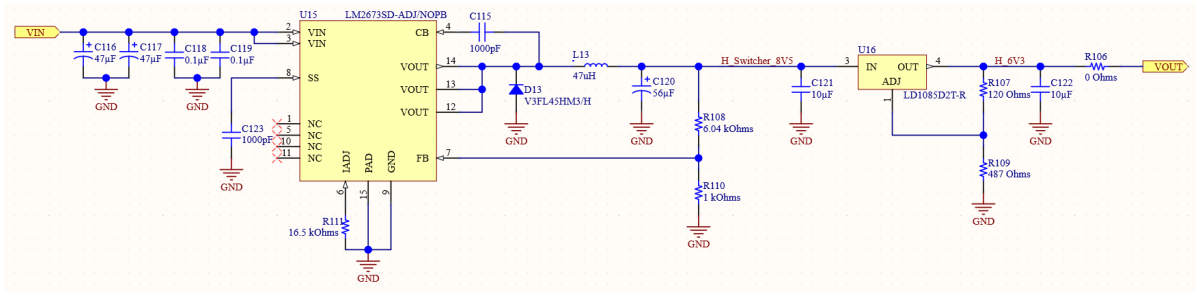


Figure 7.2: Heater Power Supply

counting for ripple voltage on the line, it would be very close to the minimum dropout voltage. As such the two 6.3 V_{AC} outputs are wired in series to achieve a $12.6\text{ V}_{AC}@3\text{ A}$ output. The resulting DC voltage is $12.6\text{ V}_{AC} \cdot \sqrt{2} = 17.81\text{ V}_{DC}$. A linear regulator would dissipate quite a bit of power in dropping 17.81 V_{DC} to 6.3 V_{DC} , therefore a switching regulator into a linear regulator will be used. The switching regulator, an LM2673, takes the incoming 18 V and reduces it down to 8.5 V . This is then used to feed the LD1085 linear regulator to supply 6.3 V to the heaters.

7.0.2 Speaker Power Supply

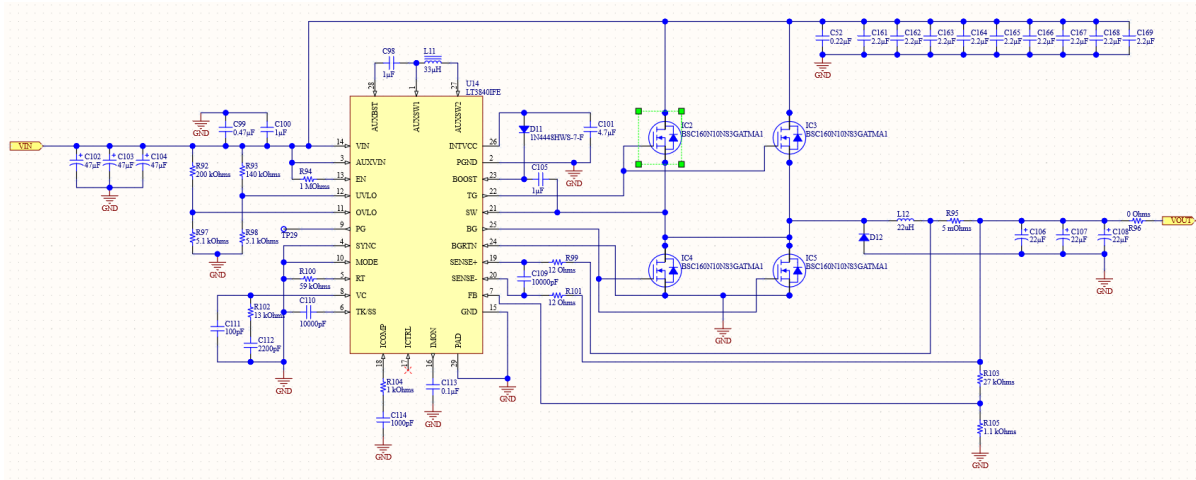


Figure 7.3: Speaker Power Supply

The speaker power supply must be able to supply up to 350 W of power to the TPA3251. As the TPA3251 is being ran off of 32 V, this means that it will draw a maximum of approximately 11 A. A switching power supply is the only solution to achieve a regulated output voltage at this current output. The LT3840 was utilized as it is only a switching controller and relies on external switches, MOSFETs in this case, to perform the actual high and low side switching. This means that the only limiting factor in the output current is the transformer and the maximum drain current on the MOSFETs. A power MOSFET with a drain current rating of 42 A and a maximum $V_{DS} = 100\text{ V}$ was utilized.

7.0.3 Operational Amplifier Supply

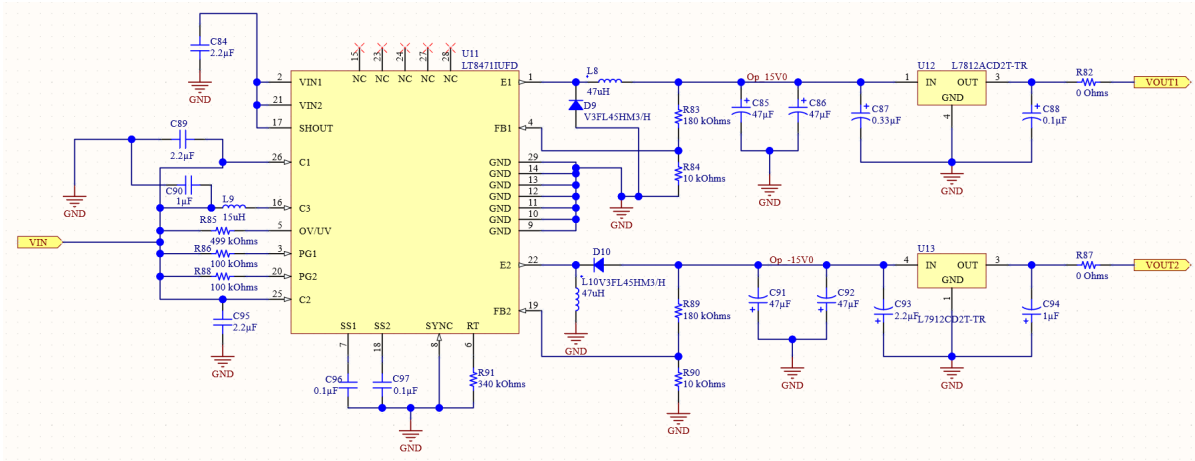


Figure 7.4: Operational Amplifier Power Supply

The operational amplifiers were ran off of $\pm 12\text{V}$, and as they are being used for the audio signal chain, are required to be a very clean power supply rail. As such, a switching regulator, the LT8471, will generate a positive and negative supply which is followed by two linear fixed regulators. One regulator each for the positive and negative rails. As these operational amplifiers are utilized only as filters or buffer stages into other operational amplifiers, the overall current sourcing capabilities of this power supply is negligible.

7.0.4 Miscellaneous 12 V Power Supply

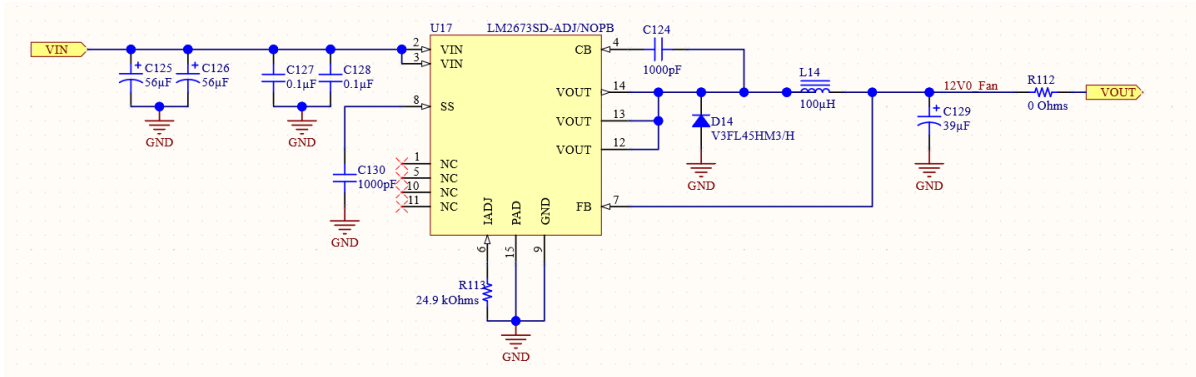


Figure 7.5: Miscellaneous 12 V Power Supply

As the TPA3251 and optional case fan require +12 V, another power supply was required as to not introduce any noise into the power supply for the operational amplifiers. The +12 V input on the TPA3251 is only utilized for the digital section of the amplifier, therefore it does not need a ultra-clean power supply rail. Due to this, a switching regulator output is sufficient for the TPA3251; this is additionally the case for the case fan. This was done with the LM2673, which was also used in the heater supply, as this minimized the bill of materials.

7.0.5 Headphone Amplifier Power Supply

The headphone amplifier can draw a maximum of 700 mA per output channel, as such the total current required for power supply is non-negligible. Additionally, since the power supply is being utilized for an analog portion of the audio chain, the noise on the power supply rail does matter. As such, the same methodology as used on the operational power supply was used. A LT8471 switching regulator was utilized to generate the positive and negative rails. These are then cascaded into two adjustable linear regulators.

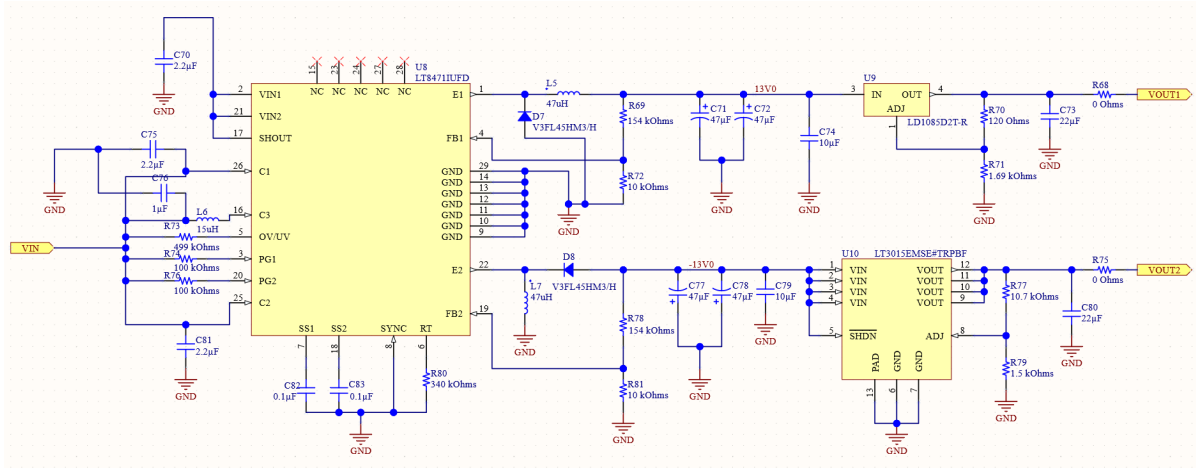


Figure 7.6: Headphone Amplifier Power Supply

Chapter 8

Conclusion

The audio receiver is currently fully simulated and designed with all real-world parts picked out; however, the layout was unable to be completed in time for the paper. As such, the validity of the overall design has not been verified. Once the layout has been completed, a complete board bringup and troubleshooting will commence. Once an initial prototype is brought to fully working order, a second board revision will be completed which will hopefully cut down on the overall board cost.

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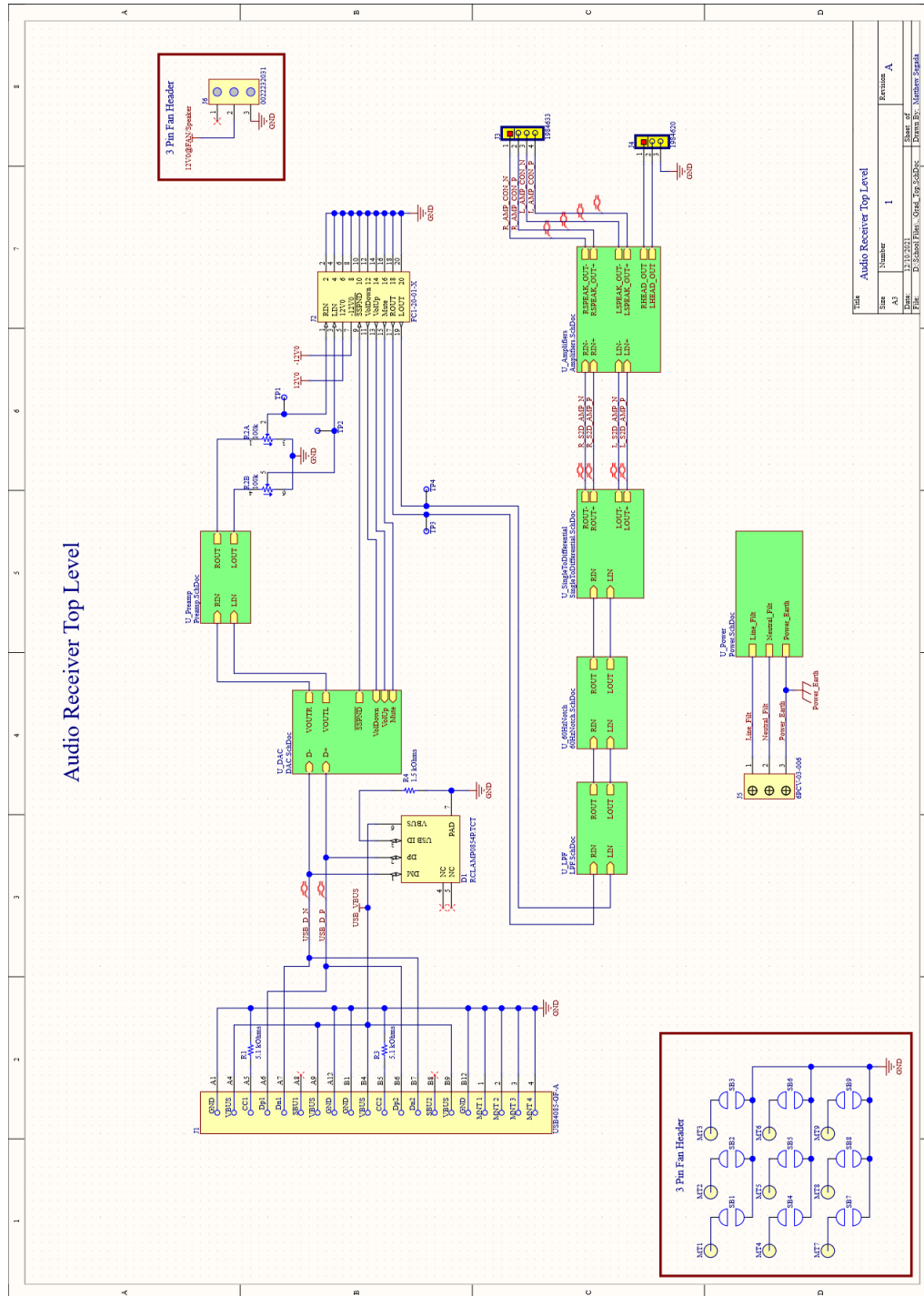
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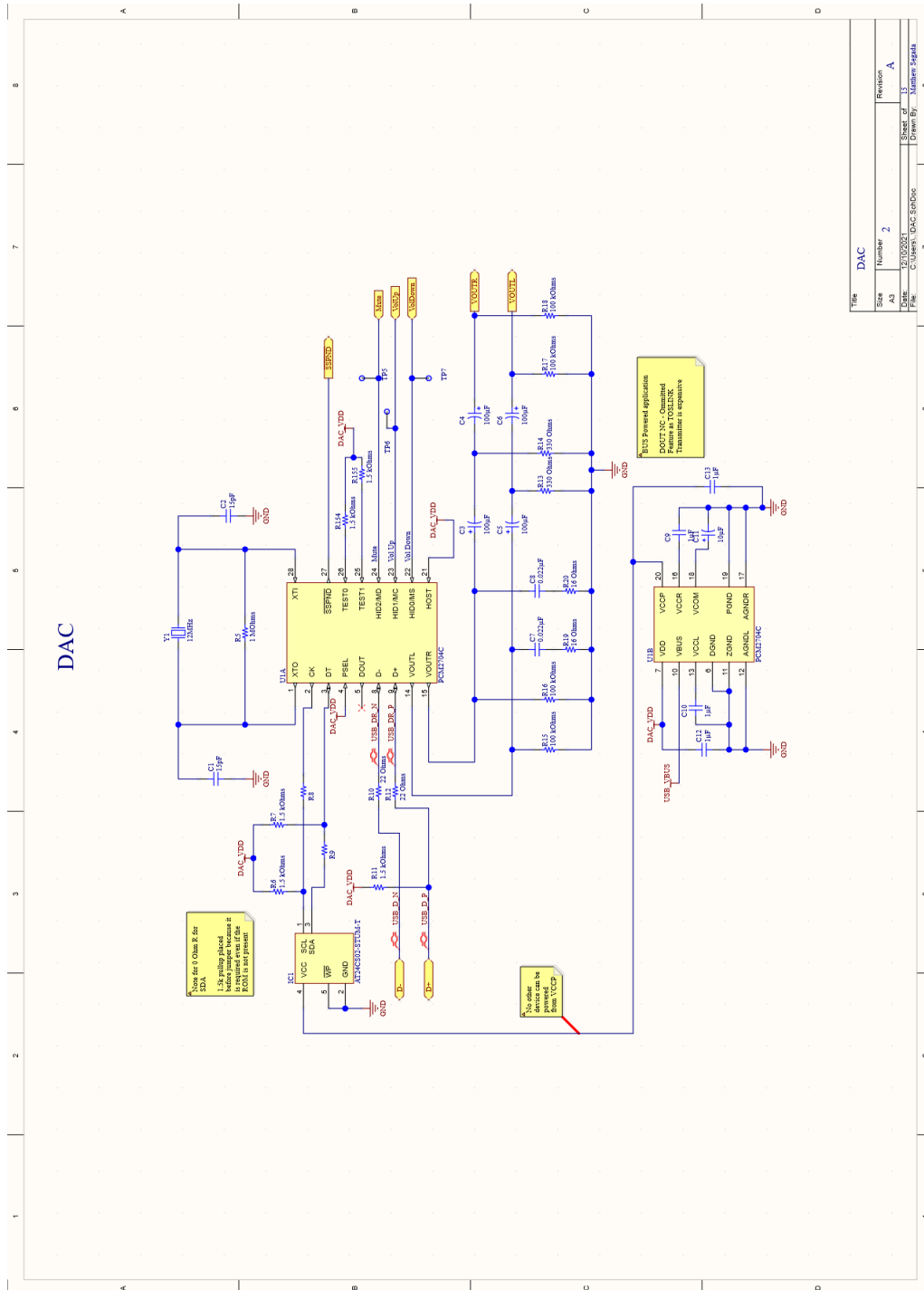
Appendix I

Altium Schematics

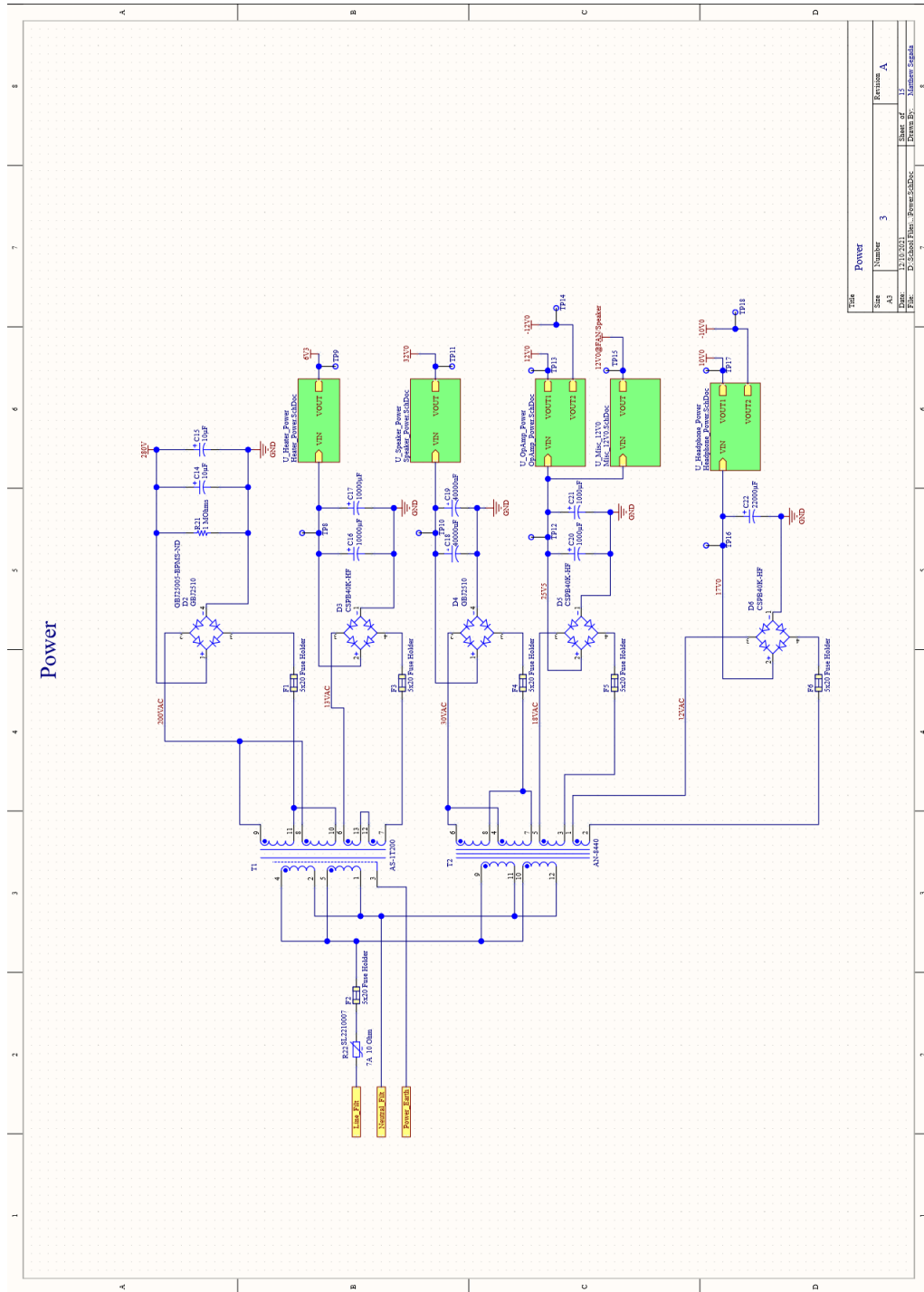
I.1 Audio Receiver Top Level



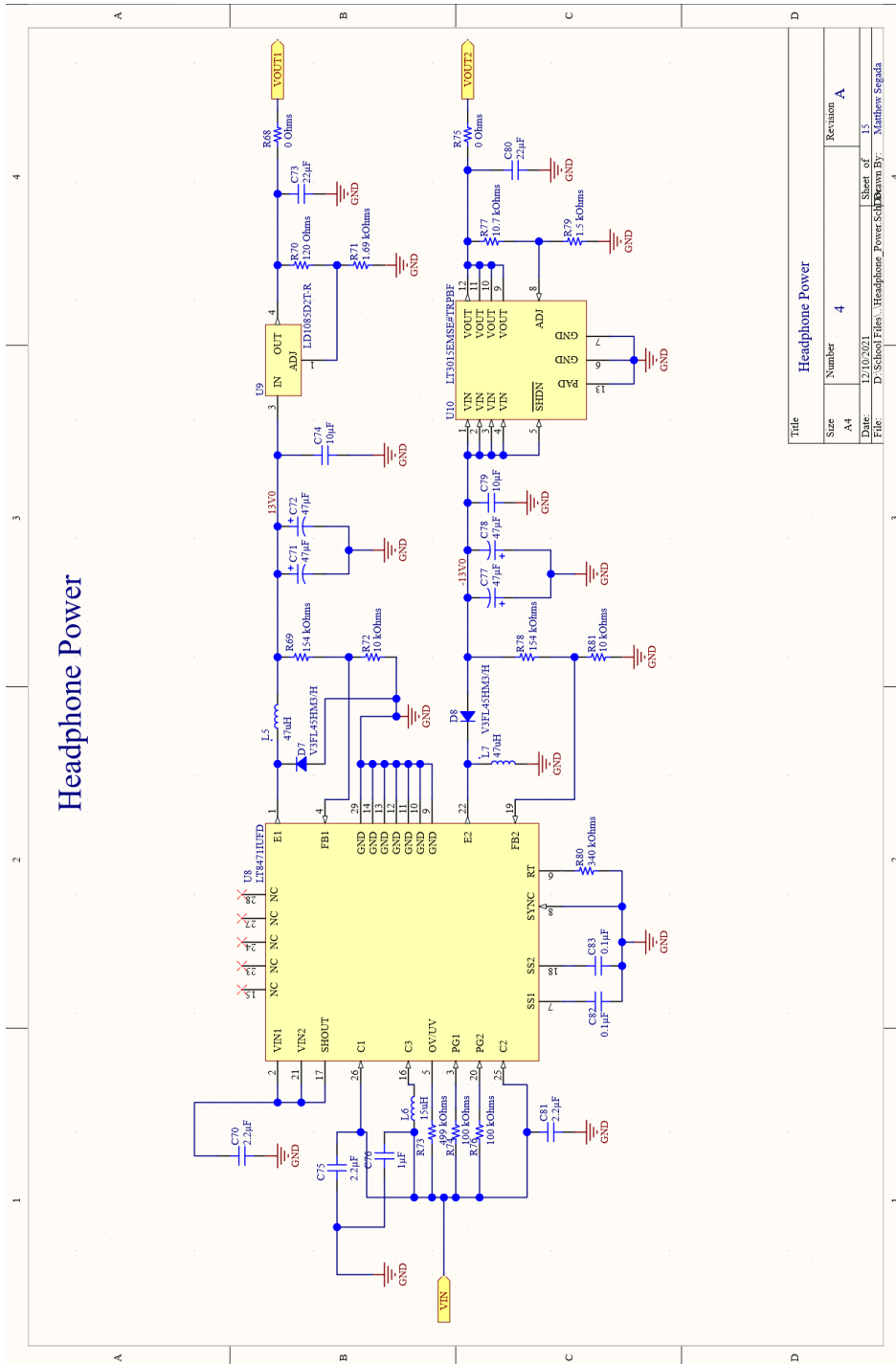
I.2 Digital to Analog Converter



I.3 Power Top Level

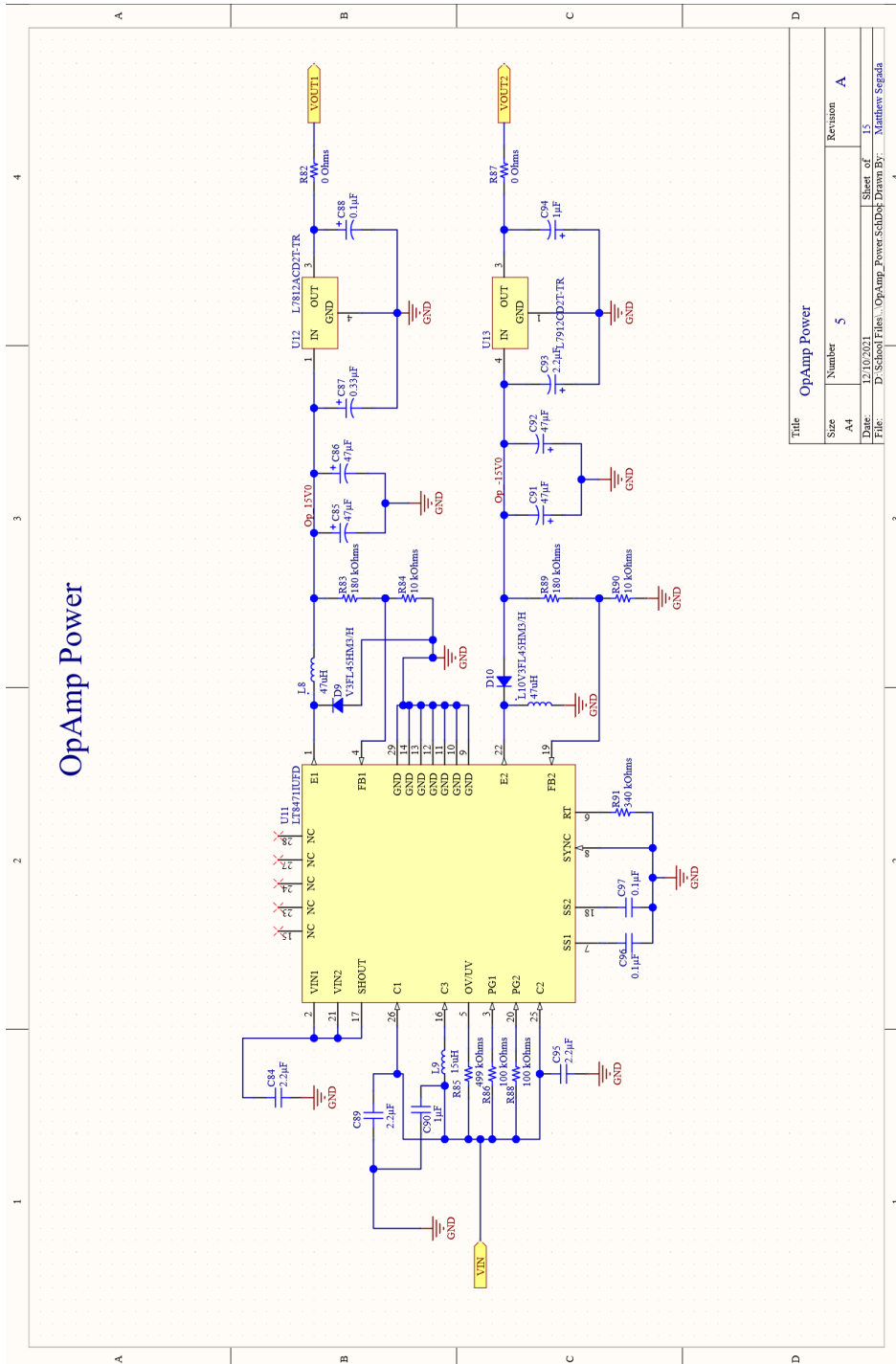


I.4 Headphone Power

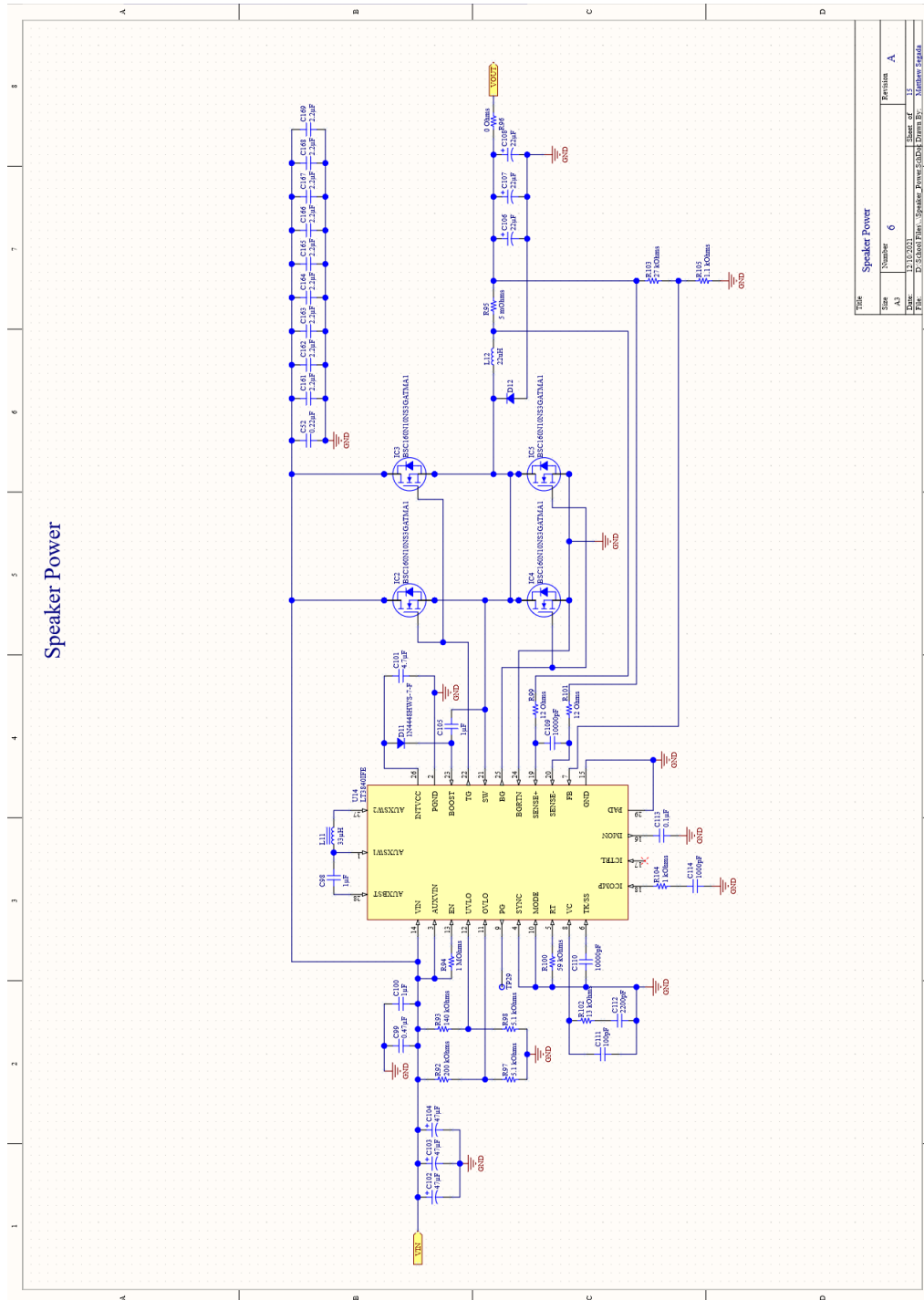


Title		Revision	
Headphone Power		Number	4
Size	A4	Sheet of	15
Date	13/10/2021	Drawn By:	Martians Sagada

I.5 Operational Amplifier Power

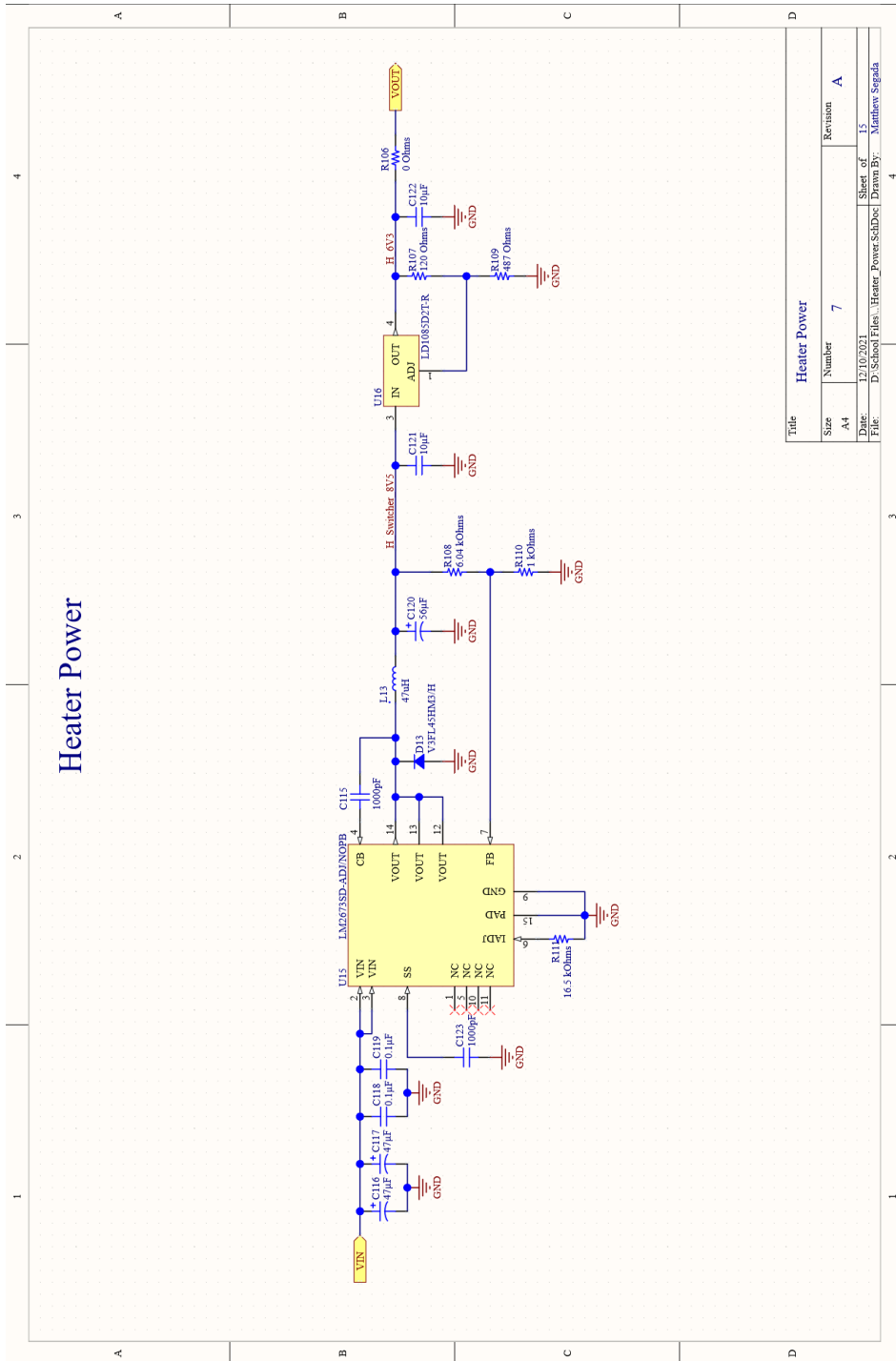


I.6 Speaker Power

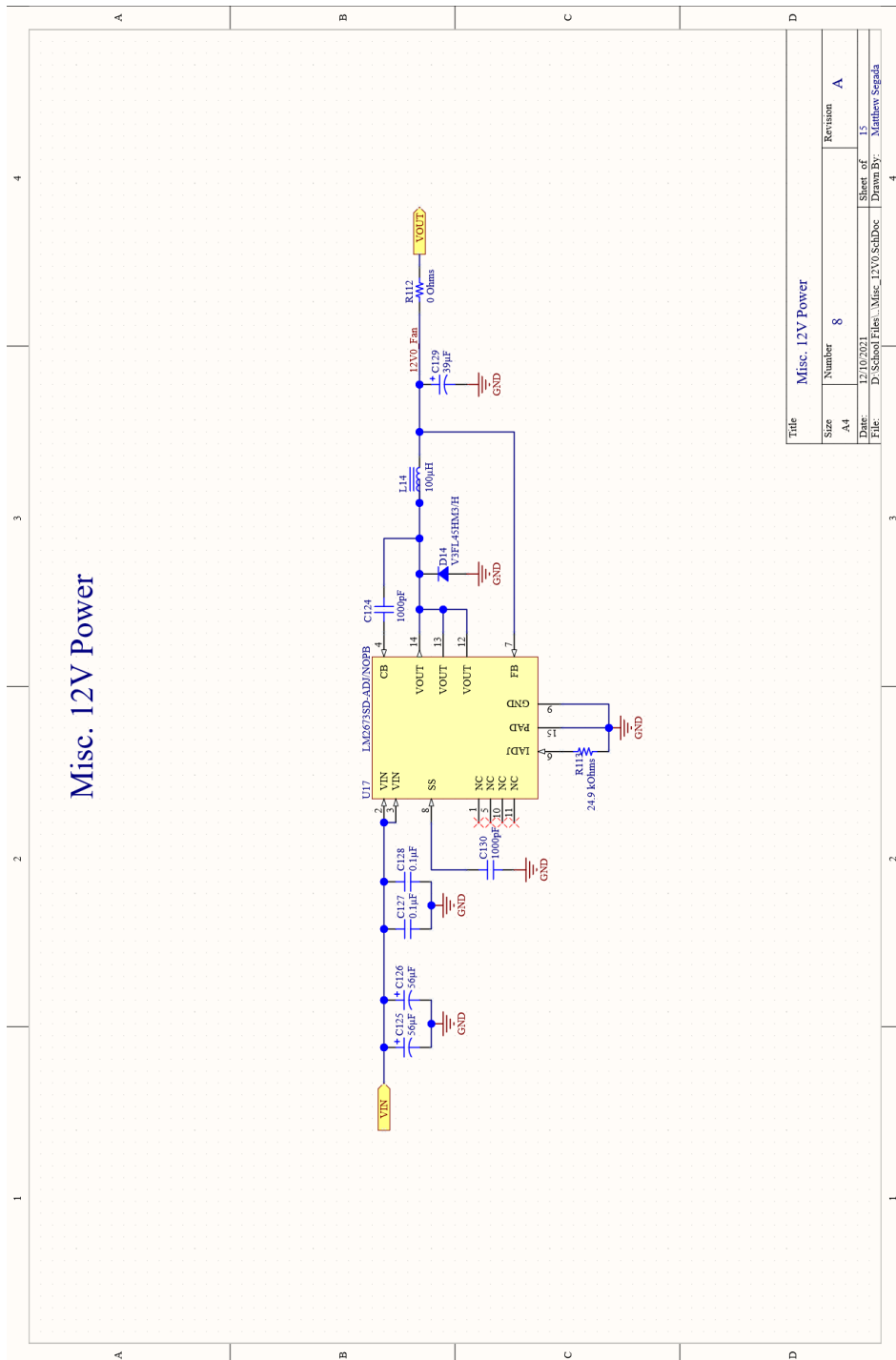


Title		
Speaker Power		
Size	Number	Revision
A3	6	A
Doc	1337333	Sheet of
Proj	25-20051-001 - Speaker Power - 20051-001 Rev. B	Number of Pages
		1

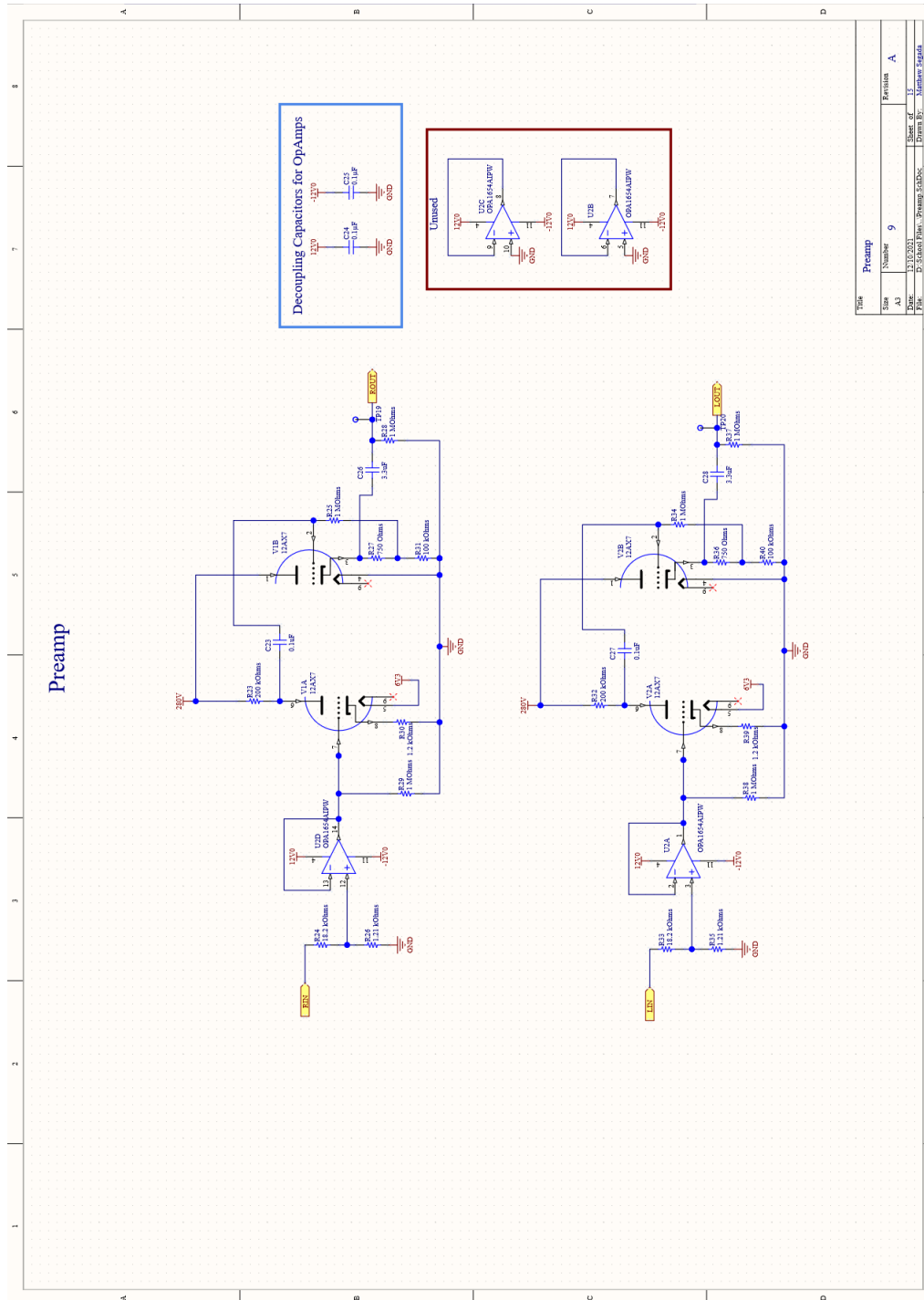
I.7 Heater Power



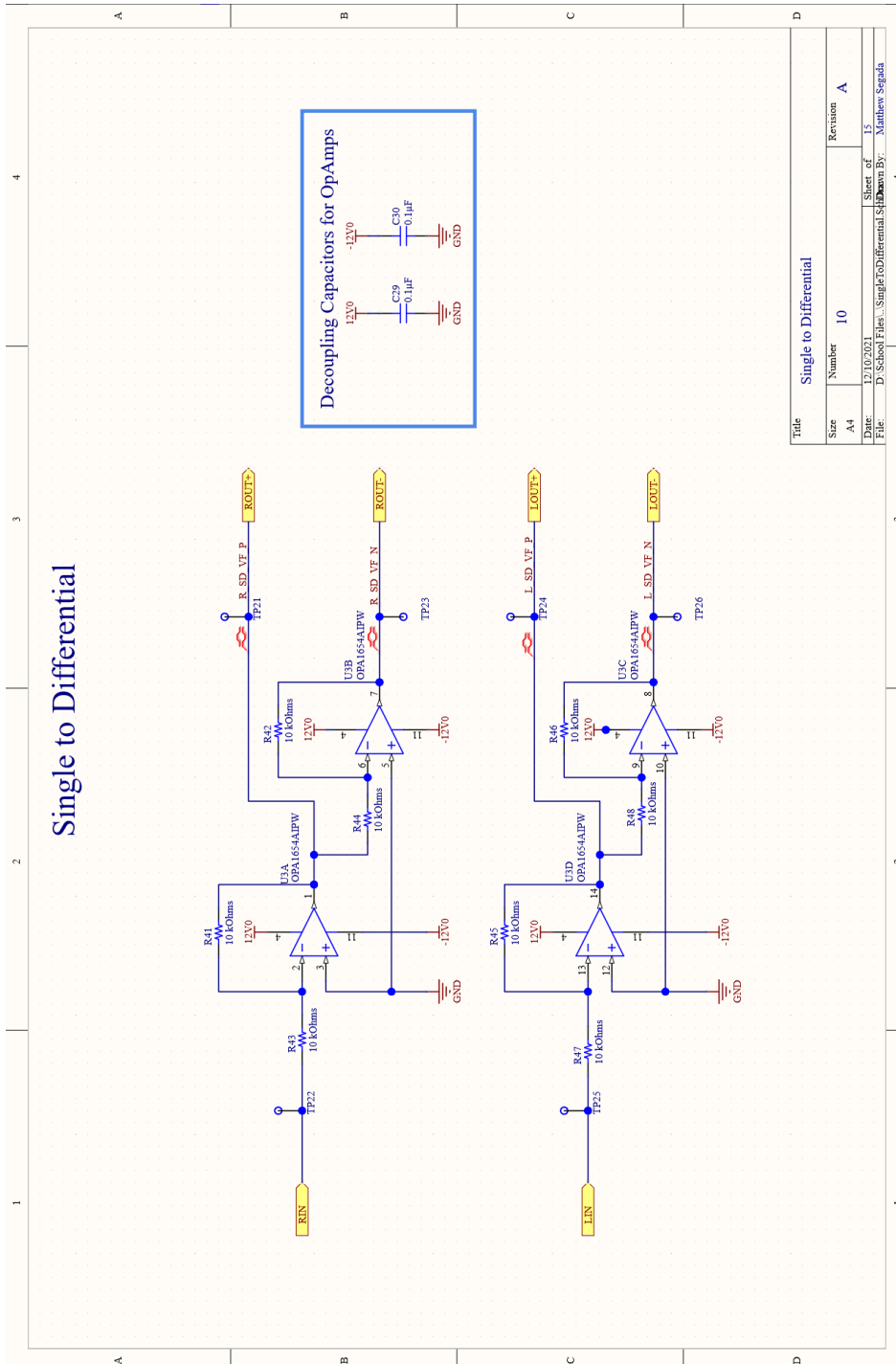
I.8 Miscellaneous 12 V Power



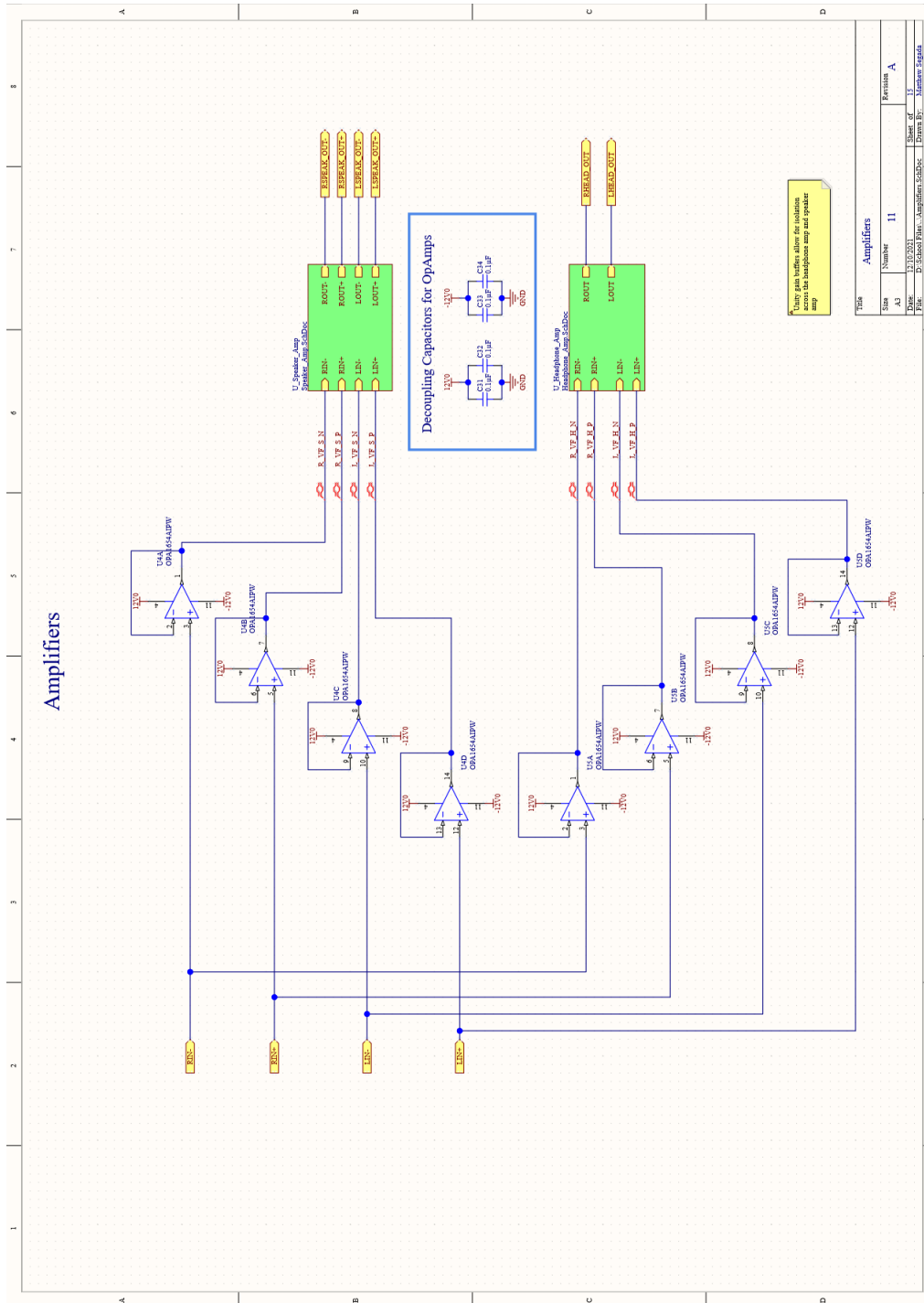
I.9 Preamplifier



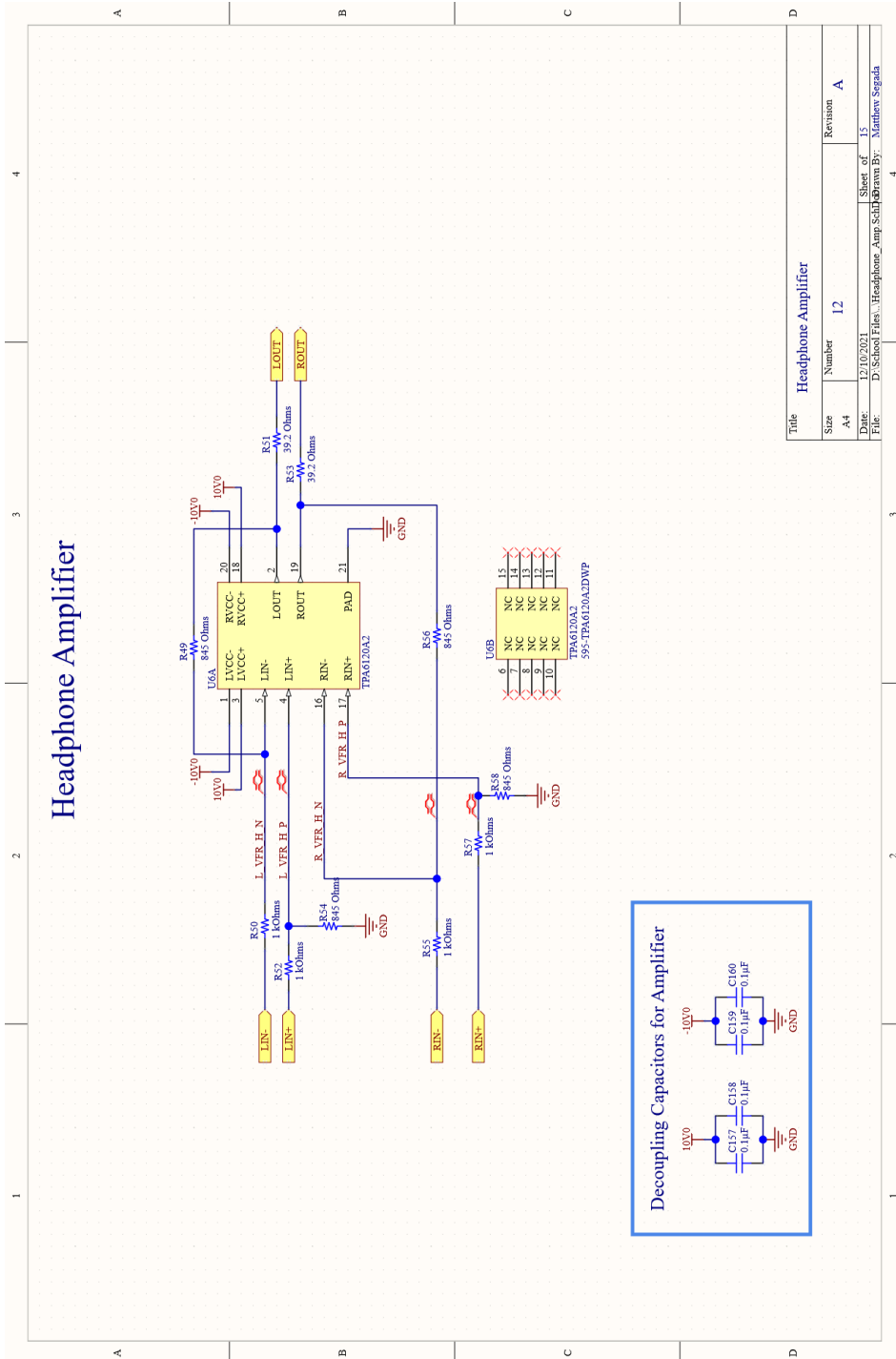
I.10 Single to Differential Converter



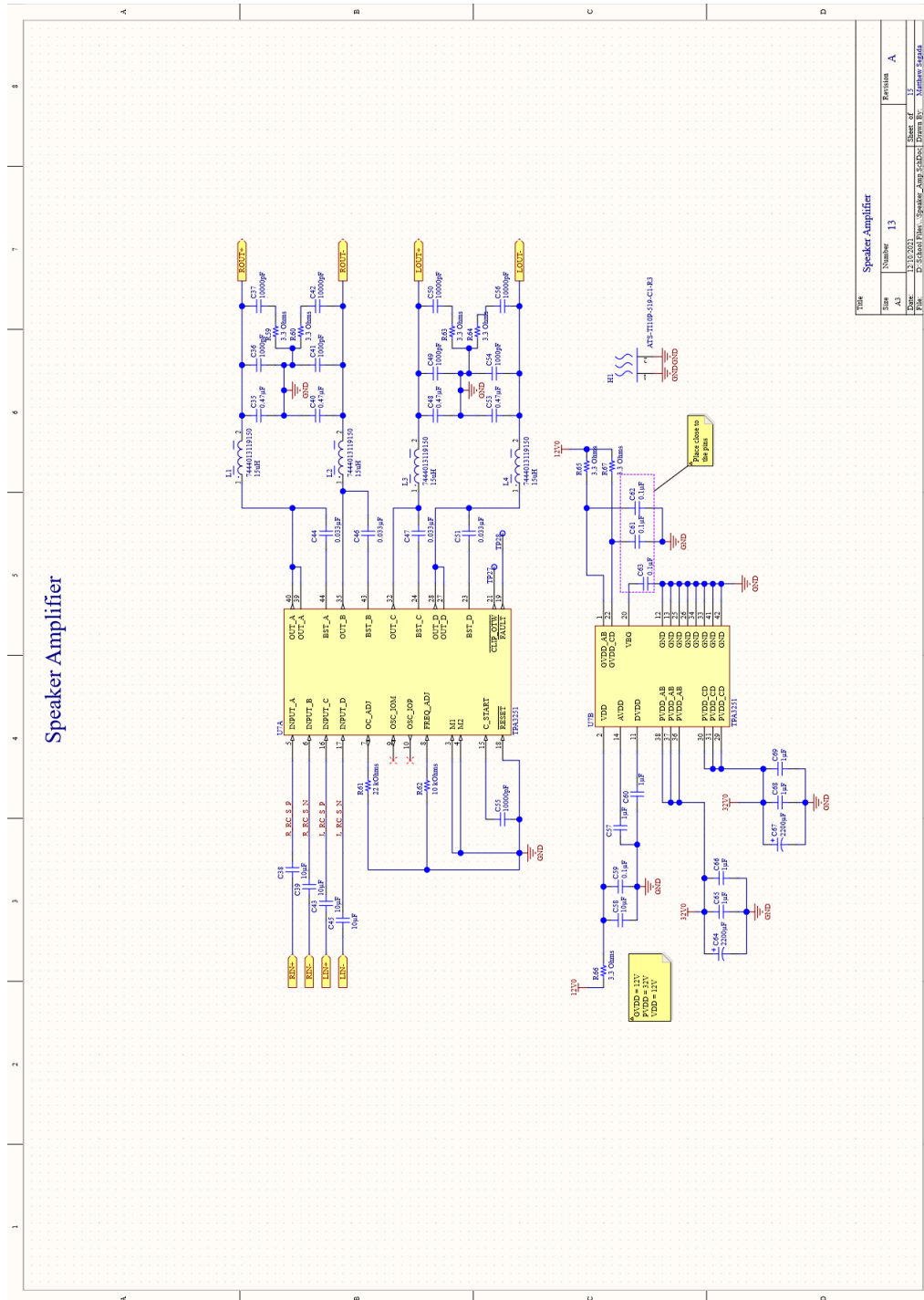
I.11 Amplifier Top Level



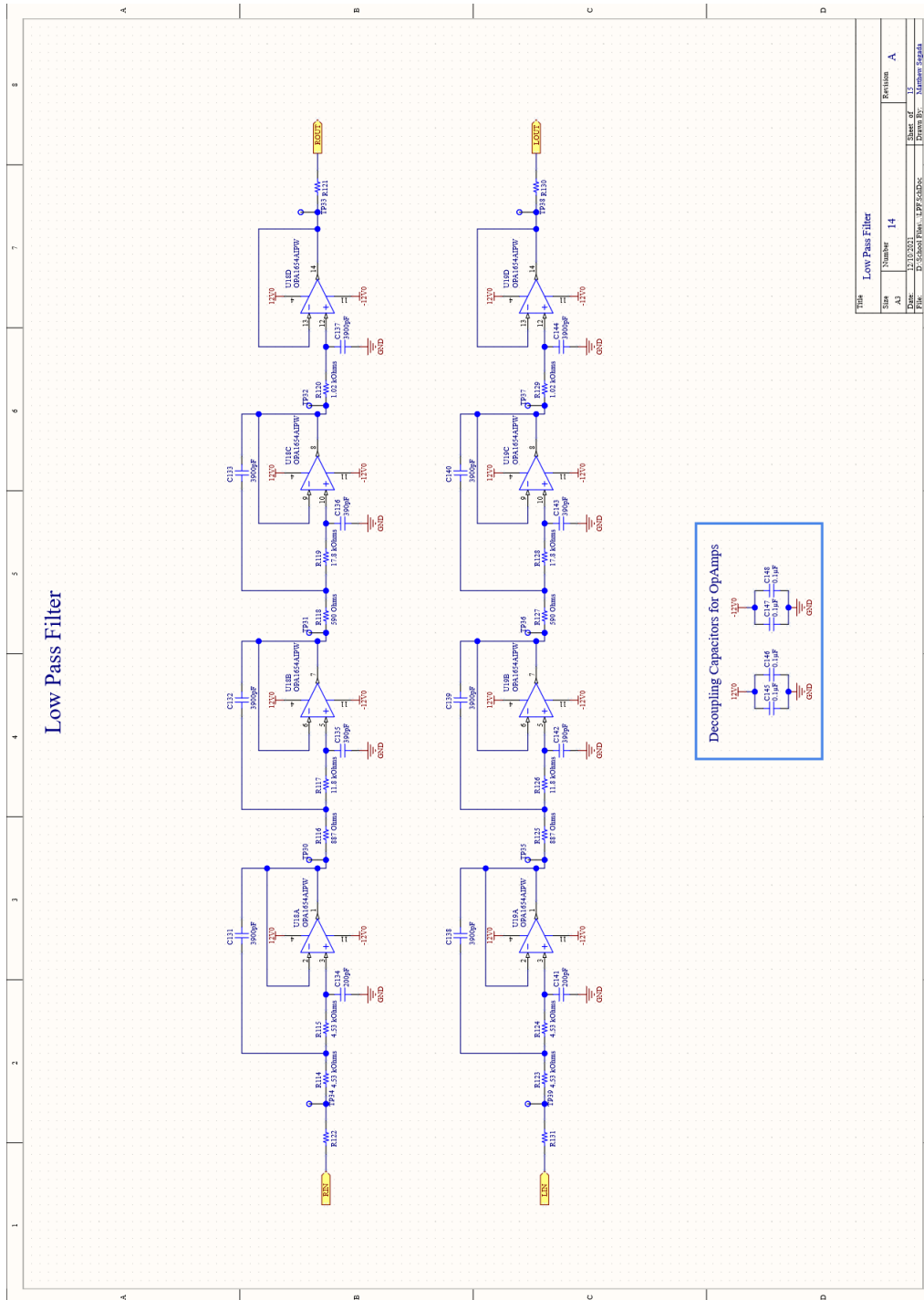
I.12 Headphone Amplifier



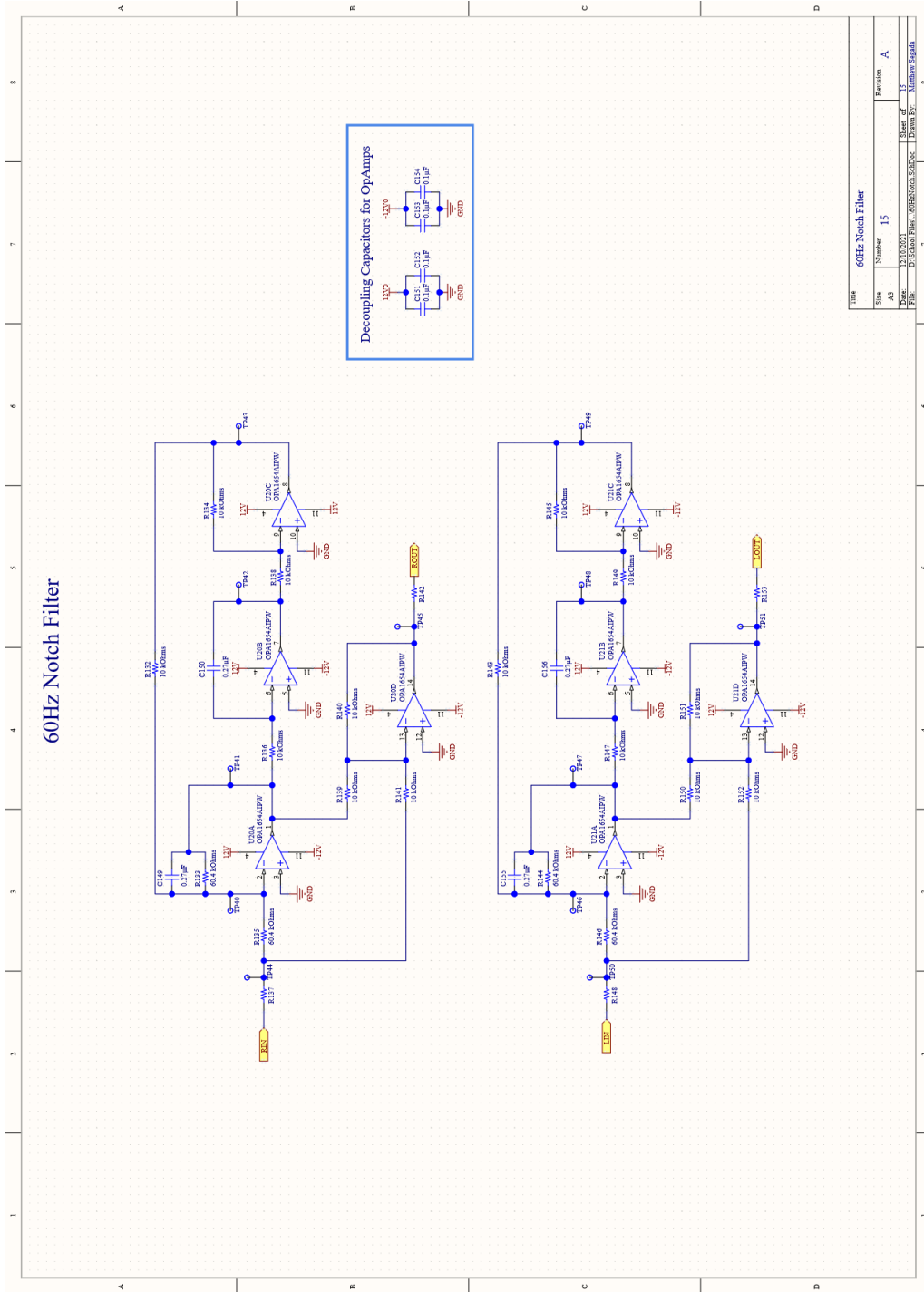
I.13 Speaker Amplifier



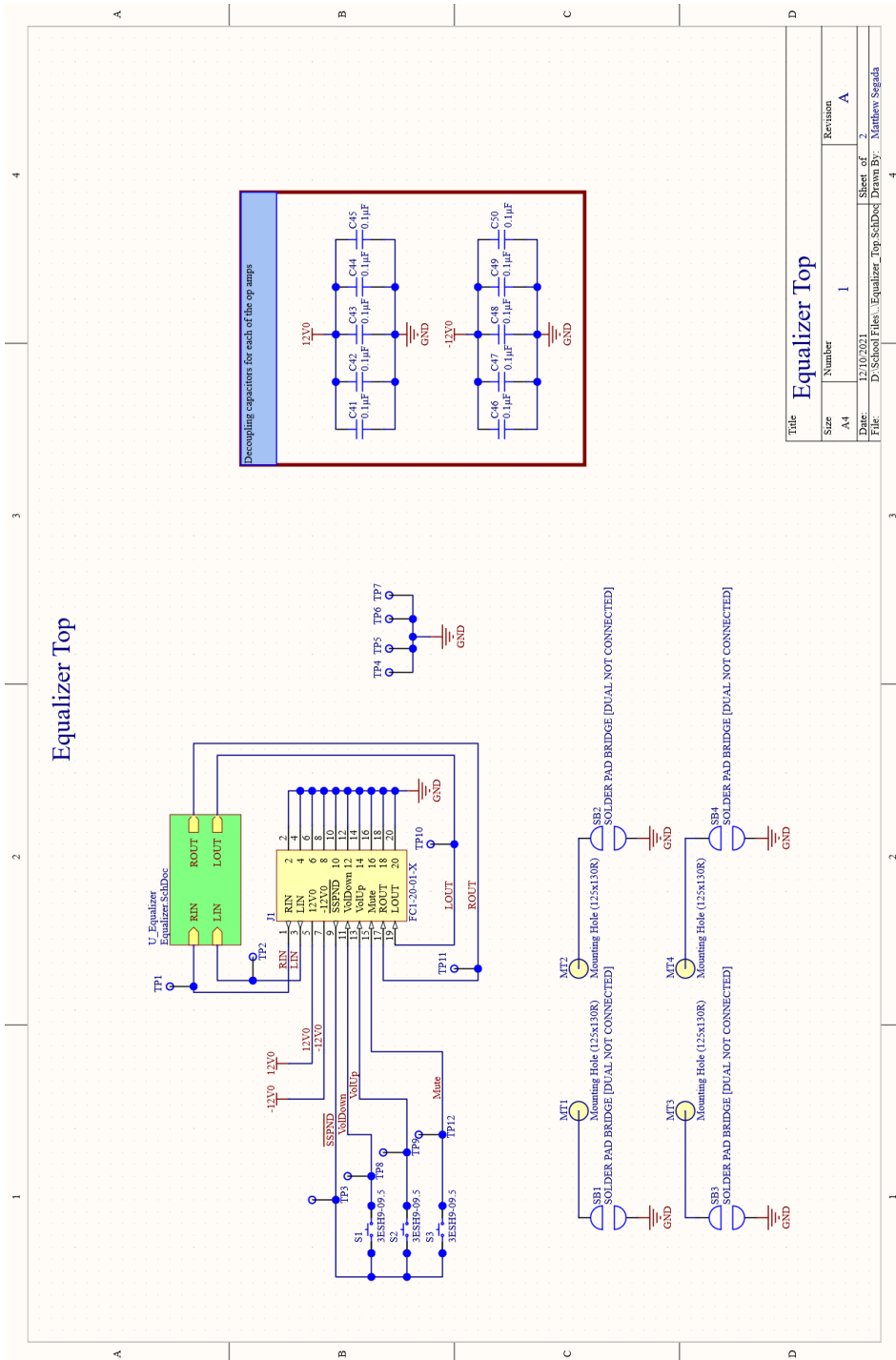
I.14 Low Pass Filter



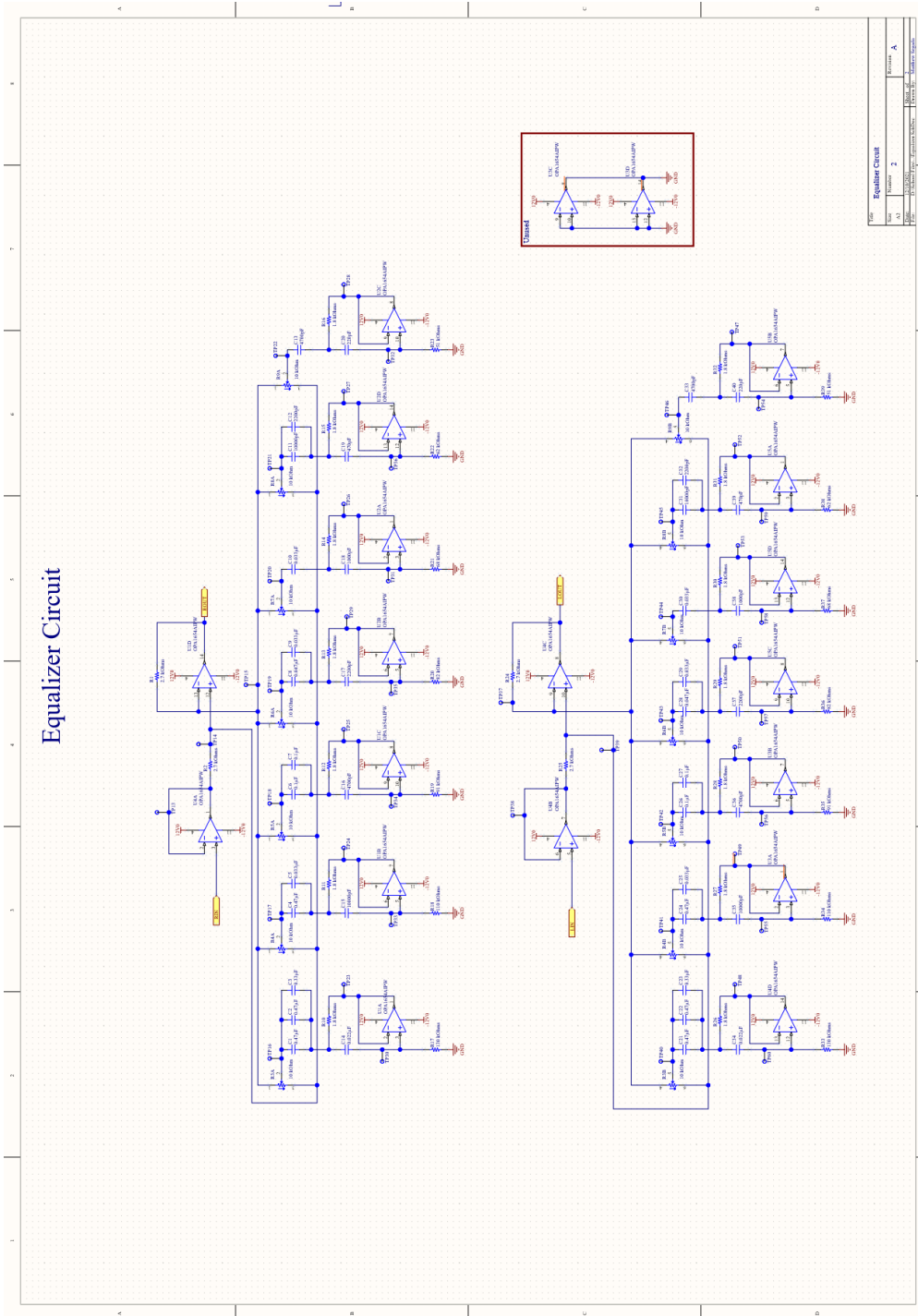
I.15 60 Hz Notch



I.16 Equalizer Top Level



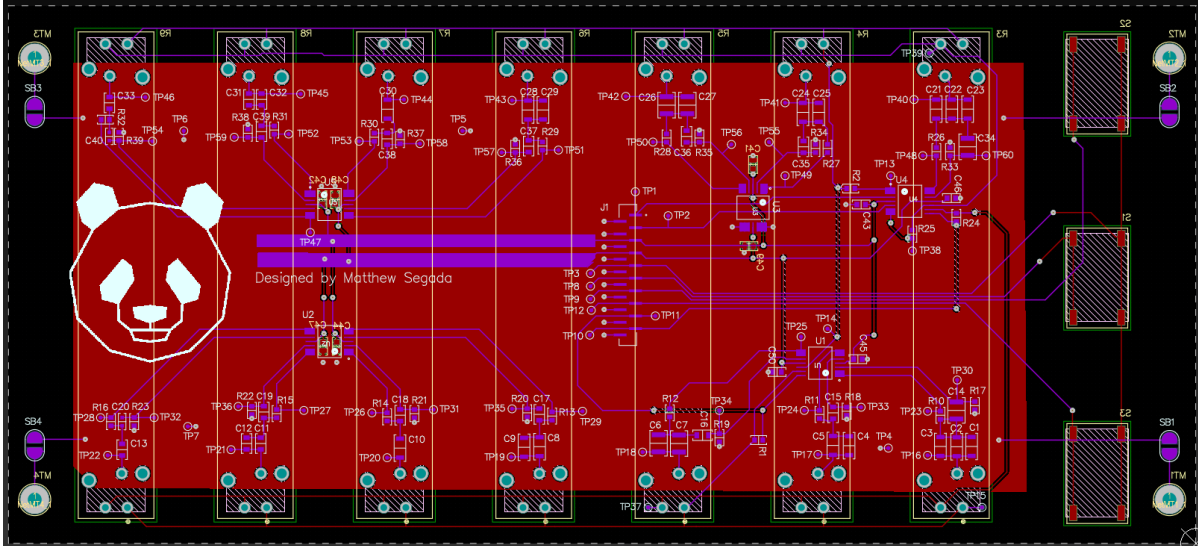
I.17 Equalizer Circuit



Appendix II

Altium Layouts

II.1 Equalizer Board Layout



II.2 Equalizer Board 3D Model - Top



II.3 Equalizer Board 3D Model - Bottom

