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Discrete Implementation of a Discontinuous Conduction Mode Flyback Regulator

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Discrete Implementation of a Discontinuous Conduction Mode Flyback Regulator

by

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I dedicate this work to my father Bill, my mother Nadine, and my brother David, for their continued support in all of my endeavors, including helping me move 2,205 miles away to build rockets.

Declaration

I hereby declare that except where specific reference is made to the work of others, that all content of this Graduate Paper are original and have not been submitted in whole or in part for consideration for any other degree or qualification in this, or any other University. This Graduate Project is the result of my own work and includes nothing which is the outcome of work done in collaboration, except where specifically indicated in the text.

Joseph Even

December, 2021

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I would like to thank my advisor Professor Mark A. Indovina for his slick jokes, sarcastic remarks, questionable guidance, and encouragement which pushed me to complete this project.

Abstract

This paper discusses the design of a flyback regulator implemented without a dedicated flyback controller integrated circuit (IC). Instead, all aspects of the voltage-mode controller are implemented discretely using a series of timing ICs, logic gates, and comparators. Utilizing a flyback transformer and an optoisolator, galvanic isolation is maintained in the design of a 12V-25V input, 5V/1A output, DC-DC flyback regulator with a constant switching frequency of 100kHz and fixed duty cycle of 0.443. After performing calculations to determine performance parameters, parts are selected to meet design specifications, schematic capture and printed circuit board (PCB) layout are performed, the PCB is fabricated, and its performance is evaluated. Metrics including load regulation, voltage ripple, line regulation, and efficiency are examined. Across the full input range, the averaged output voltage remained within 1% of the target 5V output. Voltage ripple was kept to within 5% of the output voltage across all output currents.

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Chapter 1

Introduction

Voltage regulation is a fundamental requirement for most, if not all, electronics. There is a countless number of voltage regulation schemes, but the flyback regulator offers distinct advantages. This regulator scheme is already omnipresent in commercial electronics due to its simplicity, low component count, and low cost. The increase in private space companies and increasing demand for electric vehicles has made the flyback regulator surge in popularity. The flyback regulator topology has a critical property for these applications – galvanic isolation.

The sections below describe the research goals, contributions, and organization of this paper.

1.1 Research Goals

As a "principal" intern, soon to be a hardware engineer at a private launch vehicle company, the author has seen the value and need for isolated supplies in spacecraft. Subsequently, a further understanding of the flyback regulator was desired by the author.

1.2 Contributions

The significant contributions to the project are listed below:

1. Using design equations, parameters of the desired flyback regulator are established.
2. Components are selected to meet the established design parameters.
3. Simulation is performed using the selected components to validate proper theoretical operation of the flyback regulator.
4. Schematic Capture and PCB Layout are performed in Altium Designer for the designed flyback regulator.
5. Performance of the designed flyback regulator is evaluated and results are presented.

1.3 Organization

The structure of the paper is as follows:

- Chapter 2: Provides an overview on voltage regulator topologies and the operating principle of two popular regulation schemes.
- Chapter 3: Discusses the benefits and shortcomings of the flyback regulator along with flyback regulator theory.
- Chapter 4: Presents the formulas used to determine necessary parameters in flyback regulator design and applies the formulas for the desired flyback regulator.
- Chapter 5: Shows the components selected to meet the design specifications calculated in Chapter 4 and how the components were connected to make a functional flyback regulator. This chapter also shows simulated results.

- Chapter 6: Delves into the Printed Circuit Board (PCB) for the flyback regulator, discussing some best practices in PCB design.
- Chapter 7: Describes the tests performed on the implemented regulator, and what metrics were examined.
- Chapter 8: Evaluates the performance of the implemented flyback regulator, with some comparison to the simulated results.
- Chapter 9: Concludes the study and discusses potential future work.

Chapter 2

Bibliographical Research

2.1 A Brief Overview of Voltage Regulation

In its most basic form, a voltage regulator takes in a voltage and generates a fixed output voltage. Voltage regulators come in a variety of forms, but the two main groups are linear regulators and switching regulators. As the name suggests, linear regulators operate in the linear region and "dissipate the extra voltage as heat." Linear regulators are only able to output a voltage lower than their input voltage. Switching regulators, as the name suggests, have a switching element in their control scheme. Switching regulators are considerably more efficient than linear regulators, especially when there is a significant difference between the input and output voltage. The increase in efficiency is derived from the switching element being fully enhanced with small conduction losses, or completely off with no power dissipation and ideally minimal losses in the transition. Switching regulators are also able to generate output voltages higher or lower than the input voltage or of opposite polarity.

2.2 Buck-Boost Regulator Operation

One of the most common switching regulator topologies is the buck-boost regulator as shown in Figure 2.1. The buck-boost regulator has two states[14]. In the first state, the switch is closed, the input voltage supply is connected to the inductor, and the inductor accumulates energy. In this state, the diode is reverse-biased, does not conduct, and the capacitor provides energy to the load. In the second state, the inductor is disconnected from the voltage supply and the voltage across the inductor flips, thus charging the output capacitor and also supplying energy to the load. The diode is forward-biased and allows current to flow through. To be noted, the polarity of the output voltage is opposite the input voltage.

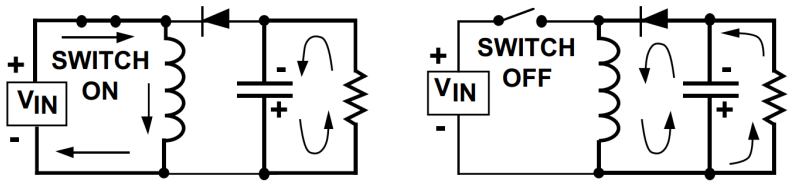

Figure 2.1: Buck-Boost Regulator States[1]

2.3 Flyback Regulator Operation

The flyback regulator shown in Figure 2.2 is remarkably similar to the buck-boost regulator, but utilizes a flyback transformer (coupled inductor). The flyback regulator also has two states. In the first state the switch is closed, the input voltage supply is connected to the primary winding of the transformer, and the transformer accumulates energy with an increase in magnetic flux. The capacitor provides energy to the load. Following the dot convention for transformers, the secondary-side diode is reverse-biased as the voltage in the secondary winding is negative and the diode does not conduct. In the second state, the transformer is disconnected from the

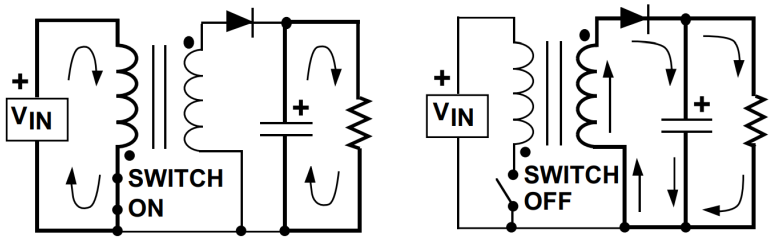

Figure 2.2: Flyback Regulator States[1]

voltage supply and the voltage across the secondary winding flips. The diode is forward-biased and allows current to flow through, charging the output capacitor and also supplying energy to the load. Similar to the buck-boost regulator, the polarity of the output voltage is opposite of the input voltage. In most graphics, however, the dots are specifically oriented diagonally from each other to keep the higher voltage on the “top” of the primary and secondary sides.

Chapter 3

Flyback Regulator Discussion

The generic flyback regulator block diagram is shown in Figure 3.1.

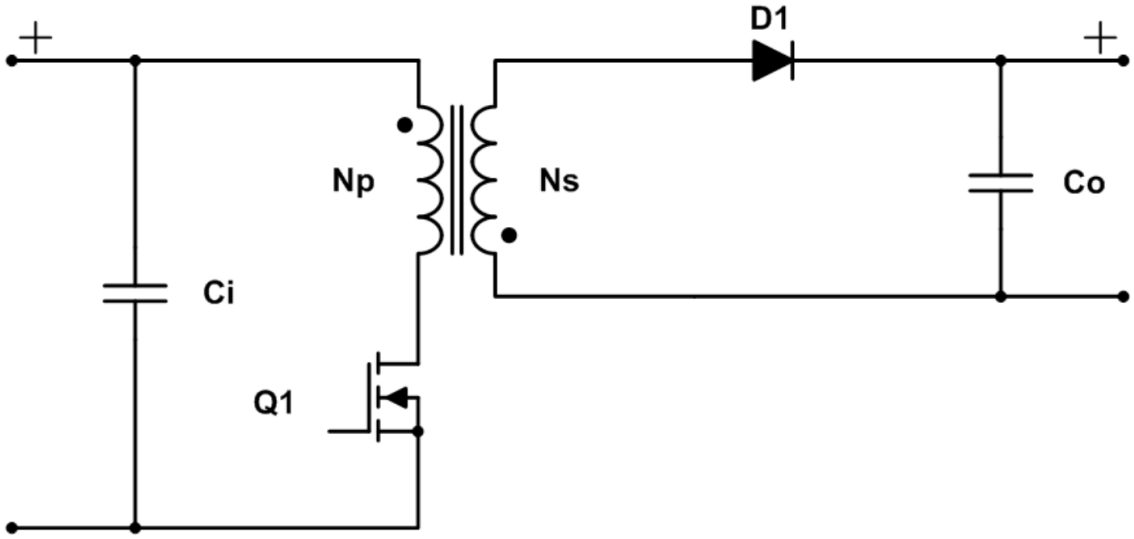

Figure 3.1: Generic Flyback Regulator Block Diagram[2]

3.1 Benefits of Flyback Regulators

Flyback regulators have several distinct advantages over other voltage regulation topologies. Specifically, flyback regulators have a low component count, offer primary-to-secondary galvanic isolation, and can generate multiple output voltages with a single set of primary-side circuitry.

3.1.1 Low Component Count

As seen in Figure 3.1, the flyback regulator has minimal components. In a typical application, a flyback controller IC could contain all control circuitry and the switching element. Subsequently, a low component count leads to a decreased cost and a decreased PCB footprint.

3.1.2 Primary-to-Secondary Isolation

For a variety of reasons, primary-to-secondary galvanic isolation can be a necessity for an electronic device. Per NASA, "Isolation means the net DC and AC extraneous or noise current is substantially reduced (the best isolation is no noise current whatsoever) in the isolated interface. If there is a DC signal ground connection between two assemblies and they each also have a separate wire ground to chassis, their signal interfaces are not isolated from each other"[3].

The first and most abundant application of the flyback regulator's isolation is in the form of AC/DC regulators in consumer electronics. The flyback regulator utilizes a rectified AC mains voltage to create a DC voltage in items such as cell phone chargers. Since this circuitry involves AC mains voltage and is used by the average consumer, the isolated nature of the flyback prevents the user from having the possibility of directly touching any metal tied to

mains voltage. Overall, this galvanic isolation increases consumer safety and is required by many regulatory agencies for consumer electronics.

More relevant to the research goals of the author, the galvanic isolation provided by circuits such as the flyback regulator is essential for proper grounding in spacecraft. NASA has extensive information about grounding in spacecraft and has even tied mission failures to improper grounding[3]. Figure 3.2 shows examples of proper isolation of grounds between two systems (left) and improper isolation between two systems (right). As shown in the figure, improper isolation can, and often does, form a ground loop. A ground loop is a condition where an electrical system contains multiple paths for current between two locations. In the case of the figure, signal return current can flow both in the return wire, as well as through the chassis ground connection. In the case of spacecraft, the chassis ground of the vehicle is often the structure (which is often metallic). Ground loops are problematic as they act as loop antennas and can radiate and receive electromagnetic fields, receiving or propagating noise.

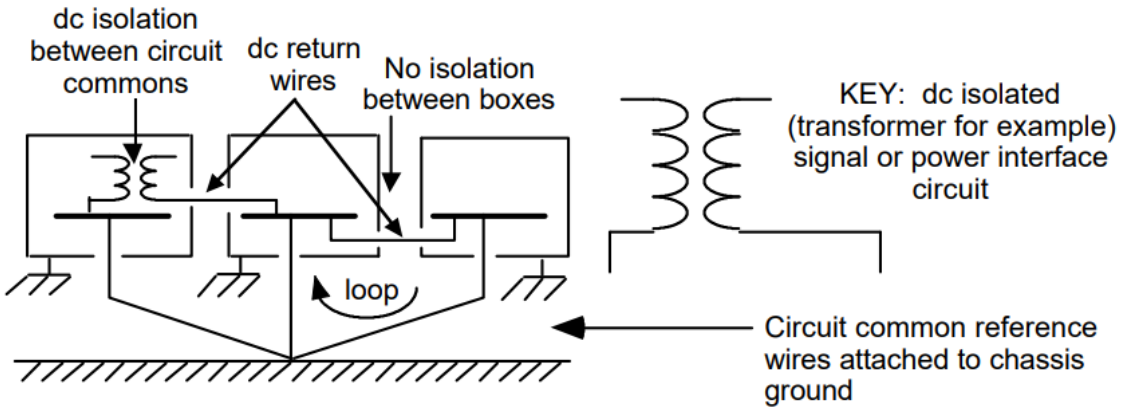

Figure 3.2: DC Isolated Ground and Non-Isolated Ground[3]

Figure 3.3 shows an “ideal” vehicle ground setup. This setup is called the Multiple, Single

Reference Ground System. In this system, each subsystem is isolated and has one connection to chassis which serves as the zero voltage reference. Since there is only one connection to chassis, there is no deliberate path for current to flow in the structure. Since each system is locally isolated, the physical size of the wire connecting the system to the chassis should be short with minimal AC impedance.

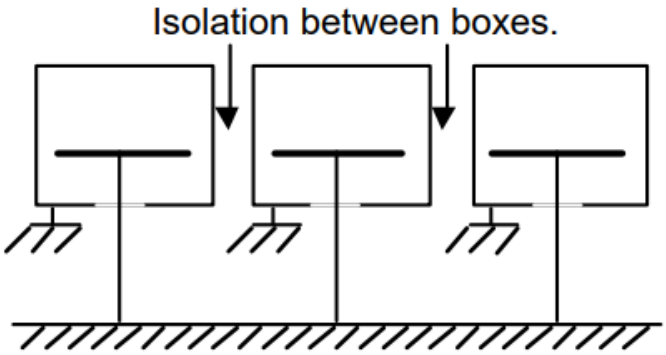

Figure 3.3: Multiple, Single Reference Ground[3]

While Figure 3.3 shows a desirable grounding arrangement, this setup is quite unrealistic for most vehicles. Creating a system with no connections between subsystems is extremely difficult (and borderline impossible) if power is not locally stored in each box. Figure 3.4 shows a far more practical grounding arrangement with "connections" between systems but without ground loops. This setup is also a Multiple, Single Reference Ground System, but makes use of isolated interfaces to create "connections" between boxes. From a power perspective, isolated power supplies, *such as the flyback regulator*, are used to deliver power from a central power distribution system to subsequent boxes. In the case of the flyback regulator, there is no galvanic connection between the primary and secondary side, so no ground loops can occur. Rather, energy is transferred through magnetic fields in the flyback transformer.

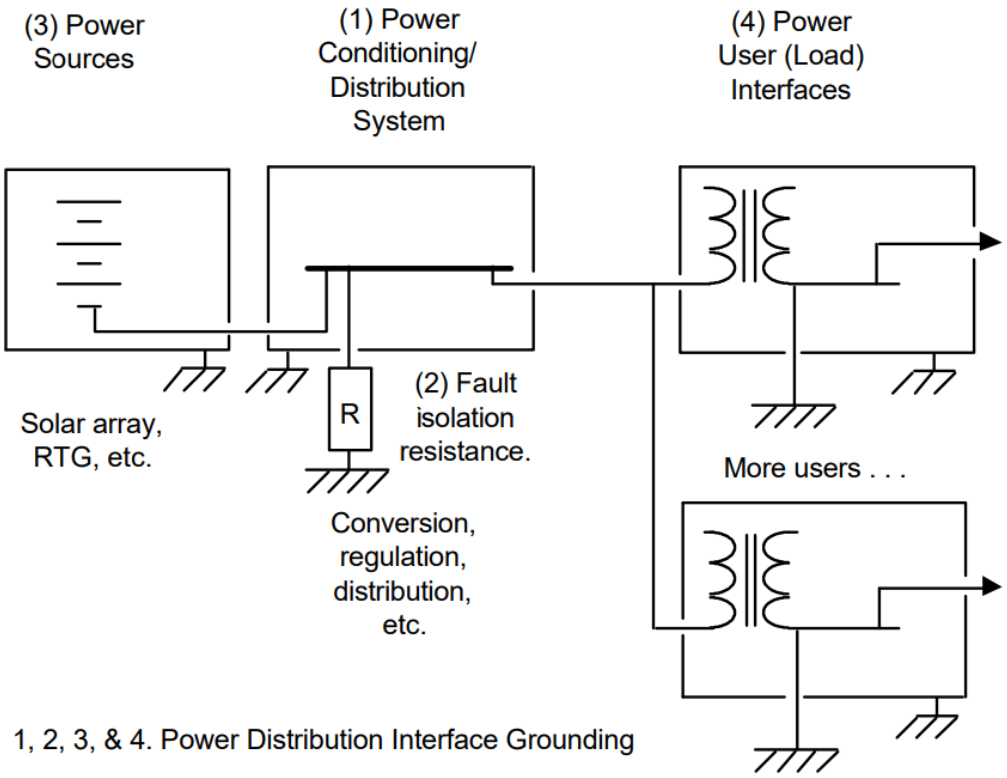

Figure 3.4: Isolated Power Supplies in a Multiple, Single Reference Ground[3]

Another aspect of spacecraft electronics solved with isolated interfaces such as the flyback regulator is the buildup of charge across a vehicle. Due to plasma in the atmosphere, it is possible for a voltage differential to occur across a vehicle. If this voltage differential were to propagate to a galvanically connected signal between boxes, a large voltage and/or current could appear on the wire, damaging electronics. In the case of an isolated interface, as long as the dielectric strength of isolated interfaces such as the flyback transformer is large enough, this current cannot flow between boxes and damage electronics.

3.1.3 Multiple Output Voltages

The flyback regulator has a unique feature. It has the ability to generate multiple output voltages with one set of primary-side circuitry[15]. As will be described in Section 3.3, the main design parameter of a flyback transformer is the turns ratio between the primary and secondary windings. When designing a multiple-output flyback regulator, the designer should begin with the highest-power output and determine the primary-to-secondary turns ratio. The designer can then use this initial turns ratio to determine the turns ratio for additional auxiliary windings.

3.2 Shortcomings of Flyback Regulators

While flyback regulators certainly have important advantages, they are not without flaw[16]. The first issue with flyback regulators is the high output ripple current and voltage. Since the flyback regulator is a switching regulator, ripple is inherent in the topology. It is possible to mitigate some of this ripple with additional filters, but adding filters takes time, increases cost, and increases board area. A second, and arguably most critical, restriction is the limitation on the power output of a flyback regulator. In the flyback regulator, the magnetic flux in the transformer core never reverses polarity, making it more likely to saturate the transformer core. Transformer saturation occurs when the magnetic flux density limit of the core is reached after current is continuously drawn[17]. During transformer saturation, the inductance begins to decrease, leaving only the trivially small winding resistance to limit the current through the transformer. While likely not an issue for the transformer, this increase in current is also experienced by the switching element, and can be so extreme that the switching element dissipates more power than it is rated for, destroying the component. The solution for avoiding this transformer saturation is to either limit the power output of the regulator or pick a large and bulky transformer with a higher saturation current.

3.3 Flyback Transformer Theory

While technically a misnomer, the flyback transformer is not a transformer, but rather a coupled inductor. The term transformer refers to a magnetic device that instantaneously transfers energy through its magnetic field. A flyback transformer is a coupled inductor with a gapped core. As stated in Chapter 2, during each cycle, when the input voltage is applied to the primary winding of a flyback transformer, energy is stored in the gap of the core. It is then transferred to the secondary winding to provide energy to the load. The relevant formulas for the flyback transformer do not differ from those of a regular transformer. The formulas for transformers are shown in Equation 3.1. When designing a flyback regulator, the turns ratio has a direct impact on the input-to-output voltage ratio. Additionally, the inductance of the primary winding is relevant for determining the mode of the regulator as will be discussed in the next section.

$$\frac{N_p}{N_s} = \frac{V_p}{V_s} = \left(\frac{L_p}{L_s}\right)^2 \tag{3.1}$$

3.4 Discontinuous Conduction Mode and Continuous Conduction Mode

Flyback converters have two basic energy-transfer modes of operation. These modes are Discontinuous Conduction Mode (DCM) where the secondary current falls to zero on each cycle and Continuous Conduction Mode (CCM) where the secondary current is always greater than zero. The advantages of DCM include lower primary inductance, often leading to a decreased transformer size, higher efficiency due to lower reverse recovery loss on the diode, and softer turn on of the switching element[18]. The disadvantages of DCM include higher primary current ripple, increased EMI, low efficiency at low output currents, and increased output ca-

pacitance.

3.5 Ideal Discontinuous Conduction Mode Waveforms

Figure 3.5 shows the critical waveforms of a standard DCM flyback regulator.

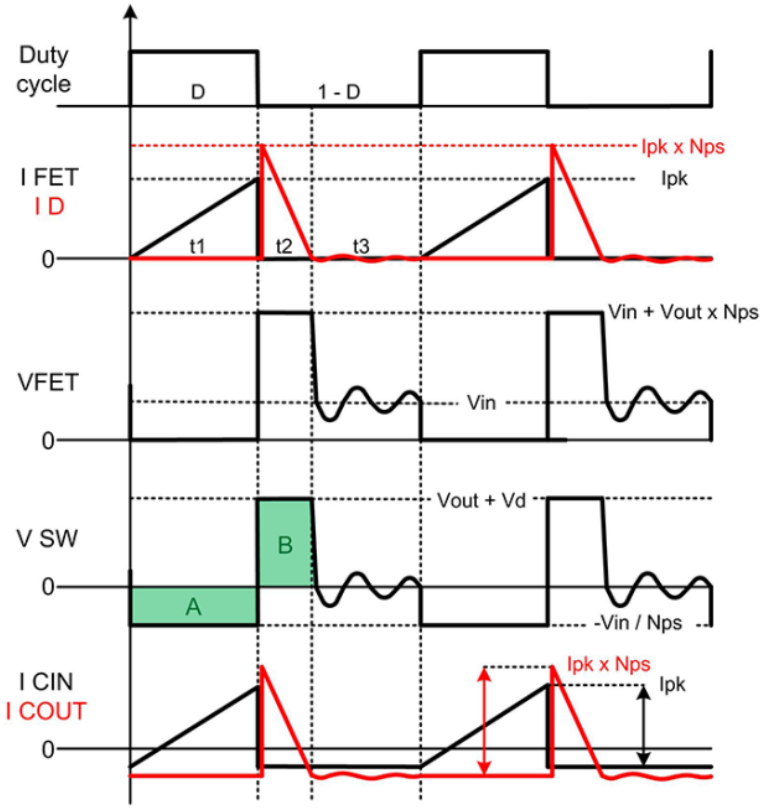

Figure 3.5: DCM Flyback Regulator Waveforms[4]

Chapter 4

Flyback Regulator Design

The implemented flyback regulator was specifically designed to accommodate the 750310471 Flyback Transformer from Wurth Elektronik as it was readily available and met the desired input voltage, output voltage, and current requirements.

4.1 Flyback Regulator Design Equations

The following equations are taken from an EDN article written by John Betten [4] and other sources that will be mentioned as required. Many of these formulas reference Figure 3.5. Please note a number of iterations were performed to alter the calculation results to accommodate the selected flyback transformer. Additionally, multiple passes through the equations were made as results from latter calculations were substituted into former calculations to produce more concrete design parameters. The results presented here are a product of these iterations. Before beginning with the design equations, the designer needs to establish some initial parameters. These parameters are defined in Table 4.1.

Beginning with the switching frequency and the maximum duty cycle, Equation 4.1 deter-

Parameter	Specification
Output Voltage (V_{OUT})	5V
Output Current ($I_{OUT(MAX)}$)	1A
Output Power ($P_{OUT(MAX)}$)	5W
Minimum Input Voltage ($V_{IN(MIN)}$)	12V
Maximum Output Voltage ($V_{IN(MAX)}$)	25V
Switching Frequency (f_{sw})	100kHz
Sense Resistance (R_{SNS})	20mΩ
Max Duty Cycle (D_{MAX})	0.480
Efficiency (η)	0.80
Diode Forward Voltage (V_D)	530mV
Transistor Drain-Source Resistance ($R_{DS(ON)}$)	210mΩ

Table 4.1: Design Specifications for Implemented Flyback Regulator

mines the length of t_1, the time the switching element is enabled and current is flowing in the primary side.

$$t_1 = \frac{D_{MAX}}{f_{sw}} \tag{4.1}$$

$$t_1 = \frac{D_{MAX}}{f_{sw}} = \frac{0.480}{100\text{kHz}} = 4.800\text{us}$$

At this point, some of the iterative results previously mentioned are presented. Equation 4.2 is used to estimate the peak current through the primary side of the flyback transformer. In order to determine the peak current (I_{pk}), the maximum output power and minimum input voltage are considered. In a constant-power scenario, these conditions would force the maximum current to be drawn. In order to determine $V_{DS(ON)}$, the drain-to-source voltage of the switching element and $V_{R(SNS)}$, the voltage across the current sense resistor, for the calculation of I_{pk}, I_{pk} was already required. Initially, a value of 3.5A was chosen for I_{pk}. After continued calculations, the final I_{pk} was determined to be 2.236A. The following equation will present

the calculation with the final calculated I_{pk} value of 2.236A.

$$I_{pk} = \frac{P_{OUT(MAX)} * (\frac{2}{D_{MAX}})}{(V_{IN(MIN)} - V_{DS(ON)} - V_{R(SNS)}) * \eta} \tag{4.2}$$

$$I_{pk} = \frac{P_{OUT(MAX)} * (\frac{2}{D_{MAX}})}{(V_{IN(MIN)} - V_{DS(ON)} - V_{R(SNS)}) * \eta} = \frac{5W * (\frac{2}{0.480})}{(12V - 0.470V - 0.047V) * 0.80} = 2.267A$$

Equation 4.3 is used to calculate the turns ratio of the flyback transformer required to generate the desired output voltage based on the minimum input voltage. When the input voltage is at its minimum, the switching element will need to be enabled for as long as the max duty cycle allows, so as to provide the needed energy to the secondary side. This equation follows the volt-second balance principle[19] as it equates areas A and B labeled in Figure 3.5. In this equation, the parameter x is a minimum idle time for t_3 shown in Figure 3.5. The value of 0.2 for x was used as per suggestion from the article. As desired and expected, the turns ratio calculation for the flyback regulator yielded a result of approximately 3.

$$\frac{N_p}{N_s} = \frac{(V_{IN(MIN)} - V_{DS(ON)}) * t_1}{(\frac{1}{f_{sw}} * (1 - x) - t_1) * (V_{OUT} + V_D)} \tag{4.3}$$

$$\frac{N_p}{N_s} = \frac{(V_{IN(MIN)} - V_{DS(ON)}) * t_1}{(\frac{1}{f_{sw}} * (1 - x) - t_1) * (V_{OUT} + V_D)} = \frac{(12V - 0.470V) * 4.800us}{(\frac{1}{100kHz} * (1 - 0.2) - 4.800us) * (5V + 0.530V)} = 3.127$$

As previously stated, the flyback transformer being utilized has a turns ratio of 3, so this value is used for all following calculations. Next, the maximum drain-to-source voltage of the switching element can be determined using Equation 4.4. When the switching element is turned off, the voltage across the secondary side of the transformer is reflected back onto

the primary side (and multiplied by the turns ratio), and is added to the input supply voltage. The maximum drain-to-source voltage is achieved when the input voltage is at its highest and is used to determine the required drain-to-source breakdown voltage rating for the switching element.

$$V_{DS(MAX)} = V_{IN(MAX)} + (V_{OUT} + V_D) * \frac{N_p}{N_s} \tag{4.4}$$

$$V_{DS(MAX)} = V_{IN(MAX)} + (V_{OUT} + V_D) * \frac{N_p}{N_s} = 25V + (5V + 530mV) * 3 = 41.590V$$

Continuing with parameters for rating components, Equation 4.5 determines the maximum reverse voltage applied to the output diode. This calculation is very similar to the previous calculation, but in the opposite direction. When the switching element is enabled, the input voltage is reflected back onto the secondary side (and divided by the turns ratio), and is added to the output voltage. The reverse breakdown voltage of the diode must be greater than the result of this calculation.

$$V_{PIV(MAX)} = V_{OUT} + \frac{V_{IN(MAX)}}{\frac{N_p}{N_s}} \tag{4.5}$$

$$V_{PIV(MAX)} = V_{OUT} + \frac{V_{IN(MAX)}}{\frac{N_p}{N_s}} = 5V + \frac{25V}{3} = 13.333V$$

Notice, these calculations do not accommodate for transformer leakage inductance. Leakage inductance is a result of imperfect coupling between the primary and secondary windings of the flyback transformer. During switching transients, this leakage energy cannot be transferred to the secondary and must be absorbed. Without a clamp circuit, the only path the leakage-

inductance current can circulate is by charging the parasitic drain-to-source capacitance of the switching element[20]. This additional voltage potentially can exceed the ratings of the drain-to-source voltage rating and destroy the component.

In order to avoid this potential damage to the switching element, a Resistor, Capacitor, Diode (RCD) Snubber is implemented. Using the following equations, the values required for these components are determined[21]. Equation 4.6 dictates the snubber voltage which is the output voltage plus the acceptable overshoot caused by the aforementioned leakage inductance. K_{SNUB} is the permitted overshoot factor, and a 50% overshoot is permitted.

$$V_{SNUB} = K_{SNUB} * \frac{N_p}{N_s} * (V_{OUT} + V_D) \tag{4.6}$$

$$V_{SNUB} = K_{SNUB} * \frac{N_p}{N_s} * (V_{OUT} + V_D) = 1.5 * 3 * (5V + 0.530V) = 24.885V$$

Equation 4.7 determines the snubber resistance. The peak current used for this formula is from the initial calculations where 3.5A was used.

$$R_{SNUB} = \frac{(V_{SNUB})^2}{\frac{1}{2} * L_{LEAK} * (I_{pk})^2 * \frac{V_{SNUB}}{V_{SNUB} - \frac{N_p}{N_s} * (V_{OUT} + V_D)} * f_{sw}} \tag{4.7}$$

$$R_{SNUB} = \frac{(24.885V)^2}{\frac{1}{2} * 430nH * (3.5A)^2 * \frac{24.885V}{24.885V - 3 * (5V + 0.530V)} * 100kHz} = 783\Omega$$

Equation 4.8 determines the snubber capacitance. The ΔV_{SNUB} parameter is the snubber capacitor voltage ripple and is set to 10%.

$$C_{SNUB} = \frac{24.885V}{\Delta V_{SNUB} * 24.885V * 783\Omega * 100kHz} \tag{4.8}$$

$$V_{SNUB} = \frac{V_{SNUB}}{\Delta V_{SNUB} * V_{SNUB} * R_{SNUB} * f_{sw}} = \frac{24.885V}{0.10 * 24.885V * 783\Omega * 100kHz} = 127.59nF$$

Equation 4.9 is used to calculate the required time for the switching element to be enabled. As expected, this resulting 4.642us is very close to the original design-specified 4.800us.

$$t_{1(MAX)} = \frac{(V_{OUT} + V_D) * \frac{N_p}{N_s} * (\frac{1}{f_{sw}} * (1 - x))}{V_{IN(MIN)} + (V_{OUT} + V_D) * \frac{N_p}{N_s}} \tag{4.9}$$

$$t_{1(MAX)} = \frac{(V_{OUT} + V_D) * \frac{N_p}{N_s} * (\frac{1}{f_{sw}} * (1 - x))}{V_{IN(MIN)} + (V_{OUT} + V_D) * \frac{N_p}{N_s}} = \frac{(5V + 530mV) * 3 * (\frac{1}{100kHz} * (1 - 0.2))}{12V + (5V + 530mV) * 3} = 4.642us$$

Equation 4.10 is used to calculate the maximum inductance of the primary winding to remain in DCM[22]. Exceeding the inductance will push the regulator towards CCM mode. The chosen flyback regulator has a primary inductance of 25uH and the result of Equation 4.10 confirms the regulator will remain in DCM.

$$L_{PRI(MAX)} = \frac{V_{IN(MIN)} * D_{MAX}}{I_{OUT(MAX)} * f_{sw}} \tag{4.10}$$

$$L_{PRI(MAX)} = \frac{V_{IN(MIN)} * D_{MAX}}{I_{OUT(MAX)} * f_{sw}} = \frac{12V * 0.48}{2.236A * 100kHz} = = 25.760uH$$

Equation 4.11 is used to calculate the maximum duty cycle of the flyback regulator. Since small alterations have been made throughout the process of choosing parameters, the maximum duty cycle has slightly changed compared to the original stipulated 0.4800. The maximum duty cycle of 0.466 agrees with the maximum length of t_1 (4.642us) as the switching frequency is

100kHz with a resulting period of 10us.

$$D_{MAX} = \sqrt{\frac{2 * f_{sw} * V_{OUT} * I_{OUT(MAX)} * L_{PRI}}{(V_{IN(MIN)})^2 * \eta}} \tag{4.11}$$

$$D_{MAX} = \sqrt{\frac{2 * f_{sw} * V_{OUT} * I_{OUT(MAX)} * L_{PRI}}{(V_{IN(MIN)})^2 * \eta}} = \sqrt{\frac{2 * 100kHz * 5V * 1A * 25uH}{(12V)^2 * 0.8}} = 0.466$$

Equation 4.12 is used to calculate the final peak primary inductor current. Using this current and Equation 4.13, the power dissipation of the switching element can be determined.

$$I_{PK(MAX)} = \sqrt{\frac{2 * V_{OUT} * I_{OUT(MAX)}}{L_{PRI} * f_{sw} * \eta}} \tag{4.12}$$

$$I_{PK(MAX)} = \sqrt{\frac{2 * V_{OUT} * I_{OUT(MAX)}}{L_{PRI} * f_{sw} * \eta}} = \sqrt{\frac{2 * 5V * 1A}{25uH * 100kHz * 0.8}} = 2.236A$$

$$P_{FET(COND)} = (I_{PK(MAX)})^2 * R_{DS(ON)} \tag{4.13}$$

$$P_{FET(COND)} = (I_{PK(MAX)})^2 * R_{DS(ON)} = (2.236A)^2 * 210m\Omega = 1.050W$$

Equation 4.14 is used to determine the power dissipation of the output diode. Using the traditional power dissipation formula for the diode of the forward voltage multiplied by the current allows the designer to determine an adequate power rating for the diode.

$$P_{DIODE} = V_{DIODE} * I_{OUT} \tag{4.14}$$

$$P_{DIODE} = V_{DIODE} * I_{OUT} = 0.530V * 1A = 530mW$$

Finally, Equation 4.15 shows the equation to calculate the voltage ripple on the output of the flyback regulator given a specified output capacitance[23].

$$V_{RIPPLE} = \frac{I_{OUT}}{f_{sw} * C_{OUT} * \left(1 + \frac{\frac{N_p}{N_s}^{-1} * V_{IN}}{V_{OUT}}\right)} + ESR * I_{OUT} * \left(1 + \frac{\frac{N_p}{N_s}^{-1} * V_{OUT}}{V_{IN}}\right) \quad (4.15)$$

$$100mV = \frac{1A}{100kHz * C_{OUT} * \left(1 + \frac{3^{-1} * 25V}{5V}\right)} + 50m\Omega * 1A * \left(1 + \frac{3^{-1} * 5V}{25V}\right) = 80.3571uF$$

4.2 Control Scheme

The control scheme for the flyback regulator is implemented using voltage feedback from the secondary side, an oscillator, and logic gates. A fixed-frequency and fixed-duty cycle oscillator is used for simplicity. In order to control the flyback regulator, two AND gates are used. The first AND gate has two inputs–the oscillator output and the output of the second AND gate. The output of the first AND gate is tied to the switching element. The second AND gate has four inputs. The first three inputs are for faults that will be described in the next chapter. The fourth input is the output of a feedback optoisolator. The operation of the optoisolator will be described in the next chapter. When there are no faults and the regulator's output voltage is too low, the output of the second AND gate is high. Subsequently, the output of the first AND

gate will effectively pass the oscillator output to the switching element. When there is a fault or the output voltage of the regulator is too high, the output of the second AND gate will go low and prevent the oscillator output from getting to the gate driver. The diagram for this logic is shown in Figure 4.1.

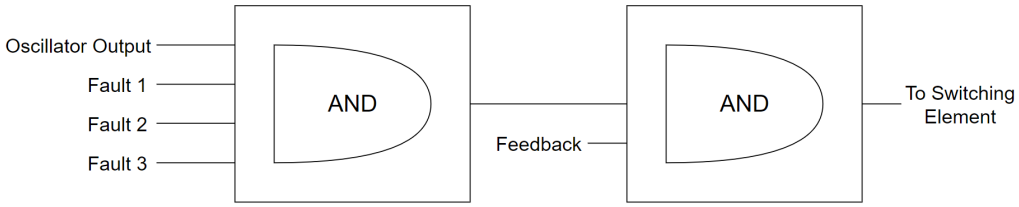

Figure 4.1: AND Gate Logic Diagram

Chapter 5

Flyback Regulator Implementation

5.1 Component Selection

The following components detail the transition from design equations to a physical realization of a discrete flyback regulator. Appendix A shows the overall schematic for the flyback regulator, as built in LTSPICE for simulation.

5.1.1 Primary-Side Regulator

Prior to discussion of the components relevant to the flyback regulator calculations in Chapter 4, one particularly important component in the realization of the flyback regulator is the primary-side voltage regulator that powers the logic ICs and other components on the primary side. For this purpose, the LT3088 Linear Regulator was chosen[5]. The block diagram for the LT3088 is shown in Figure 5.1. As discussed in Chapter 2, the LT3088 falls under the category of a linear regulator.

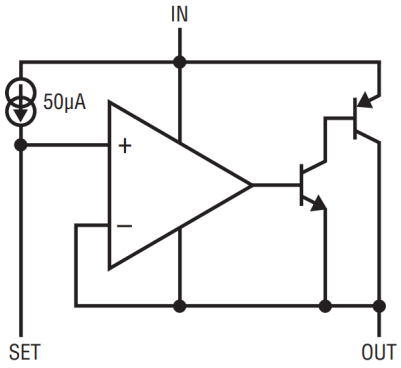

Figure 5.1: LT3088 Block Diagram[5]

Like most linear regulators, The LT3088 drives a transistor dependent on feedback from the output voltage. When the output is higher than the non-inverting input of the amplifier, the transistor is driven less, decreasing the output current and subsequently the output voltage, and vice versa. The LT3088 is an adjustable regulator, as a resistor tied to the SET pin allows the designer to select what voltage appears on the non-inverting input as a voltage reference. Since the SET pin is tied to a constant-current source, the reference voltage can be determined with Ohm's Law, which subsequently determines the output voltage. The selected output voltage of the LT3088 is 5V to accommodate the components that will follow in the next section. To achieve this output voltage, a SET resistor of 100kΩ is chosen.

While linear regulators generally have excellent output regulation and low output noise, their disadvantage comes with considerable power dissipation. The equation for linear regulator power dissipation is shown in Equation 5.1.

$$\text{Power Dissipation}(\text{W}) = (\text{V}_{\text{IN}} - \text{V}_{\text{OUT}}) * \text{I}_{\text{OUT}} \tag{5.1}$$

Clearly, the higher the differential between the input and output voltage, the higher the power

dissipation. Since the implemented flyback regulator is designed for input voltages up to 25V and the desired output voltage is 5V, only a small amount of current will generate a large amount of dissipated power. To determine the maximum amount of power the regulator can handle, Equation 5.2 can be used. The data sheet provides a Junction-to-Ambient Temperature Coefficient (ϑ_{JA}), which determines the junction temperature increase per watt dissipated. This temperature increase, along with the ambient temperature cannot exceed the maximum junction temperature of the IC, which is also stated in the data sheet.

$$\text{Junction Temperature(C)} = \text{T}_{\text{Ambient}} * (\text{Power Dissipation} * \theta_{\text{JA}}) \tag{5.2}$$

With the data sheet specifying maximum junction temperature of 150C, a maximum input voltage of 25V, and an output voltage of 5V, the maximum output of the regulator is 250mA. The expected current draw of the implemented regulator is far below this amount, but peaks of current from the gate driver to turn the switching transistor on and off can exceed this value. In order to decrease the power dissipation of the LT3088, a series resistor footprint is added to the PCB if ultimately it is determined to be required. As shown in Figure 5.2 from the LT3088 data sheet, a series resistor can be put between the supply voltage of the flyback regulator and the input of the LT3088 to dissipate some of the power.

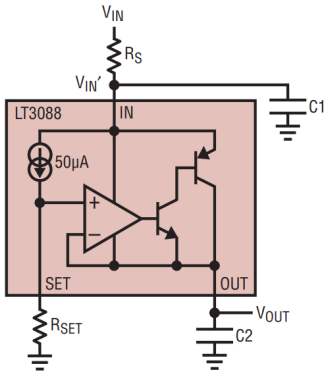

Figure 5.2: Decreasing the dissipated power of the LT3088 with a series resistor[5]

5.1.2 Flyback Transformer

As stated in Chapter 4, the implemented flyback regulator was catered to the 750310471 Flyback Transformer for its small size and availability. Figure 5.3 shows the specifications of this flyback transformer and Figure 5.4 shows its pinout.

ELECTRICAL SPECIFICATIONS @ 25°C unless otherwise noted:

PARAMETER		TEST CONDITIONS	VALUE
D.C. RESISTANCE	2–1	@20°C	.088 max.
D.C. RESISTANCE	3–4	@20°C	.057 max.
D.C. RESISTANCE	5–7	tie(5+6, 7+8), @20°C	.011 max.
INDUCTANCE	3–4	10kHz, 100mVAC, Ls	25.00uH ±10%
(6C) SATURATION CURRENT		20% rolloff from initial	2.6A
LEAKAGE INDUCTANCE	3–4	tie(1+2, 5+6+7+8), 100kHz, 100mVAC, Ls	430nH max.
DIELECTRIC	1–8	tie(2+3, 5+6), 1875VAC, 1 second	1500VAC, 1 minute
TURNS RATIO		(3–4):(2–1)	3:1, ±1%
TURNS RATIO		(3–4):(5+6–7+8)	3:1, ±1%

Figure 5.3: Flyback Transformer Specifications[6]

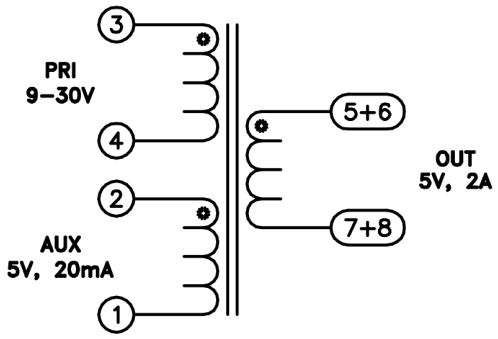

Figure 5.4: Flyback Transformer Pinout[6]

5.1.3 Oscillator

To provide the switching signal for the flyback regulator, the LTC6992 is used[7]. The LTC6992 is a silicon oscillator with voltage-controlled Pulse-Width Modulation (PWM). The oscillator's block diagram is shown in Figure 5.5.

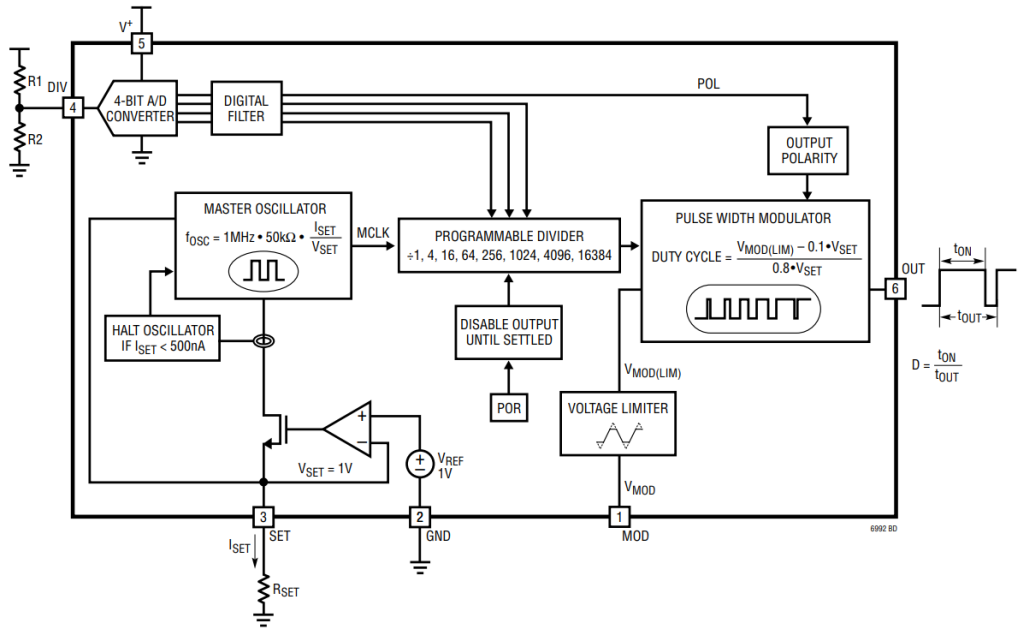

Figure 5.5: LTC6992 Block Diagram[7]

As stated in Chapter 4, a switching frequency of 100kHz was chosen. Equation 5.3 was used to determine the output frequency of the oscillator[7]. The NDIV parameter is used for coarse frequency selection, and RSET is used for fine-tuning of the output frequency.

$$\text{fout(Hz)} = \frac{1\text{MHz} * 50\text{k}}{\text{N}_{\text{DIV}} * \text{R}_{\text{SET}}} \tag{5.3}$$

In order to set NDIV, a resistive voltage divider shown in Figure 5.6 is used.

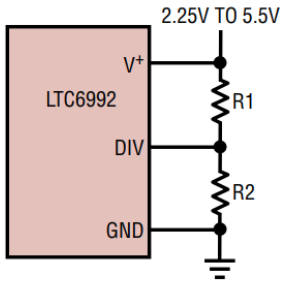

Figure 5.6: LTC6992 NDIV Voltage Divider[7]

Using the figure provided by the LTC6992 data sheet, values for R1 and R2 from Figure 5.14 were chosen. For R1, 976kΩ was chosen, and for R2, 102kΩ was chosen. This yields an NDIV of 4, polarity of 1, and a recommended output frequency between 15.63kHz and 250kHz.

DIVCODE	POL	N_{DIV}	RECOMMENDED f_{OUT}	R1 (kΩ)	R2 (kΩ)	V_{DIV}/V^+
0	0	1	62.5kHz to 1MHz	Open	Short	≤0.03125 ±0.015
1	0	4	15.63kHz to 250kHz	976	102	0.09375 ±0.015
2	0	16	3.906kHz to 62.5kHz	976	182	0.15625 ±0.015
3	0	64	976.6Hz to 15.63kHz	1000	280	0.21875 ±0.015
4	0	256	244.1Hz to 3.906kHz	1000	392	0.28125 ±0.015
5	0	1024	61.04Hz to 976.6Hz	1000	523	0.34375 ±0.015
6	0	4096	15.26Hz to 244.1Hz	1000	681	0.40625 ±0.015
7	0	16384	3.815Hz to 61.04Hz	1000	887	0.46875 ±0.015
8	1	16384	3.815Hz to 61.04Hz	887	1000	0.53125 ±0.015
9	1	4096	15.26Hz to 244.1Hz	681	1000	0.59375 ±0.015
10	1	1024	61.04Hz to 976.6Hz	523	1000	0.65625 ±0.015
11	1	256	244.1Hz to 3.906kHz	392	1000	0.71875 ±0.015
12	1	64	976.6Hz to 15.63kHz	280	1000	0.78125 ±0.015
13	1	16	3.906kHz to 62.5kHz	182	976	0.84375 ±0.015
14	1	4	15.63kHz to 250kHz	102	976	0.90625 ±0.015
15	1	1	62.5kHz to 1MHz	Short	Open	≥0.96875 ±0.015

Figure 5.7: LTC6992 DIVCODE Programming[7]

Continuing with Equation 5.3, the final step was to select a value for RSET. Using the desired output frequency of 100kHz and selected NDIV value of 4, RSET was determined to be 125kΩ. A resistor value of 127kΩ was selected, giving a final output frequency of 98.425kHz.

$$f_{OUT}(Hz) = \frac{1MHz * 50k}{N_{DIV} * R_{SET}} = \frac{1MHz * 50k}{4 * 127k\Omega} = 98.425kHz$$

The LTC6992 also gives the designer the ability to vary the duty cycle of the output. The duty cycle is controlled by the voltage presented on the MOD pin. The MOD input voltage can range between 0V and 1V, with the voltage directly representing the duty cycle. Using a resistive voltage divider of 110kΩ and 11kΩ resistors, along with the supply voltage of 5V, the voltage on the MOD pin is 455mV, generating a duty cycle of 0.443.

5.1.4 Primary-Side Switch

The switching element for the flyback regulator is a transistor, specifically the IRFR120N MOSFET[24]. This transistor has a maximum drain-to-source voltage of 100V, meaning it can

withstand the switching transients of the flyback transformer. In order to drive this MOSFET, the LTC1693 Gate Driver is used[25]. The LTC1693 is capable of outputting up to 1.5A of current, quickly charging and discharging the transistor, reducing switching losses.

5.1.5 Feedback Circuitry

The LT1431 is Linear Technology's slightly enhanced version of the ubiquitous TL431, with one of its target applications as an optoisolator driver as shown in the first page of the data sheet[8]. This IC is an adjustable shunt voltage regulator with a variety of uses. As shown by the block diagram in Figure 5.8, the IC consists of an op amp, transistor, diode, and voltage reference.

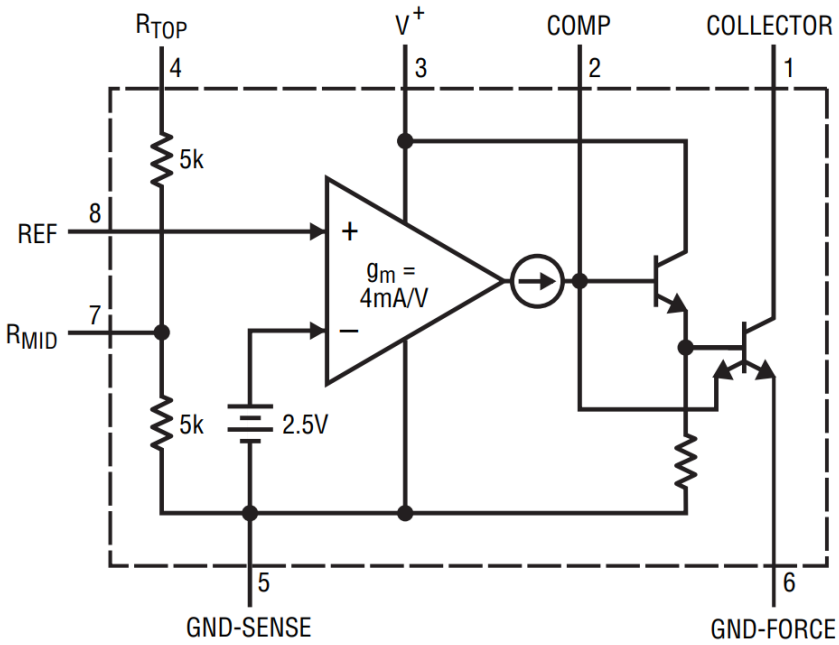

Figure 5.8: LT1431 Block Diagram[8]

Following the block diagram, the op amp inputs are a tied to a 2V5 internal reference and

an externally supplied input (REF). In this configuration, the output of the op amp is high when the REF pin exceeds the 2V5 reference. This op amp output enables the transistors. For the purpose of the implemented flyback regulator, the LT1431 is being used as a comparator. When the output voltage exceeds 5V, the switching element should be disabled. To facilitate this operation, the LT1431 is used in conjunction with an optoisolator. The selected optoisolator is the VOM617A-3T. The optoisolator's block diagram is shown in Figure 5.9[9].

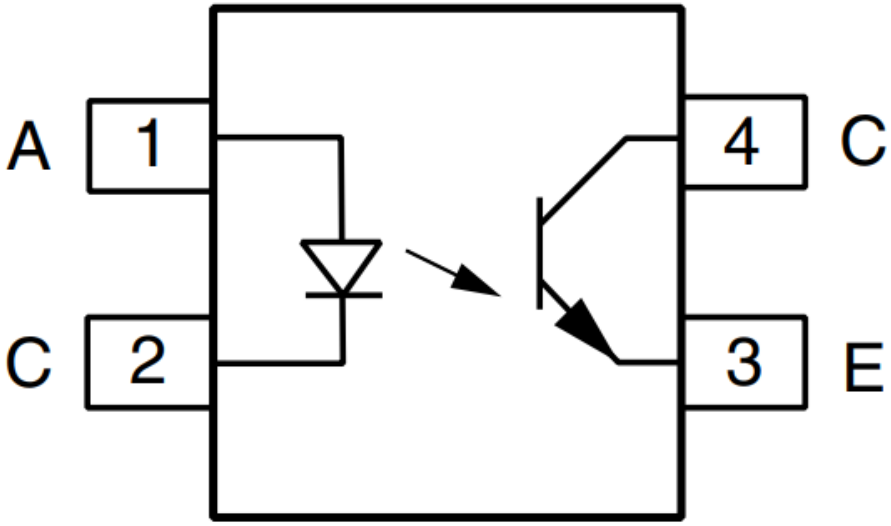

Figure 5.9: VOM617A-3T Optoisolator Block Diagram[9]

First, the non-inverting input of the LT1431 needs to be at or above 2V5 when the output of the regulator is at 5V. The LT1431 conveniently (and likely purposefully) includes an internal voltage divider with a division of 2. With this division, if the output of the regulator is tied to RTOP, the RMID voltage will be 2V5 when the output is 5V (the desired condition). This RMID voltage can be applied to REF, enabling the transistor as an open collector. The open collector nature of the IC allows for integration of the optoisolator. The anode of the optoisolator's diode can be connected to the output of the regulator to supply power, and the cathode

can be connected to the COLLECTOR pin of the LT1431. There is a resistor in between the optoisolator cathode and COLLECTOR pin of the LT1431 to limit the current through the optoisolator diode. It can now be seen the optoisolator is enabled by the open collector of the LT1431 when the output voltage exceeds 5V. Since this feedback is sent through the optoisolator, it can be utilized on the primary side without breaking the isolation barrier between the primary and secondary sides of the flyback transformer. As a quick aside, the LT1431 is supplied power by the output of the regulator as well. The final result of the implemented circuit is as follows: the optoisolator output is low when the output voltage is below 5V, and the optoisolator output is high when the output voltage is above 5V. This feedback is used the previously mentioned control scheme.

5.1.6 Output Diode

As per the calculations in Chapter 4, the max reverse voltage across the diode is not expected to exceed 13.333V. The PMEG6045ETP diode is chosen as it has a reverse voltage of 60V and an average forward current of 4.5A. Both device specifications are more than adequate for the intended application.

5.1.7 Output Capacitance

In order to achieve the high capacitance necessary to keep the voltage ripple of the flyback regulator low, tantalum capacitors were chosen. Tantalum capacitors consist of a tantalum anode covered by a layer of oxide acting as the dielectric surrounded by a conductive cathode [26]. The use of tantalum metal allows for a very thin conductive cathode, resulting in a large capacitance per volume.

5.1.8 RCD Snubber

The RCD Snubber values chosen were taken from the calculations in Chapter 4. The calculations state a resistance value of 783Ω, so a 750Ω was chosen, and a capacitance value of 127.59nF, so a 150nF capacitor value was chosen. To reduce line items in the Bill of Materials (BOM), the snubber diode is the same as the output diode.

5.1.9 Fault Circuitry

Many ICs, for their own safety, as well as the safety of downstream or upstream systems, include faults. Common faults for voltage regulators include input overvoltage, undervoltage, and overcurrent. In the flyback regulator, these three faults are implemented as non-latching faults. These three faults are implemented using comparators, with the overcurrent having some added complexity. All three faults utilize the LT1716, a rail-to-rail comparator, as shown in Figure 5.10[10]. In order to create a reference for the comparator, a resistive divider of the 5V supply consisting of two 11kΩ resistors is used to generate an output voltage of 2.5V. While significantly more reliable voltage reference ICs are available, the faults for the implemented regulator are not particularly stringent and the resistor reference is adequate.

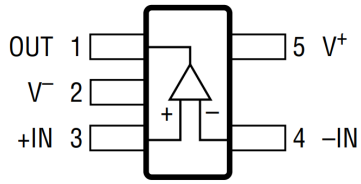

Figure 5.10: LT1716 Diagram[10]

The overvoltage and undervoltage faults are simple, consisting of a voltage divider tied to the inputs of the comparator. For the overvoltage fault, a 100kΩ and 11kΩ resistive divider is used to divide the regulator's input voltage to 2.5V when the input is 25.23V (25V desired).

The resistive divider output is tied to the inverting input of the comparator and the reference is tied to the non-inverting input. For the undervoltage fault, a 100kΩ and 27kΩ resistive divider is used to divide the regulator's input voltage to 2.5V when the input is 11.76V (12V desired). The resistive divider output is tied to the non-inverting input of the comparator, and the reference is tied to the inverting input. These faults are active low, with the output of the comparators having a pull-up resistor.

As stated previously, the overcurrent fault has some additional complexity. The overcurrent fault senses the current through the primary side of the flyback transformer, and subsequently through the primary-side switch. Using the LT6105 as shown in Figure 5.11, a current shunt topology was chosen for the current sense[11].

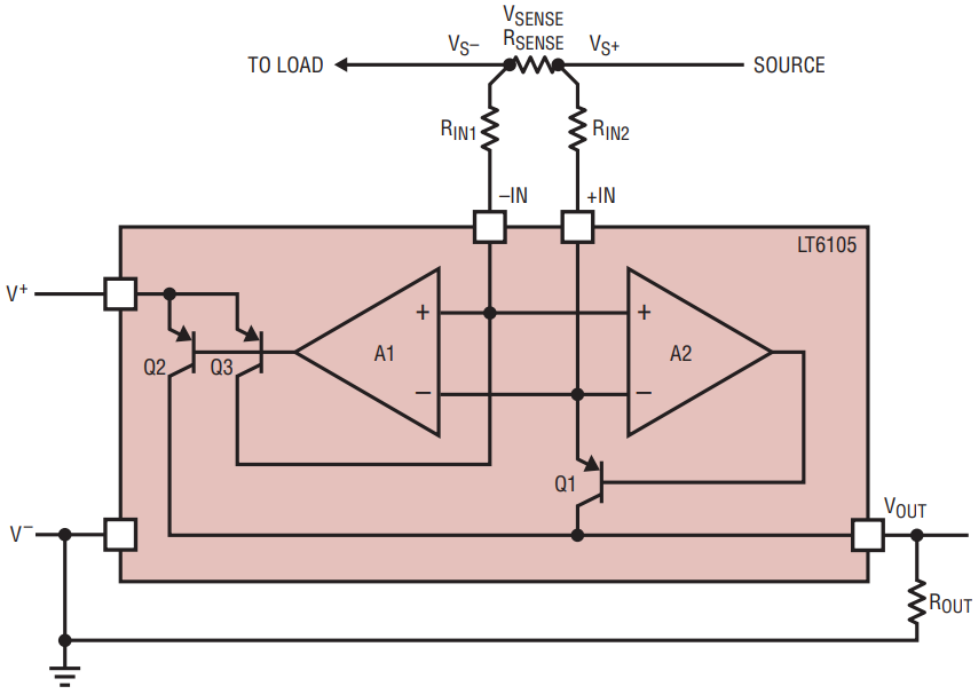

Figure 5.11: LT6105 Diagram[11]

The LT6105 is a current sense amplifier with the output voltage representing the current flowing through the sense resistor. Equations 5.4 and 5.5 determine the output voltage of the amplifier.

$$V_{SENSE}(V) = I_{SENSE} * R_{SENSE} \tag{5.4}$$

$$V_{OUT}(V) = V_{SENSE} * \frac{R_{OUT}}{R_{IN}} \tag{5.5}$$

Using the aforementioned equations, resistor values were chosen to have an overcurrent fault condition at 2.5A. As shown in Chapter 4, the expected peak current through the inductor is 2.236A, so a 2.5A current would indicate a fault. As can be seen in the following usage of the equations, a 20mΩ sense resistor, 4.99kΩ resistor for R_{OUT}, and 100Ω resistor for R_{IN} yields an output voltage of 2.5V at 2.5A. As with the overvoltage fault, the 2.5V reference is tied to the inverting input of an LT1716, and the output of the current sense amplifier is tied to the non-inverting input of the LT1716.

$$V_{SENSE}(V) = 2.5A * 20m\Omega = 50mV$$

$$V_{OUT}(V) = 50mV * \frac{4.99k\Omega}{100\Omega} = 2.495V$$

While overcurrent is a valid fault, on startup or during transients, higher-than-nominal peak currents can appear through the primary-side switch. In order to prevent an instantaneous fault event, an LTC6994 Delay Block is added to the output of the overcurrent comparator[12]. In the implemented configuration, this IC requires the comparator's output to be low for a set amount of time before the overcurrent condition is passed to the control circuitry of the regulator. Figure 5.12 shows the block diagram of the LTC6994.

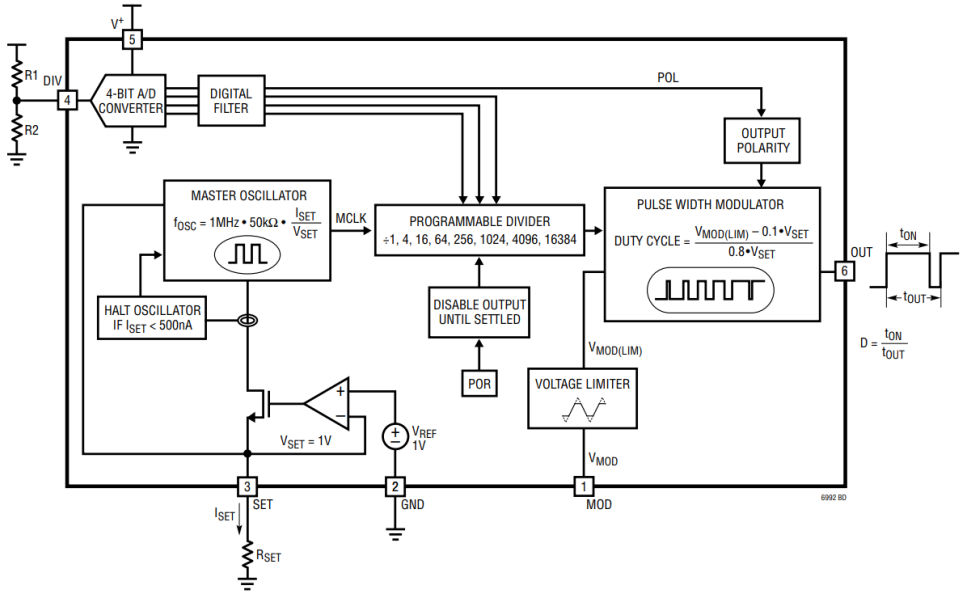

Figure 5.12: LTC6994 Block Diagram[12]

The delay for overcurrent is intended to be in the microsecond timescale, but the exact value was selected based on BOM consolidation, using resistor values from other, more critical, systems. Equation 5.6 is used to determine the delay of the module[12]. The NDIV is used to for coarse time selection, and RSET is used for fine-tuning of the time delay.

$$t_{Delay}(us) = \frac{N_{DIV} * R_{SET}}{50k\Omega} * 1us \tag{5.6}$$

In order to set NDIV, a resistive voltage divider shown in Figure 5.13 is used, identical to the LTC6992 oscillator.

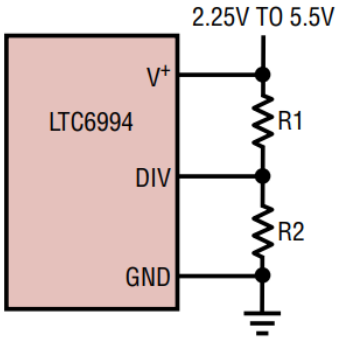

Figure 5.13: LTC6994 NDIV Voltage Divider[12]

Using the figure provided by the LTC6994 data sheet, values for R1 and R2 from Figure 5.14 were chosen. For R1, 976kΩ was chosen, and for R2, 102kΩ was chosen. This yields an NDIV of 8, polarity of 0, and a recommended time delay between 8us and 128us.

DIVCODE	POL	N_{DIV}	Recommended t_{DELAY}	R1 (k)	R2 (k)	V_{DIV}/V^+
0	0	1	1µs to 16µs	Open	Short	≤ 0.03125 ±0.015
1	0	8	8µs to 128µs	976	102	0.09375 ±0.015
2	0	64	64µs to 1.024ms	976	182	0.15625 ±0.015
3	0	512	512µs to 8.192ms	1000	280	0.21875 ±0.015
4	0	4,096	4.096ms to 65.54ms	1000	392	0.28125 ±0.015
5	0	32,768	32.77ms to 524.3ms	1000	523	0.34375 ±0.015
6	0	262,144	262.1ms to 4.194sec	1000	681	0.40625 ±0.015
7	0	2,097,152	2.097sec to 33.55sec	1000	887	0.46875 ±0.015
8	1	2,097,152	2.097sec to 33.55sec	887	1000	0.53125 ±0.015
9	1	262,144	262.1ms to 4.194sec	681	1000	0.59375 ±0.015
10	1	32,768	32.77ms to 524.3ms	523	1000	0.65625 ±0.015
11	1	4,096	4.096ms to 65.54ms	392	1000	0.71875 ±0.015
12	1	512	512µs to 8.192ms	280	1000	0.78125 ±0.015
13	1	64	64µs to 1.024ms	182	976	0.84375 ±0.015
14	1	8	8µs to 128µs	102	976	0.90625 ±0.015
15	1	1	1µs to 16µs	Short	Open	≥ 0.96875 ±0.015

Figure 5.14: LTC6994 DIVCODE Programming[12]

Continuing with Equation 5.6, the final step was to select a value for RSET. A resistor value of 100kΩ was selected as this value is used throughout the regulator, giving a final time delay of 16us.

$$t_{Delay}(us) = \frac{N_{DIV} * R_{SET}}{50k\Omega} * 1us = \frac{8 * 100k\Omega}{50k\Omega} * 1us = 16us$$

5.1.10 Logic Gates

5.1.10.1 Inverter

As stated previously, the optoisolator output of the feedback circuitry is low when the output voltage is below 5V and high when the output voltage is above 5V. The desired behavior for this feedback is inverted as per the AND gates in the next section, so an inverter is placed on the optoisolator's output. An SN74AHCT1G14 inverter from Texas Instruments is used[27].

5.1.10.2 AND Gates

As described in 4.2, there are two AND gates in the control circuitry of the flyback regulator. The SN74HCS21 is used to implement these two AND gates. Since the first AND gate only has two meaningful inputs, the remaining two inputs are tied high to remove their influence.

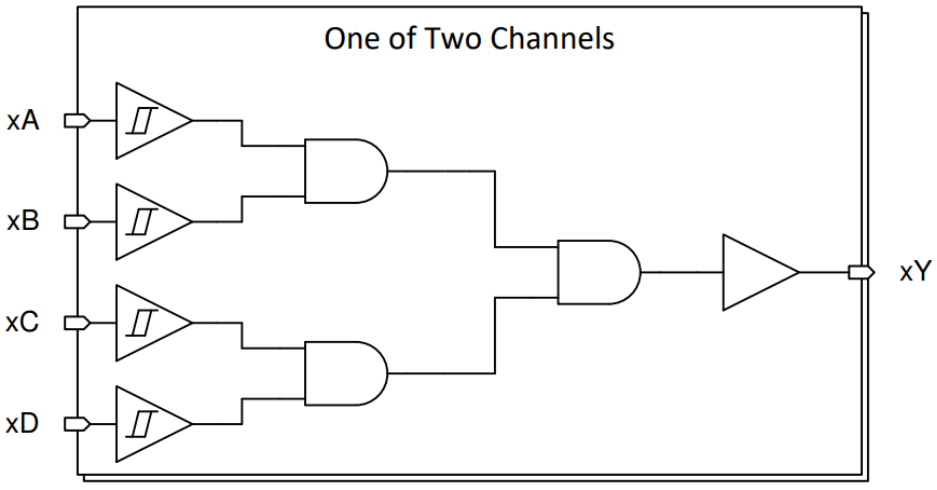

Figure 5.15: SN74HCS21 AND Gate Block Diagram[13]

5.1.11 Remaining Components

Additional miscellaneous components are added to the PCB to improve performance and increase ease of testing. An LED in series with a current limiting resistor is added to the primary-side linear regulator as an indication of power enabled. Also, a 442Ω resistor and a 10Ω resistor are added to the PCB to act as loads. The 442Ω resistor acts as a minimum load. The 10Ω resistor is separated from the output with a jumper, but serves as a nominal load when connected. Decoupling capacitors are present near all ICs which will be discussed in Chapter 6. Finally, a capacitor is added between the primary and secondary RTNs. This is known as a Y-capacitor. This provides a low impedance return path between the primary and secondary sides to reduce common mode noise and subsequently EMI. Since the "connection" between the two RTNs is across a capacitor, galvanic isolation is maintained.

5.2 Simulation

LTSPICE was used for simulation of the flyback regulator. The LTSPICE schematic can be found in Appendix A. Figure 5.16 shows the functioning control scheme in simulation. As expected, the optoisolator output is low when the output voltage is below the set point and high when the output voltage is above the set point. The clock output is only propagated to the gate driver when the output voltage is too low.

Figure 5.17 shows the oscillator output not being propagated to the gate driver when the fault is active during an input undervoltage condition.

Figure 5.18 shows the oscillator output not being propagated to the gate driver when the fault is active during an input overvoltage condition.

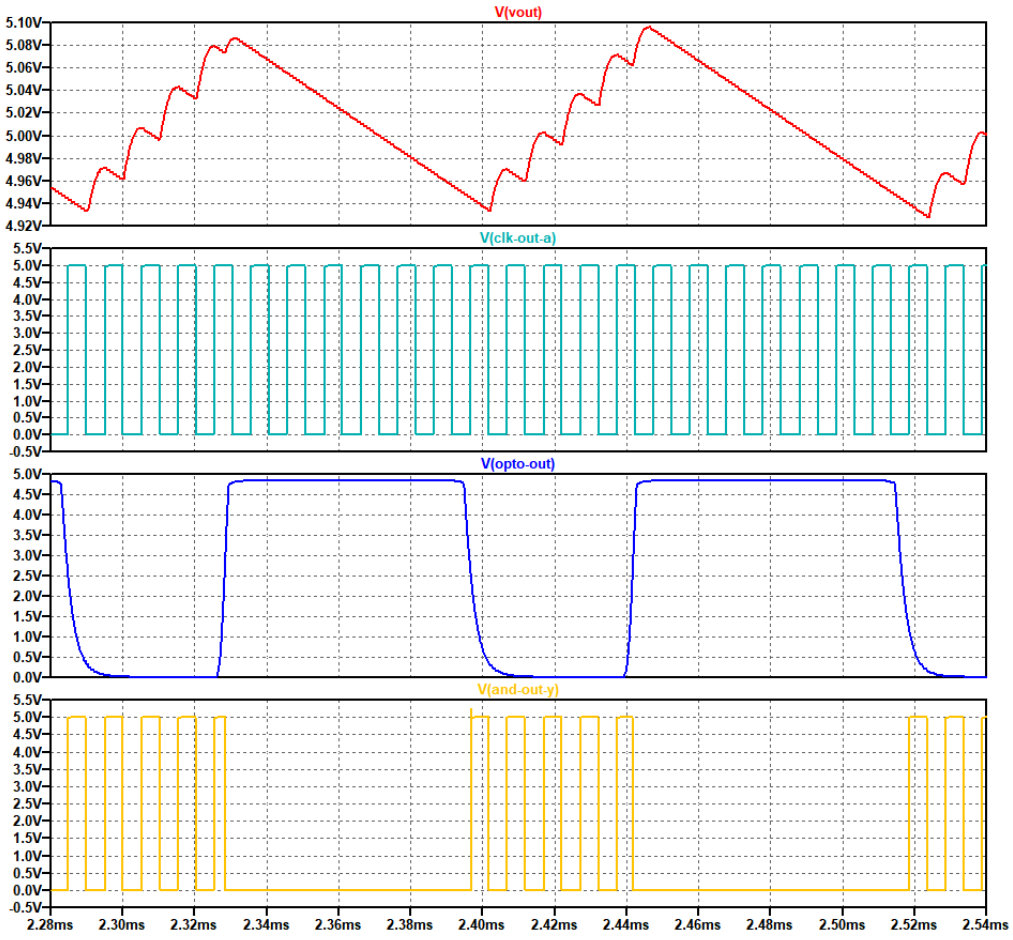

Figure 5.16: SPICE Simulation of Flyback Regulator Feedback

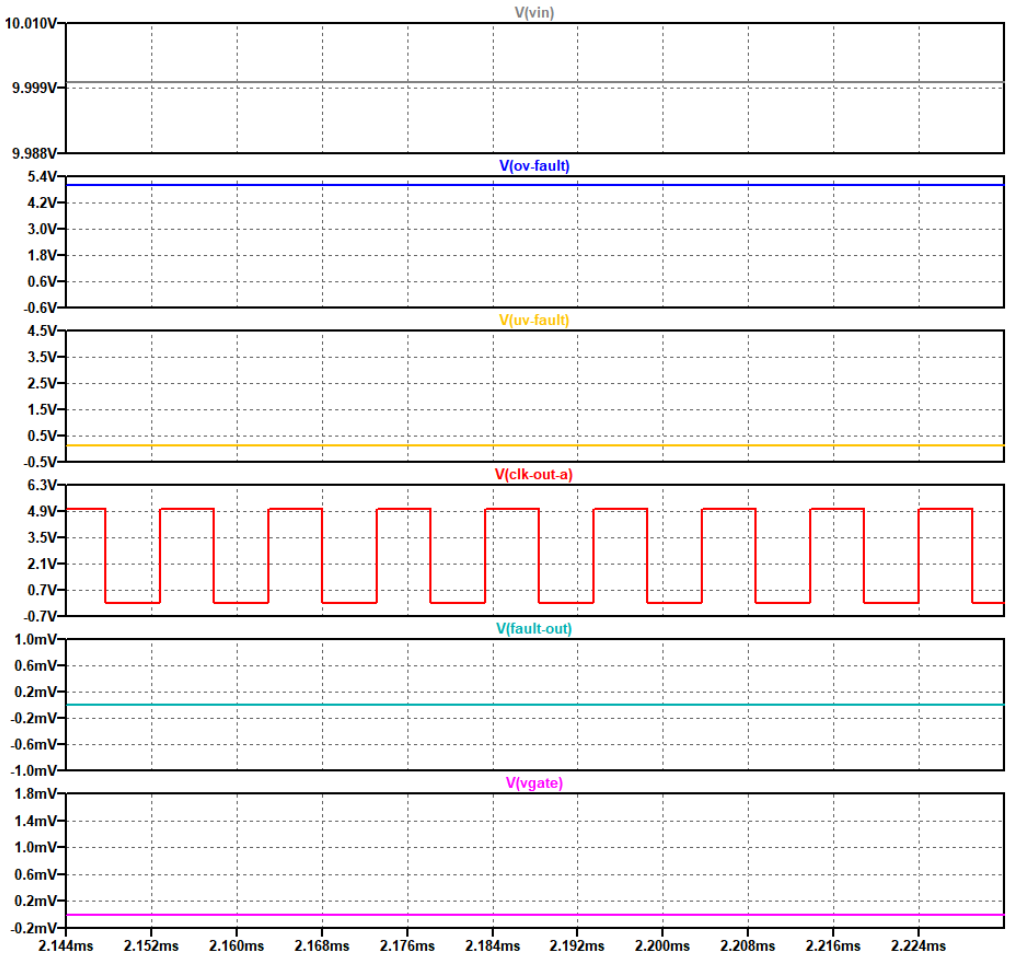

Figure 5.17: Undervoltage Fault Simulation

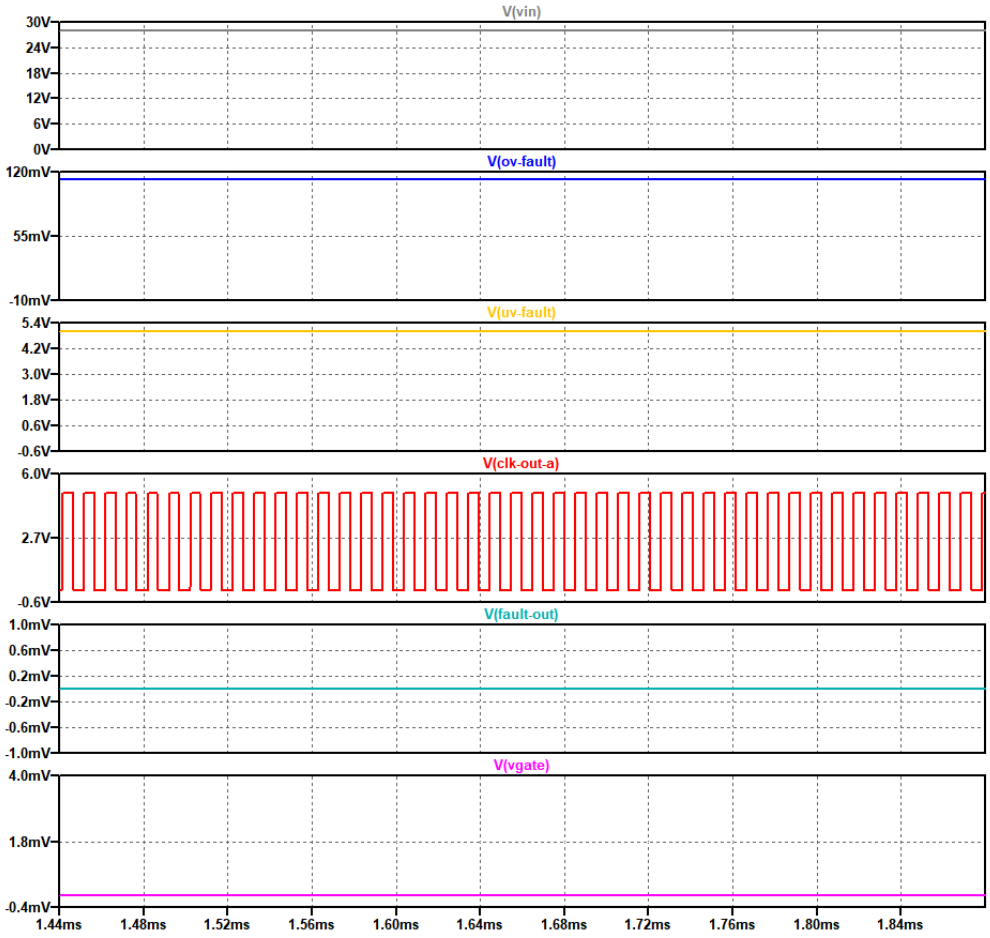

Figure 5.18: Overvoltage Fault Simulation

Chapter 6

PCB Design

The author's driving philosophy for PCB Design is as follows: "PCBs will likely work in SPITE of what you do, but should work BECAUSE of what you do." Subsequently, fundamental PCB design concepts were exercised. Figure 6.1 shows the final PCB layout, without copper polygons poured. The PCB is 3.75" x 1.75" and has 94 components. Test points are abundant for ease of troubleshooting and measuring various signals.

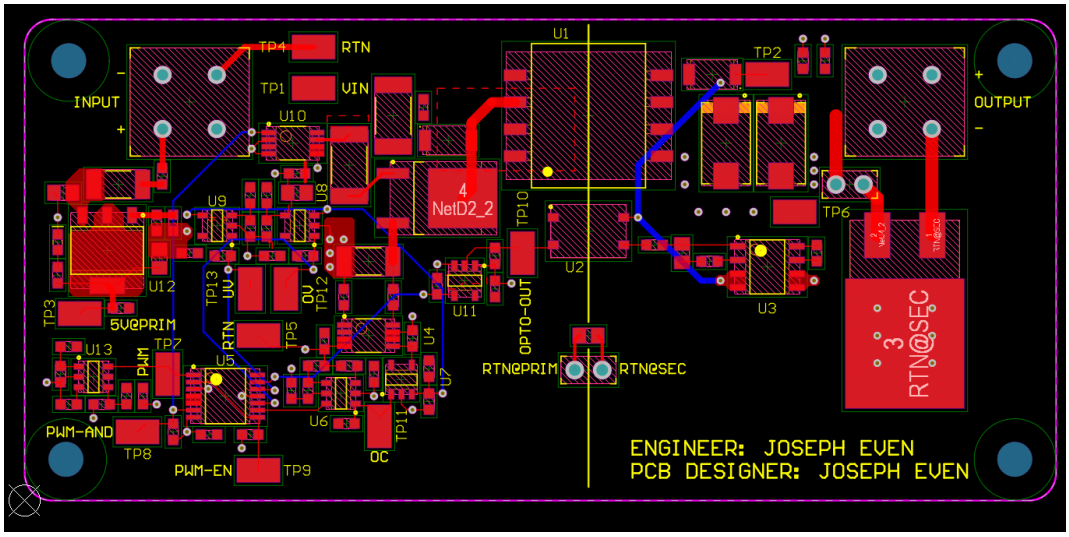

Figure 6.1: PCB Layout

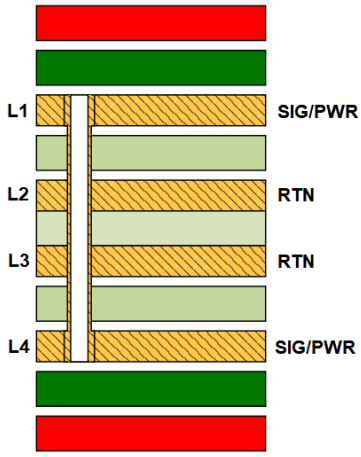

Figure 6.2: PCB Stackup

6.1 Layer Stackup

First, the selection of stackup was chosen for proper signal integrity. The layer stackup consists of four layers, ordered as shown in Figure 6.2. It can be difficult to maintain good PCB design practices with a two-layer PCB, especially with dense placement, as under every trace should be a solid, uninterrupted return path. The benefit of using a four-layer PCB layer generally outweighs the additional cost, especially with a PCB of this size.

Layers 1/2, and 3/4 are spaced closely together with only prepreg separating them. Layers 2 and 3 are far apart, separated by core. Subsequently, Layer 2 is used as a reference and return for signal and power routing on Layer 1. The same is done for Layers 3 and 4, where Layer 3 is a reference and return for signal and power on Layer 4. Layers 2 and 4 are poured polygons dedicated to the return (RTN) nets for the primary side and secondary side. Additionally, Layer 1 on the primary side is poured with the 5V generated by the LT3088. The combination of the L1 power pour and L2 return pour create a capacitor that contributes to decoupling. The low inductance of the power plane also reduces the impact of transients, decreasing EMI[28].

6.2 Decoupling Capacitors

Aside from the small decoupling capacitance generated by the aforementioned planes, discrete capacitors are added for decoupling. Also known as bypass capacitors, decoupling capacitors mitigate high-frequency noise in power supply signals by acting as a local source of energy during transient events. These capacitors are placed near all ICs on the PCB. With strategic placement of decoupling capacitors at the power pins of ICs, energy can be provided to ICs quickly enough to allow the fast output transitions to occur.

6.3 Layout Directives

6.3.1 Switching Components and Current Paths

Due to the switching nature of the flyback regulator, electromagnetic interference (EMI) is particularly relevant. In order to minimize parasitic inductance that could lead to voltage spikes and EMI, the supply voltage trace was kept wide and short.

6.3.2 Isolation

As the flyback regulator offers isolation in its topology, adequate spacing between the primary and secondary returns was necessary.

6.4 PCB Renderings

Figures 6.3 and 6.4 show 3D renders of the final PCB.

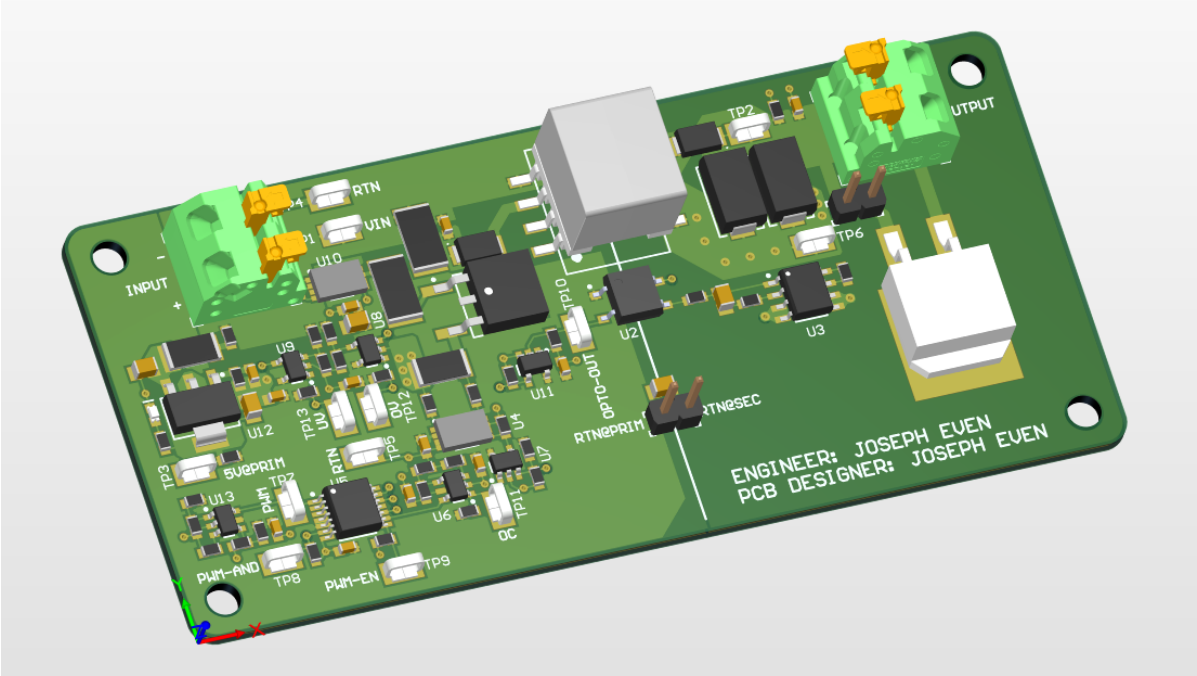

Figure 6.3: Top-side 3D PCB Rendering

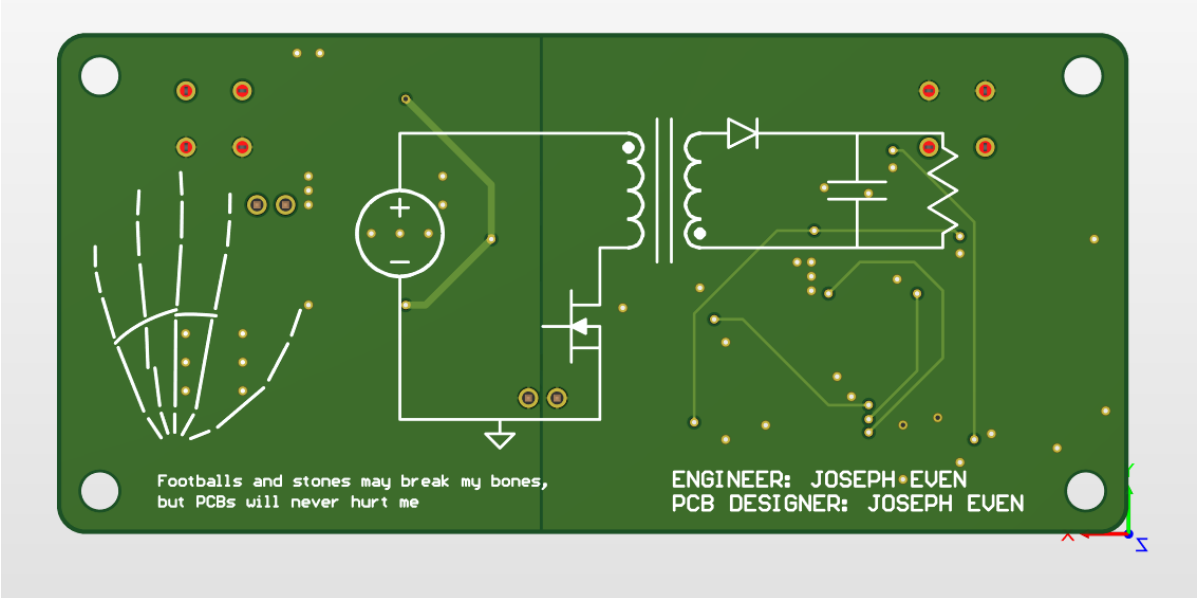

Figure 6.4: Bottom-side 3D PCB Rendering

Chapter 7

Test Procedures

7.1 PCB Bringup

Before performance metrics are determined for the regulator, basic functionality is tested. The first check is to look for shorts between power rails. Using a multimeter in continuity mode, checks are performed to confirm the input voltage, linear regulator output, and RTN are not shorted together. On the secondary side, a continuity check is performed to confirm the output voltage is not shorted to RTN. Once continuity checks are performed, components can be soldered to the PCB.

The first components soldered to the PCB are the voltage regulator and its supporting components. Prior to soldering any other components, the output voltage of the regulator is confirmed with a voltmeter. From this point, the remaining components are soldered. Each time an IC and its supporting circuitry are soldered, the output voltage is validated to check for an improper connection from the soldering or the design itself.

Once all components are soldered to the PCB, performance of critical components is evaluated. The oscillator output frequency is measured using an oscilloscope, faults are checked by

varying the input voltage, and functionality of the optoisolator in the control loop is validated using an oscilloscope.

7.2 Performance Evaluation

Typical metrics of regulator performance include Load Regulation, Output Ripple, Line Regulation, and Efficiency. These four metrics are evaluated for the flyback regulator.

7.2.1 Load Regulation & Output Ripple

Load regulation is the ability of the regulator to maintain its designed output voltage with changes in the load. To test Load Regulation, a variety of different resistive loads are used to draw varying amounts of current and the output voltage is measured at each output current.

Voltage Ripple is the AC voltage superimposed on the nominal DC supply voltage. As previously stated in the Output Capacitance section, Voltage Ripple is nearly unavoidable due to the switching nature of the flyback regulator. To test Voltage Ripple, an oscilloscope is used to measure the peak-to-peak output voltage at varying loads.

The evaluation of Load Regulation and Output Ripple are performed at the same time as they are measured against the same variable – output current.

7.2.2 Line Regulation

Line regulation is the ability for the regulator to maintain its designed output voltage with changes in the input voltage. To test Line Regulation, a 10Ω resistor is used to draw 500mA of current as a load and the input voltage is changed.

7.2.3 Efficiency

Efficiency is the ratio of the output power compared to the input power, generally expressed as a percentage. In order to determine the efficiency, the current supplied by the input voltage source is measured to determine the input power. The output voltage and current are known variables, as the regulator is maintaining its output voltage and the resistive load draws a constant current at the fixed output voltage. The input ratio of power to output power is then calculated.

Chapter 8

Results and Discussion

8.1 PCB Fabrication

The flyback regulator PCBs were manufactured by JLCPCB, a popular PCB manufacturer for hobbyists. The PCB is 1.6mm thick using an FR4 TG130 material. The surface finish is leaded hot air solder leveled (HASL). The top of the PCB with no components is shown in Figure 8.1 and the bottom of the PCB is shown in Figure 8.2.

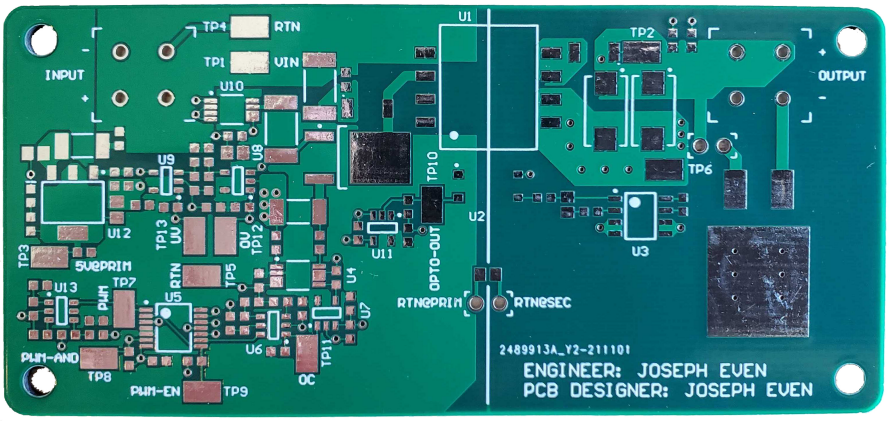

Figure 8.1: PCB Top Without Components

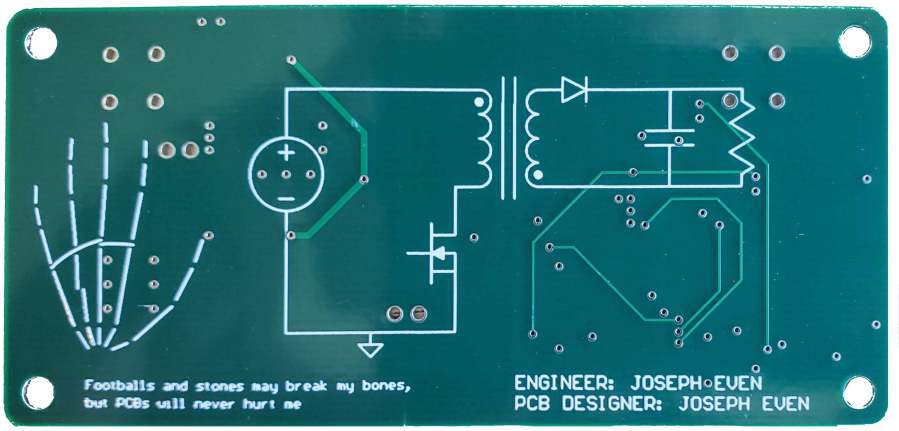

Figure 8.2: PCB Bottom Without Components

8.2 PCB Bringup

When PCBs were delivered, an initial check for shorts was performed. No shorts were found and the components were soldered to the PCB. The PCB with components populated is shown in Figure 8.3.

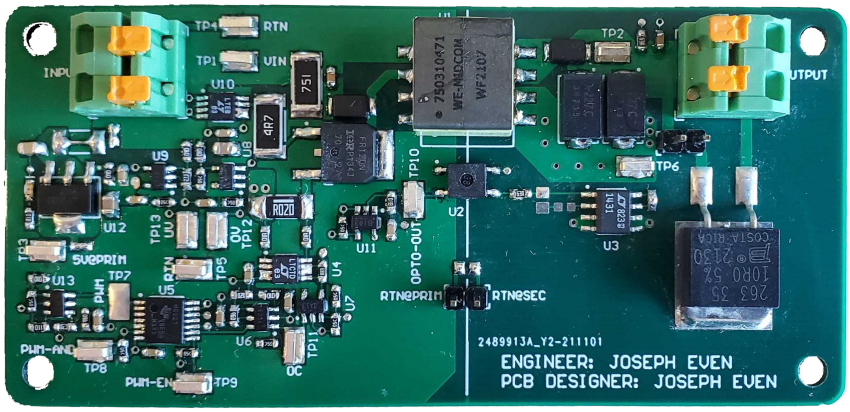

Figure 8.3: PCB Top With Components

8.2.1 LT3088 Linear Regulator

The LT3088 regulator generated an output voltage of 5.016V, with an expected output of 5V. Given the 1% tolerance of the 100kΩ resistor used to set the output voltage, this is within the performance margin specified by the data sheet.

8.2.2 LTC6992 Oscillator

The output frequency of the oscillator was determined to be 98.42kHz, using an oscilloscope as shown in Figure 8.4. The expected output frequency was 98.425kHz. Once again, using the 1% resistor tolerance of the resistor used to set the output frequency, the data sheet performance was met.

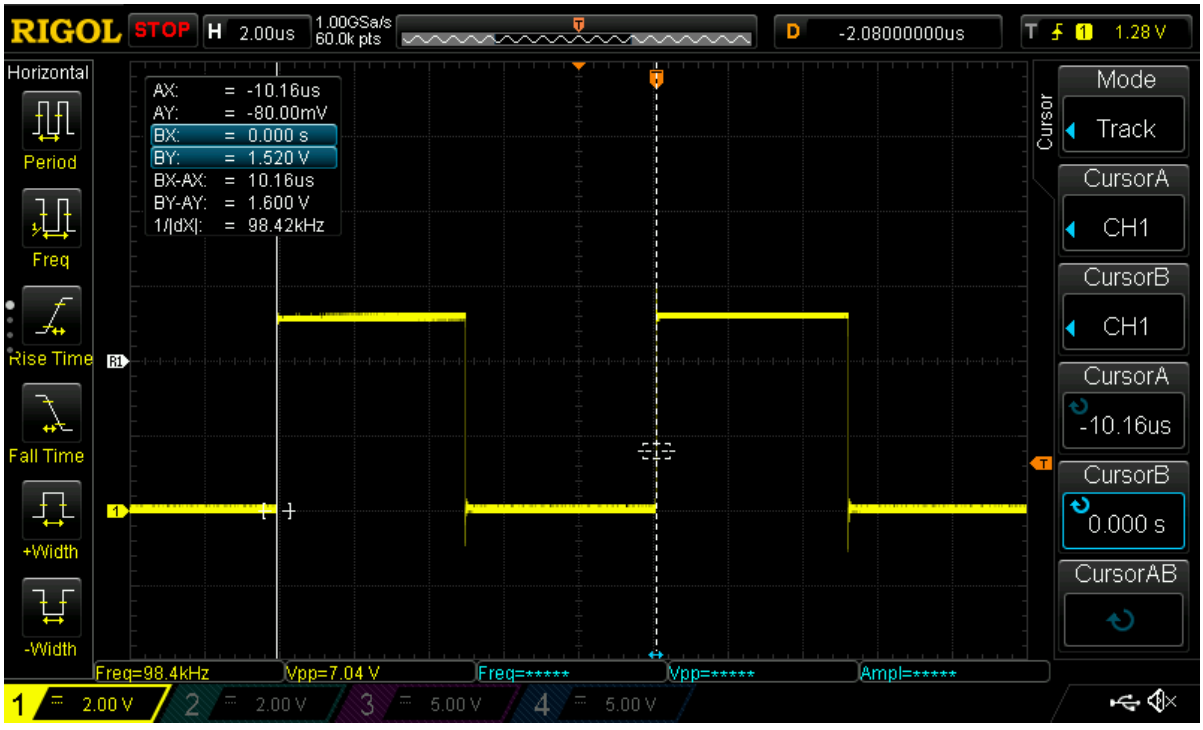

Figure 8.4: LTC6992 Output Frequency

8.2.3 Faults

The Overvoltage Threshold was determined to be 25.25V, compared to the expected 25.23V. The Undervoltage Threshold was determined to be 11.82V, compared to the expected 11.76V. At these thresholds, the output of the first AND gate went low, preventing the clock from propagating to the driver, thus disabling the regulator.

8.2.4 Optoisolator Feedback

Figure 8.5 shows the gate driver control signal (yellow) compared to the optoisolator feedback. Note the optoisolator signal is captured before the inverter. As the previously described control scheme states, when the output voltage is too low, the optoisolator will be disabled. Subsequently, the inverter will make the signal high when the output voltage is too low, allowing the clock to propagate to the gate driver.

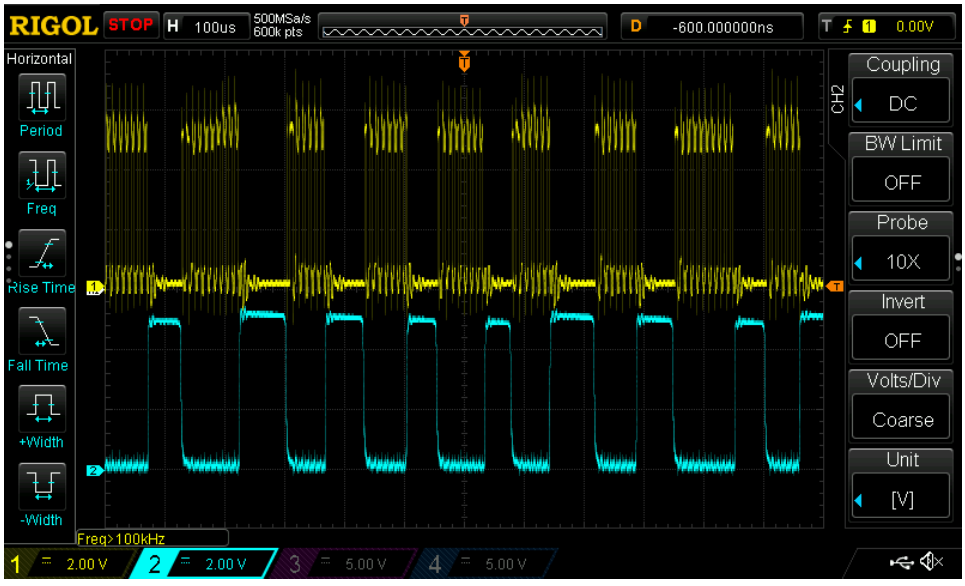

Figure 8.5: Optoisolator Output and Switching Control

8.3 Performance Evaluation

8.3.1 Load Regulation & Output Ripple

The following results were collected with an input voltage of 18V. Note, the 442Ω resistor is a minimum load resistor and is permanently installed on the PCB, so the final load resistance is the parallel combination of the nominal 442Ω resistor and the additional load resistor. Overall, the regulator was very performant in average output voltage as measured by a voltmeter, staying within 0.06% of the desired output voltage. The voltage ripple was less performant, but was still able to maintain the output voltage within 5%.

Nominal Load Resistance (Ω)	**Measured Load Resistance (Ω)**	**Final Load Resistance (Ω)**	**Output Current (A)**	**Measured Output Voltage (V)**	**Voltage Ripple (mV)**	**Voltage Ripple (%)**
442	440	440	0.011	4.998	9.60	0.192
51	50.65	45.42	0.110	4.999	33.00	0.660
18	18.20	17.48	0.286	4.998	83.00	1.661
10	10.26	10.03	0.499	4.997	99.00	1.981
6.8	7.04	6.93	0.722	4.998	126.00	2.521
5.1	5.36	5.30	0.944	4.997	144.00	2.881

Table 8.1: Output Voltages with Varying Loads (18V Input)

8.3.2 Line Regulation

When evaluating the line regulation of the flyback regulator, a nominal current of 500mA was drawn. The results of the line regulation test are shown in Table 8.2. These results show the

flyback regulator was able to maintain its output voltage within 1% over the full input voltage range.

Input Voltage (V)	**Output Voltage (V)**
12.00	4.972
13.00	4.981
14.00	4.986
15.00	4.989
16.00	4.993
17.00	4.996
18.00	4.998
19.00	4.996
20.00	4.997
21.00	4.996
22.00	4.994
23.00	4.995
24.00	4.994
25.00	4.996

Table 8.2: Output Voltages with Varying Input Voltages

8.3.3 Efficiency

Table 8.3 shows the efficiency calculated for the flyback regulator. Overall, the implemented flyback regulator has a very low efficiency. One of the factors for this result is likely the low drive voltage of the gate driver. The LTC1693 is only being supplied 5V from the LT3088, meaning the gate of the switching transistor is not as enhanced as it should be. This results in

an increased drain-to-source resistance in the transistor and an overall decrease in efficiency. The IRFR120N transistor achieves minimum drain-to-source resistance with 10V between the gate and source and the gate driver only provides 5V.

Input Voltage (V)	**Input Current (A)**	**Input Power (W)**	**Output Voltage (V)**	**Output Current (A)**	**Output Power (W)**	**Efficiency (%)**
18.00	0.022	0.396	4.998	0.011	0.057	14.348
18.00	0.084	1.512	4.999	0.110	0.550	36.402
18.00	0.181	3.258	4.998	0.286	1.430	43.906
18.00	0.273	4.914	4.997	0.499	2.493	50.742
18.00	0.368	6.624	4.998	0.722	3.608	54.468
18.00	0.472	8.496	4.997	0.944	4.721	55.567

Table 8.3: Efficiency with Varying Loads

The discrepancy between simulation and the actual implementation can be narrowed down to a few probable causes. The most probable factor leading to discrepancy is the power consumption of the logic gates. In the simulation, “ideal” logic gates are used and have no power consumption. Obviously, these components consume power in the actual implementation. These logic gates switch at a high frequency and subsequently will consume a non-trivial amount of power. Also, extraneous components such as the LED which were not included in simulation consume a small amount of power and have a proportionally significant impact on efficiency at lower load currents.

Chapter 9

Conclusion

From design equations, to simulation, to a physical realization, all aspects of the design process were worked through to create a functional end result. The discrete implementation of a flyback regulator was achieved with the resulting flyback regulating performing under various input voltage conditions and output load conditions.

9.1 Future Work

Given the implemented flyback regulator was intentionally designed discretely compared to commercially-available ICs, it would be somewhat trivial to attempt to reduce the size or number of utilized components. Potential improvements or alterations to the implemented design that would be useful even for off-the-shelf ICs are listed as follows:

- Implement an input EMI filter
- Adjust circuit parameters with the specified equations to generate a larger-than-desired output voltage, and follow with a linear regulator to improve output ripple and noise

- Adjust circuit parameters to achieve a higher voltage, or inverted voltage, relative to the input
- Increase efficiency by adding additional circuitry to drive the switching transistor harder

References

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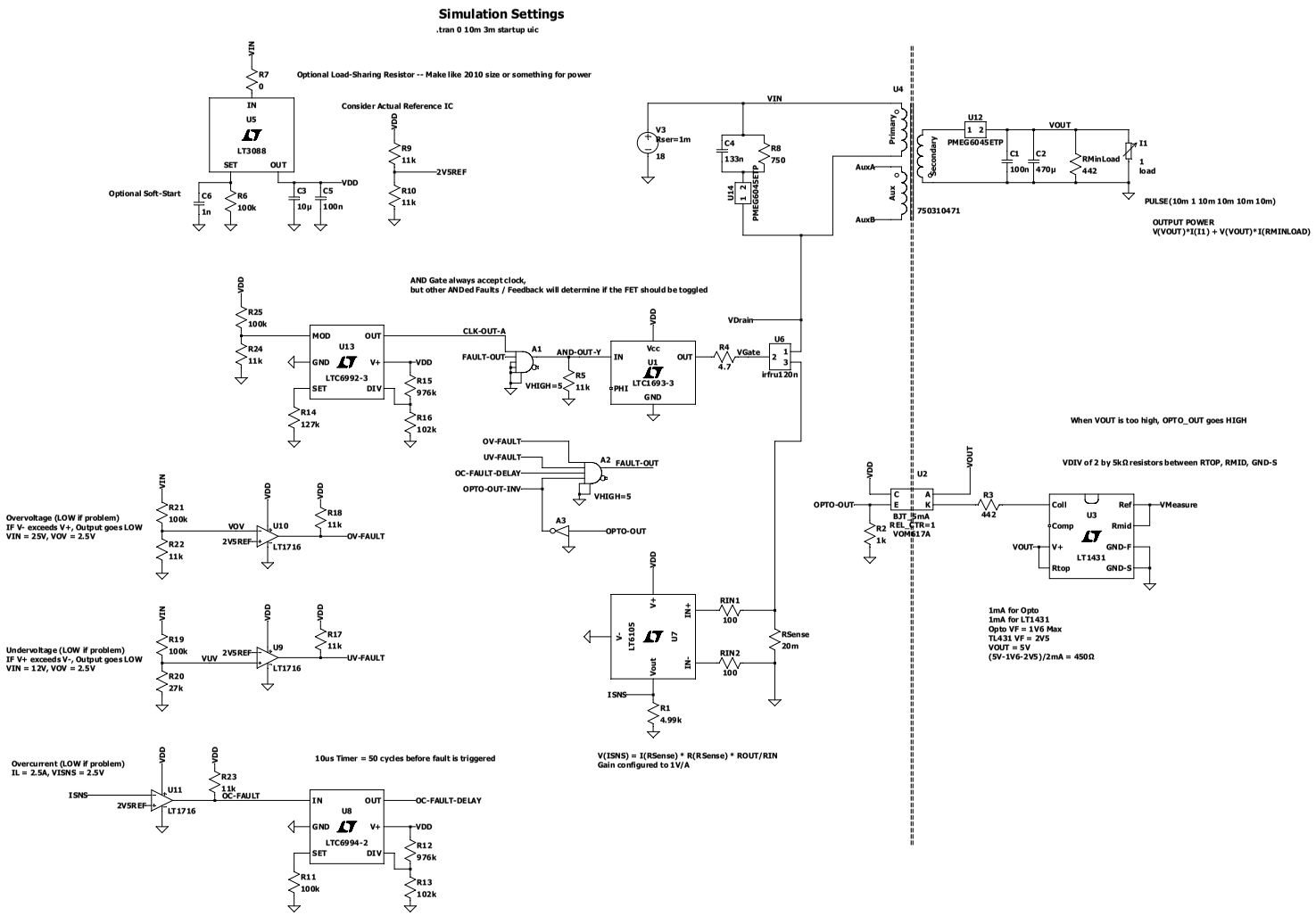
Appendix I

LTSPICE Schematic


Simulation Settings
.tran 0 10m 3m startup uic
VIN
R7
0
Optional Load-Sharing Resistor -- Make like 2010 size or something for power
U5
LT3088
IN
SET
OUT
Consider Actual Reference IC
VDD
R9
11k
2VSREF
R10
11k
Optional Soft-Start
C6
1n
R6
100k
C3
10µ
C5
100n
VDD
V3
Rser=1m
18
C4
133n
R8
750
U14
PME6604SETP
VIN
U4
Primary
Secondary
Aux
AuxA
AuxB
750310471
U12
PME6604SETP
VOUT
C1
100n
C2
470µ
RMinLoad
442
I1
1
load
PULSE(10m 1 10m 10m 10m 10m)
OUTPUT POWER
V(VOUT)*I(I1) + V(VOUT)*I(RMINLOAD)
AND Gate always accept clock,
but other ANDed Faults / Feedback will determine if the FET should be toggled
VDD
R25
100k
R24
11k
U13
LTC6992-3
MOD
OUT
GND
V+
SET
DIV
VDD
R15
976k
R16
102k
R14
127k
CLK-OUT-A
A1
FAULT-OUT
AND-OUT-Y
VHIGH=5
R5
11k
U1
LTC1693-3
Vcc
IN
OUT
GND
PHI
VDD
VDrain
R4
4.7
VGate
U6
irfu120n
When VOUT is too high, OPTO_OUT goes HIGH
VDIV of 2 by 5kΩ resistors between RTOP, RMID, GND-S
OV-FAULT
UV-FAULT
OC-FAULT-DELAY
OPTO-OUT-INV
A2
FAULT-OUT
VHIGH=5
A3
OPTO-OUT
VIN
R21
100k
VOV
U10
2V5REF
LT1716
VDD
R18
11k
OV-FAULT
R22
11k
Overvoltage (LOW if problem)
IF V- exceeds V+, Output goes LOW
VIN = 2.5V, VOV = 2.5V
VIN
R19
100k
VUV
U9
2V5REF
LT1716
VDD
R17
11k
UV-FAULT
R20
27k
Undervoltage (LOW if problem)
IF V+ exceeds V-, Output goes LOW
VIN = 1.2V, VOV = 2.5V
VDD
R23
11k
U11
ISNS
2V5REF
LT1716
OC-FAULT
10us Timer = 50 cycles before fault is triggered
U8
LTC6994-2
IN
OUT
GND
V+
SET
DIV
OC-FAULT-DELAY
VDD
R12
976k
R13
102k
R11
100k
Overcurrent (LOW if problem)
IL = 2.5A, VISNS = 2.5V
VDD
U7
LT6105
V+
V-
IN+
IN-
Vout
RIN1
100
RIN2
100
RSense
20m
ISNS
R1
4.99k
V(ISNS) = I(RSense) * R(RSense) * ROUT/RIN
Gain configured to 1V/A
VDD
U2
OPTO-OUT
C
E
A
K
BJT_5mA
REL_CTR=1
VOM617A
R2
1k
R3
442
VOUT
U3
LT1431
Coll
Comp
V+
Rtop
Ref
Rmid
GND-F
GND-S
VMeasure
1mA for Opto
1mA for LT1431
Opto VF = 1V6 Max
TL431 VF = 2V5
VOUT = 5V
(5V-1V6-2V5)/2mA = 450Ω

Appendix II

Component Data sheets

II.1 LT3088 Linear Voltage Regulator

LT3088

800mA Single Resistor Rugged Linear Regulator

FEATURES

- **Extended Safe Operating Area**
- **Maximum Output Current: 800mA**
- **Stable with or without Input/Output Capacitors**
- **Wide Input Voltage Range: 1.2V to 36V**
- **Single Resistor Sets Output Voltage**
- **Output Adjustable to 0V**
- **50µA SET Pin Current: 1% Initial Accuracy**
- **Output Voltage Noise: 27µV_{RMS}**
- **Parallel Multiple Devices for Higher Current, Heat Spreading and Lower Noise**
- **Pin Compatible Upgrade to LT1117**
- **Reverse-Battery and Reverse-Current Protection**
- <1mV Typical Load Regulation Independent of V_{OUT}
- <0.001%/V Typical Line Regulation
- 3-Lead SOT-223, 3-Lead DD-Pak, 8-Lead 3mm × 3mm DFN Packages

APPLICATIONS

- All Surface Mount Power Supply
- Rugged Industrial Power Supply
- Post Regulator for Switching Supplies
- Low Output Voltage Supply
- Intrinsic Safety Applications

DESCRIPTION

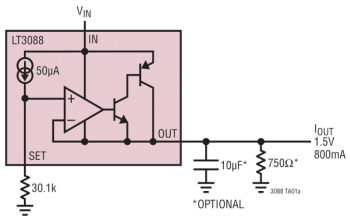
The LT®3088 is an 800mA low dropout linear regulator designed for rugged industrial applications. A key feature of the IC is the extended safe operating area (SOA). The LT3088 can be paralleled for higher output current or heat spreading. The device withstands reverse input and reverse output-to-input voltages without reverse current flow.

The LT3088's precision 50µA reference current source allows a single resistor to program output voltage to any level between zero and 34.5V. The current reference architecture makes load regulation independent of output voltage. The LT3088 is stable with or without input and output capacitors.

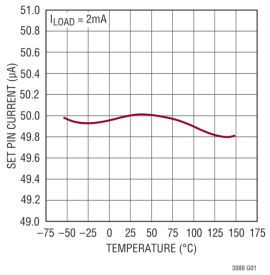
Internal protection circuitry includes reverse-battery and reverse-current protection, current limiting and thermal limiting. The LT3088 is offered in the 3-lead SOT-223, 3-lead DD-Pak, and an 8-lead 3mm × 3mm DFN package.

TYPICAL APPLICATION

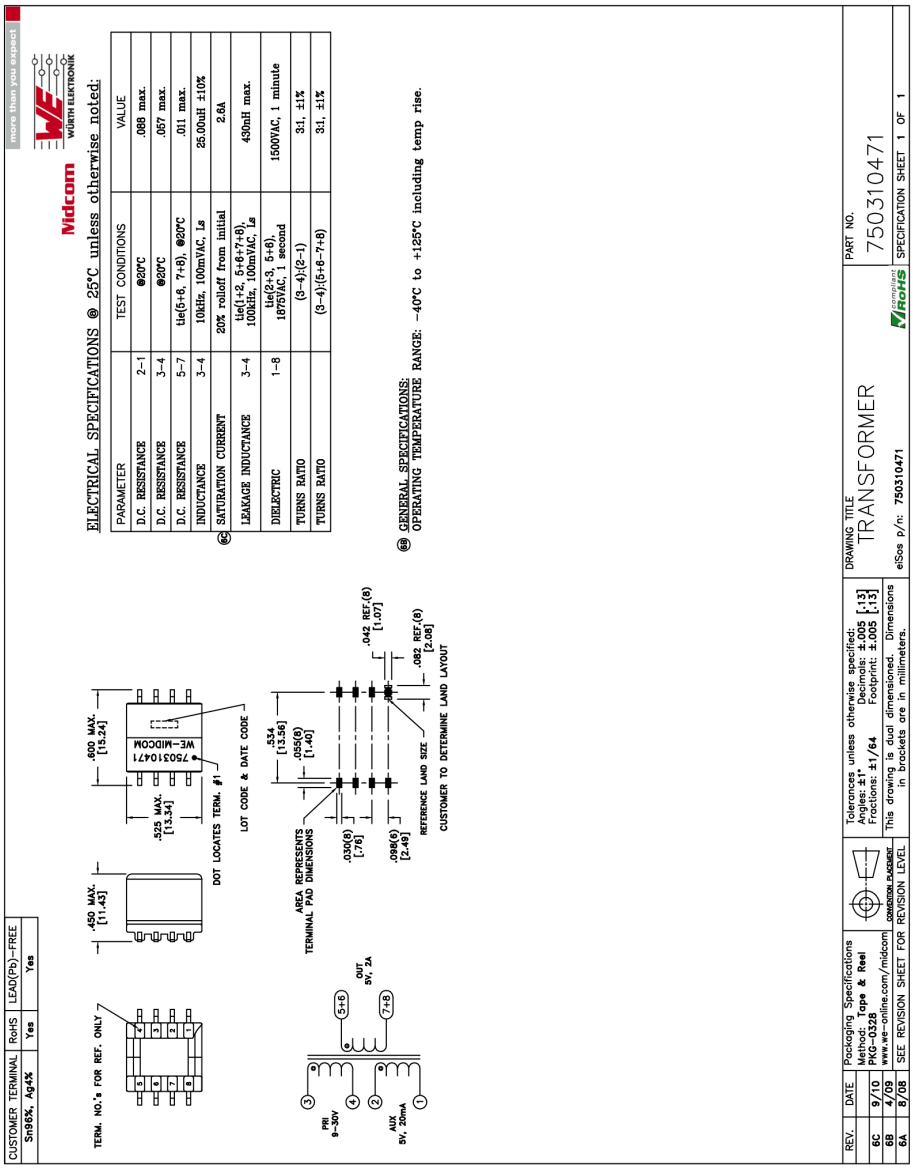
Wide Safe Operating Area Supply



SET Pin Current



II.2 750310471 Flyback Transformer



II.3 LTC6992 Oscillator

LTC6992-1/LTC6992-2/
LTC6992-3/LTC6992-4

TimerBlox:
Voltage-Controlled Pulse
Width Modulator (PWM)

FEATURES

- **Pulse Width Modulation (PWM) Controlled by Simple 0V to 1V Analog Input**
- **Four Available Options Define Duty Cycle Limits**
  - **Minimum Duty Cycle at 0% or 5%**
  - **Maximum Duty Cycle at 95% or 100%**
- **Frequency Range: 3.81Hz to 1MHz**
- Configured with 1 to 3 Resistors
- <1.7% Maximum Frequency Error
- PWM Duty Cycle Error <3.7% Maximum
- Frequency Modulation (VCO) Capability
- 2.25V to 5.5V Single Supply Operation
- 115µA Supply Current at 100kHz
- 500µs Start-Up Time
- CMOS Output Driver Sources/Sinks 20mA
- –55°C to 125°C Operating Temperature Range
- Available in Low Profile (1mm) SOT-23 (ThinSOT™) and 2mm × 3mm DFN
- AEC-Q100 Qualified for Automotive Applications

APPLICATIONS

- PWM Servo Loops
- Heater Control
- LED Dimming Control
- High Vibration, High Acceleration Environments
- Portable and Battery-Powered Equipment

DESCRIPTION

The LTC®6992 is a silicon oscillator with an easy-to-use analog voltage-controlled pulse width modulation (PWM) capability. The LTC6992 is part of the TimerBlox® family of versatile silicon timing devices.

A single resistor, R_{SET}, programs the LTC6992's internal master oscillator frequency. The output frequency is determined by this master oscillator and an internal frequency divider, N_{DIV}, programmable to eight settings from 1 to 16384.

$$f_{OUT} = \frac{1MHz}{N_{DIV}} \bullet \frac{50k\Omega}{R_{SET}}, N_{DIV} = 1,4,16 \ldots 16384$$

Applying a voltage between 0V and 1V on the MOD pin sets the duty cycle.

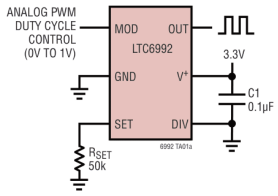
The four versions differ in their minimum/maximum duty cycle. Note that a minimum duty cycle limit of 0% or maximum duty cycle limit of 100% allows oscillations to stop at the extreme duty cycle settings.

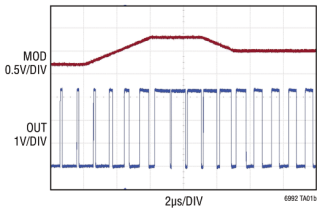
DEVICE NAME	PWM DUTY CYCLE RANGE
LTC6992-1	0% to 100%
LTC6992-2	5% to 95%
LTC6992-3	0% to 95%
LTC6992-4	5% to 100%

For easy configuration of the LTC6992, use the TimerBlox LTC6992: PWM Web-Based Design Tool.

TYPICAL APPLICATION

1MHz Pulse Width Modulator





II.4 LTC1693 Gate Driver

LTC1693

High Speed Single/Dual N-Channel MOSFET Drivers

FEATURES

- **Dual MOSFET Drivers in SO-8 Package or Single MOSFET Driver in MSOP Package**
- 1GΩ Electrical Isolation Between the Dual Drivers Permits High/Low Side Gate Drive
- **1.5A Peak Output Current**
- 16ns Rise/Fall Times at V_{CC} = 12V, C_L = 1nF
- Wide V_{CC} Range: 4.5V to 13.2V
- CMOS Compatible Inputs with Hysteresis, Input Thresholds are Independent of V_{CC}
- Driver Input Can Be Driven Above V_{CC}
- Undervoltage Lockout
- Thermal Shutdown

APPLICATIONS

- Power Supplies
- High/Low Side Drivers
- Motor/Relay Control
- Line Drivers
- Charge Pumps

DESCRIPTION

The LTC®1693 family drives power N-channel MOSFETs at high speed. The 1.5A peak output current reduces switching losses in MOSFETs with high gate capacitance.

The LTC1693-1 contains two noninverting drivers while the LTC1693-2 contains one noninverting and one inverting driver. These dual drivers are electrically isolated and independent. The LTC1693-3 is a single driver with an output polarity select pin.

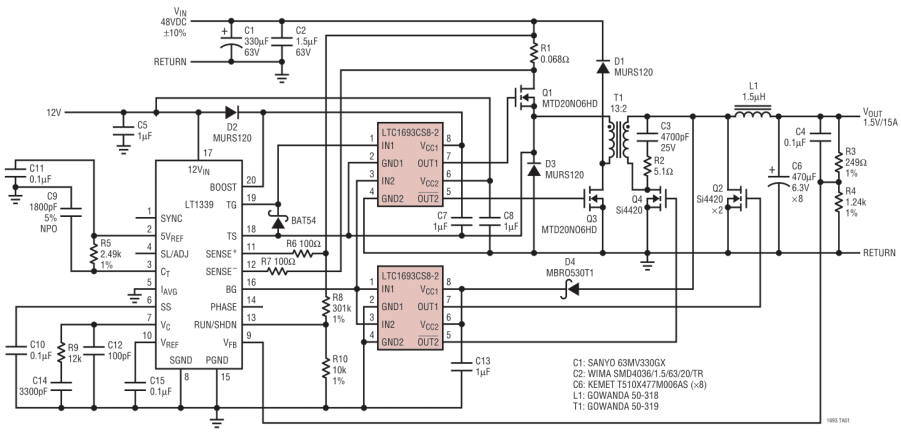
All MOSFET drivers offer V_{CC} independent CMOS input thresholds with 1.2V of typical hysteresis. They can level-shift the input logic signal up or down to the rail-to-rail V_{CC} drive for the external MOSFET.

The LTC1693 contains an undervoltage lockout circuit and a thermal shutdown circuit that disable the external N-channel MOSFET gate drive when activated.

The LTC1693-1 and LTC1693-2 come in an 8-lead SO package. The LTC1693-3 comes in an 8-lead MSOP package.

TYPICAL APPLICATION

Two Transistor Forward Converter



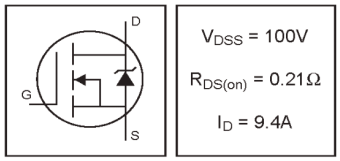
II.5 IRFR120N N-Channel MOSFET

International
IOR Rectifier

PD - 95067A

IRFR/U120NPbF

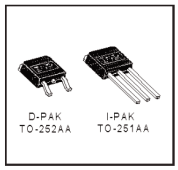
- Surface Mount (IRFR120N)
- Straight Lead (IRFU120N)
- Advanced Process Technology
- Fast Switching
- Fully Avalanche Rated
- Lead-Free



V_{DSS} = 100V

$R_{DS(on)}$ = 0.21Ω

I_D = 9.4A



Description

Fifth Generation HEXFETs from International Rectifier utilize advanced processing techniques to achieve the lowest possible on-resistance per silicon area. This benefit, combined with the fast switching speed and ruggedized device design that HEXFET Power MOSFETs are well known for, provides the designer with an extremely efficient device for use in a wide variety of applications.

The D-PAK is designed for surface mounting using vapor phase, infrared, or wave soldering techniques. The straight lead version (IRFU series) is for through-hole mounting applications. Power dissipation levels up to 1.5 watts are possible in typical surface mount applications.

Absolute Maximum Ratings

	Parameter	Max.	Units
I_D @ T_C = 25°C	Continuous Drain Current, V_{GS} @ 10V	9.4	A
I_D @ T_C = 100°C	Continuous Drain Current, V_{GS} @ 10V	6.6	
I_{DM}	Pulsed Drain Current ①⑥	38	
P_D @T_C = 25°C	Power Dissipation	48	W
	Linear Derating Factor	0.32	W/°C
V_{GS}	Gate-to-Source Voltage	± 20	V
E_{AS}	Single Pulse Avalanche Energy②⑥	91	mJ
I_{AR}	Avalanche Current①⑥	5.7	A
E_{AR}	Repetitive Avalanche Energy①⑥	4.8	mJ
dv/dt	Peak Diode Recovery dv/dt ③	5.0	V/ns
T_J	Operating Junction and	-55 to + 175	°C
T_{STG}	Storage Temperature Range		
	Soldering Temperature, for 10 seconds	300 (1.6mm from case)	

Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	——	3.1	°C/W
$R_{\theta JA}$	Junction-to-Ambient (PCB mount) **	——	50	
$R_{\theta JA}$	Junction-to-Ambient	——	110	

II.6 LT1431 Reference

LINEAR TECHNOLOGY

LT1431

Programmable Reference

FEATURES

- **Guaranteed 0.4% Initial Voltage Tolerance**
- **0.1Ω Typical Dynamic Output Impedance**
- Fast Turn-On
- Sink Current Capability, 1mA to 100mA
- Low Reference Pin Current
- Available in J8, N8, S8 or 3-Lead TO-92 Z Packages

APPLICATIONS

- Linear Regulators
- Adjustable Power Supplies
- Switching Power Supplies

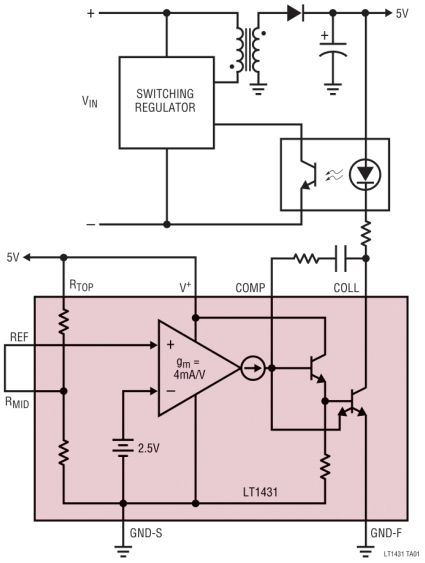
DESCRIPTION

The LT®1431 is an adjustable shunt voltage regulator with 100mA sink capability, 0.4% initial reference voltage tolerance and 0.3% typical temperature stability. On-chip divider resistors allow the LT1431 to be configured as a 5V shunt regulator, with 1% initial voltage tolerance and requiring no additional external components. By adding two external resistors, the output voltage may be set to any value between 2.5V and 36V. The nominal internal current limit of 100mA may be decreased by including one external resistor.

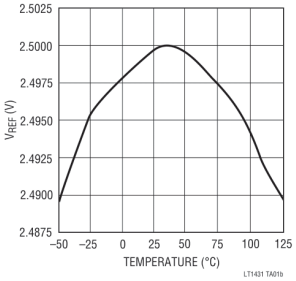
A simplified 3-pin version, the LT1431CZ/LT1431IZ, is available for applications as an adjustable reference and is pin compatible with the TL431.

TYPICAL APPLICATION

Isolated 5V Regulator



VREF vs Temperature

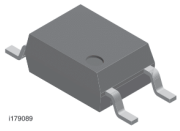


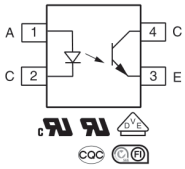
II.7 VOMA617A Optoisolator

VISHAY.
www.vishay.com

VOM617A
Vishay Semiconductors

Low Input Current, Phototransistor Output, SOP-4, Mini-Flat Package





FEATURES

- Operating temperature from -55 °C to +110 °C
- SOP-4 mini-flat package
- Isolation test voltage, 3750 V_{RMS}
- Low saturation voltage
- Fast switching times
- Low coupling capacitance
- End-stackable, 0.100" (2.54 mm) spacing
- CTR range 50 % to 600 %, I_F = 5 mA
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

Pb-free
e3
RoHS COMPLIANT
HALOGEN FREE
GREEN (5-2008)

LINKS TO ADDITIONAL RESOURCES

3D Models | Design Tools | Related Documents

DESCRIPTION

The 110 °C rated VOM617A has a GaAs infrared emitting diode emitter, which is optically coupled to a silicon planar phototransistor detector, and is incorporated in a 4 pin 100 mil lead pitch miniflat package. It features a high current transfer ratio, low coupling capacitance, and high isolation voltage.

These coupling devices are designed for signal transmission between two electrically separated circuits.

APPLICATIONS

- PLCs
- Telecommunication
- Lighting control system
- Solar inverters
- AC drives

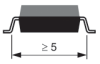
AGENCY APPROVALS

(All parts are certified under base model VOM617A)

- UL1577
- cUL
- DIN EN 60747-5-5 (VDE 0884-5), available with option 1
- CQC
- FIMKO

ORDERING INFORMATION

V	O	M	6	1	7	A	-	#	X	0	0	1	T	#
PART NUMBER								CTR BIN	VDE OPTION				TAPE AND REEL	



AGENCY CERTIFIED/ PACKAGE	CTR (%) 5 mA							
UL, cUL, FIMKO, CQC	**50 to 600**	**63 to 125**	**100 to 200**	**160 to 320**	**250 to 500**	**80 to 160**	**130 to 260**	**200 to 400**
SOP-4, mini-flat	VOM617AT	VOM617A-2T	VOM617A-3T	VOM617A-4T	VOM617A-6T	VOM617A-7T	VOM617A-8T	VOM617A-9T
VDE, UL, cUL, FIMKO, CQC (option 1)	**50 to 600**	**63 to 125**	**100 to 200**	**160 to 320**	**250 to 500**	**80 to 160**	**130 to 260**	**200 to 400**
SOP-4, mini-flat	VOM617A-X001T	VOM617A-2X001T	VOM617A-3X001T	VOM617A-4X001T	VOM617A-6X001T	VOM617A-7X001T	VOM617A-8X001T, VOM617A-8X001T2 (1)	VOM617A-9X001T

Notes

- Available only on tape and reel
(1) Product is rotated 180° in tape and reel cavity

II.8 PMEG6045ETP Output Diode

PMEG6045ETP

High-temperature 60 V, 4.5 A Schottky barrier rectifier

28 May 2018 **Product data sheet**

1. General description

Planar Maximum Efficiency General Application (MEGA) Schottky barrier rectifier with an integrated guard ring for stress protection, encapsulated in a SOD128 small and flat lead Surface-Mounted Device (SMD) plastic package.

2. Features and benefits

- Average forward current: $I_{F(AV)} \leq 4.5$ A
- Reverse voltage: $V_R \leq 60$ V
- Low forward voltage
- High power capability due to clip-bonding technology
- Small and flat lead SMD plastic package
- AEC-Q101 qualified
- High temperature $T_j \leq 175$ °C
- Capable for reflow and wave soldering

3. Applications

- Low voltage rectification
- High efficiency DC-to-DC conversion
- Switch mode power supply
- Reverse polarity protection
- Low power consumption application

4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$I_{F(AV)}$	average forward current	$\delta = 0.5$; $f = 20$ kHz; $T_{sp} \leq 155$ °C; square wave		-	-	4.5	A
V_R	reverse voltage	$T_j = 25$ °C		-	-	60	V
V_F	forward voltage	$I_F = 4.5$ A; $t_p \leq 300$ µs; $\delta \leq 0.02$; $T_j = 25$ °C; pulsed		-	460	530	mV
I_R	reverse current	$V_R = 60$ V; $T_j = 25$ °C; pulsed		-	115	400	µA

nexperia

II.9 LT1716 Comparator

LT1716

SOT-23, 44V, Over-the-Top, Micropower, Precision Rail-to-Rail Comparator

FEATURES

- **Operates from 2.7V to 44V**
- **Over-The-Top®: Input Common Mode Range Extends 44V Above V^-, Independent of V^+**
- **Micropower: 35µA I_Q**
- **Offset Voltage: 1.5mV Max**
- **Valid Output with Either Input 5V Below V^-**
- Rail-to-Rail Output Swing
- Output Can Drive Loads Above V^+
- Internal Pull-Up Current
- –40°C to 125°C Operating Temperature Range
- Low Profile (1mm) SOT-23 (ThinSOT™) Package
- AEC-Q100 Qualified for Automotive Applications

APPLICATIONS

- Power Supply Monitors
- Relay/Lamp Driver
- Oscillators
- Peak Detector
- Level Shifting

DESCRIPTION

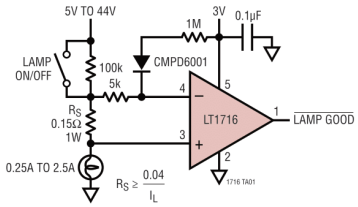
The LT®1716 comparator operates on any total power supply voltage between 2.7V and 44V drawing 35µA of quiescent current. The LT1716 has a unique input stage that can be taken 44V above V^-, independent of V^+ supply. (Built-in resistors protect the inputs for faults below the negative supply of up to 5V.) The inputs can withstand 44V both differential and common mode.

The output stage includes a class "B" pull-up current source, eliminating the need for an external resistive pull-up and saving power. Output voltage swings to within 35mV of the negative supply and 55mV of the positive supply, which makes the comparator a good choice for low voltage single supply operation. The output stage is also designed to drive loads connected to a higher supply than the LT1716 supply, the same as an open collector output stage.

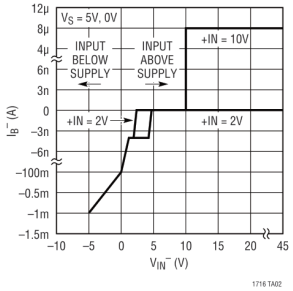
The LT1716 is available in a SOT-23 5-lead package.

TYPICAL APPLICATION

Lamp Monitor



Input Bias Current vs Input Bias Voltage



II.10 LT6105 Current Sense Amplifier

LT6105

Precision, Extended Input Range Current Sense Amplifier

FEATURES

- **Very Wide, Over-the-Top®, Input Common Mode Range**
  - Extends 44V Above V^- (Independent of V^+)
  - Extends –0.3V Below V^-
- **Wide Power Supply Range: 2.85V to 36V**
- **Input Offset Voltage: 300µV Maximum**
- **Gain Accuracy: 1% Max**
- Gain Configurable with External Resistors
- Operating Current: 150µA
- Slew Rate: 2V/µs
- Sense Input Current When Powered Down: 1nA
- Full-Scale Output Current: 1mA Minimum
- Operating Temperature Range –40°C to 125°C
- Available in 2mm × 3mm DFN and 8-Lead MSOP Packages

APPLICATIONS

- High Side or Low Side Current Sensing
- Current Monitoring on Positive or Negative Supply Voltages
- Battery Monitoring
- Fuse/MOSFET Monitoring
- Automotive
- Power Management
- Portable Test/Measurement Systems

DESCRIPTION

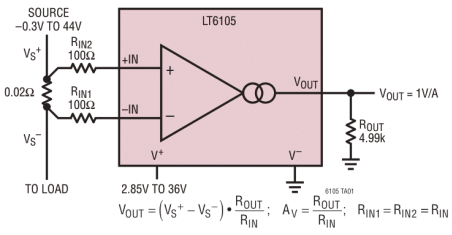
The LT®6105 is a micropower, precision current sense amplifier with a very wide input common mode range. The LT6105 monitors unidirectional current via the voltage across an external sense resistor. The input common mode range extends from –0.3V to 44V, with respect to the negative supply voltage (V^-). This allows the LT6105 to operate as a high side current sense monitor or a low side current sense monitor. It also allows the LT6105 to monitor current on a negative supply voltage, as well as continuously monitor a battery from full charge to depletion. The inputs of LT6105 can withstand differential voltages up to ±44V, which makes it ideal for monitoring a fuse or MOSFET switch.

Gain is configured with external resistors from 1V/V to 100V/V. The input common mode rejection and power supply rejection are in excess of 100dB and the input offset voltage is less than 300µV. A typical slew rate of 2V/µs ensures fast response to unexpected current changes.

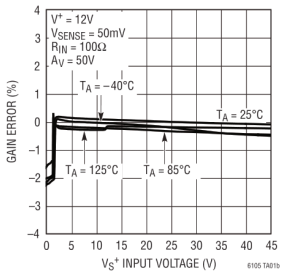
The LT6105 can operate from an independent power supply of 2.85V to 36V and draws only 150µA. When V^+ is powered down, the sense pins are biased off. This prevents loading of the monitored circuit, irrespective of the sense voltage. The LT6105 is available in a 6-lead DFN and 8-lead MSOP package.

TYPICAL APPLICATION

Gain of 50 Current Sense Amplifier



Gain Error vs Input Voltage



II.11 LTC6994 Delay Block

ANALOG DEVICES

LTC6994-1/LTC6994-2

TimerBlox: Delay Block/ Debouncer

FEATURES

- **Delay Range: 1µs to 33.6 Seconds**
- Configured with 1 to 3 Resistors
- Delay Max Error:
  - <2.3% for Delay > 512µs
  - <3.4% for Delay of 8µs to 512µs
  - <5.1% for Delay of 1µs to 8µs
- Delay One or Both Rising/Falling Edges
- 2.25V to 5.5V Single Supply Operation
- 70µA Supply Current at 10µs Delay
- 500µs Start-Up Time
- CMOS Output Driver Sources/Sinks 20mA
- –55°C to 125°C Operating Temperature Range
- Available in Low Profile (1mm) SOT-23 (ThinSOT™) and 2mm × 3mm DFN
- AEC-Q100 Qualified for Automotive Applications

APPLICATIONS

- Noise Discriminators/Pulse Qualifiers
- Delay Matching
- Switch Debouncing
- High Vibration, High Acceleration Environments
- Portable and Battery-Powered Equipment

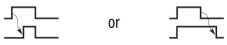
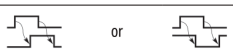
DESCRIPTION

The LTC®6994 is a programmable delay block with a range of 1µs to 33.6 seconds. The LTC6994 is part of the TimerBlox® family of versatile silicon timing devices.

A single resistor, R_{SET}, programs an internal master oscillator frequency, setting the LTC6994's time base. The input-to-output delay is determined by this master oscillator and an internal clock divider, N_{DIV}, programmable to eight settings from 1 to 2^{21}:

$$t_{DELAY} = \frac{N_{DIV} \bullet R_{SET}}{50k\Omega} \bullet 1\mu s,\ N_{DIV} = 1, 8, 64, ..., 2^{21}$$

The output (OUT) follows the input (IN) after delaying the rising and/or falling transitions. The LTC6994-1 will delay the rising or falling edge. The LTC6994-2 will delay both transitions, and adds the option to invert the output.

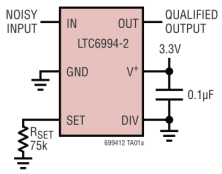
DEVICE	DELAY FUNCTION
LTC6994-1	
LTC6994-2	

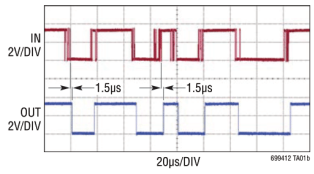
The LTC6994 also offers the ability to dynamically adjust the delay time via a separate control voltage.

For easy configuration of the LTC6994, use the TimerBlox LTC6994: Delay Web-Based Design Tool.

TYPICAL APPLICATION

Noise Discriminator





II.12 SN74AHCT1G14

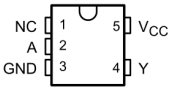
SINGLE SCHMITT-TRIGGER INVERTER GATE

Check for Samples: SN74AHCT1G14

FEATURES

- **Operating Range 4.5-V to 5.5-V**
- **Max t_{pd} of 8 ns at 5-V**
- **Low Power Consumption, 10-µA Max I_{CC}**
- **±8-mA Output Drive at 5-V**
- **Inputs Are TTL-Voltage Compatible**
- **Latch-Up Performance Exceeds 250 mA Per JESD 17**

DBV OR DCK PACKAGE
(TOP VIEW)



NC – No internal connection

See mechanical drawings for dimensions.

DESCRIPTION

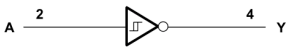
description/ordering information The SN74AHCT1G14 contains a single inverter gate. The device performs the Boolean function $Y = \overline{A}$.

The device functions as an independent inverter gate, but because of the Schmitt action, gates may have different input threshold levels for positive- (V_{T+}) and negative-going (V_{T-}) signals.

FUNCTION TABLE

INPUTS	OUTPUT
A	**Y**
H	L
L	H

LOGIC DIAGRAM (POSITIVE LOGIC)



II.13 SN74HCS21 AND Gate

TEXAS INSTRUMENTS
SN74HCS21
SCLS793A – MARCH 2020 – REVISED JUNE 2020

SN74HCS21 Dual 4-Input AND Gates with Schmitt-Trigger Inputs

1 Features

- Wide operating voltage range: 2 V to 6 V
- Schmitt-trigger inputs allow for slow or noisy input signals
- Low power consumption
  - Typical I_{CC} of 100 nA
  - Typical input leakage current of ±100 nA
- ±7.8-mA output drive at 5 V
- Extended ambient temperature range: –40°C to +125°C, T_A

2 Applications

- Combining power good signals
- Enable digital signals

3 Description

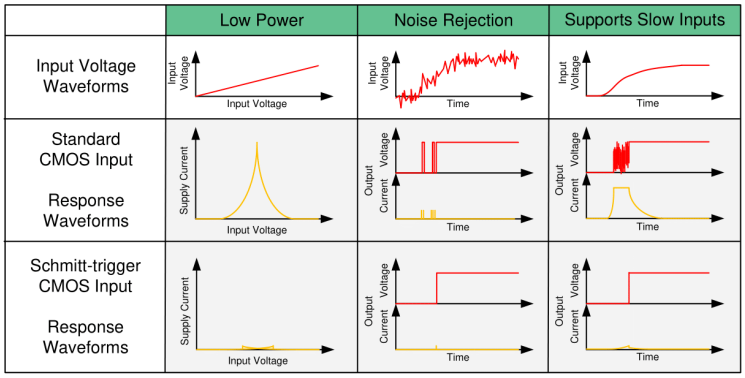
This device contains two independent 4-input AND gates with Schmitt-trigger inputs. Each gate performs the Boolean function Y = A ● B ● C ● D in positive logic.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
SN74HCS21PWR	TSSOP (14)	5.00 mm × 4.40 mm
SN74HCS21DR	SOIC (14)	8.70 mm × 3.90 mm

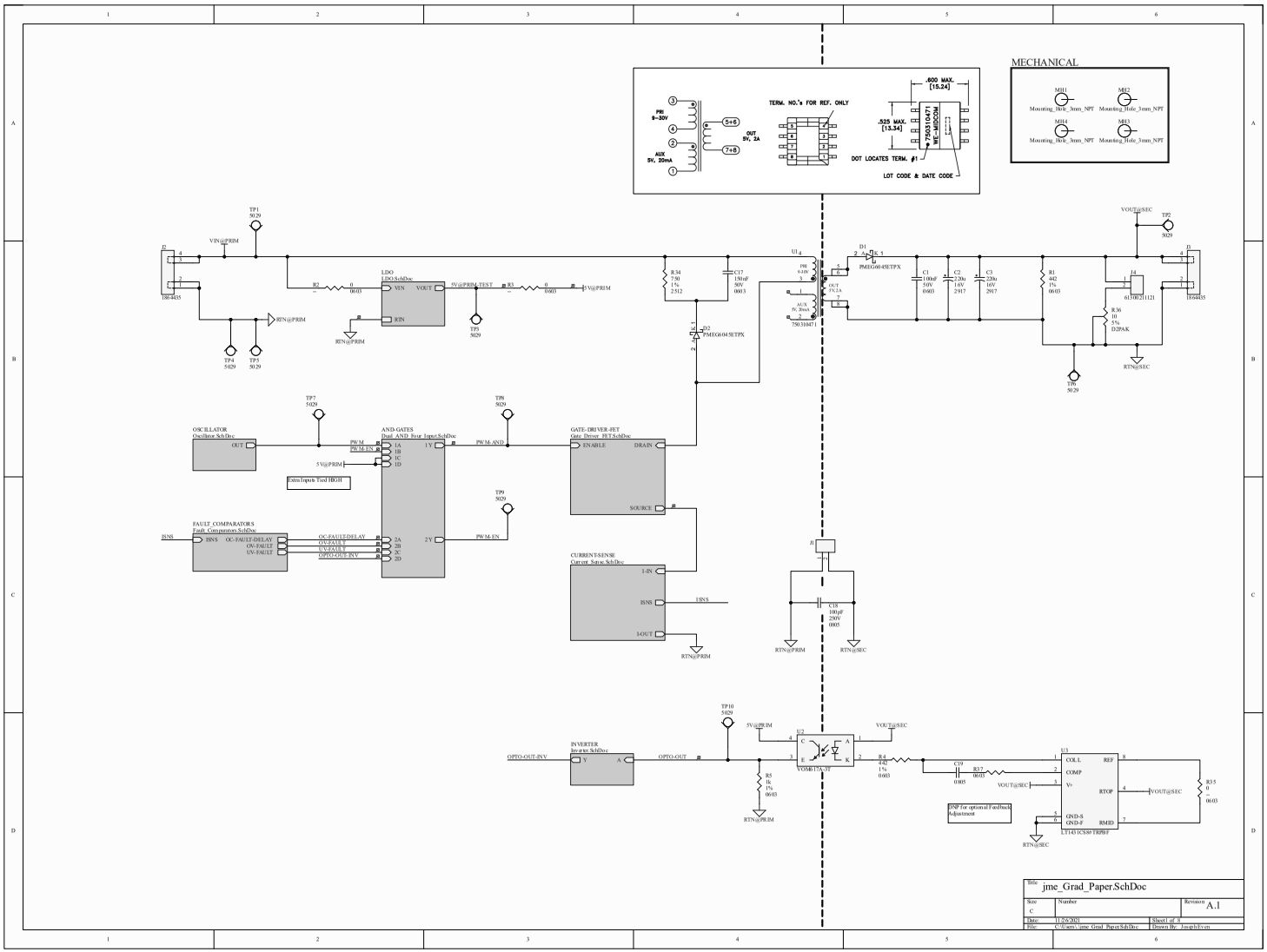
(1) For all available packages, see the orderable addendum at the end of the data sheet.

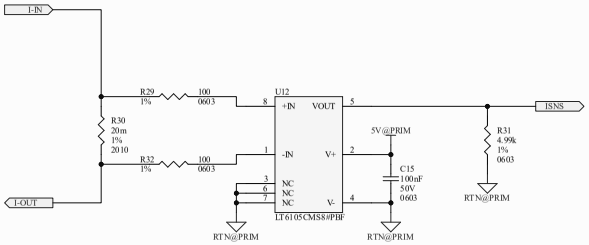
Benefits of Schmitt-trigger Inputs



Appendix III

Altium Schematics


MECHANICAL
MH1 Mounting_Hole_3mm_NPT
MH2 Mounting_Hole_3mm_NPT
MH3 Mounting_Hole_3mm_NPT
MH4 Mounting_Hole_3mm_NPT
PRI 9–30V
AUX 5V, 20mA
5+6
7+8
OUT 5V, 2A
TERM. NO.'s FOR REF. ONLY
.600 MAX. [15.24]
.525 MAX. [13.34]
WE–MIDCOM
7503110471
DOT LOCATES TERM. #1
LOT CODE & DATE CODE
J2
1864435
VIN@PRIM
TP1 5029
TP4 5029
TP5 5029
RTN@PRIM
R2 0 0603
LDO LDO.SchDoc
VIN VOUT
RTN
5V@PRIM_TEST
R3 0 0603
5V@PRIM
TP3 5029
C17 150nF 50V 0603
R34 7.50 1% 2512
U1
PRI 9-30V
OUT 5V,2A
AUX 5V, 20mA
750310471
D2 PMEG6045ETPX
D1 PMEG6045ETPX
C1 100nF 50V 0603
C2 220u 16V 2917
C3 220u 16V 2917
R1 442 1% 0603
VOUT@SEC
TP2 5029
J3
364435
J4
61300211121
R36 10 5% D2PAK
RTN@SEC
TP6 5029
TP7 5029
TP8 5029
TP9 5029
OSC ILLATOR Oscillator.SchDoc
OUT
PWM
PWM_12V
5 V@PRIM
Extra Inputs Tied HIGH
AND-GATES Dual_AND_four_Input.SchDoc
1A 1B 1C 1D 1Y
2A 2B 2C 2D 2Y
PWM-AND
PWM-EN
GATE-DRIVER-FET Gate_Driver_FET.SchDoc
ENABLE
DRAIN
SOURCE
FAULT_COMPARATORS Fault_Comparators.SchDoc
ISNS
OC-FAULT-DELAY
OV-FAULT
UV-FAULT
OPTO-OUT-INV
CURRENT-SENSE Current_Sense.SchDoc
I-IN
ISNS
I-OUT
1SNS
J1
C18 100pF 250V 0805
RTN@PRIM
RTN@SEC
TP10 5029
INVERTER Inverter.SchDoc
OPTO-OUT-INV
OPTO-OUT
U2 VOM617A-3T
R5 1k 1% 0603
R4 4.02 1% 0603
C19 0.005
R37 0603
VOUT@SEC
U3 LT1431CS8#TRPBF
COL-L
COMP
Vr-
GND-S
GND-F
REF
RTOP
RMID
R35 0 0603
DNF for optional Feedback Adjustment
Title jme_Grad_Paper.SchDoc
Size C
Number
Revision A.1
Date: 11/26/2021
Sheet 1 of 8
File: C:\Users\jme_Grad_Paper.SchDoc
Drawn By: JosephEvan



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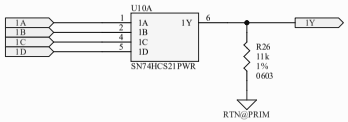

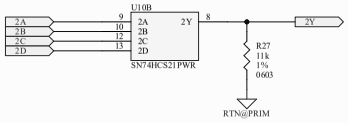

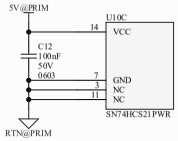

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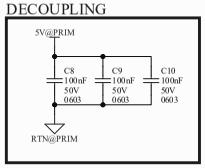
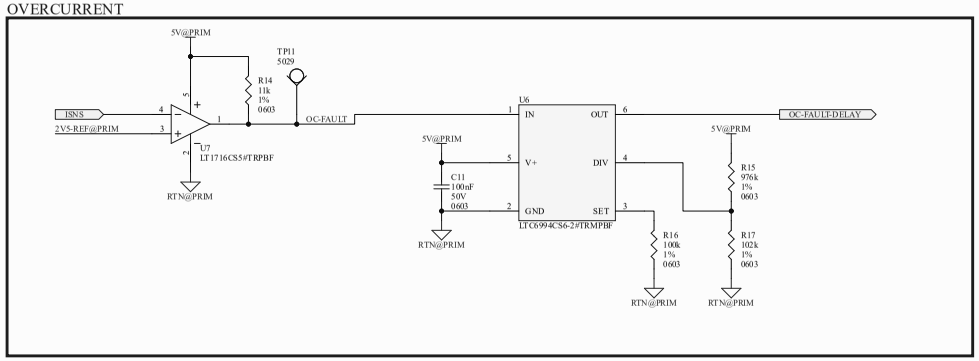
DECOUPLING



OVERCURRENT



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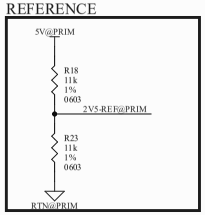
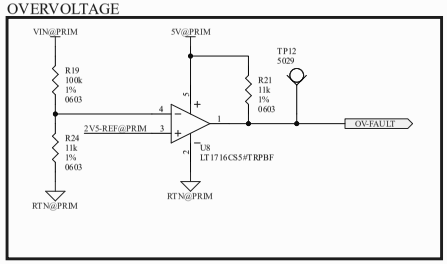


OVERVOLTAGE



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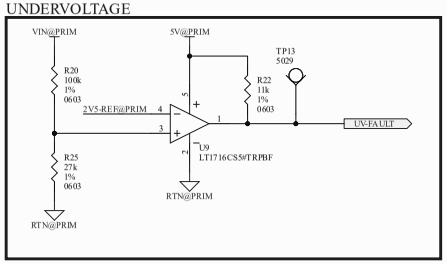

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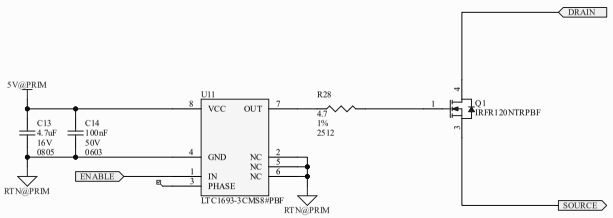

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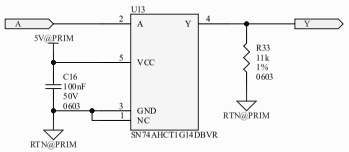

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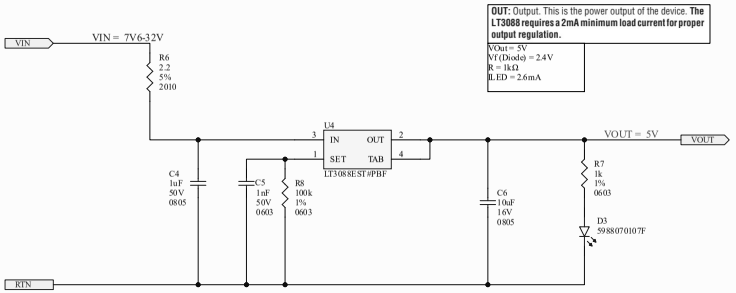

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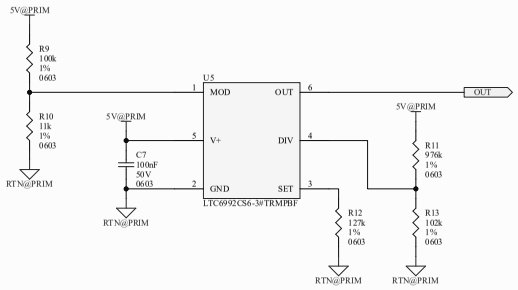

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File: C:\Users\..\Oscillator.SchDoc	Drawn By: Joseph Even		

Appendix IV

Bill of Materials

Comment	Description	Designator	Quantity
GCM188R71H154KA64D	CAP CER 0.15UF 50V X7R 0603	C1	1
GCJ188R71H104KA12D	CAP CER 0.1UF 50V X7R 0603	C2	1
TCJD227M016R0050	CAP TANT POLY 220UF 16V 2917	C3	1
TCJD227M016R0050	CAP TANT POLY 220UF 16V 2917	C4	1
GCJ188R71H104KA12D	CAP CER 0.1UF 50V X7R 0603	C5	1
GCJ188R71H104KA12D	CAP CER 0.1UF 50V X7R 0603	C6	1
GCJ188R71H104KA12D	CAP CER 0.1UF 50V X7R 0603	C7	1
GCJ188R71H104KA12D	CAP CER 0.1UF 50V X7R 0603	C8	1
GCJ188R71H104KA12D	CAP CER 0.1UF 50V X7R 0603	C9	1
GCJ188R71H104KA12D	CAP CER 0.1UF 50V X7R 0603	C10	1
GCM21BR71C475KA73K	CAP CER 4.7UF 16V X7R 0805	C11	1
GCJ188R71H104KA12D	CAP CER 0.1UF 50V X7R 0603	C12	1
GCJ188R71H104KA12D	CAP CER 0.1UF 50V X7R 0603	C13	1
GCM21BR71H105KA03K	CAP CER 1UF 50V X7R 0805	C14	1
GRM1885C1H102JA01D	CAP CER 1000PF 50V C0G/NP0 0603	C15	1
CL21B106KOQNNNG	CAP CER 10UF 16V X7R 0805	C16	1
GCJ188R71H104KA12D	CAP CER 0.1UF 50V X7R 0603	C17	1
GRM21A5C2E101JW01D	CAP CER 100PF 250V C0G/NP0 0805	C18	1
GRM21A5C2E101JW01D	CAP CER 100PF 250V C0G/NP0 0805	C19	1
PMEG6045ETPX	DIODE SCHOTTKY 60V 4.5A SOD128	D1	1
PMEG6045ETPX	DIODE SCHOTTKY 60V 4.5A SOD128	D2	1
5988070107F	LED GREEN CLEAR 0603 SMD	D3	1
61300211121	CONN HEADER VERT 2POS 2.54MM	J1	1
1864435	TERM BLOCK 2POS 45DEG 5MM PCB	J2	1
1864435	TERM BLOCK 2POS 45DEG 5MM PCB	J3	1
61300211121	CONN HEADER VERT 2POS 2.54MM	J4	1
Mounting_Hole_3mm_NPT	3mm Screw, 7.5mm Head, Non-Plated Mounting Hole	MH1	1
Mounting_Hole_3mm_NPT	3mm Screw, 7.5mm Head, Non-Plated Mounting Hole	MH2	1
Mounting_Hole_3mm_NPT	3mm Screw, 7.5mm Head, Non-Plated Mounting Hole	MH3	1
Mounting_Hole_3mm_NPT	3mm Screw, 7.5mm Head, Non-Plated Mounting Hole	MH4	1
IRFR120NTRPBF	N-Channel 100 V 9.4A (Tc) 48W (Tc) Surface Mount D-Pak	Q1	1
RMCF2512JT750R	RES 750 OHM 5% 1W 2512	R1	1
ERJ-3EKF4420V	RES SMD 442 OHM 1% 1/10W 0603	R2	1
ERJ-3GEY0R00V	RES SMD 0 OHM JUMPER 1/10W 0603	R3	1
ERJ-3GEY0R00V	RES SMD 0 OHM JUMPER 1/10W 0603	R4	1
ERJ-3EKF4420V	RES SMD 442 OHM 1% 1/10W 0603	R5	1
ERJ-3EKF1001V	RES SMD 1K OHM 1% 1/10W 0603	R6	1
ERJ-3GEY0R00V	RES SMD 0 OHM JUMPER 1/10W 0603	R7	1
ERJ-3EKF1000V	RES SMD 100 OHM 1% 1/10W 0603	R8	1
PE2010FKE070R02L	20 mOhms ±1% 0.5W, 1/2W Chip Resistor 2010 (5025 Metric) Automotive AEC-Q200, Current Sense, Moisture Resistant Metal Foil	R9	1
ERJ-3EKF4991V	RES SMD 4.99K OHM 1% 1/10W 0603	R10	1
ERJ-3EKF1000V	RES SMD 100 OHM 1% 1/10W 0603	R11	1
ERJ-3EKF1102V	RES SMD 11K OHM 1% 1/10W 0603	R12	1
ERJ-3EKF1102V	RES SMD 11K OHM 1% 1/10W 0603	R13	1
ERJ-3EKF1102V	RES SMD 11K OHM 1% 1/10W 0603	R14	1
ERJ-3EKF9763V	RES SMD 976K OHM 1% 1/10W 0603	R15	1
ERJ-3EKF1003V	RES SMD 100K OHM 1% 1/10W 0603	R16	1
ERJ-3EKF1023V	RES SMD 102K OHM 1% 1/10W 0603	R17	1
ERJ-3EKF1102V	RES SMD 11K OHM 1% 1/10W 0603	R18	1
ERJ-3EKF1003V	RES SMD 100K OHM 1% 1/10W 0603	R19	1
ERJ-3EKF1003V	RES SMD 100K OHM 1% 1/10W 0603	R20	1
ERJ-3EKF1102V	RES SMD 11K OHM 1% 1/10W 0603	R21	1
ERJ-3EKF1102V	RES SMD 11K OHM 1% 1/10W 0603	R22	1
ERJ-3EKF1102V	RES SMD 11K OHM 1% 1/10W 0603	R23	1
ERJ-3EKF1102V	RES SMD 11K OHM 1% 1/10W 0603	R24	1
ERJ-3EKF2702V	RES SMD 27K OHM 1% 1/10W 0603	R25	1
RMCF2512FT4R70	RES 4.7 OHM 1% 1W 2512	R26	1
ERJ-3EKF1102V	RES SMD 11K OHM 1% 1/10W 0603	R27	1
CRM2010-JW-2R2ELF	RES SMD 2.2 OHM 5% 1W 2010	R28	1
ERJ-3EKF1001V	RES SMD 1K OHM 1% 1/10W 0603	R29	1

Comment	Description	Designator	Quantity
ERJ-3EKF1003V	RES SMD 100K OHM 1% 1/10W 0603	R30	1
ERJ-3EKF1003V	RES SMD 100K OHM 1% 1/10W 0603	R31	1
ERJ-3EKF1102V	RES SMD 11K OHM 1% 1/10W 0603	R32	1
ERJ-3EKF9763V	RES SMD 976K OHM 1% 1/10W 0603	R33	1
ERJ-3EKF1273V	RES SMD 127K OHM 1% 1/10W 0603	R34	1
ERJ-3EKF1023V	RES SMD 102K OHM 1% 1/10W 0603	R35	1
PWR263S-35-10R0JE	RES 10 OHM 5% 35W D2PAK	R36	1
ERJ-3EKF4420V	RES SMD 442 OHM 1% 1/10W 0603	R37	1
5029	PC TEST POINT MINIATURE	TP1	1
5029	PC TEST POINT MINIATURE	TP2	1
5029	PC TEST POINT MINIATURE	TP3	1
5029	PC TEST POINT MINIATURE	TP4	1
5029	PC TEST POINT MINIATURE	TP5	1
5029	PC TEST POINT MINIATURE	TP6	1
5029	PC TEST POINT MINIATURE	TP7	1
5029	PC TEST POINT MINIATURE	TP8	1
5029	PC TEST POINT MINIATURE	TP9	1
5029	PC TEST POINT MINIATURE	TP10	1
5029	PC TEST POINT MINIATURE	TP11	1
5029	PC TEST POINT MINIATURE	TP12	1
5029	PC TEST POINT MINIATURE	TP13	1
750310471	TRANS FLYBACK LT3573 25UH SMD	U1	1
VOM617A-3T	OPTOISOLATOR 3.75KV TRANS 4-SOP	U2	1
LT1431CS8#TRPBF	Shunt Voltage Reference IC Adjustable 2.5V 36 VV ±0.4% 100 mA 8-SO	U3	1
LT6105CMS8#PBF	Current Sense Amplifier 1 Circuit - 8-MSOP	U4	1
SN74HCS21PWR	AND Gate IC 2 Channel Schmitt Trigger Input 14-TSSOP	U5	1
LTC6994CS6-2#TRMPBF	Delay Line IC Programmable 8 Tap 1µs ~ 33.6s SOT-23-6 Thin, TSOT-23-6	U6	1
LT1716CS5#TRPBF	Comparator General Purpose Push-Pull, Rail-to-Rail TSOT-23-5	U7	1
LT1716CS5#TRPBF	Comparator General Purpose Push-Pull, Rail-to-Rail TSOT-23-5	U8	1
LT1716CS5#TRPBF	Comparator General Purpose Push-Pull, Rail-to-Rail TSOT-23-5	U9	1
LTC1693-3CMS8#PBF	High-Side or Low-Side Gate Driver IC Inverting, Non-Inverting 8-MSOP	U10	1
SN74AHCT1G14DBVR	Inverter IC 1 Channel Schmitt Trigger SOT-23-5	U11	1
LT3088EST#PBF	IC REG LIN POS ADJ 800MA SOT223	U12	1
LTC6992CS6-3#TRMPBF	Oscillator, Silicon IC 3.81Hz ~ 1MHz TSOT-23-6	U13	1