Monolithic Integration of MEMs Structures and CMOS Circuitry

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Abstract— A modular approach, based on work done at Sandia National Laboratories, for the monolithic integration of a microelectromechanical system (MEMS) process and an electronics process is being investigated. A preliminary outline for an integrated two-level polysilicon MEMS/p-well CMOS process that can be fabricated in RIT's facilities has been created. This is a MEMS-first approach that places the MEMS in an isolation trench and then seals off the MEMS during CMOS processing. A recipe based on potassium hydroxide wet etching has been developed for the isolation trench etch. Masks for a simple test chip have been created to assist in troubleshooting all steps related to building MEMS in a recess trench and in successfully making electrical connections to these structures. Photoresist scumming issues related to the process used to pattern the first level of micromechanical polysilicon need to be addressed before subsequent process steps can be fine-tuned.

I. INTRODUCTION

Building microelectromechanical structures (MEMS) and their associated signal conditioning or driver electronics on the same substrate offers numerous advantages. In the case of transducers that convert mechanical forces to capacitance changes, the importance of maintaining as little distance as possible between the transducer and electronics is paramount to keeping stray capacitances and noise pickup from significantly degrading circuit performance. This paper documents the first efforts made toward bringing a modular MEMS-electronics process integration approach, similar to that developed at Sandia National Laboratories,[1,2] to the Rochester Institute of Technology.

The major advantage of pursuing a modular integration strategy is that other electronics technologies could be substituted in place of CMOS without affecting the MEMS process. Similarly, the MEMS process could be modified, within certain constraints, namely that the micromechanical structures do not exceed the trench height and that no bulk micromachining is required, without impacting the electronics process. A great need exists, at RIT, for such combined MEMS-electronics processes because testing of student-designed micromachines has historically been nearly impossible due to electrical connection issues. Furthermore, the availability of PMOS, CMOS, and bipolar processes at RIT would allow the MEMS designer a great deal of flexibility because a technology could be selected that easily presents appropriate impedances to MEMS sensors or driving voltages and currents to MEMS actuators.

Several important processing challenges are encountered when attempting to integrate MEMS with electronics. The first of these is that MEMS require high temperature processing, on the order of 1000°C in order to dope the and relieve mechanical stresses in the micromechanical polysilicon layers. Exposure to such high temperature processing would prove detrimental to metal interconnects and cause unwanted diffusion of dopants in transistors and other electronic structures. The second obstacle is that MEMS introduce rough topography, which conventional thin photoresist processes cannot cover adequately. Finally, many MEMS structures, especially those employing hinges, are fragile once they have been released. The integration strategy investigated in this project addresses all three of these issues. The first issue, that of high temperature processing, is addressed by building the MEMS first. The second and third issues, surface topography and risk of mechanical

damage to micromechanical structures, are addressed by building the MEMS in a recess trench, filling the trench with low temperature oxide, planarizing the surface through chemical mechanical polishing (CMP), and sealing off the MEMS area with a silicon nitride membrane. The fragile MEMS are not released until all processing is complete.

Figure 1 shows the recess trench. It has a depth of 6μm and is produced by an anisotropic etchant, such as potassium hydroxide (KOH).

Figure 1: MEMS recess trench.

Figure 2 shows the first of two micromechanical polysilicon layers used in the MEMS process attempted in this paper. This layer, shown after patterning, has a thickness of 5000Å. Underlying films are silicon nitride (1500Å) and thermal oxide (500Å).

Figure2: First micromechanical polysilicon in recess trench.

Figure 3 shows the completed MEMS structures in the recess trench. First and second level polysilicon can be seen , along with CVD oxide between the two polysilicon levels and around the MEMS structures.

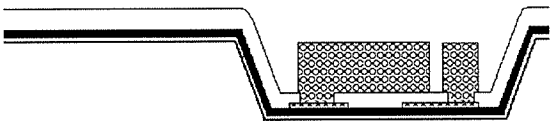

Figure 3: Complete MEMS structures in recess trench.

At this stage, the MEMS are ready to be sealed off to prepare the wafer for electronics processing. The trench is filled with CVD oxide, and the wafer is CMP planarized to yield the cross-section shown in figure 4.

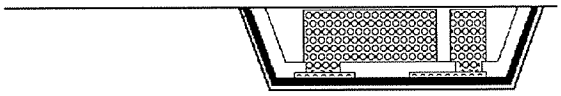

Figure 4: MEMS in oxide-filled trench after chemical-mechanical polish.

After planarization, a 500Å thermal oxide is grown, and a 1500Å layer of silicon nitride is deposited. The function of this silicon nitride layer is to isolate the MEMS area during electronics processing. Therefore, the areas of the substrate in which electronic structures are to be built need to have the nitride membrane stripped away. This can be accomplished by patterning the membrane with a negative, biased version of the trench mask to yield the cross section shown in figure 5.

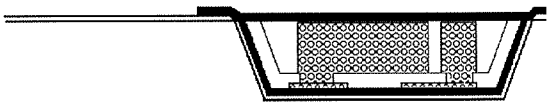

Figure 5: MEMS isolation trench with completed MEMS, CVD oxide, and silicon nitride seal.

The electronics process (a LOCOS isolated MOS process is shown) is run through all steps prior to the zeroth interlevel dielectric and first metallization. The silicon nitride MEMS seal is stripped away to yield the cross-section shown in

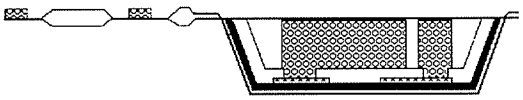

figure 6.

Figure 6: MEMS and MOS structures ready for interconnects.

The next steps are zeroth interlevel deposition, contact cuts, and metallization. When all the interconnect levels have been deposited and patterned, the MEMS are ready to be released. Release is accomplished by placing the substrate in hydrofluoric acid to etch away the low temperature oxide surrounding the micromechanical structures. The aluminum metallization needs to be protected during this etch, however; this can be accomplished by covering the metallization with photoresist. If all contacts to the MEMS are made at the

periphery of the trench, then the mask used to protect the metallization can be generated by biasing the trench mask. Figure 7 shows this protective photoresist layer in place.

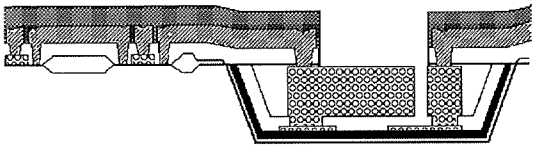

Figure 7: Cross-section after MEMS release. Note that metallization is covered with photoresist to avoid exposure to hydrofluoric acid.

The final device cross-section is shown in figure 8.

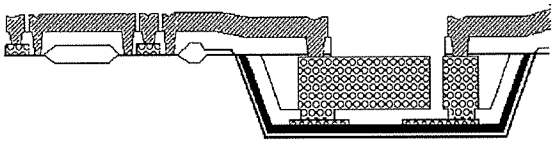

Figure 8: Final MEMS-CMOS cross-section.

II. EXPERIMENTAL PROCEDURES

KOH was chosen as the silicon etch process because KOH yields a 53° sidewall profile. This angled profile was expected to be less problematic during subsequent MEMS photolithography steps than a profile with very steep sidewalls or a profile with undercutting.

Past experiments with KOH etches at RIT had involved either etching through silicon to nitride membranes, etching holes through silicon substrates, or etching V-grooves in silicon. In these past endeavors, close control over surface smoothness and etch rate was not an issue. The first step in the research was to find an etchant mix and solution temperature that would yield the 6μm trench depth with minimum surface roughness in a reasonable amount of time. Previous experiments performed by students in RIT's facilities had investigated the etch rates of 10% and 20% solutions (measured by percent mass of KOH) of potassium hydroxide, along with the effects of incorporating isopropanol into the solution[3]. This research had shown that adding isopropanol to a KOH etchant solution significantly slows down the etch rate, but that slower etch rates usually result in smoother surfaces. A 20% KOH solution at 75°C had an etch rate of 62μm/hr, but replacing the de-ionized water in this solution with a 50-50 mix of isopropanol and de-ionized water dropped the etch rate to 20μm/hr. Other research at RIT had shown that a 10%KOH solution etched silicon at a rate of 16μm/hr when heated to 50°C[4]. The etch rate on silicon dioxide had been shown to be much lower, although not as low as that of silicon nitride.

The first experimental run was attempted by patterning Shipley 812 photoresist on a wafer, using an exposure test mask, and etching in a 10% KOH solution at 50°C. The etch apparatus for all experiments was a covered Petri dish over a hotplate, and all step heights were measured using a Tencor Alpha-Step surface profilometer. Etch time was expected to be on the order of 22 minutes. The KOH, however, immediately attacked the photoresist. The next attempt was made by patterning a 500Å dry thermal oxide in hydrofluoric acid and using this layer as an etch mask. This thin oxide successfully masked the etch and was used in all subsequent experiments.

Etching was attempted with a 20% solution of KOH in deionized water at 72°C. An etch time of 7 minutes and 15 seconds was expected to yield the required trench depth. Etching for this length of time, however, only produced 1μm of topography. Further observation of the process showed that 27 minutes of etch time achieved the 6μm trench depth, but that the depth-etch time relationship is non-linear. The surfaces of these trenches were fairly rough, however, and the etch uniformity across the wafer seemed poor.

An SF_6/O_2 plasma etch process was considered, but the idea was abandoned because photoresist liftoff occurred during development. The photoresist process used consisted of a 250°C dehydration bake, an HMDS prime, followed by an OCG ASPR-528 photoresist spin coat at 4500RPM for 30 seconds. Prebake was at 90°C for 45 seconds.

Future experimental endeavors were directed toward the use of a 10%KOH solution diluted in a 50-50mix of isopropanol and de-ionized water. This solution yielded a visibly smoother surface, although the etch rate was slower. One hour and 20 minutes were required to produce a 6μm step height. Consistency over the wafer was found to be very good, so further

processing was performed to observe surface roughness once subsequent layers of thermal oxide and silicon nitride were present. The resultant profiles showed about 0.25μm of surface roughness, with the exception of a few areas that had more roughness and some particles of unknown identity. CVD polysilicon was deposited, and step height was measured at 5.2μm.

A 5000Å sacrificial oxide growth and strip was attempted on some wafers that showed severe pitting of the etched surfaces. Although the pitting visibly decreased, it did not vanish completely.

A simple test chip, shown in figure 9, was designed for use in process development and to demonstrate functionality of the process. The chip consisted of a dual cantilever parallel plate electrostatic actuator, a resistor, a polysilicon 1-polysilicon 2 contact chain, and a polysilicon 1 serpentine. A stepper job, [10,1]TORREJON1, was created for the GCA 6700 stepper. This job was designed to accept a pass number, which selects one of the four levels found on each of the masks.

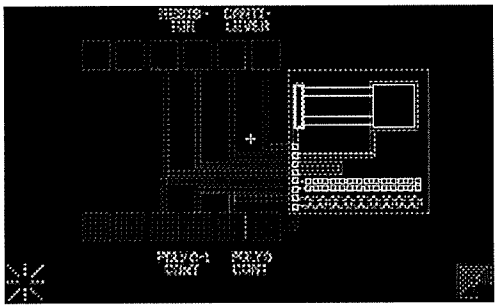

Figure 9: Test chip layout.

Device wafers were run using the new mask set. A 500Å dry thermal oxide was grown on the wafers. Photolithography was performed using the standard Shipley 812 photoresist process available on RIT's GCA Wafer Trac. Exposure was done on the GCA 6700 stepper using an exposure of 0.6 seconds (integrated) and a focus of 265. Patterning was accomplished through a 45 second dip in buffered HF. The trench etch was done with 10%KOH diluted in 50-50 isopropanol and deionized water for a duration of 1 hour and 20 minutes at a temperature of 50°C. After trench etch, the remaining thermal oxide was stripped in a 1 minute HF dip, and a new 500Å thermal oxide layer was grown. 1500Å of CVD silicon nitride were deposited over the oxide. 5000Å CVD polysilicon were then deposited over the silicon nitride. Doping of the polysilicon was accomplished by spin coating Emulsitone N-250 emitter solution at 3000 RPM for 30 seconds. Wafers were oven baked at 200°C for 15 minutes to drive away solvents. Diffusion of dopants into the polysilicon was accomplished by a 15 minute soak in a nitrogen ambient at 1000°C. A 2 minute HF dip was then performed, and 4-point probe sheet resistance measurements were taken. Imaging in the trench was done with OCG ASPR-528 thick positive photoresist. Dehydration baking was done at 250°C for 2 minutes or more. HMDS prime and subsequent photoresist spin coating was accomplished by a two-step process that gently ramped the spin speed to 250 RPM and after 15 seconds ramped up to 3500 RPM and ran at this speed for 45 seconds. This two step process does most of the spreading during the low speed cycle, while the high speed cycle establishes the coating thickness. The pre-exposure softbake was performed at 115°C for one minute. Exposure was done on the GCA 6700 stepper with an exposure time of 1 second (integrated) and a focus setting of 350. Developing was done by hand in straight Shipley MF321 developer, and hardbaking was done at 145°C for two minutes. Polysilicon patterning was done in the GEC Plasma Cell single wafer plasma chamber. The plasma was sulfur hexafluoride (SF_6) and oxygen (O_2) with the gas flows set at 42.5 sccm and 7.5 sccm, respectively. Chamber pressure was regulated at 400 mT, and 40 watts of RF were delivered to the electrodes. Etch time was one minute and 10 seconds. 2.0μm of CVD oxide were then deposited. No further processing was performed after this step due to time constraints and observation of excess polysilicon around the periphery of most of the MEMS recess trenches.

III. RESULTS AND DISCUSSION

Designing the recess trench etch process was found to involve a tradeoff between surface smoothness and the time required to complete the process. A 10% weight solution of potassium hydroxide pellets diluted in a 50-50 mix of deionized water and isopropanol, heated to 50°C was found to yield the required 6μm trench depth in 1 hour and 20 minutes. The

etch rate appeared to increase during the course of the etch, but the cause of this phenomenon is not known. 500Å of dry thermal oxide were effective in serving as an etch mask for this process. In order to produce usable trenches of consistent depth, however, care must be taken to minimize the amount of isopropanol lost to evaporation. Because of the long duration of this process, investigation into new etch apparatus that allows multiple wafer processing while minimizing the amount of solution lost to evaporation may be worthwhile. The usefulness of sacrificial oxides in improving surface smoothness also needs further investigation. While sacrificial oxides did not eliminate roughness from severely pitted surfaces, their effects on surfaces with moderate roughness were not studied.

An oxygen/sulfur hexafluoride plasma was successfully used to etch polycrystalline silicon. The gas flow rates were 7.5sccm and 42.5sccm, respectively. Pressure was 400mTorr, and RF power to the chamber was 40 watts. 5000Å of polysilicon were etched in 1 minute and 10 seconds with this process.

The photolithographic process used to image features in the MEMS recess trench needs further development to minimize photoresist scumming along the edges of the recess trench. The current process uses OCG ASPR-528 positive photoresist to cover the rough topography associated with the recess trench. While this process successfully covers the areas around the MEMS recess trenches, too much photoresist is deposited at the trench edges, leading to photoresist scumming and excess polysilicon, as shown in figure 10.

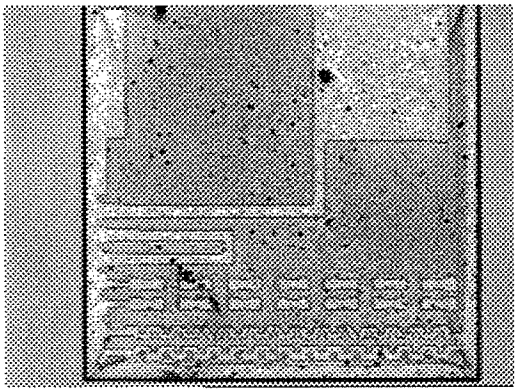

Figure 10: Excess polysilicon around recess trench edges.

The etch rate of the sulfur hexafluoride/oxygen plasma on photoresist is about one fourth of that on polysilicon, so the full 3.3μm of photoresist available from the spin coat process used are not required. The spin coat process could be modified by adding a third cycle with a speed of 5500RPM and a duration of 45 seconds. This would take the relatively smooth resist coat produced in the first and second steps and make it thinner. A more tightly controlled development process could be utilized, and the develop time could be extended until all resist clears from the isolation trench edges. Since the first polysilicon layer is the thinnest patterned layer in the MEMS recess trench, it is the most critical insofar as resist scumming is concerned. Subsequent layers would usually be much thicker (typically on the order of 2.0μm), so slight amounts of resist scumming could be tolerated because the excess resist would be consumed early on in the etch process. If the photolithographic process can be perfected for this first level of polysilicon, then that process should be usable on all lithography done in the recess trench.

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