SIMOX CMOS Process Design and Fabrication

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Abstract - The first Thin Film Transistor (TFT) CMOS process for RIT's Semiconductor Processing Center utilizing SIMOX wafers was developed. A standard 9 mask-set P-well CMOS process flow originally designed for bulk silicon was modified to accommodate the new starting material.

I. INTRODUCTION

Various techniques have been introduced to silicon MOSFET processing to improve the intrinsic problems with bulk silicon devices. One method that is gaining popularity is Silicon-on-Insulator (SOI). Of this genre, two viable processes show promising results[1], SIMOX (Separation by Implanted Oxygen) and Bonded and Etched-Back (B-E). Advantages of using these SOI substrates over bulk silicon are process simplification, improved performance and tighter packing densities.

Development began with modification of the RIT P-well, Rev 3 process. Changes made are as follows:

1. Using first level mask with well removed solved alignment issue.
2. P- thin film silicon processing was substituted for diffused well.
3. Isolation process involved RIE etch of standard field region to define active mesas.
4. Redesign of the implant, diffusion, poly, and gate oxide processes for integration with thin silicon layer.
5. Application of current contact and Al metal process.
6. Standard RIT transistor, Van der Pauw, and test procedures.

II. PROCESS DESIGN

Previous work done at RIT on SOI substrates[2] as well as thin film polysilicon device design provided the necessary starting points for the TFT design. Polysilicon RIE etches were used to etch the top silicon layer during alignment and "mesa" steps. Conditions were 75 watts RF power at a pressure of 75 mT, SF_6/O_2 flow rates of 30:5 sccm. Alignment mask was modified to remove the well openings and expose just the alignment verniers and the stepper alignment cross. Resist strip was performed in O_2 plasma for 20 min at 300W/1torr or in case of misalignment of the stepper, an acetone strip was used to clean the resist and the wafer was coated and exposed again.

Gate oxide was done using a standard 50nm recipe of dry O2 at 1000C with nitrogen flowing during the ramp cycle. Wafers were pushed in at 800C. Polysilicon deposition using CVD and spin-on-glass diffusion doping was used for the gate electrode. The same RIE as for the alignment level was used to etch the poly. Source and drain implants were done through the exposed gate oxide. Energy was chosen based on placing the projected range 100nm into the thin film silicon. The implant dose was $1x10^{15}$ atoms/cm^3 with the energy being 135 KeV and 60 KeV for the P+ and N+ respectively.

Step	Operation	Details	Completed
1	ID01 SCRIBE	Scribe wafer ID's	X
2	DE01 4PT PROBE	Initial electrical measurements	X
3	CL01 RCA CLEAN	Surface particle clean	X
4	PH03 PHOTOLITH	Alignment Photo with modified mask	X
5	ET06	Si RIE down to underlying oxide	X
6	ET05	Quick HF Dip to etch 1000A of SiO2	X
7	ET07 STRIP	Ash resist	X
8	PH03 PHOTOLITH	Active area Photo	X
9	ET06 SI ETCH	Si RIE down to underlying oxide	X
10	ET07 STRIP	Ash resist	X
11	CL01 RCA CLEAN		X
12	OX06 DRY OXIDE	Gate oxide Growth 500A	X
13	CV01 CVD POLY	Poly Gate Deposit 6000A	X
14	DI04 N-DIFFUSION	N+ Poly Doping	X
15	ET06 OXIDE ETCH		X
16	DE01 4PT PROBE		X
17	PH03 PHOTOLITH	Poly Photo	X
18	ET08 POLY ETCH	Polysilicon Etch	X
19	ET07 STRIP		X
20	PH03 PHOTOLITH	P+ D/S Photo	X
21	IM01 IMPLANT	P+ D/S Implant 135KeV BF_2	X
22	ET07 STRIP		X
23	PH03 PHOTOLITH	N+ D/S Photo	X
24	IM01 IMPLANT	N+ D/S Implant 60KeV ^{31}P	X
25	ET07 STRIP		X
26	CL01 RCA CLEAN		X
27	OX08 ANNEAL	S/D Anneal	X
28	CV03 CVD LTO	LTO Deposition 3000A	X
29	PH03 PHOTOLITH	Contact Cuts Photo	X
30	ET06 OXIDE ETCH	Contact Cuts Etch	X
31	ET07 STRIP		X
32	DE01 4PT PROBE		X
33	CL01 RCA CLEAN		X
34	ME01 AL DEPOSIT	Aluminum Deposit	X
35	PH03 PHOTOLITH	Metal Photo	X
36	ET05 AL ETCH		X
37	ET07 STRIP		X
38	SI01 SINTER	Sinter Aluminium 450C 30 min	X

Table 1: Full process flow for RIT SIMOX CMOS

LTO deposition was performed at 400C using silane and oxygen. Wafer to wafer variation was very high, as much as 50nm due to the fact that a 3" tube was being used for 4" wafers. Al/Cu/Si was sputter deposited and sintered with H_2/N_2 forming gas

III. DEVICE FABRICATION

Fabrication began with the as received wafers. Starting material for these devices was a 365nm buried oxide layer with 200nm of silicon on top. Alignment and isolation RIE steps define the alignment key and active device. A 50nm gate oxide and 600nm N+ poly electrode form the gate of both transistors. Low energy D/S implants result in placement of the implant peak

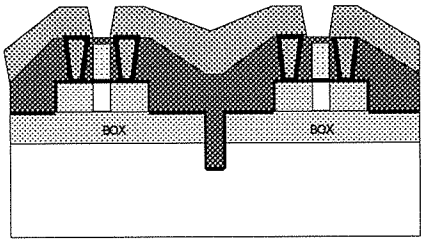

Figure 1: Cross section of RIT SIMOX CMOS design

100nm into the silicon. Subsequent diffusion spreads the dopant distribution and activates the implanted species. 600nm of LTO was patterned for contact and Al/Cu/Si was sputter deposited. Final step is to sinter the Al/Si interface at 450C for improved contact resistance.

IV. RESULTS/CONCLUSIONS

The transistor tests performed on the final device wafers exhibited no field effect from the gate. Investigation further revealed that the source, drain and gate were all shorted together. The best explanation for this is an incomplete gate electrode etch. Figure 2 shows the polysilicon shunt that resulted from this processing error. Care was taken during etch. After RIE, the wafers were inspected and determined to have cleared to the underlying gate oxide. Due to the nature of the SOI structure, color banding from the previous RIE etched made human optical endpoint detection inaccurate.

The formation of this polysilicon shunt would function as a resistor from source to drain. The measured current as a function of the drain voltage increases as shown in Figure 3. All transistors exhibited this behavior, regardless of the L/W ratio. NMOS and pMOS devices from 6/32 to 32/32 were tested and revealed the same trend.

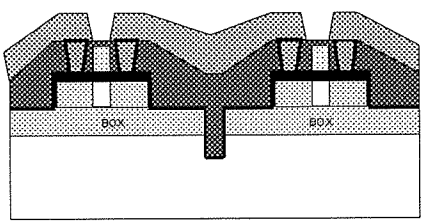

Figure 2: Cross section showing the polysilicon shunt that resulted in incompleter etch

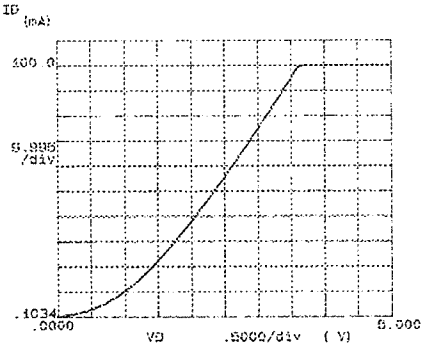

Figure 3: Transistor plot for n-MOSFET device showing "nil" effect of gate electrode.

V. RECOMMENDATIONS

Almost certainly, this process must be run again. Attention to detail is very important in all areas, but several warrant special attention. One of those is the plasma etch processes. Endpoint detection and/or etch rate monitors with identical stacks to the device wafers will eliminate any possible etch problems. This includes the initial single crystal silicon etches as well as the polysilicon etch. A complete optimization of the RIE etch process is not unwarranted.

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REFERENCES

[1] Colinge, Jean-Pierre, "Silicon-on-Insulator Technology: Materials to VLSI," Kluwer Academic Publishers, Boston, 1991

[2] Dinse, Brian, "Silicon-on-Insulator MOSFETS," RIT Department of Electrical Engineering, MSEE