Design and Fabrication of A Field Programmable Logic Array

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Abstract- Unlike conventional hard programmed gate arrays, the Field Programmable Logic Array (FLPA) offers the end user the ability to instantly change the outputted function of the circuit through an external electronic programming sequence. This project outlines the design and fabrication of a P-Well CMOS NOR logic FPLA. Consisting of roughly 1,400 transistors, three major functional components were designed: Floating Tunnel Oxide EEPROM memory bank, an EEPROM addressing system, and a 3 input / 3 output / 2 return state programmable logic array. Fabrication was carried out at the RIT fabrication facility and upon testing the completed devices it was found that the NMOS devices were too leaky for proper circuit operation. This was due to a partially blocked channel stop implant.

I. DESIGN

The logic array consists of two array planes which each carry out specific logic through the implementation of NOR logic. The NOR function can be achieved by

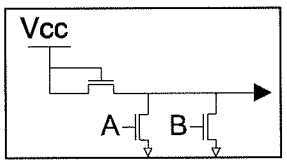

Figure 1: NMOS Implementation of NOR Logic

using NMOS transistors to pull down the output when any of the input signals are high (figure 1). The two planes used to produce combinational logic are the AND plane and the OR plane. To achieve the AND function using NOR logic, the inputs need to be inverted, while the OR function can be attained by simply inverting the output of the NOR function. By placing the two arrays so that the output of the AND plane is the input to the OR plane, combinational logic such as AB + CD can be realized. Another feature of this design is the addition of synchronized buffers at the input and output of the FPLA. Finite state machines such as parity detectors may be created by feeding the synchronized output of the FPLA back to the input buffer of the FPLA (see chart 1 for simulation results of combinational logic and finite state machine).

To make the logic array programmable, there must be a method for controlling which input signals are used in each row/column of the NOR array. By placing another controlling NMOS transistor (T1) in series with the "A" transistor, between it and the ground connection, the "A" transistor will not pull down the output until the T1 transistor is turned on (figure 2). In this design, the Floating-Gate Tunneling Oxide (FLOTOX) EEPROM is utilized to retain the programmed states of the controlling transistors. The FLOTOX EEPROM is a double polysilicon gated structure where the top polysilicon gate acts as the control and the lower poly gate is floating (see figure 3). The EEPROM is programmed by transferring electrons between the floating poly (poly 1) and the underlying N+ drain through the tunnel oxide. This process is known as Fowler-Nordheim Tunneling. When an abundance of electrons have been pushed onto the floating poly, the nominal +5V applied to the control gate (poly 2) is not great enough to turn on the underlying channel. Conversely, when the electrons have been removed from the floating poly, the Vt of the underlying transistor is artificially lowered so the channel will invert when +5V is applied at the control gate. This property allows for the NOR array row/column control lines to be controlled in a programmable manner.

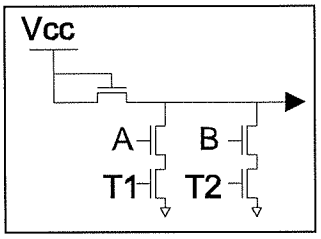

Figure 2: Programmable NOR Row

The final element of the design of the FPLA was a 64 bit MUX. This was included to provide a programming address system. This greatly simplifies the programming of the FPLA by reducing the number of input pins required to program the EEPROMs from 64 to just 6. Due to the testing limitation of the RIT prober cards, which only have

12 pins, a MUX over-ride pin was added to the FPLA I/O pad to facilitate the reading of the entire bank of EEPROM memory cells during normal operation with just 1 pin.

II. FABRICATION

The devices were fabricated at the RIT microelectronic fabrication facilities. During fabrication of the devices, two separate chips were made on the same wafers. The first was the designed FPLA chip and the second was the standard RIT P-Well CMOS test chip. This allowed for end-of-line testing of not only the FPLA chip, but a throughout method for testing the fundamental transistor characteristics. In the case of misprocessing, this method allows the engineer to ascertain the root cause and invalidate non-functional FPLA results.

The fabrication process used to construct the FLOTOX EEPROM device (figure 3) varies from the

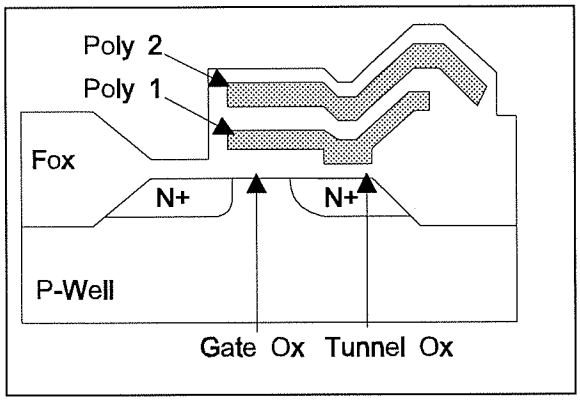

Figure 3: FLOTOX EEPROM Device

nominal RIT P-Well CMOS process in 3 major ways. First, a separate N+ drain implant must be performed since the N+ drain is under Poly 1 which normally blocks the N+ implant. Second, a 100A tunnel oxide must be grown above the N+ drain mentioned previously to facilitate the programming of the floating poly gate. Finally, a second layer of polysilicon must be deposited and patterned to form the control gates.

III. TESTING/OPERATION

Testing of the completed circuits begins with a comprehensive analysis of the quality of the transistors. This is performed using the standard procedure for testing the RIT test chip. There are also several test structures on the device chip to be used to ascertain the functionality of the EEPROM devices as well as some subcircuit blocks. The first test structure is located in the middle of the chip on the right hand side. Here there are 12 pads which facilitate the testing of two devices. First on the left is a simple 2:1 MUX which simulates the operation of the 64 bit addressing MUX. On the right is a simple positive-edge D-Latch which can be used to test the synchronous I/O features of the FPLA. The 12 pads to the left of these two devices houses two EEPROM cells which can be tested to characterize the quality of the EEPROM devices. OUT1 and OUT2 are direct connections to the EEPROM while OUT3 and OUT4 are inverted outputs of the OUT1 and OUT2 lines to simulate the actual output of the EEPROM devices to the PLA. The third test device is above the three aforementioned testing structures and is a hard-wired PLA. This circuit is a designed finite state machine to detect 4 consecutive 1s at the input (as in chart 1). This structure will allow for the array to be tested independent of the memory control.

Operating the FPLA is done in two separate stages: programming and operation. The programming sequence is carried out by connecting the 12 prober pins to the upper-left probe pad. The programming sequence is two basic suboperations. First, the EEPROM devices must be precharged to effectively turn all the programmed states of the array "Off". This is done by setting all the select lines to +15V and then setting the bit line to GND and the control line to +15V. Next, each EEPROM should be selected to activate a specific site on the array to be "On". Set the select lines as determined by chart 2 to specify the EEPROM cell and then set the bit line to +15V and the control line to GND. The final step is the operation of the FPLA. To perform this step move the 12 probe pins down to the 12 probe pads in the bottom center of the chip. Set GND to 0V, Vss to +5V, and READ to +5V which will activate all the EEPROM devices. Next establish a clock signal on the CLK pin and monitor the inputs and outputs of the chip.

IV. RESULTS AND DISCUSSION

The FPLA was not testable due to a misprocessing of the devices. During the testing of the basic transistor characteristics it was noted that there was an abnormally high leakage current at Vgs = 0V. Upon testing the devices at Vgs = -20V, the 16/32um device still exhibited a leakage current of 7uA. This suggests a leakage path which is not at the surface of the channel. This is consistent with a known error in the fabrication of the devices. During the channel stop lithography it was a noticed that the mask was incorrect. To circumvent this problem a dual resist process was attempted which would manually or the

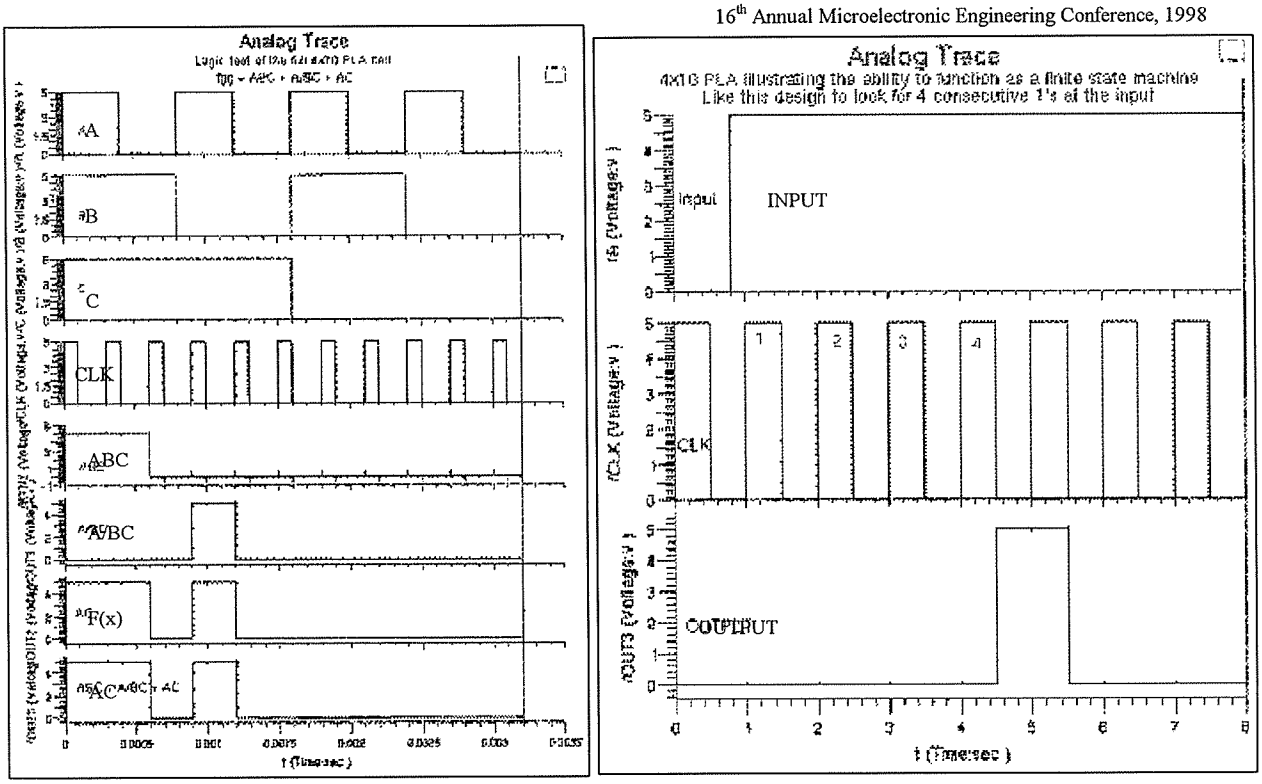

Chart 2: Accusim Simulation Results of FPLA: a) Testing combinational Logic F(x)=ABC+A/BC, b) Testing Finite State Machine to detect 4 consecutive 1's.

And Plane Select Assignments

Row	Input	Select
1	/A	000100
1	A	001000
1	/B	001100
1	B	010000
1	/C	010100
1	C	011000
1	/RTN1	011100
1	RTN1	100000
1	/RTN2	100100
1	RTN2	101000
2	/A	000101
2	A	001001
2	/B	001101
2	B	010001
2	/C	010101
2	C	011001
2	/RTN1	011101
2	RTN1	100001
2	/RTN2	100101
2	RTN2	101001
3	/A	000110
3	A	001010
3	/B	001110
3	B	010010
3	/C	010110
3	C	011010
3	/RTN1	011110
3	RTN1	100010
3	/RTN2	100110
3	RTN2	101010
4	/A	000111
4	A	001011
4	/B	001111
4	B	010011
4	/C	010111
4	C	011011
4	/RTN1	011111
4	RTN1	100011
4	/RTN2	100111
4	RTN2	101011

Special Select Assignment

Select	Function
000000	Idle Prog State
000010	None
000011	None
111111	Select all output pins

OR Plane Select Assignments

Input AND Row	Output	Select
1	RTN1	101100
1	RTN2	110000
1	OUT1	110100
1	OUT2	111000
1	OUT3	111100
2	RTN1	101101
2	RTN2	110001
2	OUT1	110101
2	OUT2	111001
2	OUT3	111101
3	RTN1	101110
3	RTN2	110010
3	OUT1	110110
3	OUT2	111010
3	OUT3	111110
4	RTN1	101111
4	RTN2	110011
4	OUT1	110111
4	OUT2	111011
4	OUT3	000001

Chart 1: Addressing Select Assignments

inverse well with the active layer. Upon completion of the lithographic step it was noted that there was still residual photoresist in the areas which should have been cleared for the ensuing channel stop implant. After multiple attempts to rectify the situation the wafers were sent on to be implanted. This resulted in a partially blocked channel stop implant. The lack of a channel stop implant allows for a leakage path to be established along the edges of the transistors where the field oxide defines the edge of the device due to the positive fixed charge in the field oxide.

V. CONCLUSIONS

The design of the FPLA was illustrated to be successful through the use of Accusim simulation as seen in chart 1. The partially blocked channel stop implant resulted in abnormally high leakage current in the NMOS devices which made it futile to test the FPLA for functionality. It is my recommendation that the devices be fabricated again at the RIT facility with the following three improvements:

1. Regenerate the channel stop reticle,
2. Regenerate the contact reticle with a +1um bias,
3. Use a Bottom anti-Reflective Coating to perform the metal 1 lithography to reduce line variations.

With these three improvements to the process a successful testing of the FPLA in actual silicon can be realized.

ACKNOWLEDGEMENTS

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