Twin-Well CMOS Integration

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Abstract - A self-aligned twin-well process has been developed for RIT's Student CMOS Factory. These wells are self-aligned providing increased packing density; which, will allow for increased speed and reduction in defectively levels. In addition the twin-well process offers: decreased Early effect, increased punchthrough voltage and, reduced latch-up susceptibility, for those devices normally manufactured in substrate. Standard RIT Student Factory CMOS implements a p-well process. Four micron by 32 micron p-channel devices were tested to determine process performance. Early voltage was increased from 9.4V for p-well, to 38.8V for twin-well CMOS. Punchthrough voltage was increased in magnitude from 8V for p-well to 12V for twin-well. Saturation current at 5V Vds and 2.5V above Vt dropped in magnitude from 151μA/μm for p-well to 81μA/μm for twin-well.

I. INTRODUCTION

As device geometries shrink the requirements for device performance become more and more strict. As devices are reduced in size drain-source punchthrough becomes an issue. In addition Early effects become more noticeable as well as latch-up related issues. The need for a process that will elleviate these problems while maintaining device performance and process simplicity becomes necessary.

In a typical p-well CMOS process, such is used in RIT's student factory, a p-type well is created in an n-type substrate. The p-well is optimized for n-channel device performance; however, p-channel devices are manufactured in substrate where the bulk doping level is fixed and unchangeable. Consequently, in p-well CMOS, p-channel devices are more susceptible to punchthrough and other degrading effects, and, these effects become more pronounced as device sizes are shrunk.

To reduce punchthrough several techniques may be implemented including: punchthrough implant, HALO implant or, raising the doping level. All these solutions work by reducing the propensity of the drain to make contact with the source under high electric fields. Early effect is inversely related to doping level and can therefore be reduced by increasing the doping level. Latch-up, caused by the regenerating switching in a p-n-p-n path by parasitic p-n-p and n-p-n bipolar devices, can be reduced through the use of: guardband structures around devices to reduce lateral resistances, epitaxial layers on low-resistivity substrates to minimize parasitic resistances or, increased doping which reduces the parasitic resistances and beta[i].

Most of the approaches just described require complex process's and, not all solve the problems of punchthrough, Early effect and, latch-up susceptibility, except one, increased doping level. In p-well CMOS the well is at a high doping, which, reduces punchthrough, Early effect and, latch-up for n-channel devices. To reduce these degrading effects for the p-channel devices the substrate doping must be raised; however, arbitrarily raising the well doping would have an adverse effect for the n-channel devices. A better solution would be to use a twin-well approach where the substrate is selectively doped higher, in addition to the standard well formation. This approach allows the ability to optimize both n- and p-channel devices, allowing for the reduction of punchthrough, Early effect and latch-up susceptibility with devices normally manufactured in substrate. In addition, a self-aligning process can be designed that eliminates the need for extra photolithography steps, and allows for increased packing density, reduced defectivity levels, and increased speed[ii].

II. PROCESS SEQUENCE

The final twin-well CMOS cross-section is shown in figure 1. A 500Å pad oxide is first grown on a lightly doped n-type substrate. A 1500Å silicon nitride (Si_3N_4) layer is deposited through LPCVD that will be used for n-well definition. After n-well definition P_{31} is ion implanted at an energy of 130keV with a dose of 6e12cm^{-2}. After the n-well implant a 10000Å oxide is grown that will provide the masking layer for the B_{11}, 4e12cm^{-2}, 50keV p-well implant. The p-well is implanted second to prevent boron segregation into oxide during the oxidation step. The wells are driven in for 17hours in N_2 at 1150°C with an O_2 soak of 4hours.

The existing oxide layer is removed

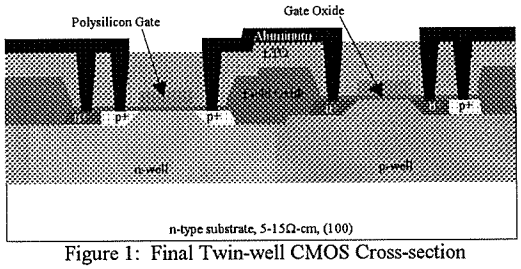
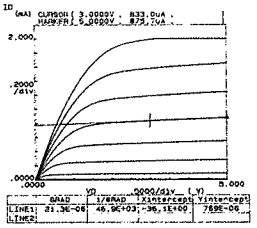


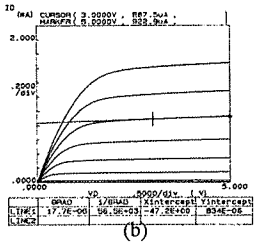
Figure 1: Final Twin-well CMOS Cross-section

and a second 500Å pad oxide is grown. A 1500A layer of silicon nitride is deposited through LPCVD to provide LOCOS isolation. After the active regions are defined a 10000Å field oxide is grown to isolate adjacent devices. The ONO stack is removed and a 1000Å KOOI oxide is grown to provide masking for the Vt adjust implants and to prevent the white ribbon effect. A B_{11} blanket Vt adjust implant is performed at 60keV with a dose of 7e11cm^{-2}. Due to the work function of the p-well an additional Vt adjust implant is required with a dose of 6e11cm^{-2}. The KOOI oxide is striped and a 500Å gate oxide is grown. 6000Å of polysilicon is deposited using LPCVD and is doped with arsenic spin-on dopant to produce n+-polysilicon. Once gates are defined the BF_2 p+ source/drain implant is performed at 150keV with a dose of 2e15cm^{-2}. N+ source/drains are formed through a P_{31} 120keV, 4e15cm^{-2} implant. An anneal is performed to repair the damage done by the source/drain implants. 5000Å of low temperature oxide (LTO) is deposited through LPCVD. Contact holes are defined and etched using a CF_4:H_2 plasma. Aluminum is plasma vapor deposited (PVD) and patterned. Finally a sinter is performed in forming (H_2N_2) gas at 450°C to achieve low contact resistance and uniform metal-silicon interface.

III. RESULTS



(a)

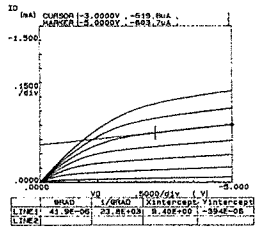


(b)

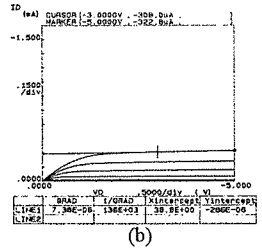
Figure 2: 4μm/32μm n-channel I-V curves, (a) p-well, (b) Twin-well

Twin-well CMOS was compared to p-well CMOS by analyzing 4μm/32μm p-channel test devices. Two similar n-channel fet's were tested so that an accurate comparison of p-channel devices could be performed. Figure 2 displays I-V curves for both twin-well and p-well CMOS n-channel devices; while, figure 3 displays I-V curves for both twin-well and p-well CMOS p-channel devices.

Analysis of the p-channel devices indicated that the Early voltage was increased from 9.4V for p-well to 38.8V for twin-well CMOS. Punchthrough voltage was also increased in magnitude from 8V for p-well to 12V for twin-well CMOS. Latch-up susceptibility was not compared but is expected to improve.



(a)



(b)

Figure 3: 4μm/32μm p-channel I-V curves, (a) p-well, (b) Twin-well

Due to the high body effect caused by the elevated substrate doping level several device characteristics were reduced in magnitude. Saturation current at 5V Vds and 2.5V above Vt was reduced in magnitude from 150.9μA/μm for p-well to 80.7μA/μm for twin-well CMOS. Transconductance or gain was reduced from 41.9μmho for p-well to 7.4μmho for twin-well

	P-well	Twin-well
Vt (V)	-1.1	-2.2
Va (V)	9.4	38.8
Punchthrough Voltage (V)	-8.0	-12.0
|Idsat| (μA/μm) @ 5V Vds and 2.5V above Vt	150.9	80.7
|Idleakage| (pA/μm)	73.9	59.9
Gm (μmho) Saturation Regime	41.9	7.4
S (mV/dec)	85.0	128.0

(a)

	P-well	Twin-well
Vt (V)	0.9	1.2
Va (V)	-36.1	-47.2
Punchthrough Voltage (V)	9.0	9.0
|Idsat| (μA/μm) @ 5V Vds and 2.5V above Vt	218.9	230.5
|Idleakage| (nA/μm)	824.0	1.0
Gm (μmho) Saturation Regime	21.3	17.7
S (mV/dec)	279.0	144.0

(b)

Table 1: 4μm/32μm results for, (a) p-channel devices, (b) n-channel devices

CMOS. Subthreshold swing was increased from 85mV/dec for p-well to 128mV/dec for twin-well CMOS. Leakage current was expected to rise due to the larger subthreshold swing; however, the reduction in leakage current between p-well and twin-well CMOS is due to the higher Vt of the twin-well device.

Results for both n-channel and p-channel devices are found in table 1.

IV. CONCLUSIONS

The twin-well CMOS process has been integrated into the RIT student factory. These wells are self-aligned to increase package density and offer increased punchthrough voltage, increased Early voltage and, reduced latch-up susceptibility, while minimizing the loss in saturation current, transconductance and, subthreshold swing. The only drawback of twin-well CMOS is the high body effect encountered in devices manufactured in substrate.

REFERENCES

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[ii] Chen, J.: 'Quadrupole-Well CMOS for VLSI Technology', IEEE Tans. on Electron Devices, Vol. ED-31, p.918, 1984

Kenneth Gendron obtained his BS in Microelectronic Engineering at Rochester Institute of Technology in May, 1998. He is currently employed with Rockwell International Semiconductor in Newport Beach, California, as a Device Integration Engineer.