

SOI via Wafer Bonding

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Abstract- An attempt is made at the preparation of silicon-on-insulator (SOI) substrates suitable for device fabrication. This is done by the high temperature bonding of a pair of silicon wafers upon which oxide layers have been thermally grown. One of the pair is then ground back to a suitable thickness. Bonding strength and defects are also evaluated.

I. INTRODUCTION

SOI in conjunction with trenches is a very effective method of device isolation. Because the devices are fabricated in islands of silicon which are completely isolated from each other and the bulk substrate by silicon dioxide, as per Fig. 1 below, the devices gain several benefits. A few of these are[1]; no leakage between devices which prevents such things as latch-up, lower parasitic capacitances, and radiation hardening. In addition, this method of isolation yields considerable savings in area over local-oxidation-of-silicon (LOCOS) isolation schemes.

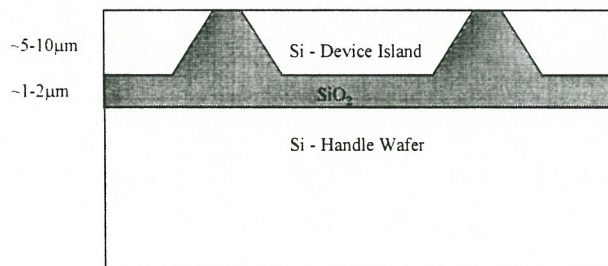


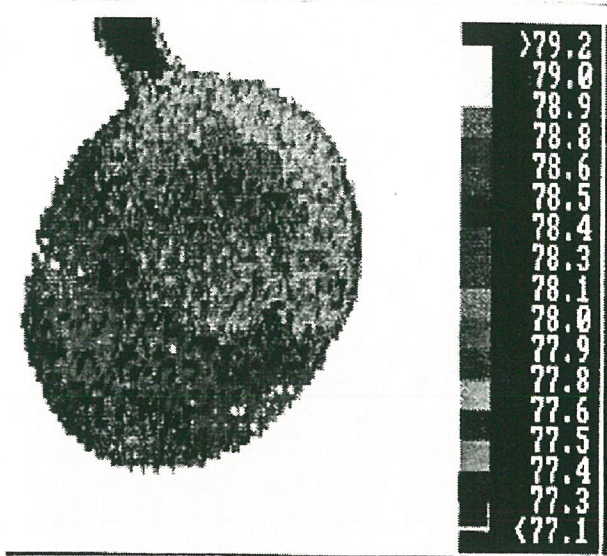
Fig. 1. A schematic cross-section of SOI substrate constructed using wafer bonding and inverted triangular trenches to form trapezoidal silicon device islands.

As with most technologies in the industry, for which there are often many methods of achieving the same goal, SOI is no different. This paper deals with the method of wafer bonding. Wafer bonding as a method of SOI has, as is to be expected, advantages and disadvantage over other methods. Some advantages include; good single crystal silicon substrate in which to

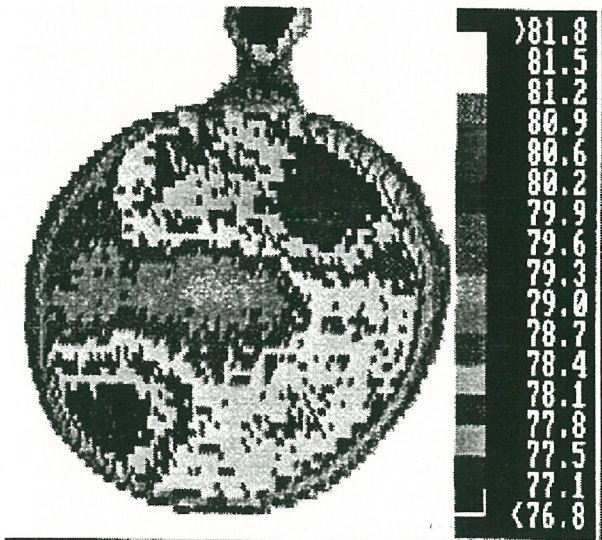
fabricate devices, as opposed to separation-by-implantation-of-oxygen (SIMOX) or perhaps a polysilicon layer deposited over an oxide film, and no unusual materials, as opposed to silicon-on-sapphire (SOS). Its disadvantages include; two silicon wafers are needed to form each bonded pair and somewhat unusual processing, though this is becoming somewhat less of a factor with increasing usage of chemical-mechanical-polishing (CMP) tools.

II. WAFER BONDING

Initially, the ability to bond wafers successfully needed to be verified and evaluated before preparation of wafers with the full process flow were constructed. The first step was to grow 5000Å SiO₂ on sets of wafer pairs via a thermal oxidation step at 1100°C for 48 minutes in wet O₂. Upon removal from the furnace, the wafers were then immediately placed in intimate contact via an applied physical force starting in the center and working out in an attempt to remove any trapped gas. The wafer pair, now room temperature bonded was then placed back into the furnace, resting horizontally with a quartz weight on top, for a soak at 1100°C in N₂ for 30 minutes. Upon removal, the wafers were then placed in buffered HF for approximately 5 minutes to remove the oxide grown on the back sides of both wafers. The wafer bonds were then tested via two methods. The first and non-destructive method was using an infra-red camera to look through the wafers, as silicon is transparent in the infra-red range, to look for any voids, places where trapped gas prevented bonding, in the bond. Fig. 2(a) is of a well bonded wafer, showing a variation of approximately 0.5° across the wafer. Fig. 2(b) is of a deliberately poorly bonded wafer, showing a 2° variation between bonded and unbonded regions. These observations were confirmed by the second and destructive method, the forcible separation of the bonded pair. As SiO₂ is amorphous, a break should appear to be at random and not be along a crystal plane as per silicon. Thus if breaking the wafer yielded smooth areas, indicating the original interface, that region did not bond, but rather formed a void.



(a)



(b)

Fig. 2. Infra-red pictures of bonded silicon wafer pairs. In (a), a well bonded wafer pair is shown. Case (b) is of a poorly bonded wafer pair.

Once verification of the bonding process was completed, the final wafers were constructed. This time, the device wafer received additional processing. After growing the 5000Å of oxide, now to be used for masking, the wafers were coated with resist and patterned using a custom stepper job to expose blank die at the edge of the

wafer in a 2x2 RxC pattern. The resist was then developed and the revealed oxide etched in buffered HF for approximately 5 minutes. The wafers were then etched in a 42:7.5 F₂:O₂ plasma for 10 minutes to produce 5µm deep trenches. The oxide was then stripped in buffered HF, again for about 5 minutes. An additional 5000Å of oxide was then re-grown on the device wafer. The wafers, both device and handle, were then subjected to a clean to remove any particles which might prevent bonding. The two wafers were then placed in intimate contact, followed by the high temperature thermal step to bond them, and then the backside oxide was removed in buffered HF. Next came the attempts to grind/polish back the bonded pair. Unfortunately there was insufficient time to complete the actual grinding step. An attempt was made though to polish the back sides of a wafer pair to try and obtain better resolution with the infra-red camera. This resulted in the breaking of the wafer edges. Whether due to poor bonding or inadequate equipment is unclear. It is however highly unlikely, with the current equipment, that a uniform and repeatable enough process could be achieved for this step. Thus it has been concluded that while wafer bonding is possible, preparation of a usable SOI substrate via wafer bonding is not.

REFERENCES

- [1] S. Wolf, "Silicon Processing for the VLSI Era," Vol. 2, Lattice Press, © 1990, pp 66-78.