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# Implementation and Electrical Characterization of Shallow Trench Isolation

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***Abstract*-Shallow trench isolation (STI) planarized with chemical mechanical polishing (CMP) has replaced LOCOS as the conventional isolation technique for sub-micron devices [7]. The implementation and feasibility of STI has been examined for future device fabrication at RIT. STI test structures have been fabricated to investigate leakage currents between adjacent NMOS transistors in a p-substrate. Trenches were dry etched to a target depth of 2 μm to isolate n+ regions with a junction depth of 0.89 μm. Trench Refill was done with LTO planarized by chemical mechanical polishing (CMP). By testing source/drain n+ regions isolated by two trenches, leakage current of 36.8 pA/μm was measured for a 3.3 V on drain. It is evident that continued experimentation with STI should be implemented with a twin well process to subdue the possible effect of punch through.**

## I. Introduction

Current shallow trench isolation consists of a trench etched in the silicon substrate 0.35 - 0.5 μm in depth [9]. Following a 100 - 200 Å thermal oxide growth for Si-$SiO_2$ interface quality [5], a refill of 8000 -9000 Å of dielectric is deposited. Planarization is done by chemical mechanical polishing (CMP) with a 1500 - 2000 Å layer of silicon nitride as an etch stop.

Shallow trench isolation offers many advantages over

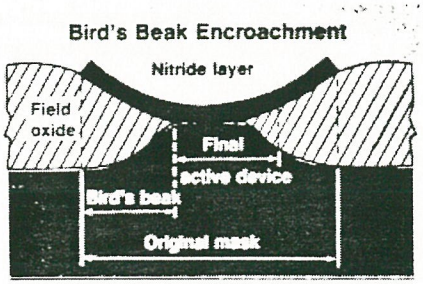


**Figure 1. Birds Beak Encroachment**

LOCOS isolation for submicron devices. Birds beak, a characteristic of LOCOS illustrated in Fig. 1, reduces the effective channel by the encroachment of field oxidant during its long thermal process [5]. STI is free of birds beak allowing for higher packing density [1]. Also reducing the effective channel width is the oxidation enhanced diffusion of boron from the channel stop implant into the active region [5]. The low thermal budget of STI reduces this boron encroachment [3]. By resulting in a more planar topography, STI eases restraints on following lithography steps and multilevel metalization [6]. As LOCOS field oxides are scaled for submicron devices, resulting oxide growths are thinner for narrowly exposed silicon spaces. STI's process is not susceptible to this oxide thinning effect. Furthermore, STI combined with the use of an epi layer increases resistance to latch-up.

Patented in 1979, trench isolation originated with deep grooves partially filled with a dielectric material [2]. In 1983 trench isolation was applied to vertical DRAM technology and high value resistor loads for mixed MOS static RAM cells [2]. Early challenges of trench isolation involved trench etch and refill.

Trench etch control over smoothness and slightly tapered sidewalls were both considerations for the following refill. Trenches were wet etched isotropically to prevent damage of sidewalls induced by RIE [2]. RIE, however, had the quality of producing U - grooves which reduced "stress induced defects" and benefited oxide growth.

In the early eighties, trench refill consisted of a partial fill of polysilicon because conformal depositions of CVD oxide were not attainable [1]. The polysilicon fill followed by an oxidation of it's surface led to poor reliability with the formation of a buried floating gate. Furthermore topography problems were encountered as wide field isolations were difficult to refill uniformly. Current technology allows for complete dielectric refill with conformal deposition. SACVD, $O_3$ - TEOS, HSQ - SOG, and high density plasma CVD (HDP-CVD) oxides are the best refill dielectrics today [6].

## II. Fabrication Process

The mask design, illustrated in Fig. 2, was a three level process including trench, contact cuts, and metal. Window like active regions were designed to represent the n+ source and drains of adjacent NMOS transistors (Figure 3). The n+ regions were separated by varying trench widths of 1, 2, 3, 5, and 7 μm. The metal level included lines over trenches to investigate a parasitic MOS effect.

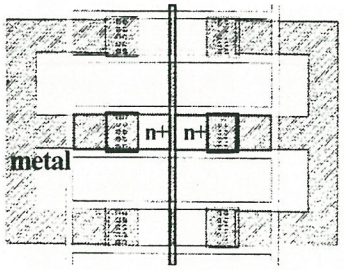


**Figure 2. Three level mask design**

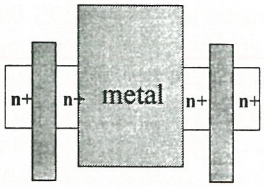


**Figure 3. Adjacent NMOS transistors in p-substrate**

The fabrication process began with 600Å of pad oxide grown in a ambient of dry $O_2$. Next, a field implant of $P^{31}$ was done through the pad oxide at 100 keV with a dose of 5E15/cm$^2$. A nitride layer 1200 Å thick was deposited over the pad oxide for a CMP etch stop. Following the first photolithography step of trench, the nitride stop was etched by RIE and pad oxide wet etched by buffered HF. The RIE of the silicon substrate for trenches consisted of 42 sccm of $SF_6$ and 7.5 sccm of $O_2$ at a pressure of 400mT and power of 40 W. The etch was 3.5 minutes for a target depth of 2 μm to isolate n+ junction depths measured to be 0.8 μm. Trench etch was followed by a channel stop implant of $B^{11}$ at 35 keV with a dose of 4E13/cm$^2$. A 1000 Å thermal oxide was grown in a wet $O_2$ ambient to limit diffusion of n+ junction depth. Trench refill was accomplished by LPCVD oxide with a 2

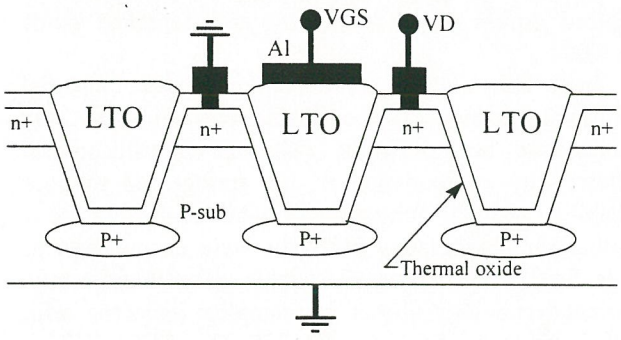


**Figure 4. Final STI test structure cross-section**

hour deposition for a thickness of 2μm. Planarization by means of CMP was followed by back end processing of photo II contact cuts and photo III metal. Figure 4. Illustrates the resulting STI test structure. After sinter, STI was electrically characterized with a HP4145 oscilloscope.

## III. Experimental Results

*N+ Junction Depth*

In order to find the necessary depth of the trench etch to properly isolate active areas, the junction depth of the n+ regions needed to be measured. A separate dummy wafer with pad oxide and field implant was subjected immediately to the thermal oxide step using an ambient of nitrogen only. A Groove and stain method was used followed by interference microscopy. Three fringes were observed resulting in a determined junction depth of 0.89 μm.

*Trench Etch*

Trenches were originally thought to be successfully etched to a depth of 2μm by the use of a dummy wafer patterned by RIT's exposure test matrix (ETM) mask. The ETM pattern was trench etched for 3.5 minutes and

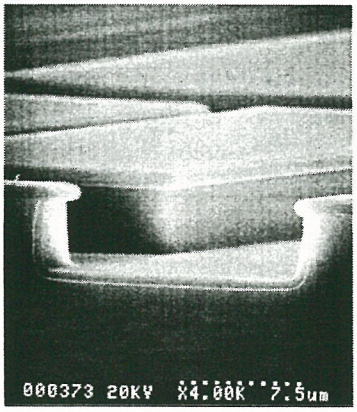


**Figure 5. SEM of trench with incomplete refill**

trenches were visually determined to be about 2 μm by comparison with a 3μm line width.

However, in a subsequent SEM with scale (+/- 10 % accuracy) the trenches were clearly deeper than 2 μm. Referring to Fig. 5, the trenches appear to be about 5.5 μm deep.

*Trench Refill*

Trenches were incompletely filled with the resulting depth of trenches and thin depositions of LTO. Fig. 5 shows a LTO thickness of 7500 Å. The incomplete refill resulted in very poor planarity for the back end processing of contact cuts and metal. Patterned metal lines for parasitic gate investigation and test pad connection were lost by the aluminum etch undercutting the metal where lines crossed trenches. Additionally,

difficulty in alignment was encountered for the metal level.

*Electrical Results*

Due to the loss of metal over trenches, only large designed n+ regions of 300 X 100 μm were measured by making direct contact with manual probes to metal over contact cuts. Testing was done with the diode program on the HP4145 by varying the voltage of one n+ region from -10 V to 10 V. The other n+ region was grounded with a floating substrate. Preliminary testing of single trenches with a width of 3 μm resulted in asymmetrical leakage current plot. With a negative bias applied. single trench test plots exhibited characteristics of a diode. By measuring n+ regions separated by two trenches, a bias of 3.3 V resulted in a current of 11 nA. Because the

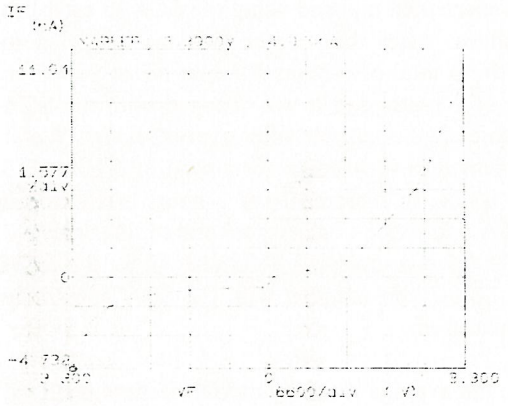

**Figure 1. Leakage current for 3.3 V supply**

width of the n+ region measured was a width of 300 μm, the resulting leakage current was 37/ pA/μm.

*Future Work*

Future work should aim for a shallow junction depth of 0.5 μm or less. This will allow for a shallow target depth when etching trenches, without the concern of n+ junctions extending beneath them. This shallow of a junction may not be possible until rapid thermal processing (RTP) becomes available; a ten minute soak for thermal oxide resulted in a n+ junction depth of 0.89 μm. The addition of plasma enhanced CVD at RIT will allow for implementation of TEOS. TEOS is a better dielectric fill and may result in a more conformal deposition. Application of a twin well concept in further experimentation would reduce the chance of punch through as junction depths and trenches become more shallow. A p+ field implant into the p-substrate before the n+ implant would reduce the depletion width extension.

## IV. Conclusion

A successful mask design was created for the examination of leakage currents between adjacent NMOS devices separated by varying trench widths in p-substrate. Processing resulted in 5.5 μm deep trenches separating n+ regions with a junction depth of 0.89 μm. CVD refill was incomplete resulting in poor planarity for remaining back end processing. The natural isolation of reverse biased p-n junctions (back to back diodes) was not apparent for the testing of individual trenches. The testing of n+ regions separated by two trenches, each a width of 20 μm, resulted in a leakage current of 37 pA/μm. Future work will progress towards more shallow junction depths and trenches for isolation.

## References

[1] Mikoshiba, H., et al. "A New Trench Isolation as a Replacement of Locos," Tech. Dig. IEDM, 1984, p. 578.

[2] Rung, R.D. "Trench Isolation Prospects for Application in CMOS VLSI," Tech. Dig. IEDM, 1984, p. 574.

[3] Davari, B., et al. "A Variable-Size Shallow Trench Isolation (STI) Technology with Diffused Sidewall Doping for Submicron CMOS," Tech. Dig. IEDM, 1988, p. 92.

[4] Shibahara, K., et al. "Trench Isolation With ∇(Nabla) - Shaped Buried Oxide for 256 Mega-Bit DRAMs," Tech. Dig. IEDM, 1992, p. 275.

[5] Wolf, S., Silicon Processing for the VLSI Era, Vol. 2: Process Integration, Lattice Press, 1990.

[6] Nag, S., et al. "Comparative Evaluation of Gap-Fill Dielectrics in Shallow Trench Isolation for Sub 0.25 μm Technologies," Tech. Dig. IEDM, 1996, p. 841.

[7] Chen, C., et al. "A Novel 0.25 μm Shallow Trench Isolation Technology," Tech. Dig. IEDM, 1996, p. 837.

**John Castellana** received his BS degree in microelectronic engineering from the Rochester Institute of Technology.