Test Patterns for Chemical Mechanical Polish Characterization

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Abstract **– I studied the effect of wafer topography on the chemical mechanical polishing (CMP) process. This was done by first designing test structures. A mask set of these structures was then designed and fabricated. Wafers were patterned with the test mask and then were polished. The result was that a pattern dependency was seen on the wafers. The polishing process was effected by the surface topography.**

I. INTRODUCTION

Chemical mechanical polishing (CMP) of semiconductor devices has gained much recent attention. As transistor dimensions continue to shrink, planarization schemes are needed to reduce the depth of focus (DOF) constraints on microlithography. Too much surface topography will result in difficulties in focusing across the entire resist film. By planarizing the wafer's surface, the step heights are reduced which relaxes the DOF needed from the lithography tools. The trend is towards using a planarization step before every lithographic process. Already, most advanced CMOS processes are using full planarization of the dielectric stack to overcome the large step heights over the metal lines.

CMP has become the dominate means of planarizing submicron devices. This is because CMP is the only technology which can provide global planarization of the wafer. Global planarization means that the film thickness in uniform across the entire wafer. Non-uniformities from the film deposition steps can be reduced through a CMP polish process. CMP also provides local planarization of topography within the die.

The usual parameters of interest in a CMP process are the pressure on the wafer, pad rotational speed, wafer rotational speed, slurry flow, as well as the composition of the pad and the slurry. To evaluate the effects of these parameters on the polish process, it is necessary to have a series of test structures to qualify what is happening on the wafer. The goal of this experiment is to design and fabricate a test mask for use in developing and characterizing CMP processes.

The pad used in a CMP polish process will conform to the topographic features of the wafers surface. This results in greater pressure being applied to those features which have the largest step height. Fig. 1 shows the pad conforming to surface features.

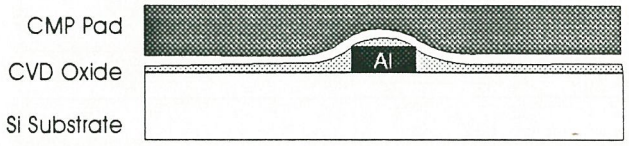

Fig. 1. Cross-section showing the pad conforming to wafer topography.

This pressure differential results in the "hills" in the wafer's topography polishing faster and the "valleys" on the film's surface polish slower. The result is the topography is reduced as the wafer polishes.

The benefit of the conformal pad can also cause problems. If a feature is isolated, it will also polish at an elevated rate when compared to densely packed features. This is because the neighboring features tend to protect the adjacent features. Isolated features lack this protection and polish at a quicker rate. Dishing is a similar phenomena in Damascene style polishes where the center of a filled trench polishes faster then the edges. The edges of the region surrounding the trench will also polish faster because the pad will push into the trench and will round the edges.

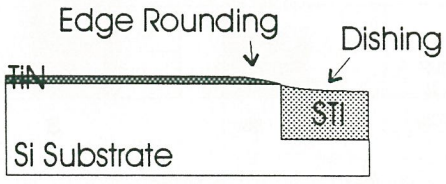

Fig. 2. Example of dishing and rounding.

All of these effects need to be characterized and understood to develop a controlled CMP process.

II. CMP Test Structures - Design Methodology

A good set of test structures should be designed to capture the variability which may be encountered in the process which they are characterizing. The goal was to design a series of test structures to examine the effects of topography and feature density on different styles of polishing. They should work on Damascene style trench polishes, like shallow trench isolations (STI), vias, and copper metallization. They were also designed to work on planarizing interlevel dielectrics (ILD).

To capture the variability in the process, the test structures were designed to capture the worst case situations encountered. This occurs when polishing very isolated and very densely packed features. By focusing on these styles of structures, it becomes possible to get an idea of the process variability.

The very isolated structures consisted of five 30μm x 30μm pads scattered in a 2mm x 2mm isolation region. The inverse of this structure was also put on the die. These structures are extreme worst cases in the polishing process. There are four possible scenarios, depending on which process is being used. For example, in an STI trench polish, the very isolated trenches will be the slowest polishing features on the die because the most material needs to be removed from the large active area surrounding the trench. The inverse of this structure is a huge trench region with isolated 30μm pads of active region. This case will show severe dishing in the trench region due to the lack of active area to protect the trench die.

The opposite process would be an ILD style process. In this case, isolated pads of metal would be covered with a conformal dielectric deposition. The ILD over the isolated metal would polish very quickly compared to the ILD over the substrate. In a densely packed area, the ILD over the substrate would be protected by the adjacent hills of ILD over the metal lines. So the isolated features should have the thinnest remaining ILD thickness while the densely packed features should have the thickest.

The next series of structures were isolated arrays. These consisted of a series of ten 30μm x 30μm pads also contained in the isolated regions. These structures provide similar information as the very isolated pads with less severe dishing effects since adjacent structures will help protect their neighbors.

A series of lines/space pairs of varying sizes was also added to provide a measure of what effect feature size has on the polish process. There were also a series of densely packed via arrays which provide the other extreme versus the very isolated structures. The densely packed structures (lines / vias) represents the most common features seen on a wafer.

III. Validation

After the test structures were designed, a test cell layout was done using Design Architect. A mask set was then fabricated on a MEBES E-beam mask writer. The design was then validated using two sets of test structures.

The main testing was done using an STI polish process. A 700Å thermal pad oxide was grown on the wafers, followed by the deposition of a 2000Å silicon nitride. This layer served as the planar stop when the trenches were polished. The nitride was patterned and the trenches were etched in a fluorine plasma to a target depth of 1.5μm. The trenches were then filled with a CVD low-temperature oxide (LTO). The LTO was then CMP polished to leave behind the filled trenches.

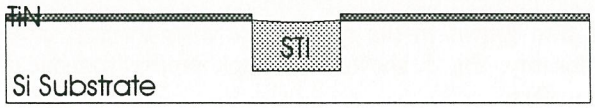

Fig. 3. Finished STI Structure

The other process which was tested was an ILD polish. 0.5μm of aluminum was deposited and patterned on the wafers. A thick (>1μm) LTO was then deposited on the wafers. The ILD was then polished and the wafers were measured.

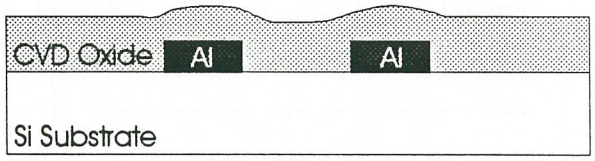

Fig. 4. Finished ILD Structure

The finished structures were then measure to determine the effect of the polishing process on the wafers.

IV. Results

Problems were encountered in the measurement phase. The measurement tool was only able to measure oxides on silicon. I was unable to measure the sites over nitride or aluminum which would have given a better indication of the planarization process. The second problem was that the resolution of the measurement tool wasn't high enough. The spot size of the measurement was about a 25 μm circle. Most of the structures that I was looking at were smaller then this, so I was unable to get good measurement data off of the Nanospec. New equipment which is still in installation should fix this problem. It is a newer machine, so it should have a smaller spot size for the measurement. It is also fully automated, so a larger number of points will be able to be measured.

The LTO CVD deposition reactor also provided some additional problems. It was impossible to get a thick (>1 μm) film of LTO on the wafer using the existing recipe (400°C, wafers loaded in center of furnace). After some experimentation, thick films were achieved by loading the wafers half-way between the furnace door and the center of the furnace tube. 1μm films were easily achieved using this modification. Not sure if this was due to the lower temperature near the door or that the wafers were closer to the incoming gas inlets. The second problem introduced by the CVD furnace was that the film grown in the reactor had a severe edge non-uniformity. Fig. 5. shows an example profile from one of the wafers.

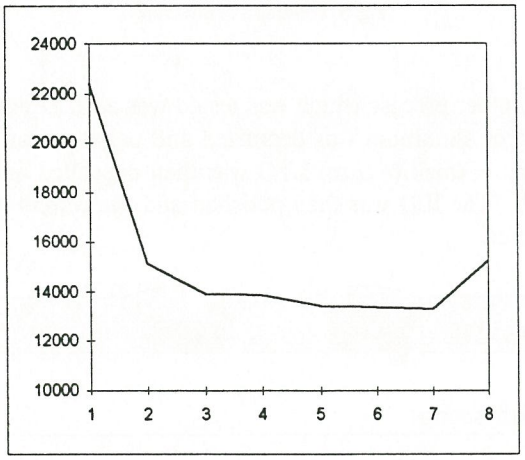

Fig. 5. Edge-thick profile after LTO deposition

The thick ring of LTO around the edge of the wafer made it difficult to polish the wafers uniformly. So this edge ring was removed by protecting the center of the wafer with resist and etching the thick outer ring of LTO off of the wafer. Much better results were achieved after performing this step.

The final problem was that the trenches in the STI structures were etched too deep. This resulted in impartial filling of the trenches and added some severe topography to the wafer. This resulted in the STI structures showing more dramatic polish effects, since the step height was much larger then expected. The conformal pad would try and fill these gaps resulting in the edges of the trenches polishing being severely overpolished.

Visual examination of the wafers showed the effect of the polish process on the finished wafers. Fig. 6. shows a isolated STI trench. There is a halo around the trench in the nitride. This is a result of edges of the trench polishing quickly resulting in a thinner ring of nitride on the edge of the trench.

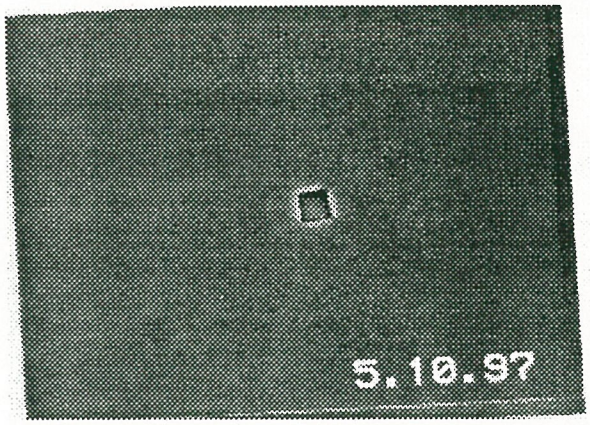

Fig. 6. STI trench showing over-polish on edge.

The next picture shows the densely packed via arrays and some large pads, all composed of nitride surrounded by an LTO filled trench. You can see that the edges of the pads polished down to silicon, while the nitride is still thick in the center. This picture shows the severity of the over-polishing due to the trenches being deep and only partially filled.

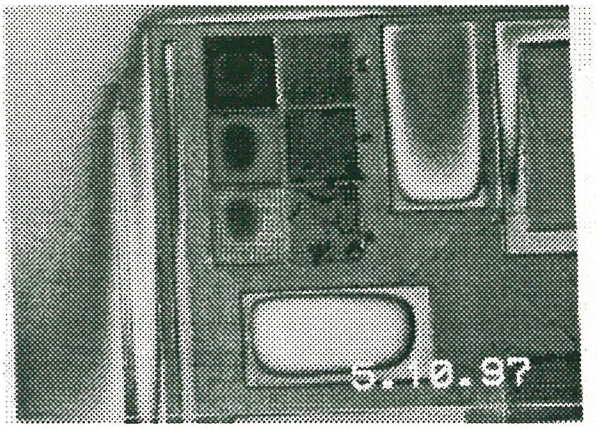

Fig. 7. STI trench showing corners rounding.

Some SEM pictures were taken of these structures. They show the edge effects caused by the polish process. Fig. 8. shows the active region between a large trench and an isolated array. The nitride forms a small hill between the two regions.

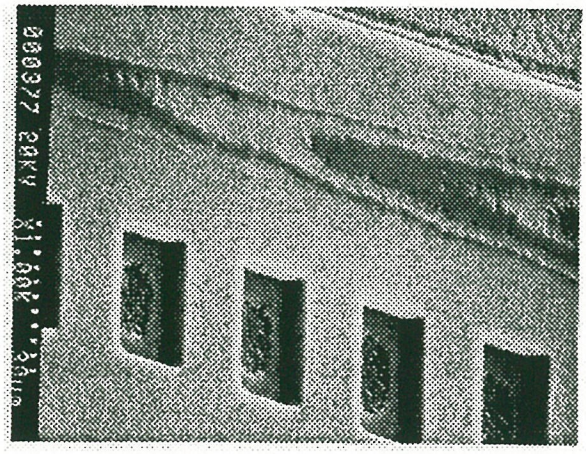

Fig. 8. Nitride hill between trench regions.

Fig. 9. shows the edge of a nitride pad where the nitride polished thin next to a trench. This picture shows the edge of the nitride being beveled where the pad conformed to the edge of the trench.

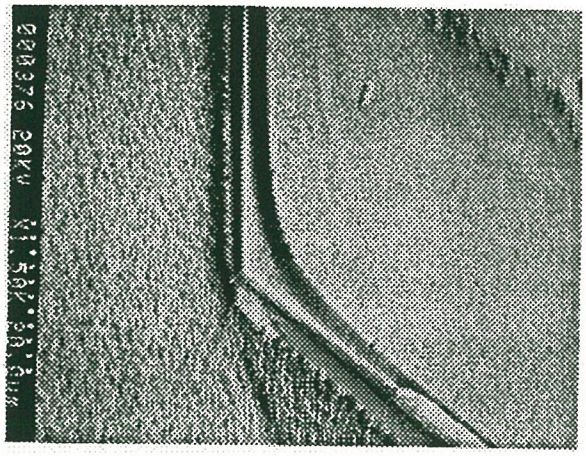

Fig. 9. Edge of nitride pad.

The polisher added an edge-thin profile to the wafer. This was due to the design of the wafer carrier in the polishing tool. The wafer carrier had a 1" ring surrounding the wafer which was slightly thinner then the wafer. A backing film was also behind the wafer to try and push the center of the wafer out. The net result was that the edges of the wafer extended over the sides of the carrier. This means that they would tend to "round" in the polishing process. The ILD test wafers confirmed this, as they averaged about 13kÅ in the center and 11kÅ at the edge of the wafer.

V. Conclusion

The goal of this experiment was to design and fabricate a mask set consisting of test structures to evaluate various CMP processes. This goal was met and a mask set was delivered. Validation of the mask set has shown a few phenomena.

The topography of the wafer has been shown to have am effect on the local removal rate on wafers. Densely packed features will polish at a different rate then isolated features. Also, the steps heights due to topography will cause different polish rates. These steps can cause different polish rates on edge features and in the center of features.

Test structures for CMP polishing need to account for the effects of topography and feature density so they can provide the best indication of the variability in the process. This information can then be used to select test sites on the device wafers for process monitoring.

VI. Future Work

The development of test structures for CMP leads into future projects to design CMP process modules. First, the polishers need to be characterized so that the non-uniformities introduced by the polisher can be understood. This will ensure that the variability introduced into the process by the polisher is understood. After this is done, specific polish processes for different films can be developed, examining factors such as different pads, slurries, and machine parameters to find the optimal mix of parameters which give a good removal rate and uniformity. After suitable process modules are developed, they can be integrated into an advanced RIT CMOS process to provide a fully-planarized, submicron process with multilevel metallization.

VII. Acknowledgments

I would like to thank Dr. Santosh Kurinec and Dr. Richard Lane for their advice during this experiment and John Castellana for help with running the wafers.