Investigation of Buried Channel PMOS

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Abstract — The objective of this project is to investigate the electrical characteristics of Buried Channel PMOS for twin-well CMOS process. Project involves the investigation of the P-MOSFET by varying the standard boron (B11) threshold adjust implant dose. In addition, the effect of adding a phosphorus (P31) counter doping implant on the device characteristics is also investigated. The addition of counter doping implant will reduce the thickness of the buried channel created by the threshold adjust implant. Test results for the counter doped twin-well process shows stronger transistor turn-off and lower off-state leakage current without significantly affecting the on-state current drive.

I. INTRODUCTION

The demand for faster and smaller chips has driven the semiconductor manufacturers to continuously shrink down their devices. The emphases on the transistors being high drive current with low threshold voltage for faster charge up, faster device turn-off with low leakage current for low off-state power dissipation. These goals have made the twin-well CMOS technology of choice for semiconductor fabrication. Twin-well process allows device engineer to customize the doping concentration of both n-well and p-well, thus optimizing the device characteristics of both types of transistors. To achieve the high drive current, it is necessary to have the threshold voltage as low as possible to maintain a full current drive above threshold. The transistor turn-off is also desired to be instantaneous to obtain fast discharge and device characteristics that closely resemble an ideal transistor. With channel length dropping below submicron, the device design becomes increasingly difficult as the short channel effects such as GIDL, DIBL, Vt roll-off begin to play a stronger role in the device performance. To make the task even more challenging, the buried channel P-MOSFET exhibits higher susceptibility to short channel effects and degraded device operation.

Buried channel PMOS has an advantage of larger drive current due to the buried channel having higher mobility than the surface. This allows approximately 15% increase in the carrier mobility that results in higher drive current. However, buried channel devices has several disadvantages that are more accentuated than the surface channel devices. It is more susceptible to threshold voltage roll-off due to higher carrier diffusion into the channel through the p-channel region. It has lower subthreshold swing because of the higher conduction path in the p-channel created by the Vt adjust implant, thus decreasing the gate-to-substrate coupling. The barrier between the source and drain is also lowered by the boron threshold adjust implant resulting in higher leakage current.

To reduce the buried channel effect, a counter doping implant, which implants a layer of phosphorus as n-type dopant, will be performed to reduce the boron layer introduced by the threshold adjust implant.

II. EXPERIMENTAL BACKGROUND

Counter doping implant is introduced to the twin-well process to control the thickness of the p-channel layer. This implant will place an n-type layer beneath the p-type layer to reduce the depth of the p-channel. This will move the potential minimum of the channel closer to the surface of the substrate and result in closer resemblance to a surface channel device. Adding this implant could also reduce the bulk punchthrough and the Vt roll-off susceptibility.

Two factors are varied in the experiment to change the net doping profile and the p-channel depth. The first factor is the threshold adjust implant dose. Second factor was the counter doping implant energy. Using TMA SUPREM IV simulation, counter doping implant dose is determined so that the threshold voltage will be approximately -1V. Figure 1 shows the doping concentration profile of each type of dopant and net doping of the substrate.

Threshold voltage is initially calculated by taking 60% of the implant dose (shown in figure 2). This is approximately the amount of boron implanted into the substrate when implanting through the Kooi oxide. The results show that the effective dose in the substrate should

be approximately 8E11 boron ion/cm^2. For every 2E11 boron ions/cm^2 increase in threshold adjust implant dose, the threshold voltage shifts by about 0.4V.

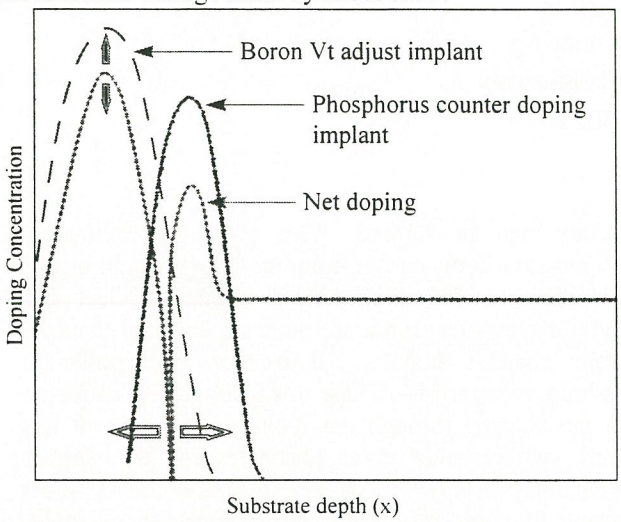


Figure 1. The doping concentration profile of dopants and the net doping profile in the n-well.

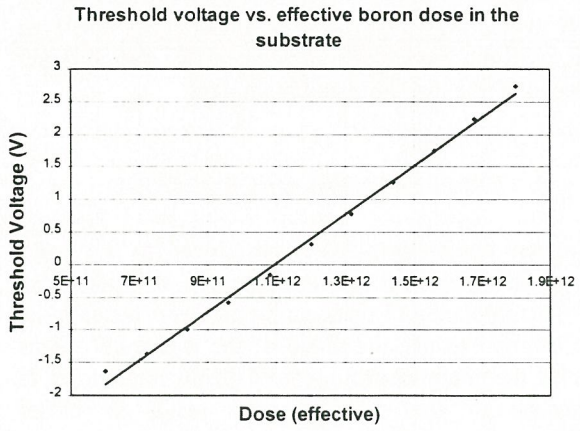


Figure 2. Projected threshold voltage as function of effective boron dose implanted into the substrate.

III. RESULTS AND DISCUSSION

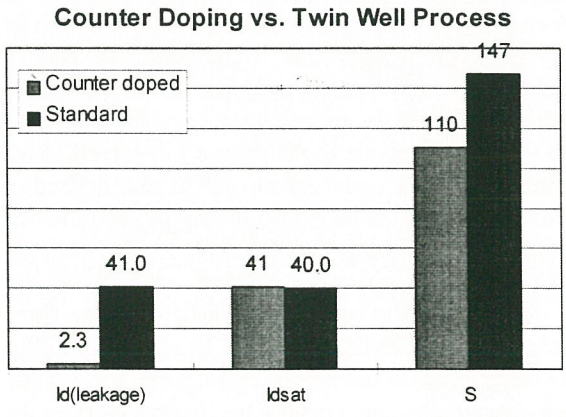
The PMOS device performance was tested using HP4145 Semiconductor Parameter Analyzer. All PMOS devices tested had channel length of 6um and channel width of 32um. The tests were done for both counter doped twin-well process and standard twin-well process. Both processes were identical with the exception of adding counter doping implant process. Furthermore, the counter doped twin-well process is compared to the RIT n-well process to draw some conclusion about its effectiveness in device performance improvement over n-well process. Device testing was limited to I-V characteristic, threshold voltage extraction, and subthreshold performance. The source-drain punch-through and Vt roll-off were not studied since the devices under 4 um failed to operate.

The electrical performance distribution of the device fabricated using counter doped twin-well is shown in table 1. The devices show extremely tight performance distribution. The leakage current averaged about 3 pA and the drive current had a mean of 34 uA. Subthreshold swing averaged at 119 mV/decade.

	Leakage Current (pA)	Drive Current (uA)	Sub Vt Swing (mV/dec)
Mean	3	34	119
St. Dev.	3	5	10
Min. Value	1	25	110
Max. Value	8	41	146

Table 1. Statistical device characteristics distribution of the devices fabricated using counter doped twin-well process. The data was compiled after removing the highest and lowest data point for each category.

Simulation results obtained from TMA SUPREM IV were used to target the threshold voltage around -1V. However, the actual test results show the threshold voltage varying from +0.3V to -0.7V. The shift in the threshold voltage placed the lowest leakage current at positive gate voltage, and not when V_G=0. Therefore, the leakage current values were extracted where the lowest leakage occurred. The data should still be valid since the threshold voltage can be adjusted by further optimizing the Vt adjust/counter doping implant combination. This should not affect the result since test results show no dramatic change even with +0.3 to -0.7V Vt swing.



Graph 1. Direct comparison of device fabricated using counter doped twin-well process and standard twin-well process. The leakage current is reduced by a decade with no noticeable drive current loss. The subthreshold swing also improved by 37 mV/decade.

Graph 1 shows direct comparison of a device fabricated with counter doped twin-well and standard twin-well process. It is shown that the counter doped device exhibits significant improvement in leakage current and subthreshold swing without suffering significant drive current. Counter doped device shows leakage current reduction of 94% with only 2.5% drive current loss. The subthreshold swing improved by 25%, proving that the device turn-off is enhanced by the addition of counter doping implant.

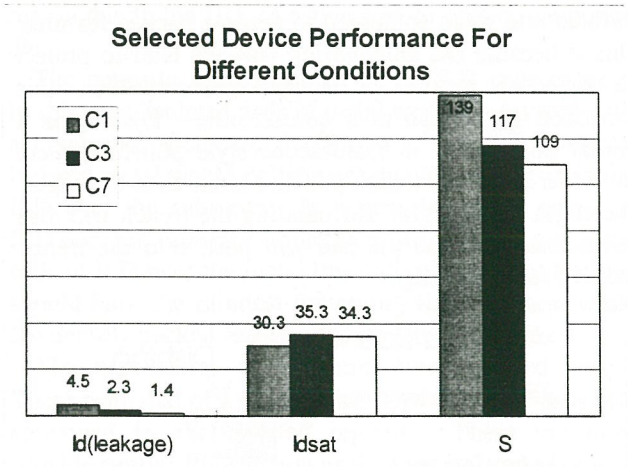
The RIT n-well process shows mixed results. Approximately 65% of the devices tested show leakage current in the nano-Ampere range and subthreshold swing of ~200 mV/decade. The other 35% had device characteristics comparable to the counter doped implant process.

The comparison of test results from three different counter doping conditions is shown by graph 2. The process conditions are shown in table 2.

	Vt adjust dose (ions/cm2)	Counter doping dose (ions/cm2)	Counter doping energy (keV)
C1	2E12	6.0E11	135
C3	3E12	1.3E12	120
C7	4E12	1.9E12	120

Table 2. Implant condition settings for each wafer. Threshold adjust implant energy is fixed at 35 keV.

The test results show that C7 gave the best results. It has the lowest leakage current and subthreshold swing. It has second highest drive current. It can be seen that the counter doping implant dose is about half of the threshold adjust implant dose. The leakage and the subthreshold swing improved as the threshold adjust implant dose is increased.



Graph 2. Test result of three different Vt adjust/counter dope implant combinations.

The true relationship between the factors cannot be concluded without complete design of experiment involving all factors.

IV. CONCLUSION

The counter doping implant process was introduced to the standard twin-well process to investigate its effects on the buried channel P-MOSFET. The results show improved subthreshold and leakage performance over the standard twin-well process. An indirect comparison to RIT n-well process shows that the counter doped twin-well process yields better device performance distribution.

REFERENCES

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Chuan-Hsing Chen received his Bachelor degree from Microelectronic Engineering Department in Rochester Institute of Technology. He has cooped as Product Engineer and Plasma Etch Engineer. He is currently employed in Samsung Austin Semiconductor.