BF_2 Implanted Stacked α-Silicon Gate Capacitors

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Abstract - BF_2 implanted stacked α-silicon (SAS) electrode capacitors were fabricated on n-type silicon substrates. The purpose of this electrode scheme was to quantify the effectiveness of stacked films in suppressing boron penetration into the dielectric and substrate. A 150A thick silicon dioxide was used as the capacitor dielectric. The top α-silicon electrode was deposited in a three step process using low pressure chemical vapor deposition (LPCVD). A controlled sample was fabricated using LPCVD polysilicon (Poly) as the top electrode. The samples were tested for dielectric degradation using voltage ramping techniques. The breakdown field was recorded for 2 different size capacitor areas. This testing shows that there is not significant differences between the SAS and poly gate structures on oxide quality. However, further investigation must be done on other issues such as oxide charge trapping, flat band shift and oxide growth before a complete conclusion is made.

I. INTRODUCTION

As CMOS technology continues to scale into the deep submicron region, p+ polysilicon gate pMOS is becoming widely used to eliminate short channel effects [1] and, decrease channel leakage and improve subthreshold characteristics. Currently buried channel pMOS is the dominant process technology. However this device requires a p-type threshold adjust implant. This implant has the effect of creating a more conducive leakage path between the source and drain regions of the transistor and of increasing the subthreshold swing parameter S. In addition, as threshold voltage reductions continue, the dose of this implant must become larger while reducing the implant energy. However, the low energy required is becoming hard to control. P+ gate provide more process control over subthreshold and threshold voltage characteristics [2]. In addition it has been shown that p+ poly-Si gate pMOS is more resistant to hot carrier induced instability than n+ poly-Si pMOS [2].

However, p+ poly-Si gate pMOS is not without drawbacks. Boron dopant, which is widely used fore p+ regions, segregates into the oxide dielectric resulting in degradation. Further diffusion of boron into substrate can lead to threshold voltage shifts. It has also been shown that fluorine, introduced from the BF2 species, can enhance boron diffusion, lead to negative-charge interface states [3] and increase oxide thickness when subjected to additional thermal cycles[4]. In addition, since phosphorus acts as a getterer for mobile ions, p+ poly-Si gates are more susceptible to mobile ion contamination than n+ poly-Si gates. Lastly, p-type dopants segregate more easily into silicides than n-type dopants leaving a depletion region near the silicide-polysilicon interface.

There have been many solutions suggested to reduce the negative effects of p+ poly-Si while maintaining it's advantages. Oxynitrides have been widely used as gate dielectric to acts as a barrier to boron diffusion. These nitrides could be grown using NO_2, NO, NH_3 treated oxides or nitrogen implanted silicon. However, it is important that the peak nitrogen concentration be near the gate-dielectric interface. Phosphorus in the gate materials has also been shown to act as a getterer of fluorine and decrease boron penetration into the gate oxide [5].

Another method to suppress boron and fluorine diffusion is to use stacked gate material. It has been shown that boron penetration effects can be suppressed by using a stacked α-silicon (SAS) gate structure. In this structure dopant atoms tend to segregate at the stacked film and gate-oxide interfaces. Oxide quality and flat band shift as function of dopant annealing temperature can be monitored to quantify the effectiveness of the SAS structure. This experiment focuses on oxide breakdown characteristics for both SAS and poly electrode capacitors. Results show that there are not significant differences in oxide breakdown characteristics between the two capacitors.

II. EXPERIMENTAL PROCEDURES

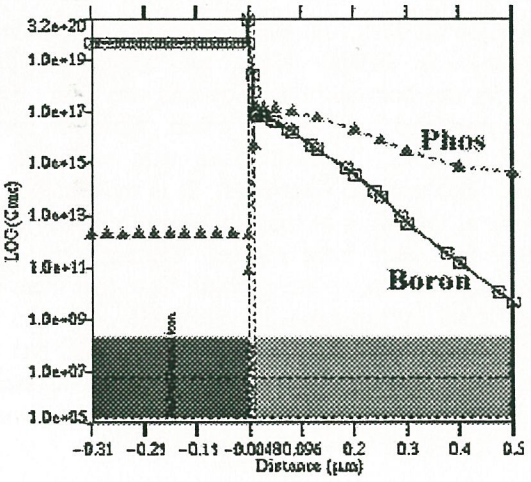
Capacitors were fabricated on 100mm n-type silicon wafers with a crystal orientation of <100> and a substrate resistivity of 10Ω-cm. The sample wafers were clean using a standard RCA clean process and capacitor areas were formed using a LOCOS process. This help to ensure that total removal of oxide would not occur at the

edges of the polysilicon electrodes and that probe contact would not disturb the thin capacitor oxide. A P31 3e12 ions/cm^2 80KeV threshold adjust implant was performed through a sacrificial oxide.

Oxide growth was performed in dry O_2 at 950C for eleven minutes. This included the 4 minute ramp up time from the push in temperature of 900C. A twenty minute anneal in nitrogen at 950C followed the oxidation to ensure full oxidation. The wafers were then pulled at 700C to reduce any oxidation from the clean room ambient. The resulting oxide thickness was 140-150A.

The SAS electrode was performed in a three step silane LPCVD process. A 1500A α-silicon layer was deposited at 560C with a chamber pressure of 375mT. The silane was then pumped out of the system and the chamber was purge with nitrogen for twenty minutes. It was hoped that this purge would stop any grain growth and change the surface slightly to suppress any continues grain growth. A second 1500A α-silicon layer was then deposited resulting in a total film thickness of 3000A. The α-silicon deposition rate was 28A/min. The poly electrode was deposited at 610C with a chamber pressure of 375mT. The poly deposition rate was 80A/min.

Figure 1. Simulated dopant profile after 1025C anneal for 10 minutes.



The capacitor electrode was patterned using RIE etching with a SF_6/O_2 chemistry. The etch rate was 6800A/min. The samples were then ion implant with BF_2 at an energy of 120KeV and a dose of 2e15/cm^2. Implant time was 30 minutes per sample. The dopant atoms were then activated using a furnace tube at 1025C for 10 minutes in nitrogen. The backside of the samples were then etched in an RIE chamber to ensure good electrode contact to the substrate. Figure 1 shows the SUPREMIV simulated dopant profile in the substrate after anneal.

Sample were tested electrically using an HP4145 semiconductor parameter analyzer. The substrate was grounded while a positive voltage was applied to the p+ electrode to put the substrate into accumulation. The voltage was swept from 0 to 22V in 0.2V increments. Capacitor current was monitored to determine breakdown voltage. Two different area size capacitors were tested (1kμm^2 and 10kμm^2).

III. RESULTS AND DISCUSSION

Figure 2 shows a typical breakdown curve of a tested capacitor. Typical breakdown fields were in excess of 10MV/cm for both medium and small area capacitors. Capacitors with large breakdown field had current densities in excess of 50nA/um^2 at breakdown. Current densities at fields below the onset of Fowler-Nordheim tunneling were <20fA/um^2, indicating that the oxides were good quality and that the large current densities at higher fields was not due to pinholes. In addition, surface charge analysis of the capacitor dielectric was performed before the electrode deposition and indicated good quality oxides with less than 1e11/cm^2 fixed oxide charge.

Figure 2. Typical breakdown curves of a medium area capacitor. The curves at the far left is the breakdown curves while the second sweep gives the characteristics of a diode (right curve).

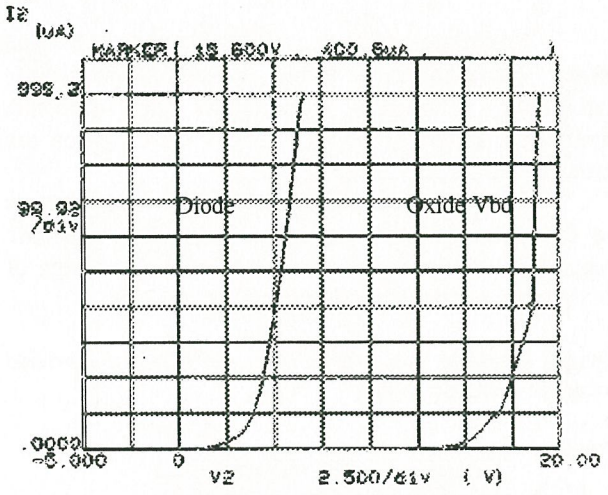
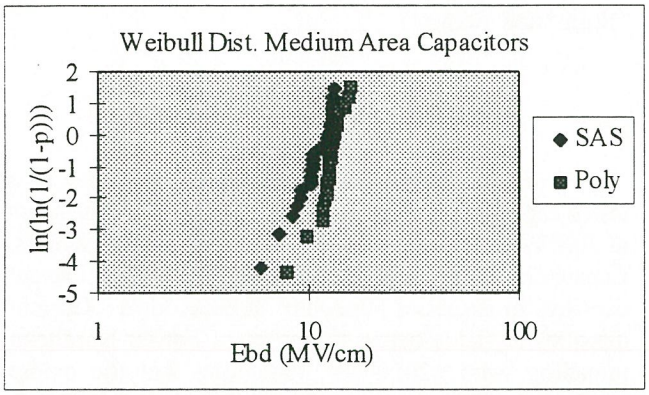


Figure 3 shows the electric field breakdown distributions for the small area capacitors. Analysis of variance shows that there are no significant differences between the SAS and poly gate structures. However, the SAS structures show slightly less breakdown field strength. Figure 4 show the breakdown distribution for medium area capacitors. Analysis of Variance shows that there does seem to be a difference in these two samples. The poly electrode structure seems to show greater strength than the SAS electrode capacitor. However this does not agree with the small area capacitor data. This differences between the SAS and poly capacitors may be due to process defects inherent to one wafer.

Figures 3-4. Weibull breakdown distributions for small and medium area capacitors. 40 capacitors were tested for each sample



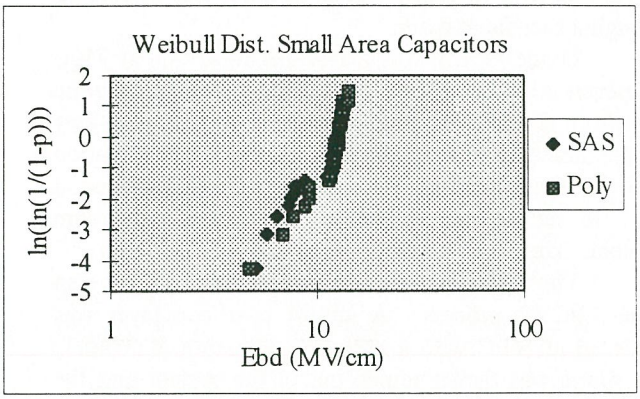


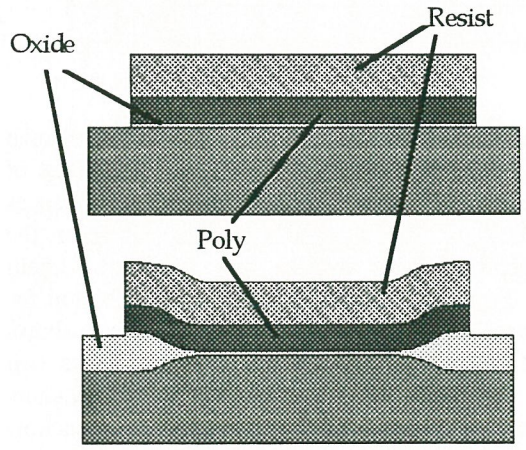
Table 1. Fitted Distribution Parameters. All values are in MV/cm. Significance levels show probability that samples are the same at the 95% confidence level.

Structure	Cap Size	Normal		Weibull		ANOVA 95% confidence
		Mean (u)	Stdev. (σ)	Scale (α)	Shape (β)	Sig. Level
POLY	Medium (10 kμm^2)	13.0	1.4	13.7	9.9	0%
SAS	Medium (10 kμm^2)	11.4	1.9	12.7	6.3	Different
POLY	Small (1 kμm^2)	11.9	2.1	13	5.2	47.3%
SAS	Small (1 kμm^2)	11.5	2.4	12.7	4.5	NOT different

Breakdown data was fitted to weibull and normal distributions. Table 1 summarizes these distribution parameters and show the ANOVA significance levels. Note that ANOVA calculation are made based on a normal distribution.

An interesting side note of these capacitors is the formation of p+/n junction diode after dielectric breakdown. The samples showed a turn on voltage of ~0.5V and a reverse breakdown voltage of -71V.

Figure 5. Capacitor cross section with and without field oxide around the electrode edges.



In addition to fabrication of capacitors with thick field oxide at the electrode edges, additional capacitors were fabricated using a sample electrode/thin oxide/substrate stack (figure 5). However, patterning the electrode was difficult since the silicon to oxide selectivity was poor and the oxide was very thin. These sample were also annealed and tested. However, testing showed an already formed diode with seemingly no dielectric between the electrodes. It is thought that the charging at the edges of the capacitor electrodes during the RIE etch may have severely damaged the oxide resulting in early oxide breakdown. Note that there was a thick field at the capacitor electrode edges on the previous tested samples. These capacitors also had one difference in processing. These electrode was etched after the BF_2 implant, while the previous sample were etched before the BF_2 implant step.

IV. CONCLUSION

Voltage ramp tests of the fabricated SAS and poly electrode capacitors show no significant differences between the two structures for small area capacitors. There does seem to be a difference for medium area capacitors, with the poly electrode capacitors displaying higher breakdown field strength. However, it is not totally clear if this due to the electrode structure or slight differences in process quality between the two wafers. In addition it was found that thick oxide around the edges of the electrode region are needed to decrease oxide damage from RIE etching.

Additional work in the way of oxide stressing, flat band voltage shift, charge trapping tests should be done on the prepared samples to further investigate differences between the SAS and poly structures. Moreover, additional samples should be prepared at thinner dielectric thickness and tested.

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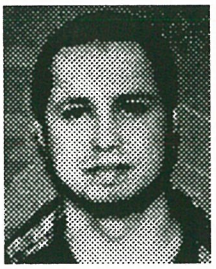

David Sanchez was born in San Gabriel, California on February 19,1974. He recived a B.S. in Microelectronic Engineering from the Rochester Institute of Technology in 1997. From 1994 to 1997 he obtained co-op assignments at such companies as SEMATECH, Rockwell Semiconductor Systems and Intel. His projects included software development for electrical data analysis, Flash memory process development and product engineering for high density flash memory. He is currently employed as a process integration engineer at WaferTech in Camas, Wa. On his freetime he enjoys jamming with other musicians, road biking, developing statistical routines in RS/1, and watching Pulp Fiction.