The Fabrication of Corrugated Silicon Surfaces

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ABSTRACT: Corrugation of silicon surfaces is desired for a variety of applications requiring availability of increased surface area and modification of optical properties of thin films. Such surfaces also prevent refractive trapping in luminescent films and can provide lambertian emissive surfaces. The objective of this research is to fabricate these corrugated silicon surfaces using a specially customized mask consisting of four different design patterns. The goal is to prove that the smallest design pattern will provide the best characteristics for enhancing the light emission of luminescent films. The surface morphology, etching process and the luminescent properties of the etched samples have been described.

I. INTRODUCTION

Silicon anisotropic etching is an important process for the fabrication of micromachined sensors and devices (pressure sensors, accelerometers, etc.). The process was first demonstrated in the early 1970's. There is a range of different solutions used in anisotropic etching, but potassium hydroxide is used for this experiment.

Potassium hydroxide or KOH etches quickly and gives a rough surface. Etching silicon involves an oxidation-reduction process, starting with the injection of holes into the silicon from the etch solution. The holes then attract the OH ions present in the etchant and oxidation occurs over the silicon surface. Silicon dissolves in the solution being one of the reactants. The reaction takes place as long as the etchants are present. Temperature also plays a major factor in the process for silicon etching.

When exposed to an etching solution such as KOH mixed with water, silicon etching takes place at different rates in different crystallographic directions. In silicon, etch rates in the <100> and <110> directions are faster than in the <111> direction because of the differences in their atomic densities. Etching along the <100> direction results in an inverse pyramidal groove which exposes (111) triangular planes.

The purpose of fabricating corrugated silicon is to help outcouple more light from phosphor thin films. Phosphors have an index of refraction of 2 or greater. Therefore, most of the light generated by the electron beam for cathodoluminscence is internally trapped. Light strikes the air-to-phosphor interface and it will experience some reflection. Figure 1 depicts this situation.

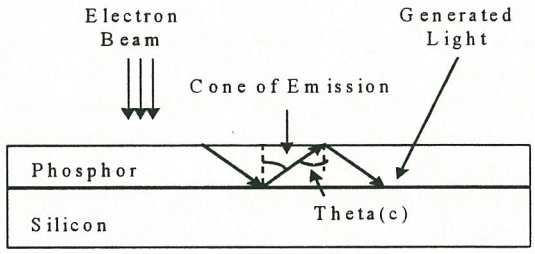

Figure 1: Internally trapped light in a phosphor film.

The light is internally reflected and is waveguided down so that the viewer can't see any light emission. The equation for reflection dependence on index of refraction is:

$$R = (n-1)^2 / (n+1)^2$$

The larger the n, the least likely for light to escape. The critical angle ($theta_c$) is defined as:

$$theta_c = \sin^{-1} (1/n_{phosphor})$$

The closer the index of refraction of the phosphor is to 1, the larger the cone of emission. One way to increase the cone of emission is to introduce corrugated surfaces. Making the surface nonplanar will result in light hitting the surface at angles less than the critical angle. The light emission becomes a function of this new $theta_c$ and a function of the size, shape and slope of the rough corrugated surface. Figure 2 displays what happens when using a rough surface.

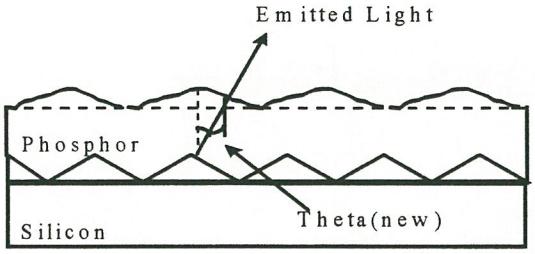

Figure 2: Emitted light with nonplanar surface.

This shows that using the corrugated silicon surfaces will increase the efficiency of luminescent phosphor thin films. Diffuse reflectance instead of specular reflectance arises with formation of rough surfaces.

II. EXPERIMENTAL PROCEDURE

With this, a job for wafer stepper GCA 6700 was implemented for the four different mask designs and fabrication of these corrugated silicon surfaces was initiated. The optical mask consisted of a series of opaque squares; each of different size for the four designs. In this report, the smallest design will be referred to where it consisted of 3μm squares separated by 5μm spaces.

The processing began with cleaning (100) oriented, p-type wafers using the standard RCA clean. A 1500Å layer of thermal oxide was grown using a 20 minute soak time in Wet O_2 at 1000°C. This oxide serves as the masking oxide for photolithography. The next processing step is to spin on positive photoresist and expose the etch pattern. After development, reactive ion etching to etch the oxide anisotropically is performed. The recipe used was: RF power of 60 watts, chamber pressure of 100 mTorr and a flow rate of 30 sccm of CF_4. Each wafer was etched for approximately 5 minutes to etch the 1500Å of oxide.

The silicon was etched crystallographically using a potassium hydroxide, isopropyl alcohol and water etchant solution. The percent volume of each was 12.5% KOH, 18.5% IPA and 69% H_2O. This solution was mixed and heated to 80°C for etching the silicon. After the silicon etch, the resist was stripped using acetone until it cleared. The final processing step is the removal of the remaining oxide using a buffered oxide etch in hydrofluoric or HF acid.

A second experiment was run to determine the difference in using an RIE etch versus a BOE etch after photolithography. A wafer was run using the same processing steps as stated except it received a BOE etch for 1.5 minutes instead of the RIE etch for 5 minutes.

III. RESULTS

Figures 3 and 4 show the change in morphology of the silicon after etching and with the deposition of tantalum zinc oxide, a phosphor film, respectively.

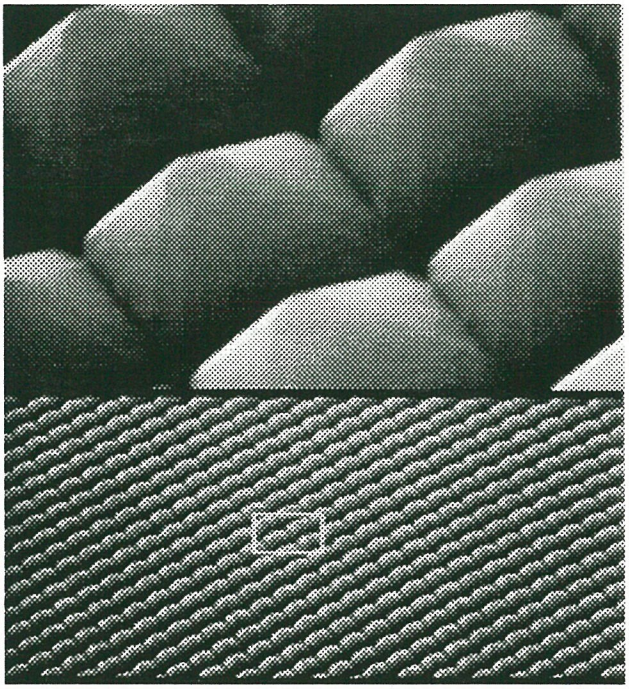

Figure 3: Corrugated silicon surfaces. Each structure has a base width of ~5μm.

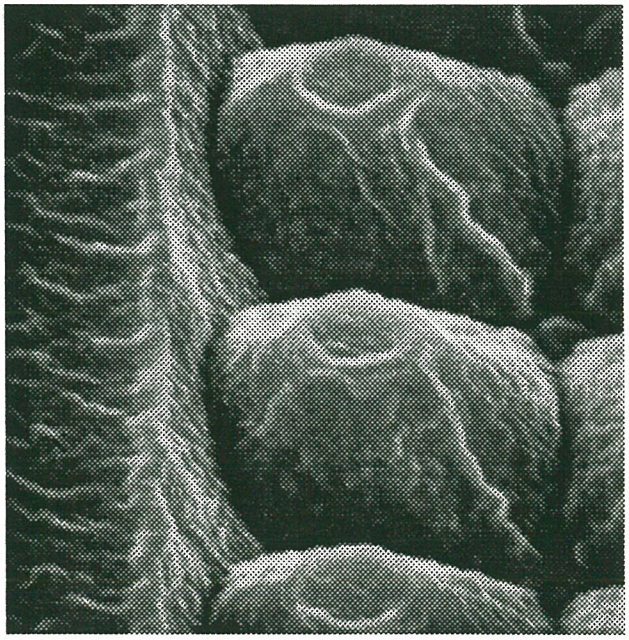

Figure 4: Structures with tantalum zinc oxide deposited.

The scanning electron micrographs are photos of the smallest mask design. A KOH etchant interacting with (100) oriented silicon wafers result in these dome-like structures. Notice the very conformal coating of the phosphor film on these structures in Figure 4. Figure 5 gives the orientation of the planes located on the pyramid.

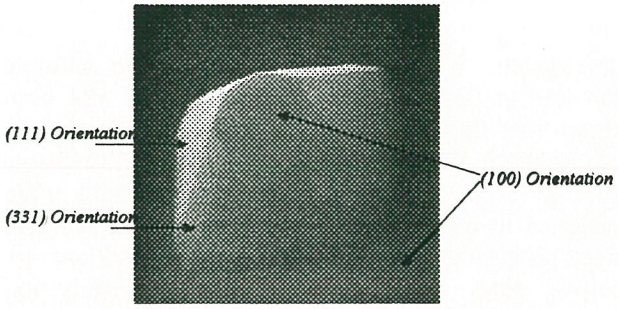

Figure 5: Orientation of corrugated silicon surface.

The (100) orientation is the original orientation of the silicon wafer. The (111) triangular surfaces emerge when using the KOH etch. Preliminary results show that the double four-fold symmetry rounding the outside corners may be (331) planes.

The experiment performed using a BOE etch rather than an RIE etch after photolithography was unsuccessful. The BOE removed all the oxide on the wafer, including the backside. Therefore, during the KOH etch, all silicon unprotected by the photoresist was etched. This gave lumpy silicon on the backside of the wafer which affected the corrugated surfaces. Also, the structures didn't fully form into the pyramid using this process.

IV. SUMMARY

In conclusion, the fabrication of corrugated silicon surfaces was successfully implemented at RIT for all four designs using the specially customized mask and the stepper job that was written. A KOH:IPA:H_2O etchant was properly mixed and used to etch the silicon wafer. Reactive ion etching in comparison to a buffered oxide etch in HF acid proved to be the better process. Preliminary results show more intensity of luminescent phosphor films with the corrugated silicon surfaces, however, further investigation is still in process.

V. ACKNOWLEDGMENTS

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VI. REFERENCES

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Alicia Bineyard is a native of Buffalo, NY. She received her B.S. in Microelectronic Engineering from the Rochester Institute of Technology in May of 1997. She has accepted a position with Motorola, Inc. in Phoenix, AZ.