Integrated Electronics for Micro-Electromechanical Devices

Michael J. Frachel
Senior Microelectronic Engineering Student
Rochester Institute of Technology
Rochester, New York 14623

Abstract - With the increased usage of micro-electromechanical devices (MEMs) today, the use and design of systems to control and monitor such devices has become increasingly important. In interests of simplifying packaging and increasing yield, the possibility of putting such control and monitoring systems on chip with the micro-electromechanical machines is suggested as an elegant solution. Simplified scaling of the micro-electromechanical machine/circuit system as one can also be a benefit of this integrated process.

This project integrates a basic n+ poly gate PMOS process with the additional steps necessary to create simple suspended polysilicon beam micro-machines. These beams can be used as accelerometers. The circuitry integrated into the design is used to measure capacitance in the Femto-farad range, and can be applicable to nearly any micro-machine that utilizes changes in capacitance for operation. While off-chip electronics are still necessary for this design to function completely, the completed process demonstrates the feasibility of a more complex version of the system for future fabrication.

A layout was designed and a specialized photomask was made to test the circuitry. This layout contains a multipurpose micro-electromechanical structure, as well as a structure specifically designed as an accelerometer. Implementation of the fabrication process occurred in the clean room at Rochester Institute of Technology.

The multipurpose structure utilized in the design can be used to test various basic properties of the polysilicon beams, including beam resonance frequency and changes in beam resistance and capacitance as a result of applied mechanical and electrostatic stresses to the beam.

I. INTRODUCTION

A MEM is a device that is built using processing techniques used in the microelectronics industry. They are usually divided into two types. Bulk MEMs machines are built with processes that utilize the substrate to form some part of the device, and thin film types, with devices built on top of the substrate. Both types of micromachines are rather large when compared to current microprocessor dimensions.

Micromachines can perform many functions, either acting alone or as part of a system. A few specific examples are sensors, such as accelerometers for airbags, pressure sensors for vacuum systems, or actual moving machines, such as springs, actuators for tiny valves, or tiny electric motors.

The one thing common to all MEMs is that they all need supporting circuitry to control them, or in the case of sensors, utilize their output. When designing and fabricating these devices, a choice has to be made whether to put the supporting circuitry on chip with the MEM device, or off chip. Integration of the electronics with the MEM device is an elegant solution that simplifies packaging and can make scaling the devices to move on to the next generation easier.

There are tradeoffs, however. The processing of such a design is more complex than either a standard MEM process or MOS process. It can also be tougher to upgrade the electronics or the MEM separately, as they were designed as a system and completely new products would have to be fabricated.

The goal of this project is to integrate a PMOS transistor fabrication process with a MEM fabrication process. This involved the design of a photomask, planning and implementation of the process, fabrication of the device and testing of the circuitry. electromechanical device with supporting on-chip electronics. The MEM device chosen for fabrication was a polysilicon beam. This beam can act as both a electrostatic actuator and accelerometer. The PMOS integrated circuit layout was intended to detect small changes in capacitance that would occur when the beam moves.

II. THEORY

A suspended beam type MEM was chosen as the basis of the MEM structure. This was done for its relative simplicity. A PMOS transistor based integrated

circuit would be incorporated into the MEM fabrication process to complete the test structure.

The MEMs structure, a simple suspended polysilicon beam, is shown in Figure 1. This figure also shows one of the PMOS transistors, as well as an electrostatic pad. The beam can be manipulated either by mechanical means, such as pushing on it with a probe, or accelerating it by mounting the completed chip on a moveable fixture.

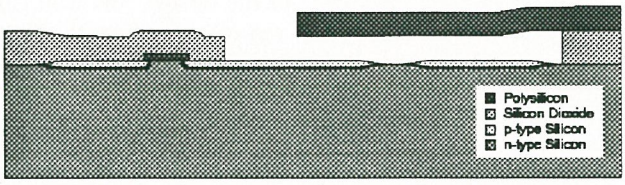

Figure 1: Example Cross Section of Test Structure

The beam can also be manipulated by electrostatic force, by charging and discharging the beam and its surroundings, such that it either is repelled or attracted from or two those surroundings, respectively.

Often, as shown in Figure 1, the beam is used as the top plate of a capacitor. Therefore, when it moves, the capacitance of the system will change proportionally to the displacement of the beam.

The relationship between the force to move the beam and its displacement are shown in the Equation 1.

Equation 1

$$)d = \frac{F * 12 * L^3}{3*E*b*h^3}$$

Where:
)d = Displacement
F = Force applied to beam (newtons)
E = Young's Modulus (1.9e11 newtons/meters^2 for Si)
b = Width of beam (meters)
h = Height of beam (meters)
L = Length of beam (meters)

This displacement causes a change in capacitance of the system. The change in that capacitance caused by the change in displacement is shown in Equation 2. As seen from the relationship, the capacitance of the system can either increase or decrease depending on the direction of deflection of the beam.

Equation 2

$$)C = \frac{g_o g_r A}{)d}$$

Where:
)C = Change in capacitance (coulombs)
)d = Displacement of beam
A = Area of beam that overhangs implanted capacitor region
g_o = Permitivitty of free space
g_r = 1 (relative permitivitty of air)

When force is applied to the beam, more occurs than simple displacement. The amount of stress in the beam, measured in dynes, also changes. This stress can be quantified by measuring the amount that the resistance of the beam changes. This is referred to as piezo resistance. The amount this resistance changes is defined by a piezo resistivity coefficient, A, which is typically 10^{-10} cm/dyne. The fractional change in resistance is determined by the Equation 2.

Equation 2:

$$)R/R = AF$$

Where:
)R = Change in resistance (ohms)
R = Initial resistance (ohms)
A = Piezo resistivity coefficient (10^{-10} cm/dyne)
F = Stress (dynes)

In the interest of maximizing the chances for success, the integrated electronic contained within the test structure were kept simple. As a result of this, some off-chip supporting electronics were required for operation of the test structure. The testing scheme that would detect the minute changes in capacitance that moving the beam requires a two phase non-overlapping clock. An example of the output of a circuit that produces the two phase non-overlapping clock, with a given clocked input, is shown in Figure 2.

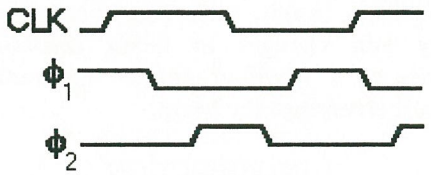

Figure 2: Two phase non-overlapping clock

The layout of the off-chip circuit is shown in Figure 3. This design is called a cross coupled latch. The circuit was built from TTL logic and tested separately.

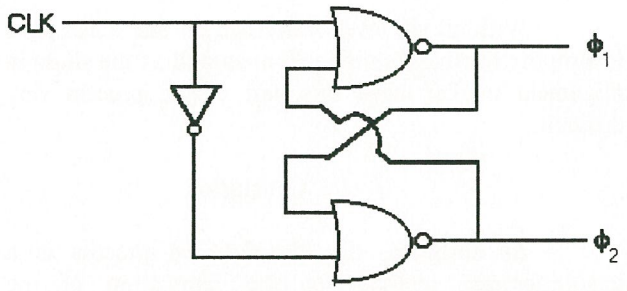

Figure 3: Layout of two phase non-overlapping clock

The final layout of the test structure has 12 input/output pads and four transistors. The pads are defined in Table 1. The beam is separated from the support circuitry such that it can be independently biased for electrostatic movement or piezo-resistance tests. M1 and M2 are required to bias the beam as an electrostatic device, which can require high voltages, while keeping the other electronics intact. A complete schematic is shown in Figure 4.

Pad	Purpose
A1	Ammeter 1
A2	Ammeter 2
N 1	Clock 1
N 2	Clock 2
B1-B4	Beam Contacts
M1, M2	Actuator Contacts
GND	Ground pads

Table 1: Contact Pad Definitions

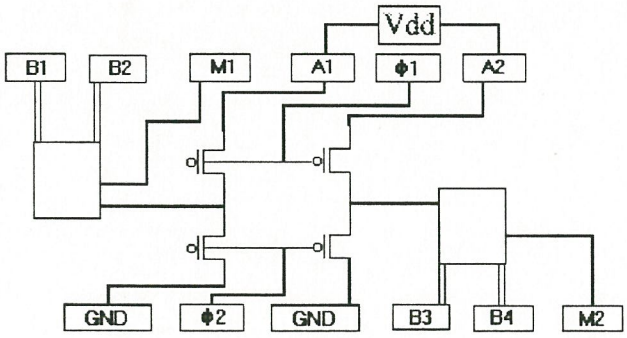

Figure 4: Schematic of Test Structure

Operation of the test structure is as follows for testing as a capacitive device. The N1 and N2 pads, as well as the both ammeter pads are used. The beam to be tested is grounded.

As the two non-overlapping clocks are applied to N1 and N2, the difference current in both ammeters is noted. This difference is then used to calculate the capacitance that is measured. This relationship is shown in Equation 3.

Equation 3: Current and Capacitance relationship

$$I_{net} = C * V_{dd} * f$$

Where:
$I_{net} = |I1 - I2|$
f = Frequency of clock source
C = Capacitance of interest

III. PROCESS

Step #	Process
1	Pad Oxide Growth
2	LOCOS Nitride
*3	Active Photo
4	Nitride etch
5	Strip Photoresist
6	RCA Clean
7	Field Oxide (FOX) growth
8	Strip LOCOS nitride
9	Wet etch PADOX
10	KOOI oxide growth
11	PMOS Vt adjust (blanket)
12	Etch KOOI
13	RCA Clean
14	Grow Gate Oxide
15	Poly deposition 1
16	Poly dope (SOG application and anneal)
*17	Pattern Polysilicon 1
18	Etch Polysilicon 1
19	Strip Photoresist
20	P+ D/S implant
21	Low temp oxide passivation (thermal)
22	Thick LTO deposition
23	Poly 2 deposition (thick)
24	Poly 2 Dope (SOG application and anneal)
*25	Poly 2 Photo
26	Poly 2 etch
27	Photoresist strip
*28	Contact Cut Photo
29	Contact Cut etch (oxide)
30	Photoresist Strip
31	RCA Clean
32	Metal deposition
*33	Metal Photo
34	Metal Etch
*35	Release Photo
36	Release etch in BOE
37	Strip Photoresist

Table 2: Process Flow

The fabrication process was designed such that the PMOS transistors would be completed first. After completion, they would then be passivated with 2 micron of oxide, then a 2 micron thick polysilicon beam would be fabricated and incorporated into the circuit.

The complete 37 step process is shown in Table 2. Since the beams are deposited directly on top of the oxide, this oxide layer would also act as a sacrificial layer for the release of the beams.

The Release step, #36, is done in fresh buffered oxide etch, because it has been shown to have a higher selectivity to polysilicon than older, used etchant.[2] This is important, as the release step can last several hours until the oxide underneath the beams is etched away laterally, leaving a polysilicon beam suspended in air. The photomask for this step was designed such that windows that expose only the beams are opened. This eliminates the need for a step that would anchor the beams to the substrate, which would introduce more topology. The MEM fabrication process, with its relatively thick layers, as opposed to the normally thinner layers in device fabrication, can introduce problems with severe topology.

Another concern was the alignment marks from layer to layer being blurred away. The layout was designed with several to cope with this possibility. This introduced problems in programming the photo-stepper.

With all six levels patterned on one mask plate to simplify the mask's production, as well as the shifts in alignment marks, made this part of the process very difficult.

IV. Conclusion

As designed, the PMOS/MEM process is a straightforward method for the fabrication of the integrated electronics test structure. Due to delays in fabrication of the mask, the PMOS/MEM fabrication process for the test structures was not completed. Once completed, demonstrating that the process will work, more complex circuits can be designed for more capable test structures. The two non- overlapping phase clock generator, however, was completed and functioned as expected.

References:

[1] A Simple On-chip, Sub-Femto Farad Interconnect Capacitance Measurement, IEEE Electron Device Letters, Volume 18, No. 1, January 1997

[2]New Method of Purification of HF Chemicals for Very Large Scale Integration Manufacturing, Journal of the Electrochemical Society, Volume 143, No. 12, December 1996