

The IRIS Project: CCD's, Image Recognition, and All That Jazz

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Abstract— The Identity Recognition and Imaging System (IRIS) Project was initiated to explore the fabrication and integration of a CCD imaging array into a complete image recognition system. Such a system has now been realized in part, and consists of an surface-channel 64-by-64 pixel CCD array, external driver circuitry, data acquisition board, and a Win95-based PC running a custom pattern recognition software package called TALONir.

I. INTRODUCTION

A charge-coupled device (CCD) is quite simply a series of overlapping MOS capacitors which can be biased in sequence to transport charge packets through the semiconductor bulk. A surface-channel CCD transports *minority* carriers through a potential minimum located at the oxide-silicon interface. A buried-channel CCD (BCCD) differs from a surface channel CCD (SCCD) in that it transports *majority* carriers through the substrate at a potential minimum.

Image recognition using a CCD involves creating the driver/interface circuitry and integrating it with pattern analysis software or firmware which performs the classification. The driver circuitry must be robust enough to provide significant current to overcome the high coupling capacitances seen at the CCD gates. Additionally, it must be able to read-out all of the cells in a time-frame small enough such that significant signal degradation does not occur. The pattern analysis software used must have a high level of noise immunity, and be capable of generalization over a broad range of light levels and object orientations.

II. CCD LAYOUT AND PROCESS DEVELOPMENT

Several attempts have been made to make working CCD's at RIT in the past. These have yielded limited success due to a variety of process, design and time constraint issues [1] [2] [3].

It was decided that this project would part from former efforts and create a new chip design and fabrication process. Figure 1 is the completed CCD design which consists of a 64-by-64 pixel CCD imaging array, two linear arrays, and various test structures. The clocking

arrangement chosen consists of three overlapping phases. The maskset layout which was designed by George Lungu consists of six levels aligned on a single quartz plate. A defect was noted in the mask design in that all of the metal pads along one side of the die were cropped too closely and

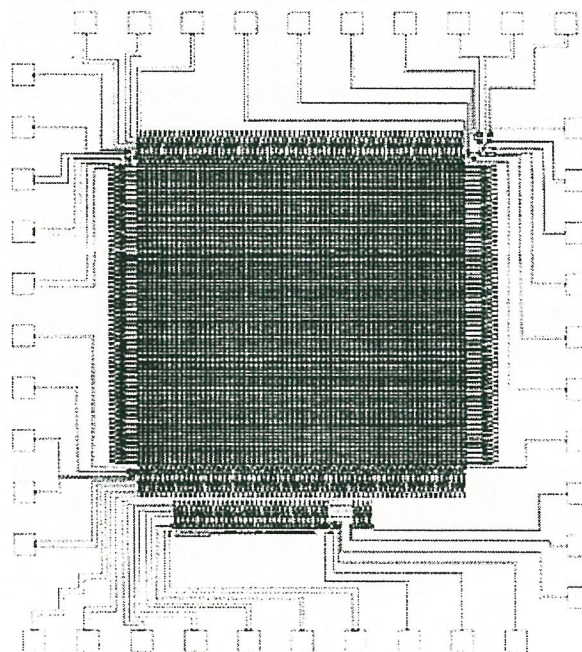


Figure 1. A schematic of the CCD chip design layout.

became shorted together. This can be solved in the short-term by slicing the aluminum pads free with a sharp modeling knife and a steady hand. Two poly1 and poly2 bridging defects were found in the final mask as well due to undeveloped photoresist protecting the chrome during etching. It is quite possible that the shorted poly gates can be "blown" like fuses commonly used in PLA's.

The developed process consists of 54 steps which includes RIT's established LOCOS sequence for channel-stop isolation. The starting substrate is a p-type <100> oriented wafer. Unlike the surface-channel CCD wafers, buried channel devices receive a blanket n- phosphorus channel implant before LOCOS channel-stop formation. Following LOCOS, Gox1 is grown and 200nm of poly1 is deposited, doped and patterned. Next, a wet etch is done to

remove the exposed gate oxide and a new gate oxide is grown. 200nm of poly2 is deposited, doped and patterned and a wet etch is done to clear the source/drain regions. A blanket n+ self-aligned source/drain implant is now performed. The p+ contacts to the substrate are then patterned, etched, and implanted with boron. 400nm of LTO is now CVD deposited on the wafers and contact cuts are patterned and etched. Finally, aluminum is deposited, patterned, and sintered, completing the design.

The process was created and modeled with TMA SUPREM4 and MEDICI. Process monitoring was accomplished by using several control wafers and device wafer test sites. No major process deviations from target values were observed.

Final wafer cross-sections were performed using an Hitachi SEM to inspect for defects in thin film integrity. LTO deposition was observed to be of a grainy consistency, but no pinholes were observed. The thin polysilicon films contained some voids, but were conformal over the active/field transitions and were without cracks. Some gate oxide thinning at the edges suggests that remnants of the LOCOS nitride "white ribbon" remained despite the Kooi sacrificial oxide sequence.

III. CCD DEVICE PERFORMANCE

Capacitive-breakdown tests of test structures created just after LOCOS revealed a critical field of 13 MV/cm² for 50nm oxides and 9 MV/cm² for 100nm oxides. Breakdown stress tests between adjacent phases in the CCD

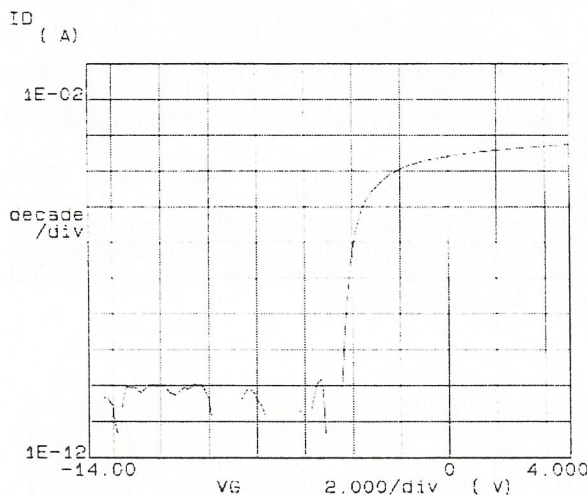


Figure 2. A typical SCCD Id Versus Vgs Curve

array revealed a significantly less 4 MV/cm² breakdown strength. The difference is probably due to the electrically weaker and uneven surfaces where poly1 and poly2 overlap. Sharp points provide local regions where electric field intensity is higher than over planar regions.

The buried-channel transistor devices were shown to be very leaky with an off-state current in the high nanoamp range. This is most likely due to the channel junction being too deep, making it difficult for gate action to adequately turn-off the devices. Moving the blanket channel implant to just after LOCOS would have solved this problem.

The surface-channel transistors, however, performed adequately. Figure 2 illustrates a typical Id versus Vgs curve. The off-state leakage current was a respectable 10pA, and the on-state drive current at 0V Vgs (these are depletion-mode devices) was 80uA. Interestingly, the threshold voltage differed significantly between poly1 and poly2. The Vt of poly2 was -2.5V and poly1 was -4.0v. Gate oxide thickness variation can only account for a small percentage of the Vt difference observed. A plausible theory is that excess dopants diffused through the gate oxide from poly1, shifting the Vt of the cell in the negative direction. A contamination experiment was performed to verify this, and revealed that dopants were indeed migrating to the substrate in significant numbers. The surface concentration of arsenic and phosphorus contaminants (using SUPREM4 analysis and empirical results) was calculated to be about 1e15/cm³. This concentration is nearly enough to counterdope the background concentration of the wafers. A solution to diminish the effects of this dopant migration in the future might be to either increase the polysilicon thickness, decrease its dopant predeposition time, and/or perform a low-level boron blanket Vt adjust implant before processing SCCD wafers.

Although the SCCD transistors performed adequately, charge transfer in the linear or area arrays has not conclusively been demonstrated.

IV. THE CCD DRIVER AND CONTROL CIRCUITRY

Testing the CCD array is somewhat of an art form. Not only is one concerned with the creation of a three-phase overlapping clock signal driver with strong buffers at the outputs, but that detecting of a valid output signal from the array is distorted with electrical noise. There were two driver circuit configurations constructed for this project. The first circuit contained op-amp switches which were driven by a PC through a data acquisition board created by Ontrak Control Systems, the ADR101. Waveforms were created in the Qbasic or C++ languages and sent to the board via a serial connection. This format was good in that it allowed for the greatest amount of development flexibility and an ultimately reduced development time. Unfortunately, this arrangement was rather slow, having a minimum pulse width of 10ms, for a maximum frequency of 50 Hz. This restriction is imposed by the serial connection bottleneck, not the microprocessor speed. The input signal fed op-amps in a schmitt-trigger arrangement which served to toggle between two voltage rails, 0V and -10V. This

output driver operates adequately up to a maximum frequency of 10 kHz.

To overcome the 50 Hz speed barrier, a new circuit was built for testing purposes which consisted of an oscillator, a counter, TTL logic circuitry to generate the three phases, and a high-speed TTL output buffer to toggle between the voltage rails. This circuit operates up to frequencies of 200 kHz with a tolerable level of output distortion.

V. IMAGE RECOGNITION WITH TALONir

Aside from the creation of a working CCD, part two of the IRIS project has been to explore the use of CCD's in conjunction with "intelligent" pattern recognition models. One such model that was chosen for this project is called the holographic neural method. [4] A software package called TALONir was written in the "C" language which successfully implemented the holographic learning and recall algorithms.

The holographic neural method operates on the principle that stimulus/response pairs can be directly mapped onto a correlation matrix composed of complex numbers. Analog information is represented internally as having both a magnitude (confidence level) and a phase orientation. A linear or gaussian transformation of unbounded real data to bounded complex values before processing makes this internal structure possible. The

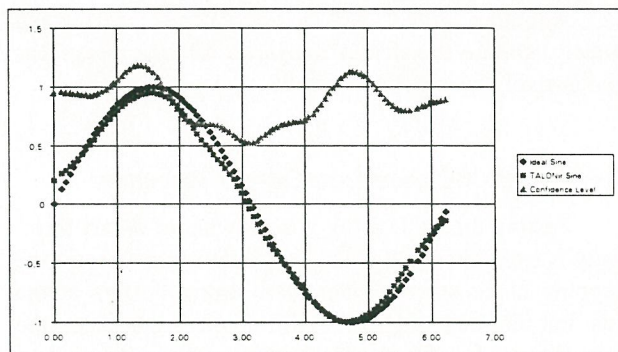


Figure 3. Recall of a sine function.

learning of new patterns involves "enfolding" these complex stimulus/response pairs directly over previously learned patterns with a method of vector multiplication. This design exhibits rapid learning with a strong propensity for dense pattern storage and functional generalization of highly non-linear relationships.

Three separate tests were performed to validate TALONir as a recognition instrument. The first test done was to teach the network a basic sine wave function and have it regurgitate the proper response. Figure 3 illustrates the recall of this simple sine function. TALONir can be seen to model this sine wave quite well. The second test performed was to teach the network empirical data gathered

from a resist characterization experiment and have it find the main effect variables and higher-order interactions. TALONir was able to identify these causal relationships equally as well as ANOVA analysis done in parallel. The last test done was to teach the network the alphabet using a two-dimensional binary mask of 25 pixels and measure its recall error as a function of stimulus noise. TALONir was shown to have a noise immunity of up to 25%.

TALONir has since been augmented with the capability to do basic image processing operations which clean up a noisy image field and further simplify the data being input to the network. These additions should be able to keep noise levels to below the 25% threshold.

VI. CONCLUSIONS AND FUTURE WORK

The components for a complete image recognition system were created and demonstrated. Pattern analysis with TALONir has shown to perform well with small and medium-sized datasets. This suggests that larger dataset analysis such as complex image fields is well within reach. Although SCCD transistors performed adequately, electrically-injected charge transfer was not conclusively demonstrated. It is suspected that the sensing circuitry used contains a great deal of noise which makes extracting a valid signal exceedingly difficult. Other avenues for noise suppression such as cooling the wafer to reduce phonon interaction should be investigated before any major process or design changes be implemented.

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Abram Detofsky received his BS in Microelectronics from the Rochester Institute of Technology in 1997. Past work experiences include several design, reliability, and high-volume manufacturing internships with Intel Corporation. His pioneering work with reliability monitoring earned him Intel's Q4 1995 CMD Divisional Recognition Award. His multidisciplinary research interests include device physics, process integration, artificial intelligence, and brewing the perfect cup of coffee. He is currently pursuing an advanced degree in optical computing at the University of Arizona and hopes to be a driving force in semiconductor research and development in the very near future.

