Pinched Diodes

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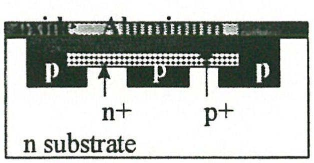
Abstract- While applications for diodes operating under forward bias have been researched extensively, the useful application in reverse bias mode is relatively unexplored. Resistance modulation in avalanche mode offers new possibility for utilization. The purpose of this experiment is to characterize a diode utilizing a differential negative resistance (DNR) scheme showing a decrease in current with an increase in voltage.

I. INTRODUCTION

A pinched diode consists of a p+n+ junction in parallel with and bounded on its circumference by a less heavily doped pn junction. As the reverse bias is applied to both junctions, the space charge region of the more lightly doped junction widens, constricting the current carrying breakdown region of the p+n+ diode. The space charge region is the region on either side of the metallurgical junction in which there is a net charge density due to ionized donors in the n-region and ionized acceptors in the p-region[1].

The pinched diode fabricated in this study has two metallurgical junctions, a p+n+ junction that is heavily doped and a pn junction that is lightly doped on both sides of the metallurgical junction. The heavily doped p+ layer is built on top of the n+ layer, overlaying two concentric lightly doped p-regions, with all three layers concatenating to a lightly doped n-substrate. The cross section and top view of this structure are shown in Figure 1a and 1b, respectively.



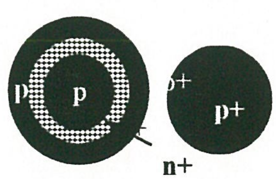


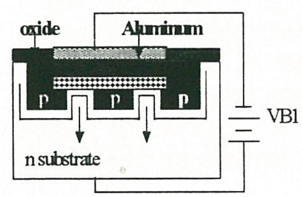
Figure 1a: cross section Figure 1b: top view

where p+ is aligned

on top of p and n+

II. THEORY

When a reverse-bias voltage is applied to the structure shown in Figure 1, the heavily doped p+n+ junction begins to breakdown and the reverse bias current is generated. As the reverse-bias voltage is increased the space charge region of the pn junction will extend resulting in a decreased current. A situation may reach when the space charge regions will merge causing a pinch off as illustrated in Figure 2(a,b).



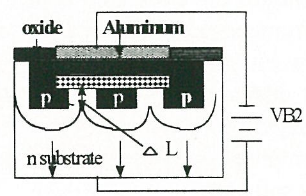


Figure 2a:
Figure 2b:
VB1 of heavily doped VB2 of
lightly doped

If the electric field in the pinch off region reduces below the critical field for the p+n+ junction (Fig.3), the avalanche current will ideally drop to zero. Further increase in reverse voltage will eventually approach the breakdown voltage of the pn junction and the current will rise suddenly. It is noticed that between the two breakdown voltages, there may be a differential negative resistance regime if the device design is optimized as shown in Figure 4.

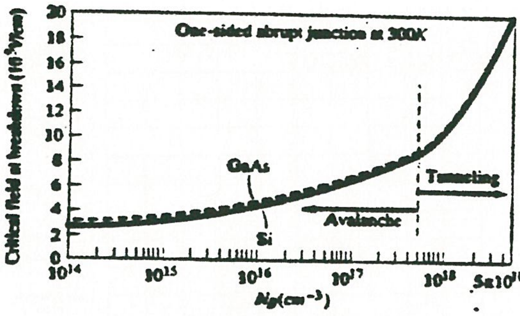


Figure 3: Critical electric field at breakdown in a one-sided junction as a function of impurity doping concentration.

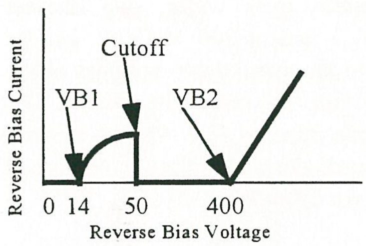


Figure 4. IV Characrteristic

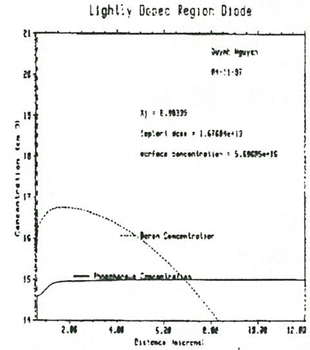
The breakdown voltage in an asymmetric diode is primarily controlled by doping of the lightly doped region.[1] The avalanche breakdown process occurs when electrons and/or holes, moving across the space charge region, acquire sufficient energy from the electric field to create electron-hole pairs by colliding with atomic electrons in the space charge region.[1] From TMA SUPREM simulation tool, with chosen implant dose and energy, surface and junction doping concentration have been simulated. Breakdown voltage can be determined using equation 1.

$$V_B = \frac{\varepsilon_s E^2_{crit}}{2qN_B} \qquad (1)$$

Where N_B is the semiconductor doping in the low-doping region of the one sided junction. The critical electric field (E_{crit}), plotted in Figure 3, is a slight function of doping.[1]

III. DESIGN AN D SIMULATION

For the lightly doped region, the junction concentration is at 1e15 cm-3 which has a breakdown voltage at 300 volts. For the heavily doped region, the junction concentration is 1E17 cm-3 which has a breakdown voltage at 14 volts. See Figure 5a and 5b.



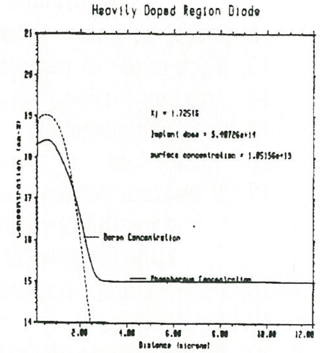


Figure 5a. Concentration at the lightly doped region.

Figure 5b: Concentration at the heavily doped region.

The mask is designed such that the diodes are cylindrical and are isolated from each others. Twenty different sizes of diodes have been designed on the same mask to look for pinch off condition. Figure 6 shows the top view of the mask layout.

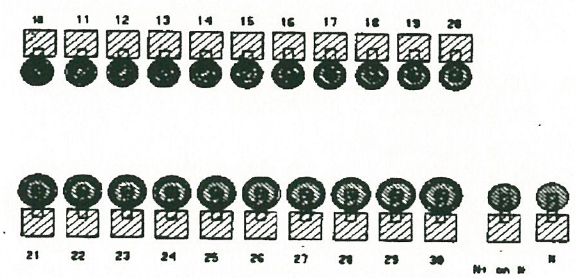


Figure 6: Mask Layout.

IV. EXPERIMENTAL PROCEDURE

1. RCA Clean.
2. Growth Masking Oxide (5000 Å), 48 minutes, WetO2, 1100 °C.
3. Coat Photoresist.
4. Etch oxide on back (5 minutes).
5. Strip Photoresist on front .
6. Deposit Spin on Dopant N250 on back for good contact.
7. Diffusion Drive-in
   15 minutes in N2 1050 °C
   15 minutes in O2 1050 °C.

Etch all the Oxide.

1. RCA Clean.
2. Growth oxide for p-well (5000 Å)

48 minutes, WetO2, 1100 °C.

12. Level 1 Photo - Mask 1 - p-well.
13. Etch oxide (5 minutes).
14. Implant p-type (80KeV, B11, 1E14).
15. Strip Photoresist.
16. RCA Clean.
17. P Implant Anneal
    6 hr. in N2 1100 °C
    30 hr. in DryO2 1100 °C.
18. Etch oxide (5 minutes).
19. RCA Clean.
20. Growth oxide (3000Å)
    18 minutes in WetO2, 1100 °C.
21. Level 2 Photo - Mask 2 - N+
22. Etch oxide
23. Implant N+
    (100KeV, P31, varied dose from 8E14, 9E14, 1E15, 2E15).
24. Strip Photoresist.
25. RCA Clean
26. N+ Implant Anneal (60 minutes in N2 1100 °C)
27. Level 3 Photo - Mask 2 - P+
28. Implant P+ (50KeV, BF2, 2.3E15).
29. RCA Clean
30. P+ Anneal
    45 minutes in N2 1100 °C
    30 minutes in O2 1100 °C.
31. Level 4 Photo - Mask 2 - Contact.
32. Etch Contact.
33. Strip Photoresist.
34. RCA Clean.
35. Deposit Aluminum (6000 Å).
36. Level 5 Photo - Mask 4 - Metal one.
37. Aluminum Etch (2 minutes).
38. Strip Photoresist
39. Sinter (25 minutes in H2N2 450 °C)
40. Test.

V. RESULTS AND DISCUSSION

The fabricated diodes show different breakdown voltages in different regions. When n+-channel is too narrow, the diode is in cutoff mode, and the p+n+ diode breakdown is not observed before the pn diode breaks down at 300 volts. Figure 7 shows the reverse I-V characteristics of diode number 10

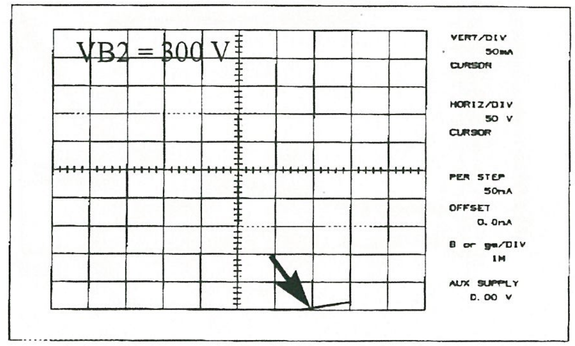


Figure 7. I-V_R characteristics of diode number 10.

As the diode geometry gets wider, two distinct breakdowns at 12 V (V_{B1}) and at 300 V (V_{B2}), can be observed corresponding to the breakdown voltages of the two parallel diodes. Figure 8 shows the reverse I-V characteristics of the diode number 30 (?). A current saturation and not current cut-off regime is obtained between the two breakdown conditions.

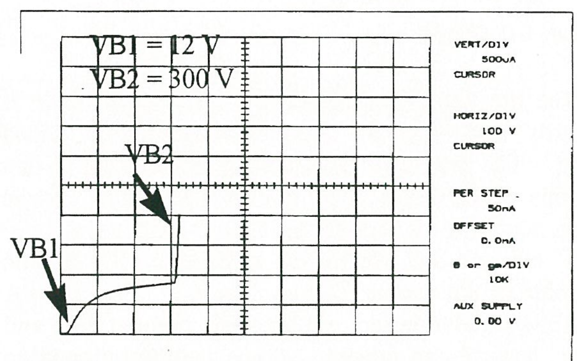


Figure 8. I-V_R characteristics of diode number 30.

For diode geometries in between these two extremes, for instance, diode number 16, the I-V_R curve shows a 'kink' and not a cut-off at 14 V (2V beyond V_{B1}). See Figure 9.

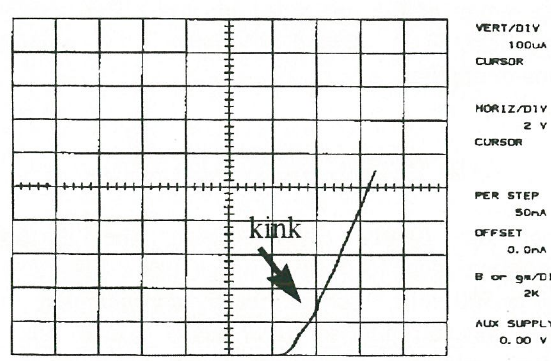


Figure 9. I-V_R characteristics of diode number 16.

The diode has not completely shown the sign of pinch off perhaps due to the effect of the junction depth of the pn junction. If the pn junction is not deep enough, the space charge region will merge closer to the p+n+ region sustaining the critical electric field causing a continuous current flow as observed. If the pn junction is deep enough to allow pinch off further away (ΔL from Figure 2b is increased), the field may drop below the critical field which may result in a cut-off. Extensive 2-D modeling is required to determine the appropriate design.

VI. CONCLUSION

A new structure referred to as 'Pinched diode' has been proposed. The pinched diodes with different geometries have been designed and fabricated. Absolute pinch off has not been observed. However, a current saturation regime is observed. Further work is required in diode modeling , design and simulation.

VII. ACKNOWLEDGES

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VIII. REFERENCES

[1]Neamen, Donald A. Semiconductor Physics and Devices: Basic Principles. Richard D. Irwin, inc., 1992.