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Development of a Monolithically Integrated GaN Nanowire Memory Device

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by

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Finally, I would like to thank my parents and sister for their love, help and support throughout my life.

Abstract

Gallium nitride (GaN) devices are of particular interest for a variety of fields and application spaces. The materials properties of GaN make it an ideal semiconductor for electronics and optoelectronics. Within electronics, GaN is of great interest for high-power and high-frequency electronics. Within optoelectronics, GaN has enabled efficient lighting and continues to be scaled for augmented reality and virtual reality (AR/VR) application spaces through the realization of micro-LEDs. In scaling such devices for incorporation into larger systems that span multiple fields, monolithically integrating other devices and components would provide greater flexibility and improve system-level performance. One such avenue for explored here is the development and integration of a GaN-based memory device with a light-emitting diode (LED). Specifically, a nanowire memory device integrated vertically with an LED.

Initial work involved developing and verifying a high-κ dielectric memory stack on Si for memory characteristics. This was followed by fabrication of the integrated memory device and LED on a green LED GaN-on-sapphire substrate through a top-down approach. Initial electrical testing showed a functional, blue-shifted LED and the existence of a 2.5V memory window for a +/-10V program/erase window. Finally, a new self-limiting etch technique was examined to address possibilities for further scaling nanowires.

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1. Introduction

1.1 Gallium Nitride

Gallium nitride (GaN) is a III-V semiconductor, combining Ga from Group III of the periodic table with N from Group V of the periodic table. GaN has a number of material properties that lends itself to be used in a wide variety of application spaces within the semiconductor industry. It is a direct, wide bandgap semiconductor with an energy gap of 3.4 eV. This enables the use of GaN extensively in optoelectronic applications and in high-power applications as well. Directly utilizing the Planck-Einstein relationship with the bandgap value previously mentioned, it can be seen that GaN would emit at a wavelength of 365nm (within the UV range). This wavelength of emission has enabled GaN as the primary material system to fabricate emitters such as Light Emitting Diodes (LEDs) and laser sources.

While GaN wafers cannot be manufactured in methods that are more commonly utilized for crystalline Si, it can be produced through epitaxial crystal growth. This involves typically utilizing a substrate with a relatively similar lattice constant and growing subsequent layers of GaN through metal organic chemical vapor deposition (MOCVD) or molecular beam epitaxy (MBE) techniques. Most common substrate materials for GaN growth are Al_2O_3, SiC, Si, as well as free-standing GaN templates (GaN-on-GaN growth). During epitaxial growth, other elements can also be incorporated to produce ternary compounds. For the GaN material system, typical ternary compounds are InGaN or AlGaN with the ability to vary compositions of the additive elements. Epitaxial growth with the incorporation of ternary compounds provides an extra degree of freedom

in being able to directly tune the bandgap of the semiconductors based on the composition. Figure 1.1 shows the lattice constant against bandgap of GaN in relation to InN and AlN.

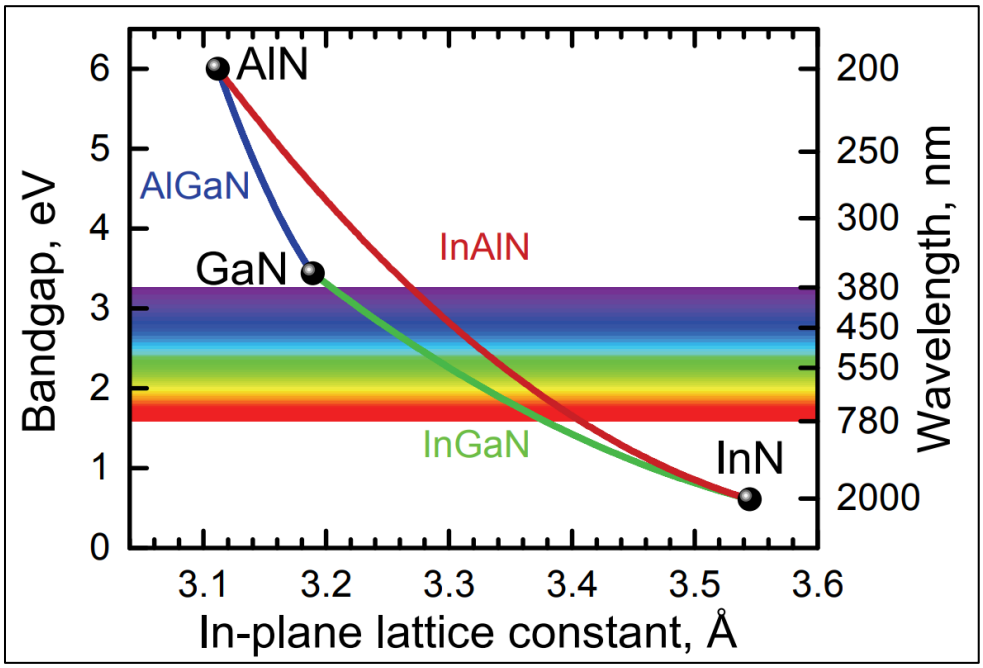


Figure 1.1: Lattice Constant vs Bandgap for GaN, InGaN and AlGaN [1]

Table 1.1 shows material properties of GaN. GaN has a Wurtzite crystal structure. It is also extremely hard as a material (refer Knoop hardness) with a fairly high thermal conductivity and high heat capacity. These properties have enabled GaN to be utilized for high-power and high-frequency devices.

Table 1.1: Material and Electrical Properties of GaN

Property	Detail
Band Gap	3.4 eV
Band Gap Type	Direct
Crystal Structure	Wurtzite, Zinc Blende
Lattice Constant	a = 3.186 Å, c = 5.186 Å
Electron Mobility	$\leq 1000\ cm^2\ V^{-1}\ s^{-1}$
Hole Mobility	$\leq 350\ cm^2\ V^{-1}\ s^{-1}$
Thermal Conductivity	$1.3\ W\ cm^{-1}\ °C^{-1}$
Surface Microhardness (Knoop Hardness)	$1200\text{-}1700\ kg\ mm^{-2}$

1.2 Scaling

Scaling has played and continues to play a major role in the continual advancement of the semiconductor industry. In keeping up with Moore's law, where the number of transistors per chip double every 12-18 months, devices have moved from planar structures to FinFETs for higher resolution. Figure 1.2 shows a projection of future scaling as published in 2020 by IEEE within the International Roadmap for Devices and Systems (IRDS): More Moore report. The outlook of modern devices as projected within the report suggests that FinFET technology would be viable and sustain till 2025 with a transition in development work estimated around 2022 to enable lateral gate-all-around (GAA) FETs and further development towards vertical GAA FETs beyond that point. [2]

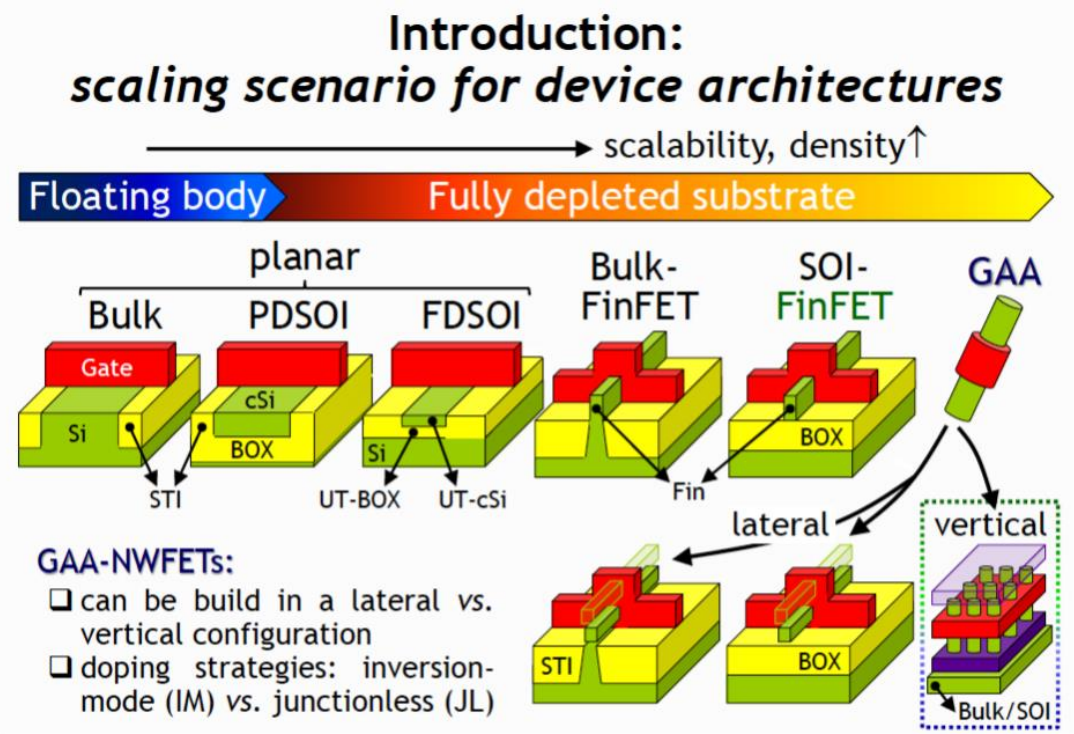


Figure MM-4 Planar to GAA transition [11].

Figure 1.2: Scaling projection according to IEEE-IRDS More Moore Report 2020 [2]

Figure 1.3 shows an earlier projection in scaling as projected and presented by the Interuniversity Microelectronics Centre (IMEC) in 2015. [3] The logic device roadmap projects the movement towards GAA vertical nanowire structures in both scenarios and cases.

Both roadmaps show the need to move towards vertical nanowire structures as a method to enable further scaling within the semiconductor industry

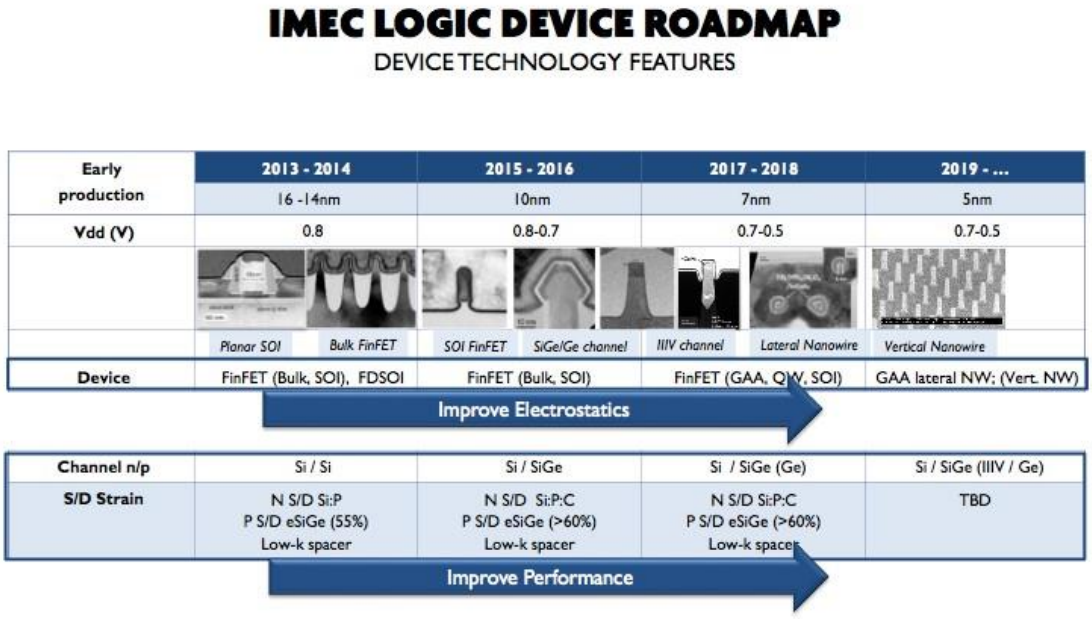


Figure 1.3: IMEC Logic Device Roadmap – Scaling towards vertical nanowire FETs [3]

1.3 Monolithic Integration

A key area of work within the semiconductor industry has been to integrate multiple functional modules all onto the same chip. This provides a means to reduce overall manufacturing costs while also improving system level performance with reductions in overall power consumption and system-level delays. A trade-off here is the increased complexity in fabrication and processing as well as the need for better device and system level design when considering monolithic integration.

1.4 Motivation and Goals

It is clear therefore that vertical, gate-all-around devices show promise for future devices. Integrating such devices monolithically provides increased performance gains and is of great interest for future technology nodes and generations. GaN, with its unique material properties, also provides several advantages in looking towards vertical, nanoscale devices. Exploring and developing novel integration schemes and developing unique devices with GaN provides promise in pushing technology forward.

The main motivation and goal, for the rest of this thesis, is to explore and develop a unique and novel flash memory device with GaN. Specifically, a vertical GaN nanowire memory device monolithically integrated with an LED.

2. Background

GaN devices cover a gamut of application spaces. These include electronic and optoelectronic devices. Within optoelectronic devices, GaN has been the key material system in providing highly efficient LEDs. The realization of highly efficient blue LEDs enabled the possibility of white LEDs for commercial lighting applications. Further development of GaN LEDs, and work towards scaling them has facilitated the development of LED displays. Scaling down further has opened new application spaces moving towards micro-LED devices and displays. AR/VR technology are front-runners within the possible application spaces for micro-LED devices.

Prior work has shown the ability to fabricate GaN nanowires to then form GaN nanowire devices.[4] These include LEDs and FETs as well. Published work has also shown GaN LEDs fabricated in series with a transistor.[5]–[7] This integration scheme allows a unique integrated approach for addressing GaN LEDs with associated driver circuitry. In order to make LED displays and arrays, the LEDs would need to be arranged in an orderly manner and be individually addressable. Actively addressable arrays are achieved through driver circuitry associated with every LED.[8]–[10] There are multiple addressing schemes that have been utilized within modern products and systems. Control of the LED switched on or off within a matrix (an array of LEDs) is provided through the driver FET. Along with the driver FET, a storage capacitor is also utilized to hold and sustain a pixel's value through holding the voltage on the driver FET's gate. The charge sustained on the capacitor would need to be refreshed periodically in order to keep the LED on. In

low-refresh rate displays, this would mean a periodic cycling and constant need to charge up the storage capacitor to keep the LED on.

Figure 2.1 shows a typical 2 transistor, 1 capacitor configuration for an active LED matrix. As shown in the circuit schematic, the storage capacitor ensures the gate is held high when it is charged up. Over a period of time, the charge storage capacitor would also leak charge, losing it through the switching FET. The presence of a leakage pathway would mean the charge storage capacitor would need be recharged on a fixed clock cycle to maintain and keep the LED on.

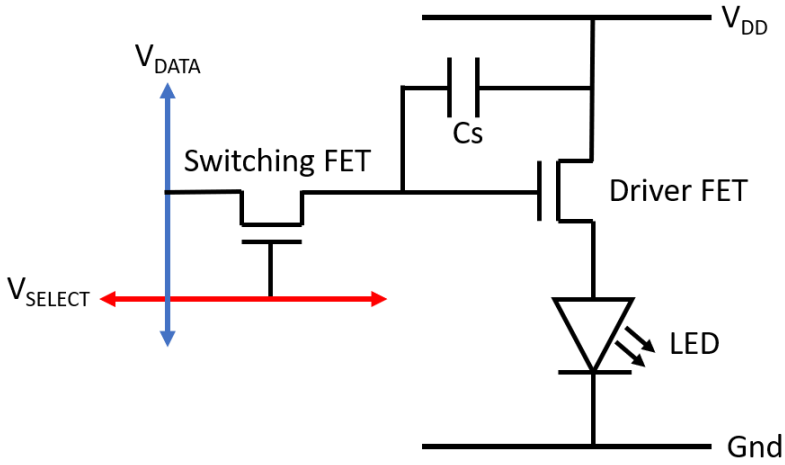


Figure 2.1: 2 transistor, 1 capacitor circuit for active matrix displays

To address this short-coming, literature has shown utilizing a possible memory device for the driver thin film transistor (TFT) to hold a value instead.[11], [12] Changing the threshold voltage of the memory device additionally regulates and controls the pixel brightness. Figure 2.2 shows the circuit schematic of an integrated memory device as a driver FET. While such circuit schemes have been investigated with TFTs integrated with OLEDs, at the time of writing, there

have not been similar devices and circuits monolithically integrated on GaN utilizing GaN memory devices.

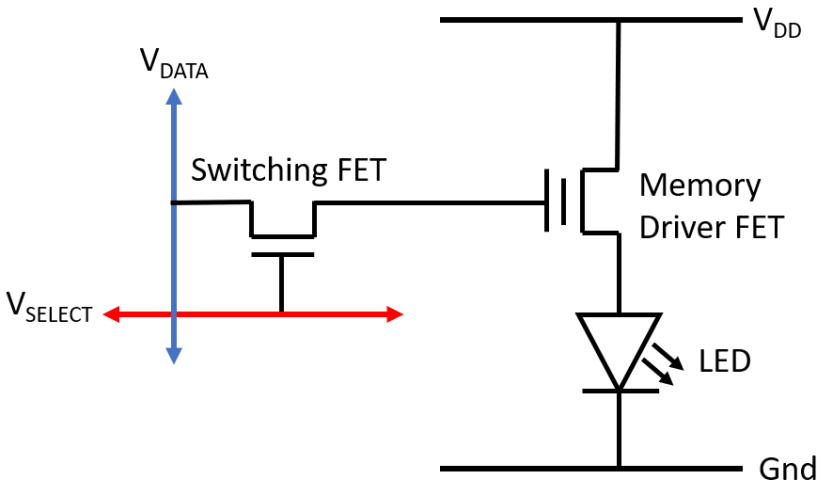


Figure 2.2: Memory integrated circuit

GaN nanowire FETs have been fabricated and realized in a variety of ways.[4] Figure 2.3 (a) shows an example of a process flow to fabricate a nanowire GaN MOSFET through a top-down approach. The electrical results of the resultant device are also shown in Figure 2.3 (b). The device utilizes a n-i-n structure with an Al_2O_3 gate oxide. [13]

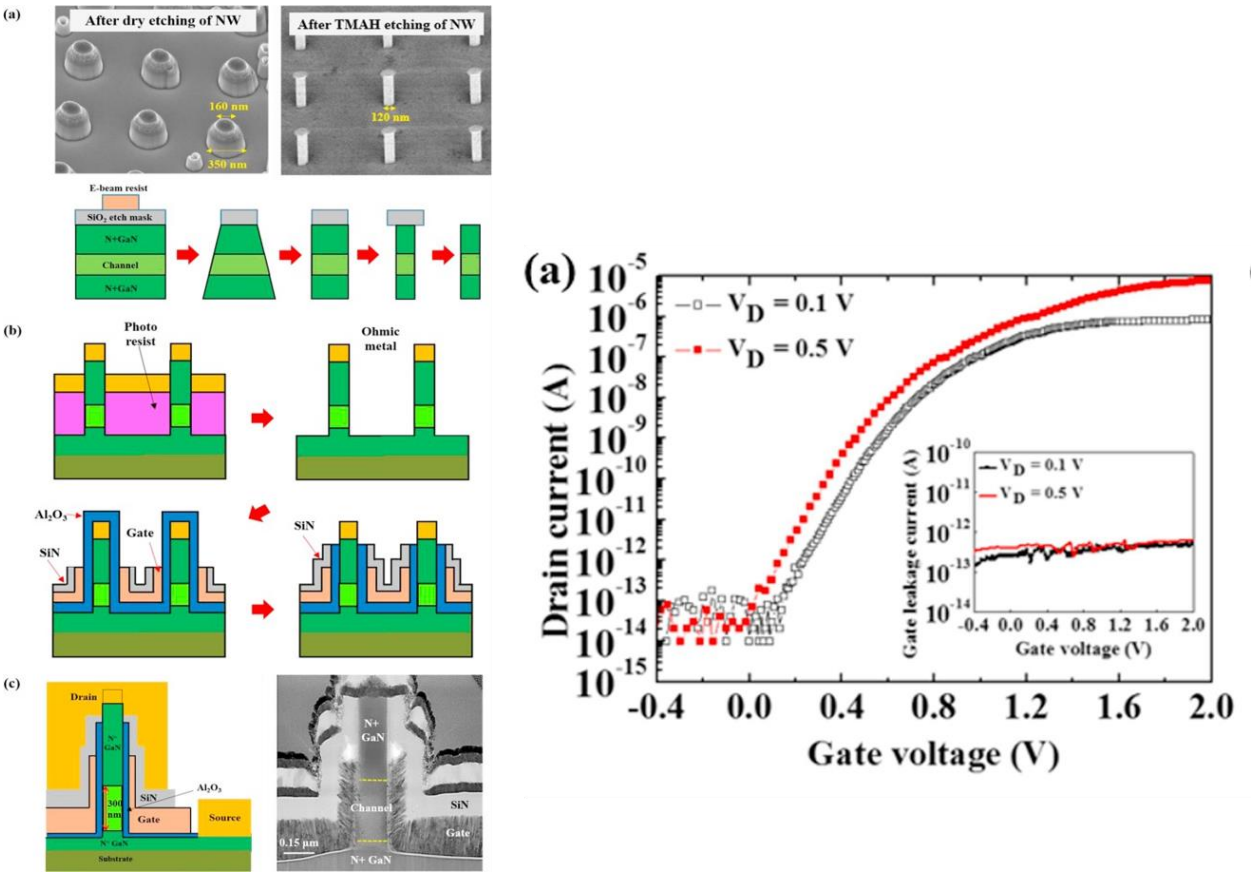


Figure 2.3: (a) Process flow of a GaN nanowire MOSFET and (b) Electrical results of nanowire MOSFET [13]

Still other FET variations have been realized. Figure 2.4 shows a GaN nanowire FET schematic based off a static induction transistor (SIT) that also utilized an n-i-n structure. [14]

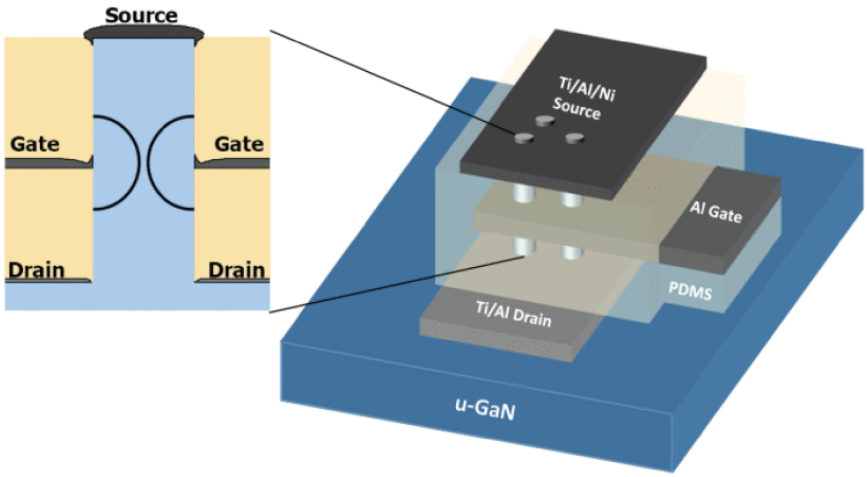


Figure 2.4: SIT-based GaN nanowire FET [14]

Flash memory devices with GaN has not been a prominent area of research. This is primarily because Si-based devices are the mainstay within industry and continue to remain cost-efficient. A lateral nanowire GaN memory device has been investigated in literature. In that case, the GaN lateral nanowire was used between layers of SiO_2. The oxide surrounding the nanowire was used to trap charge.[15] However, it is conceivable that for future applications that require extensive GaN integration, the availability of vertical GaN nanowire memory devices would be required and will be more cost-effective and offer superior system-level performance (one such application case being the aforementioned low refresh-rate active LED matrix displays).

The main motivation and goal, for the rest of this thesis, is to explore and develop a unique and novel vertical GaN nanowire flash memory device monolithically integrated with an LED.

3. Charge Trap Flash Memory

3.1 Background and Theory

Typical charge trap flash memory devices utilize an Oxide-Nitride-Oxide stack. The Oxide-Nitride-Oxide stack is commonly referred to as a SONOS (Semiconductor-Oxide-Nitride-Oxide-Semiconductor) memory device. SONOS memory is the industry standard to provide non-volatile memory (NVM), to make solid state drives used in all forms of electronics. In a SONOS memory device, as shown in Figure 3.1, charge is stored within the nitride trap layer while the bottom thin oxide layer functions as a tunneling layer just above the channel and a thicker oxide layer functions as a blocking layer on top of the nitride layer.[16] Higher charge retention time is always desired, and as such, various methods have been investigated in improving overall retention characteristics in typical SONOS devices. These retention time improvements include using multiple layers of oxide and nitride layers progressively below the final blocking oxide layer. The multiple layers combined together typically provides for a wider memory window.

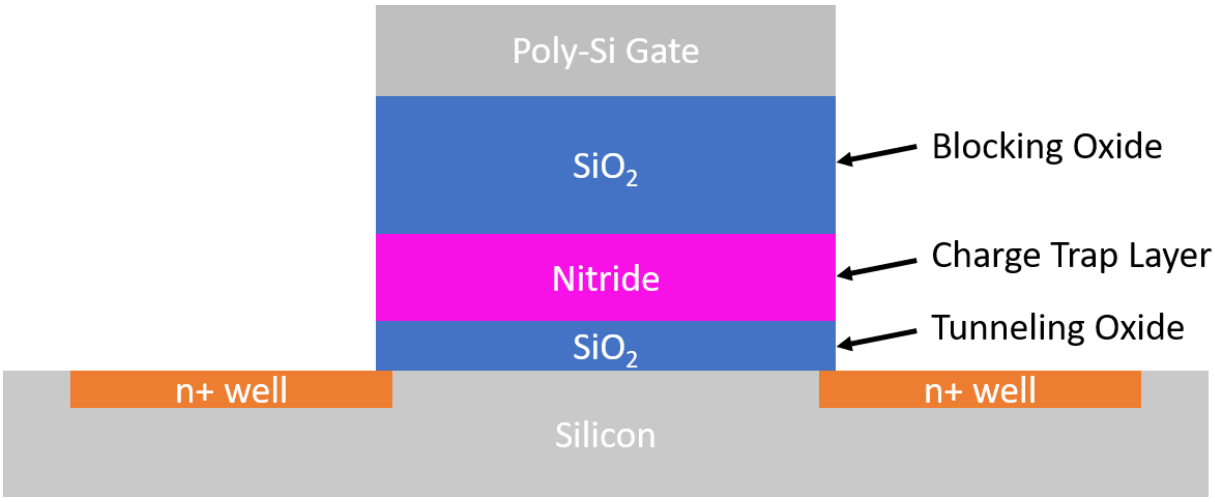


Figure 3.1: SONOS memory device example

Figure 3.2 shows the band diagram of a SONOS stack found within a standard charge trap memory device. The tunneling oxide is a thin layer with a high potential barrier that allows for charge carriers to tunnel through from the substrate but prevents tunneled charges (now trapped within the charge trap layer) from escaping back into the substrate unless sufficiently biased. The

blocking oxide, also conventionally of a higher potential barrier than the charge trap layer, prevents any charge losses to the gate.

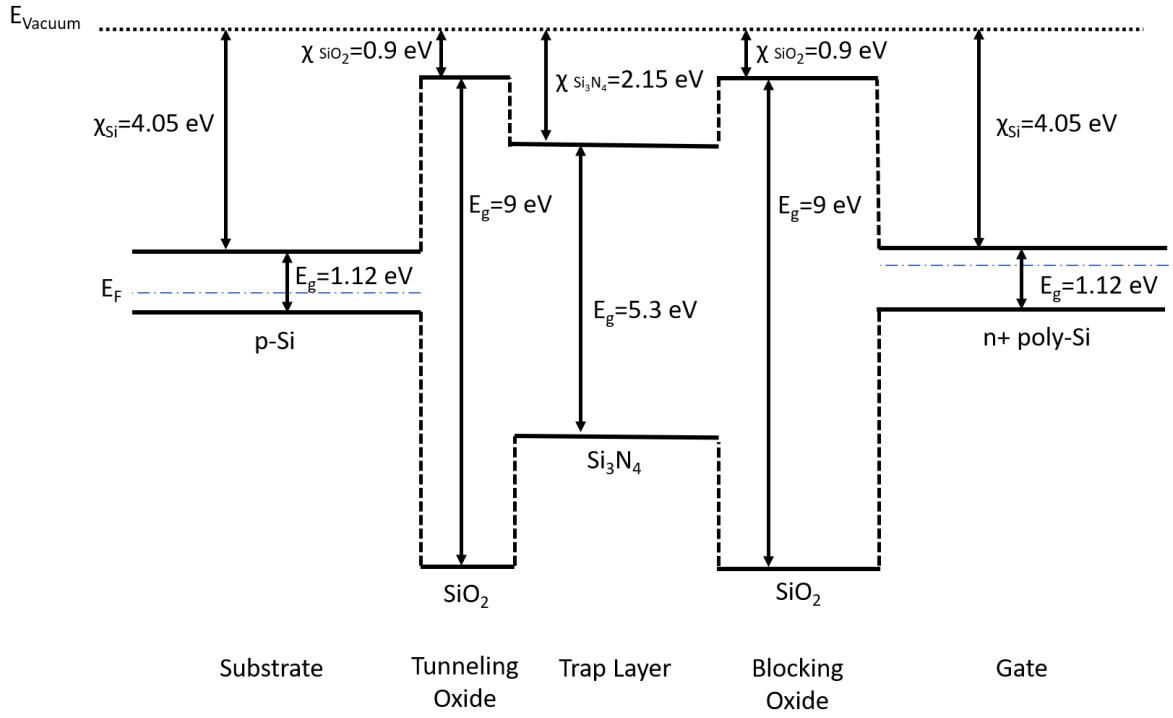


Figure 3.2: SONOS Band Diagram

In charge trap memory, charge carriers can be injected from the semiconductor through the tunneling layer into the charge trap layer through two different mechanisms depending on the charge trap stack utilized. It is either through hot-carrier injection (HCI) or through Fowler-Nordheim (F-N) tunneling. In hot-carrier injection, a charge carrier is considered to gain enough energy from the field to then "jump" over the energy barrier of the tunneling layer and effectively get trapped within the charge trap layer. In Fowler-Nordheim tunneling, there is a triangulation caused by the electric field from a gate bias, and thus effective thinning of the barrier when biased,

leading to charge carriers being able to tunnel through the barrier to be trapped within the charge trap layer.[17]

For modern charge trap memories, with continuous scaling, there is a need to move the multiple functional layers towards high-κ dielectrics in place of the lower-κ SiO_2 and Si_3N_4 layers. The motivation here is that with continued scaling, it is possible to have thicker dielectric layers for the same equivalent oxide thickness of SiO_2. Thicker, higher-κ dielectrics provides a continued means to scale device dimensions while also maintaining control over the channel region. If SiO_2 tunneling layers were too thin, charges tunneled into the charge trap layers can easily be lost back into the semiconductor through tunneling again and a programmed memory state would therefore be lost. High-κ dielectrics also provide a means to improve the gate coupling ratio. This limits the overall scaling as well in terms of the total amount of charge trapped within the layer as well as the voltage operating conditions required in such cases. High-κ dielectrics such as HfO_2, also have additional benefits such as improved charge trap characteristics as compared to Si_3N_4 due to the existence of increased densities of trap states and deep-level trap states that improve the overall data retention and prevent excessive charge loss.[18] The improved charge retention and charge trap characteristics therefore means it is beneficial to investigate and develop high-κ dielectric charge trap memory stacks.

One such stack investigated in literature that utilized high-κ dielectrics is $Al_2O_3/HfO_2/Al_2O_3$. Figure 3.3 shows the band diagram as derived through experimental results for the charge trap stack reported.

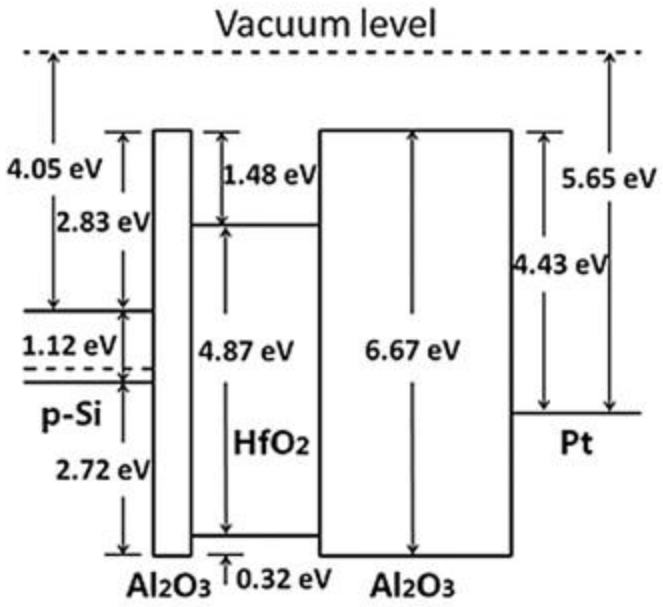


Figure 3.3: Band diagram of $Al_2O_3/HfO_2/Al_2O_3$ charge trap memory stack [19]

Utilizing the $Al_2O_3/HfO_2/Al_2O_3$ stack, results in literature show a memory window that increases with gate voltage sweeps. The effects of utilizing multiple stacks and the effects of thermal treatment have also been reported in literature.[19], [20] There are multiple avenues of continued work to improve the overall memory window, retention characteristics and applicable voltage ranges while also improving material quality and combinations.[17]

3.2 Charge Trap Layer Fabrication

Validation of the charge trap layer stack was done through fabrication and characterization of Si-based planar capacitors. GaN has a similar electron affinity to Si - validating the functionality of the charge trap stack on Si provides a cost-effective method to initially test and characterize the

performance of the stack and corresponding memory windows. Validation of the memory stack was also required since the high-κ dielectric $Al_2O_3/HfO_2/Al_2O_3$ combination selected had previously not been done experimentally at RIT.

Initial work involved a p-type Si wafer with a substrate doping of $1.8x10^{14}$ cm^{-3}. The wafer was cleaved into pieces and RCA cleaned prior to atomic layer deposition (ALD) of the charge trap stack. Based off of the work shown in literature[19], 3 nm of Al_2O_3, 10 nm of HfO_2 and 15 nm of Al_2O_3 were deposited consecutively at 200°C. An experimental split was done after the charge trap layer deposition. One p-type Si sample was annealed in an O_2-ambient at 800°C for 40 seconds, while the other was not. The annealing experimental split was done to investigate whether a wider memory window was achievable with a single added, simple and fast processing step. This was followed by 100 nm of Al deposited through thermal evaporation for all samples. Square capacitor structures were defined through contact lithography followed by an Al wet-etch. It should be noted that it was expected that a certain amount of Al_2O_3 from opened areas were expected to also etch in this scenario, but controlled etching with a minimal over-etch time was done to prevent excessive undercutting. The Al wet etch was followed by a CF_4-based dry etch to remove the remaining $Al_2O_3/HfO_2/Al_2O_3$ layers in field regions. (See 7.2 for dry etch details). The same fabrication process to form the high-κ charge storage capacitors on p-Si was repeated on an n-type Si wafer with a substrate dopant concentration of $1x10^{15}$ cm^{-3}.

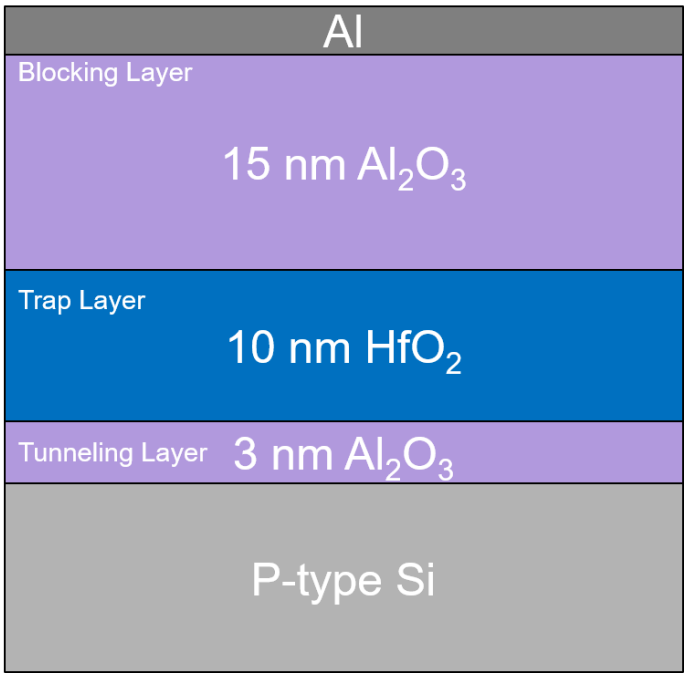


Figure 3.4: Flash memory capacitor layers

3.3 Electrical Testing

The fabricated capacitors were tested for memory windows to explore initial device operation. The tests here would provide an understanding of the expected electrical results for a GaN-based memory device. Initial testing was done on the p-type samples followed by the n-type samples.

3.3.1 P-type Samples

High-frequency (1 MHz) capacitance-voltage (C-V) plots were used to determine memory windows. The high-κ memory stack capacitors were swept from inversion through to accumulation and back to inversion. The hysteresis obtained between the two sweep directions determines the

total memory window, where inversion to accumulation is considered one sweep direction, and accumulation to inversion is considered the second sweep direction. The effect of the sweep window against the memory window was tracked. Consistency of the memory window at the same sweep conditions were also tracked across multiple devices to verify reliability of the devices.

Figure 3.5 shows the C-V characteristic for the annealed p-type sample with the memory stack. The overlay shows 5 different devices measured with a voltage sweep from +5V to -5V back to +5V. The flat-band capacitance, C_{FB}, was found for each C-V curve. To find the flat-band capacitance, the intersection point of the C-V curve with its second derivative was found. This point of inflection has been shown in literature to be close, in cases of low doping (as is the cases presented here), to theoretically calculated flat-band capacitances.[21], [22] A MATLAB code was written to directly import high frequency C-V text files to automatically find the inflection points of the forward sweep and backward sweep curves. The MATLAB code finds the memory window associated with the device through measuring the difference between the two derived flat-band voltages. As seen in Figure 3.5, a majority of the devices do not show a wide memory window, with an almost perfect overlay between the two sweep directions. The lack of a wide memory window is mainly attributed to the high temperature annealing done. It is conceivable that there was an intercalation of the Al_2O_3 and HfO_2 layers creating a graded increase at the interface.[23] The graded increase and intercalation results in little to no charges being trapped within the HfO_2 layers. Table 3.1 shows a summary of the memory windows derived for the annealed devices tested and presented.

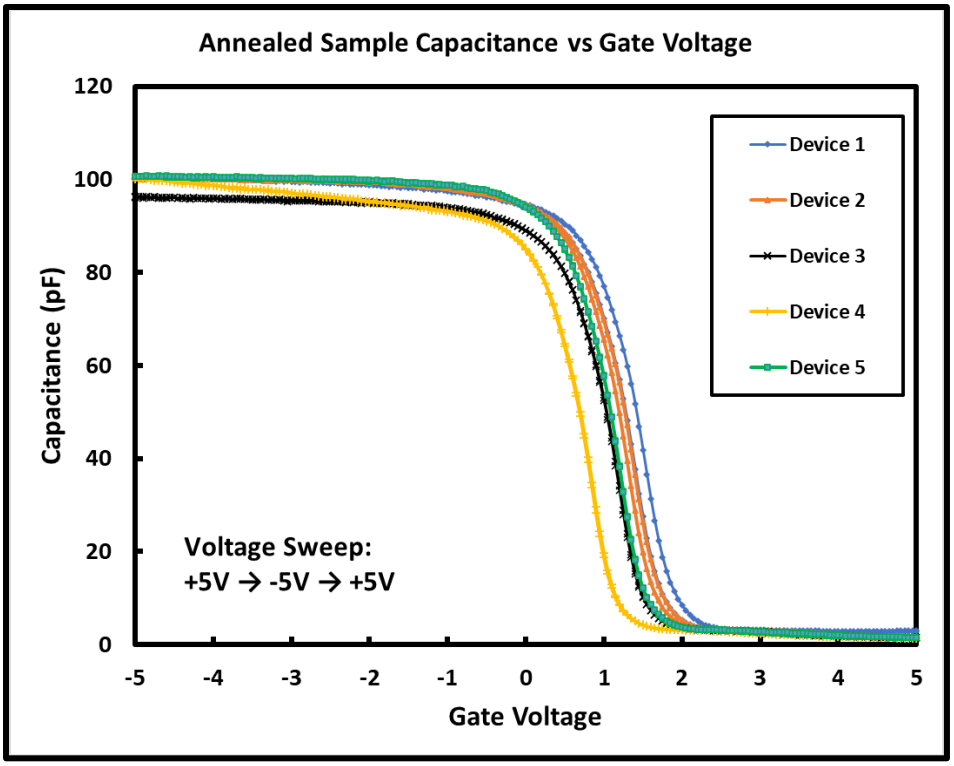


Figure 3.5: Annealed Sample Capacitance vs Gate Voltage Overlay

Table 3.1: Memory Windows for Devices Tested on Annealed Sample

Number	Memory Window (V)
Device 1	0.1301
Device 2	0.0658
Device 3	0.012
Device 4	0.0117
Device 5	0.0042

Figure 3.6 shows an overlay of 12 different devices tested on the unannealed sample. All devices had a voltage sweep from +5V to -5V back to +5V. As shown, all devices tested overlay over each other consistently and show a similar memory window with an overall average of 0.496V. This shows consistency across the sample in terms of the overall memory capability of the stack developed. The overall standard deviation in the memory window was 0.04V.

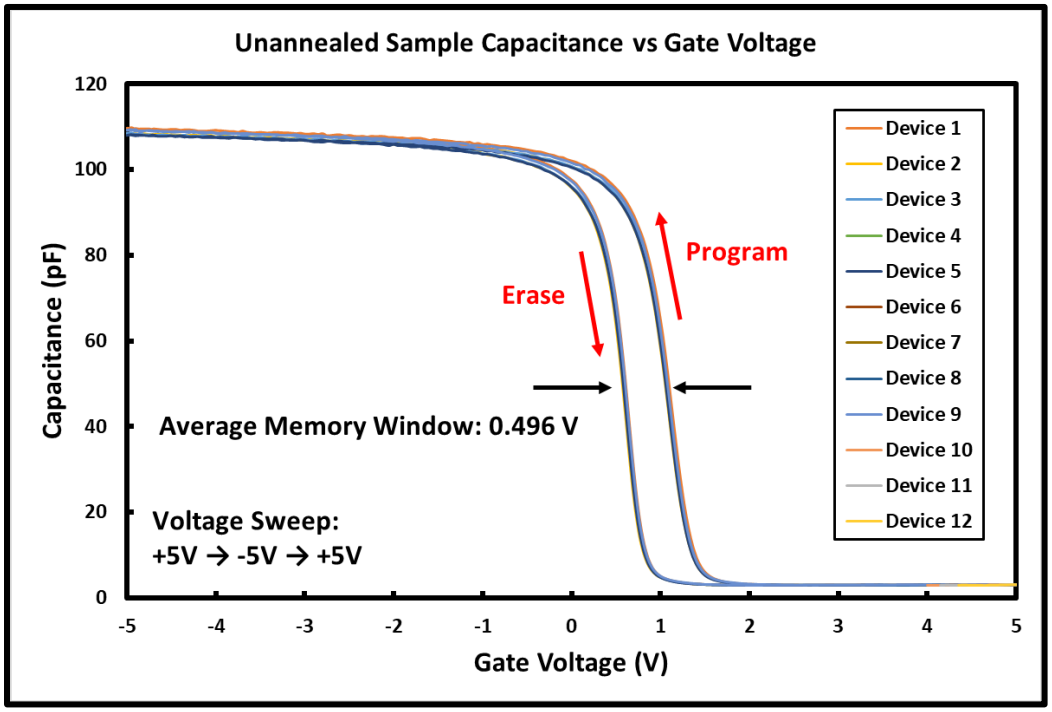


Figure 3.6: Unannealed Sample Capacitance vs Gate Voltage Overlay

Figure 3.7 shows the C-V plots obtained for different voltage sweep ranges as applied to a single unannealed device. As shown, larger voltage sweep ranges yield wider memory windows. The increased biasing yields a greater bending of the bands that allow for more electrons to tunnel from the silicon into the trap-layer oxide.

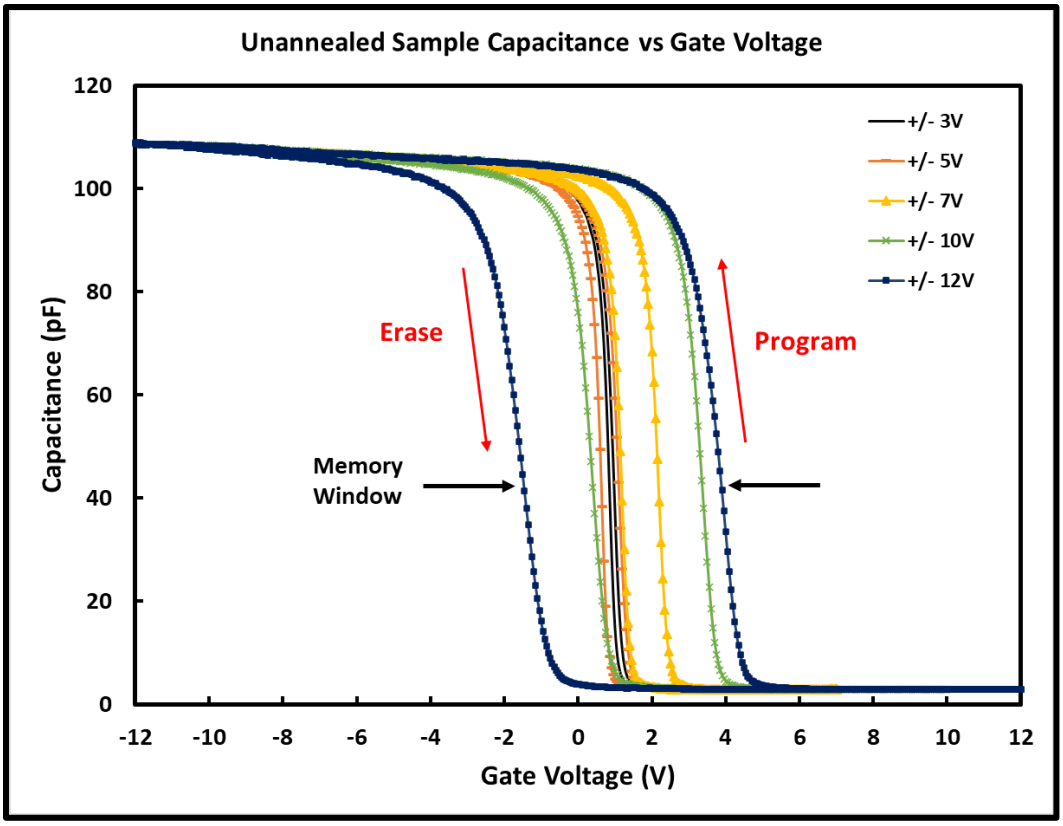


Figure 3.7: Unannealed Sample C-V memory windows at different sweep ranges

Figure 3.8 shows the summary of the total memory window achieved for each of the voltage sweeps done. As seen, there is an almost exponential increase in the memory window with higher biasing voltage conditions. The exponential increase in the memory window is in agreement with what was described and found in literature.[19] The main contributing factor yielding this exponential trend is the band alignment at much higher biases. Higher biases lead to greater band bending which allows electrons to tunnel from the quasi-fermi level within the semiconductor through the tunneling oxide layer, to then be trapped within the charge trap layer through F-N tunneling. Even higher biases lead to the conduction band of HfO_2 being lower than the quasi-fermi level within the semiconductor, allowing for much higher numbers of electrons to directly

tunnel through the Al_2O_3 layer to allow much greater number of charges to be trapped within the HfO_2 layer. Figure 3.9 shows the band diagrams of the complete stack at flat-band conditions, and at increasingly higher biases.

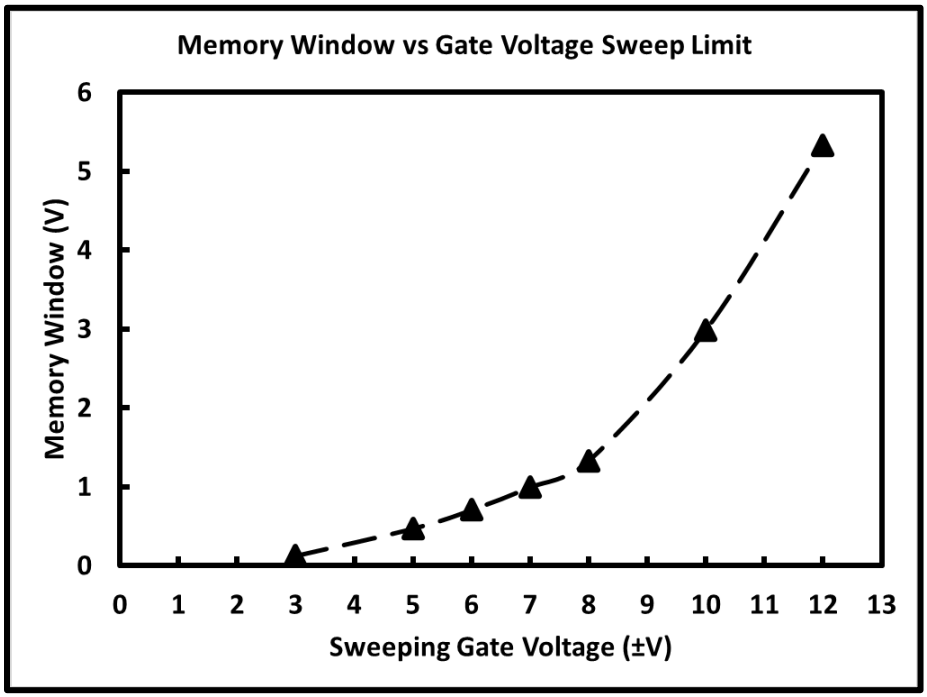


Figure 3.8: Memory window vs Sweep Voltage for Unannealed Sample

Table 3.2: Sweeping Voltage and Memory Window for Unannealed Sample

Sweeping Voltage (±V)	**Memory Window (V)**
3	0.128
5	0.473
6	0.709
7	0.997
8	1.332
10	2.986
12	5.330

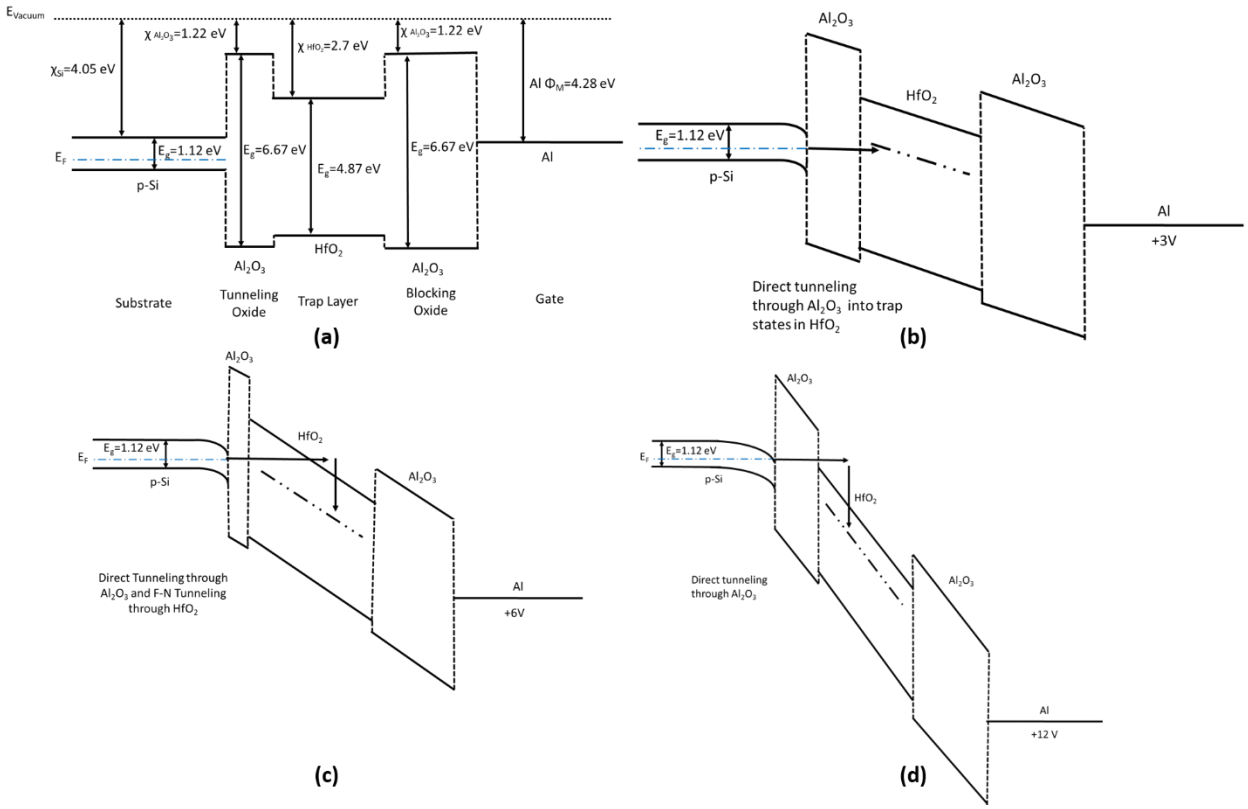


Figure 3.9: (a) Flat-band condition of p-Si/Al_2O_3/HfO_2/Al_2O_3/Al stack, and with applied biases of (b)+3V, (c) +6V and (d) +12V

3.3.2 N-type Samples

As previously described, n-type samples were also fabricated and tested. The expectation was a wider memory window for a given sweep voltage due to the majority charge carriers being electrons, instead of the band-to-band tunneling mechanism responsible for electron injection in the case of the p-type devices.[19] Electrons being the majority charge carriers would shift the fermi level closer to the conduction band. A lower bias would therefore be necessary to allow for F-N tunneling and contribute to more charge carriers trapped within the HfO_2 charge trap layer. N-type Si was used to confirm that this principal worked for a n-type wafer and for this particular

memory stack since the majority charge carriers in GaN are electrons (holes also have very low mobility in GaN). An annealing split was not done here since previous results had shown that annealing at the conditions previously presented was ineffective. The MATLAB code previously developed and implemented was modified to accommodate for the change in substrate type and the resultant change in the voltage sweep direction.

Figure 3.10 shows C-V plots at different sweep voltage ranges. Here again, voltages were swept from inversion to accumulation and back to inversion (-V to +V to -V). As seen in the p-type Si samples, larger sweep voltage ranges yield wider memory windows. It was also observed that, on average, for a given sweep voltage, the memory windows were wider for the n-type samples as compared to the p-type samples. The wider memory windows achieved on the n-type samples suggests that there are a greater number of charges trapped at a given bias condition and plays into the originally expected outcome.

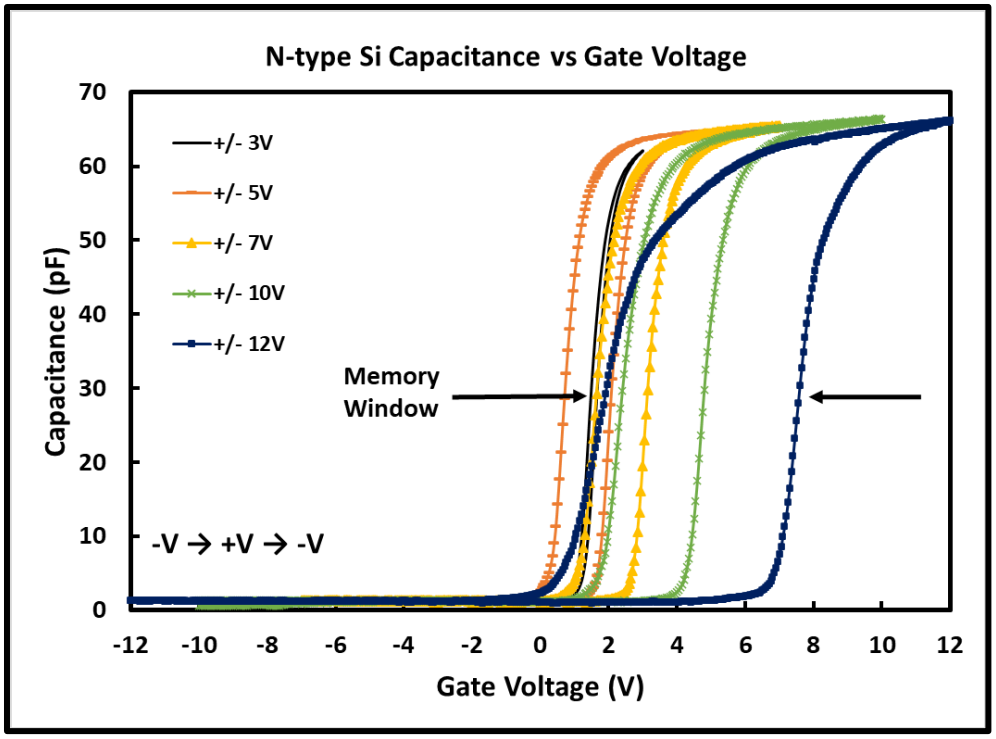


Figure 3.10: N-type Si C-V memory window

Figure 3.11 shows the summary of the memory window achieved at different gate sweep voltage values. The memory windows still follow an exponential form (excluding the +/-3V sweep).

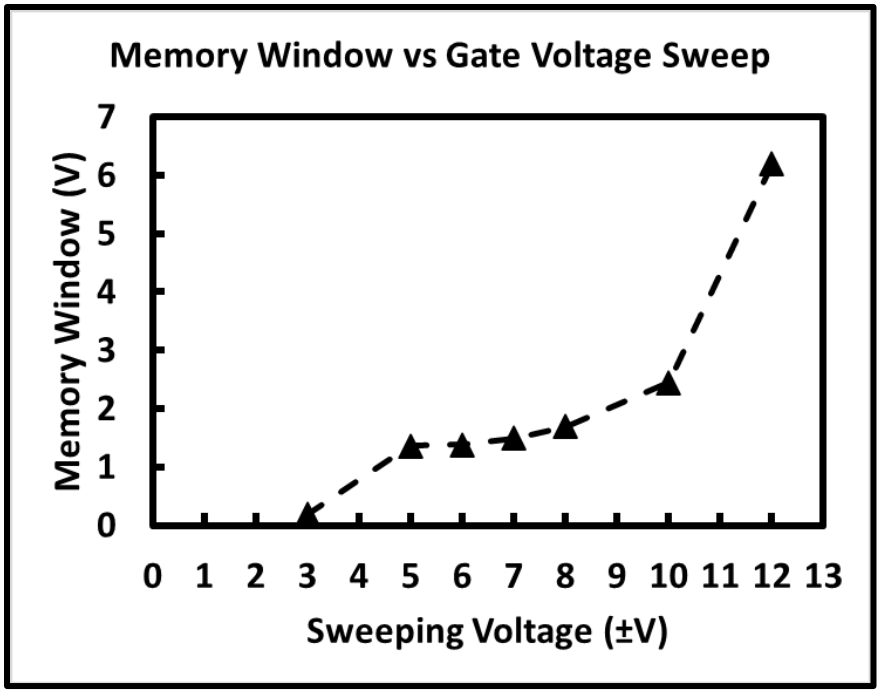


Figure 3.11: Memory Window vs Sweep Voltage for n-type Si sample

Table 3.3: Sweeping Voltage and Memory Window for n-type Si sample

Sweeping Voltage (±V)	**Memory Window (V)**
3	0.187
5	1.362
6	1.381
7	1.495
8	1.693
10	2.445
12	6.192

3.3.3 Summary

The electrical results show that a charge trap memory stack made with high-k dielectrics is possible on Si. Additionally, electrical results shows that the stack works on p-type and n-type Si substrates. These results also show promise in applying the same charge trap memory stack to GaN as well. Figure 3.12 shows the comparison between Si and GaN bands. Si and GaN both have electron affinities that are within 0.05 eV of each other. When compared against the band alignment presented in Figure 3.3 for p-Si, and the band alignment against n-Si presented in Figure 3.12, there is a great likelihood of GaN successfully working with the memory stack developed and validated on Si. The comparison of memory windows within p-Si and n-Si provides a reasonable background framework in terms of proving electrons tunneling under bias from the semiconductor into the charge trap layers and the same mechanism expected to extend and work with GaN as well.

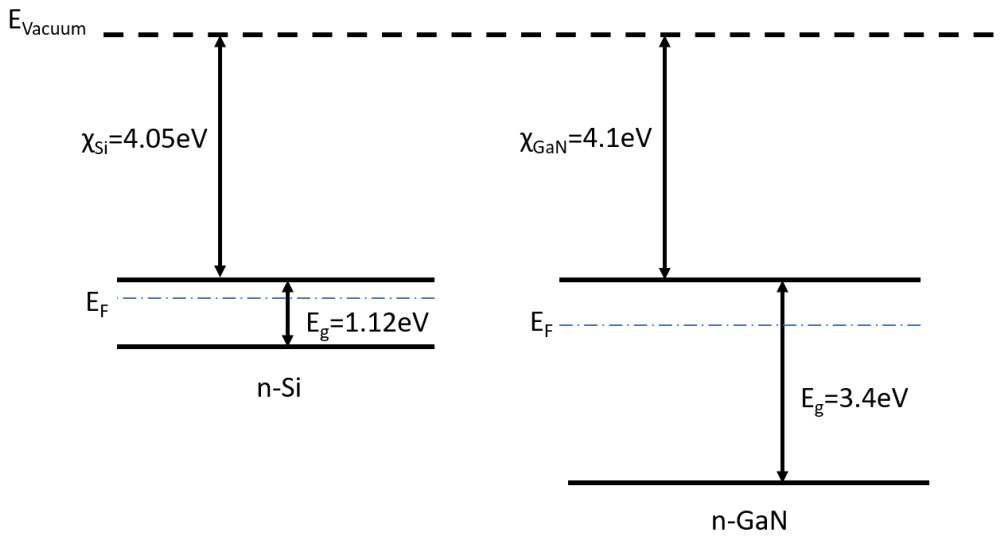


Figure 3.12: n-Si and n-GaN band diagram comparison

4. Proposed Device

Figure 4.1 shows for the first time, a GaN vertical nanowire memory device integrated with an LED. The memory device is in series with an LED, all vertically integrated. The drain shown on the top of the device is in contact with the p-type layer of the LED. The multiple quantum well (MQW) is beneath the p-GaN region, with an n-GaN region underneath the MQW completing the LED structure. The gate, as shown in the cross section, wraps around the GaN nanowire. The Ni gate is within the u-GaN region. The charge trap layer shown represents the previously investigated and validated stack of $Al_2O_3/HfO_2/Al_2O_3$. The source is also within the u-GaN region. However, the Ti/Al metal contact proposed for the source, when annealed, has been shown in literature to yield N-vacancies within GaN to provide a source of electrons along with the formation of TiN.[24] This is also combined with an increased number of O-vacancies that also increase the total electron concentration within the deeper u-GaN regions that is a resultant of increased growth defects closer to the carrier interface regions. [25]

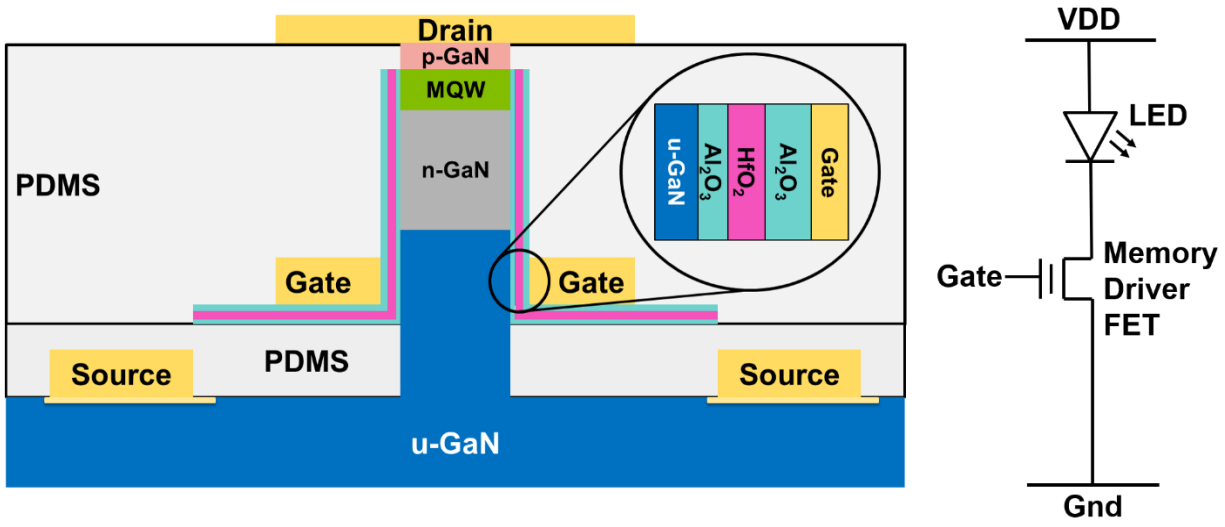


Figure 4.1: Final Proposed Device Structure

Based on previous work in literature[14], [26], [27] , the proposed device is electrically expected to work similar to a static-induction transistor (SIT) in series with an LED. This is primarily due to the gate length of the devices fabricated and the relative position of the gate to the drain. Small gate length devices such as an SIT, take advantage of, and control the short-channel effect known as punch-through. Harnessing punch-through leads to triode-like, or non-saturating characteristics in contrast to the pentode-like, or saturating characteristics of a common MOSFET. These nanowire n-i-n devices have a dependence on the diameter, being conventionally depletion mode devices operating with a negative threshold voltage. However, it is expected that use of a charge trapping layer can be utilized to shift the threshold voltage to positive values. Integration of the charge trapping layers can also lead to novel brightness control over the LED. Furthermore, this work can establish a foundation for the future of vertical device integration and vertical memory integration. Demonstration of a charge trap memory device vertically integrated with a LED on GaN is explored here for the first time.

5. Device Fabrication

Figure 5.1 shows the initial material stack of the green LED substrate utilized in fabrication. Two different samples were used through the complete fabrication process. Sample 1 was a whole, single-side polished (SSP) 2” GaN-on-sapphire substrate while Sample 2 was half of a double-side polished (DSP) 2” substrate. The double-side polished sample was used to explore the possibilities of a transparent memory device. Both samples had the same material stack.

From bottom to top, the material stack consists of the initial sapphire substrate with a 20 nm GaN buffer, followed by 2 µm of unintentionally doped GaN (u-GaN) , 3 µm of n-type GaN, 3 InGaN/GaN super-lattice layers, 8 InGaN/GaN quantum wells tuned for green emission at 530 nm, 150 nm of p-type GaN and 1 nm p-type InGaN to act as a cap.

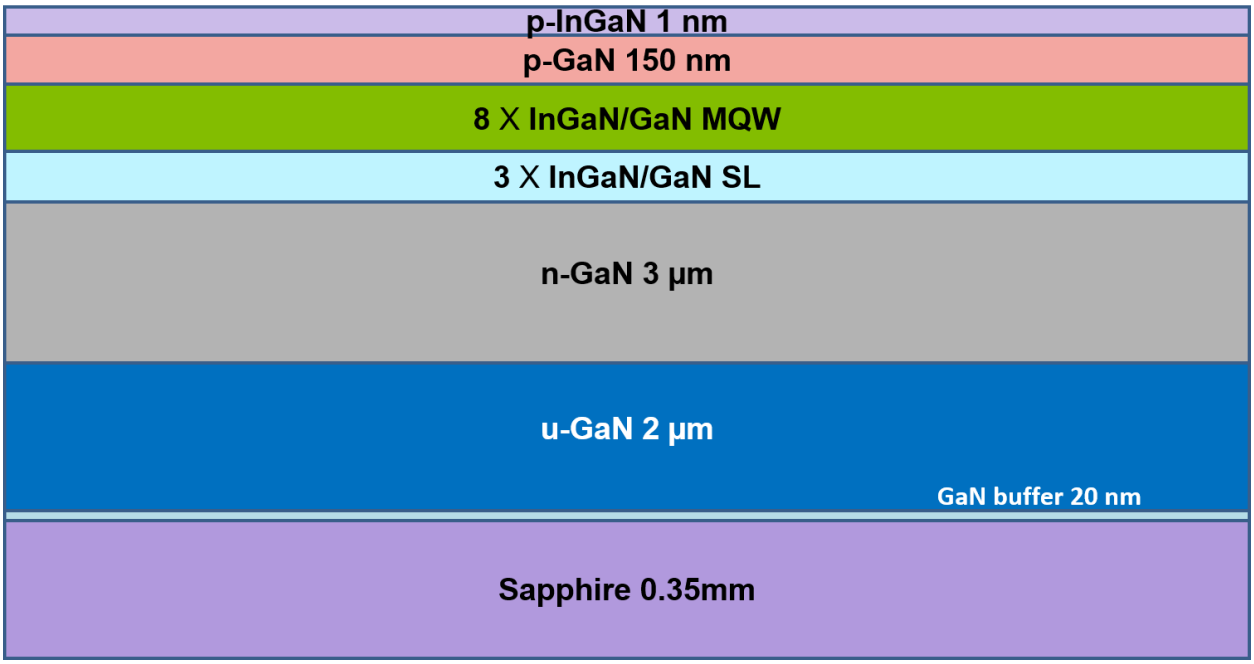


Figure 5.1: Initial GaN green-LED substrate stack

Figure 5.2 shows the overall process flow proposed and used to fabricate the GaN nanowire memory device. Steps 1 to 3 highlights the method to form vertical GaN nanowires through a top-down approach. This is followed by patterning and lifting off the source metal in Step 4. Polydimethylsiloxane (PDMS) was used as an inter-layer dielectric. PDMS coating and etching is followed by conformal ALD deposition of the $Al_2O_3/HfO_2/Al_2O_3$ memory stack and subsequent patterning of the memory stack. A directional deposition of the gate metal around the nanowires in combination with liftoff patterning follows. PDMS is again used as an inter-layer dielectric prior to a final liftoff patterning of the drain metal at the tips of the nanowires.

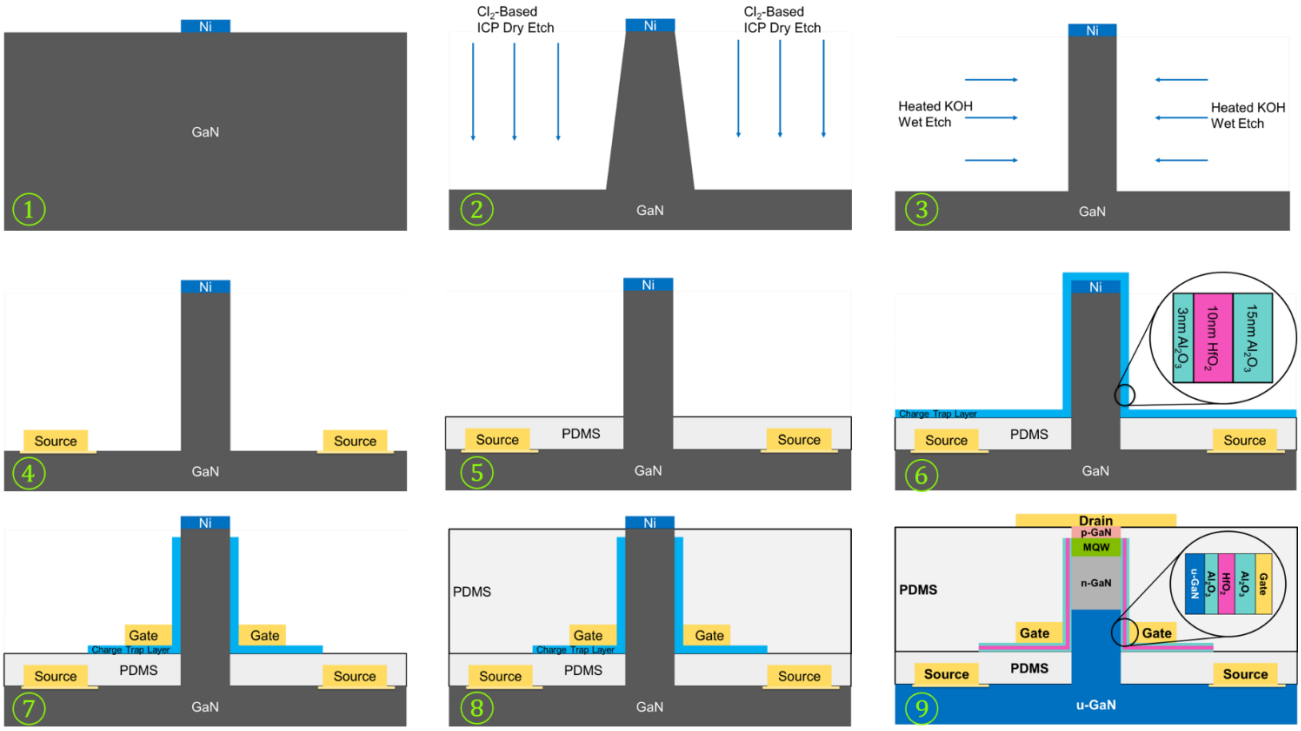


Figure 5.2: Overall Process Flow

5.1 Fabrication Steps and Details

5.1.1 Vertical Nanowire Formation

Vertical GaN nanowires were formed through a top-down approach. A top-down approach is more cost-effective as compared to selective area epitaxy required for growth of nanowires in a bottom-up approach. A bottom-up approach also presents problems in terms of overall material quality and scalability. Location of vertical wires were defined through liftoff processing. Lift-off resist, LOR-5A, in combination with positive photoresist, AZ-1512 was used to define wire tips for hard mask deposition. While the overall design aimed at patterning minimum dimensions down to 1µm diameter wires, minimum dimensions achieved through lithography were 1.5µm for wire

diameters. Wire diameters designed and achieved over both samples were 1.5µm, 2µm and 3µm. 1x1, 2x2 and 3x3 wire arrays of each diameter were patterned for the devices.

100 nm of Ni was deposited through electron-beam evaporation to act as a hard mask for a subsequent dry etch. After lift-off of Ni utilizing N-methyl-2-pyrrolidone (NMP), vertical GaN wires were made through a Cl_2-based inductively coupled plasma dry etch. Figure 5.3 shows a Scanning Electron Microscope (SEM) image of a GaN wire after the initial dry etch. As shown, there is considerable micro-masking that occurred around the wires during the dry etch. The micro-masking observed can be attributed to several different factors. To start, Ni from the tips of the wires could redeposit and cause subsequent micro-masking. The other, more likely possibility is the presence of defects within GaN that are more resistant to the directional and physical dry etch utilized. Instead of a directional, physical dry etch, a more chemical dry etch can be used instead that will prevent the micro-masking. A more chemical dry etch however, will not provide as much vertical anisotropy.

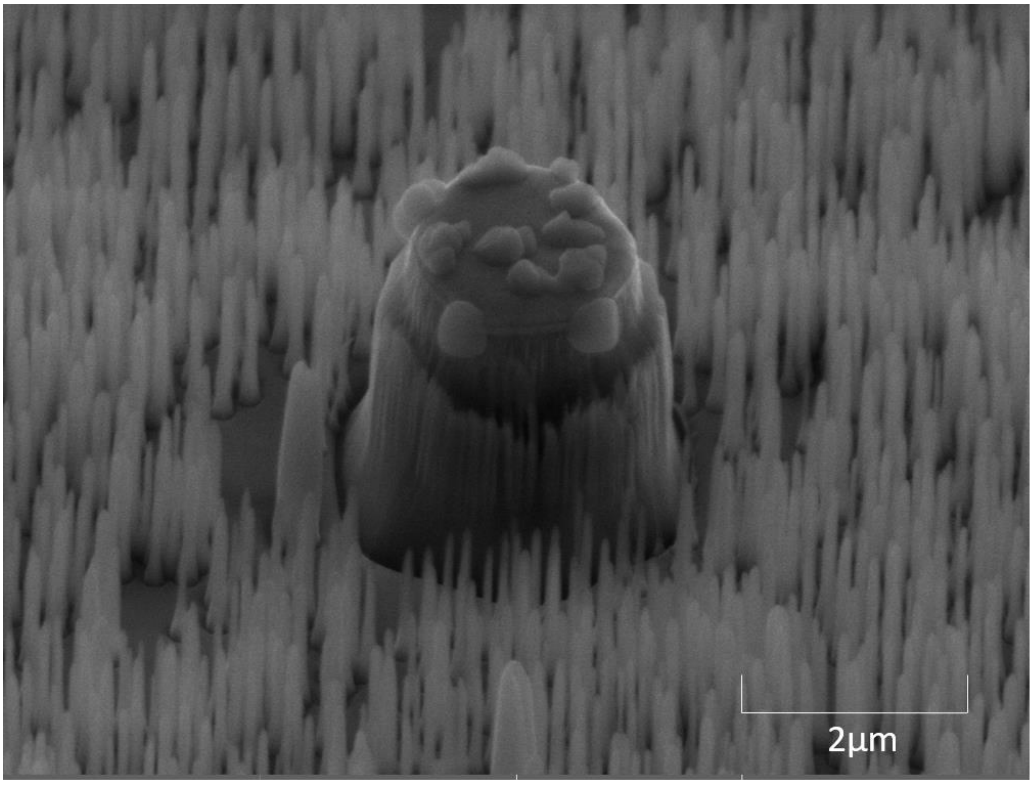


Figure 5.3: SEM image of GaN nanowire after dry etch. Shows wires and micro-masking. [Image courtesy Bryan Melanson]

The initial dry etch is followed by a chemical etch. Diluted AZ-400K developer heated to 80°C-85°C was used. The diluted AZ-400K contains about 0.8 wt% KOH. KOH and similar hydroxyl-based chemistries selectively etches GaN. The Ga-polar surface repels the hydroxyl groups in KOH and prevents etching of the c-plane. Other planes of GaN etch at a much more rapid pace. This results in an effective straightening of the nanowire's vertical planes.[28], [29] This also aids in eliminating the micro-masking previously seen since the exposed crystal surfaces of GaN during the chemical etch are etched away as well. Figure 5.4 shows an SEM image after a 10-minute KOH etch was done on Sample 1.

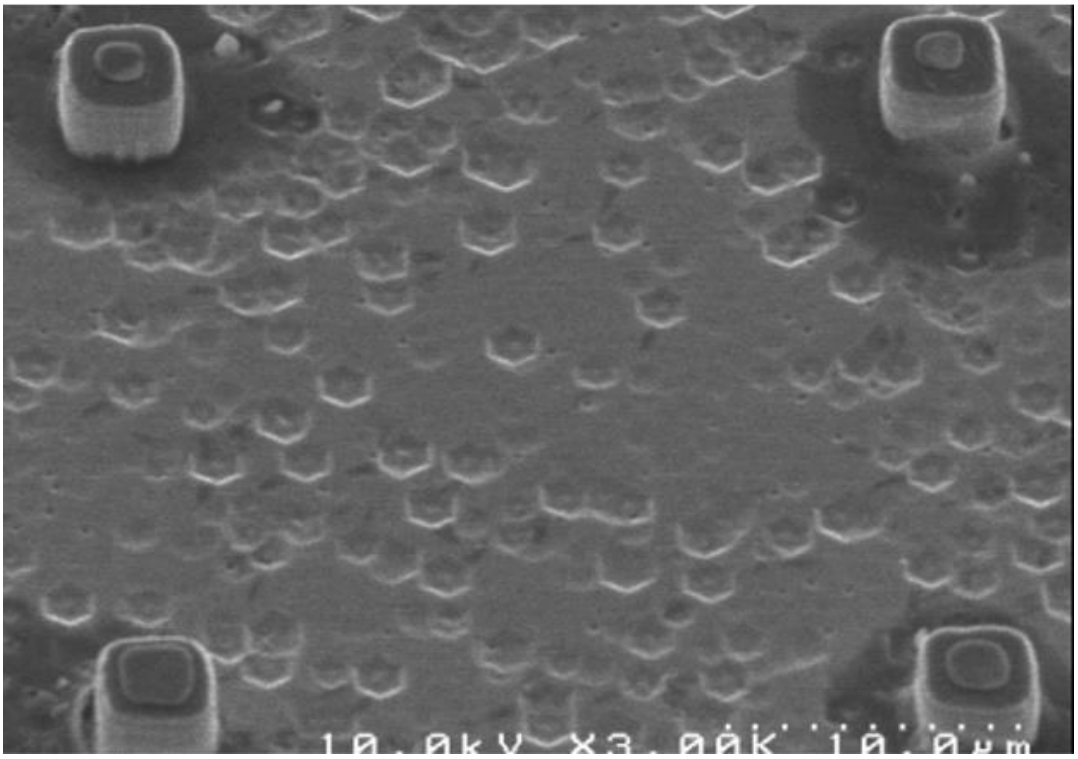


Figure 5.4: SEM image of nanowires on Sample 1 after heated KOH etch

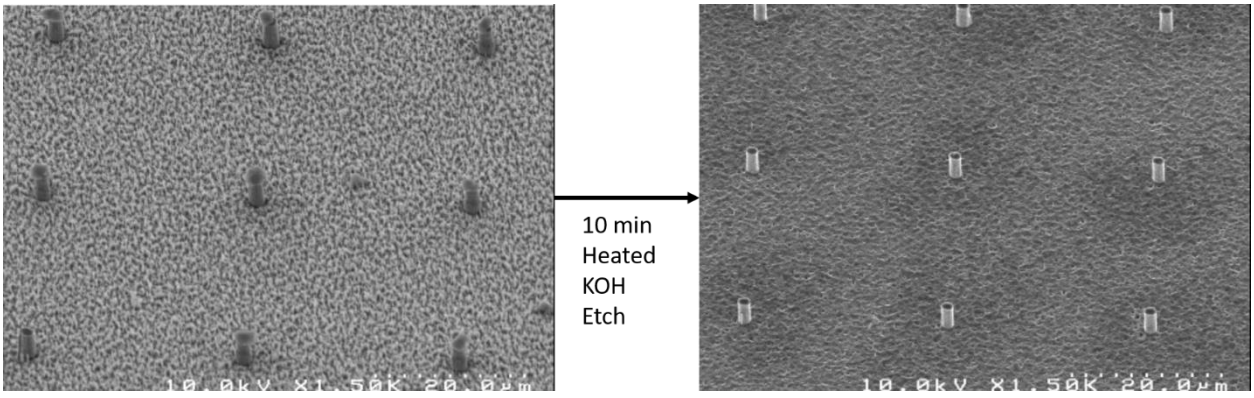


Figure 5.5: SEM image of Sample 2, before and after heated KOH etch

5.1.2 Source Metal

Source regions were defined through lift-off. A Ti/Al stack was used obtain ohmic contacts. Sample 1 (single-side polished wafer) had 50 nm of Ti evaporated through electron-beam evaporation followed by thermal evaporation of 150 nm of Al. 40 nm of Ti and 122 nm of Al were evaporated on Sample 2 (double-side polished wafer). Measurements reported here were based on values obtained with a quartz crystal. This was followed by a Rapid Thermal Anneal (RTA) in a N_2 ambient for 40 sec. at 650°C for both samples. The Ti/Al stack on GaN after annealing forms an ohmic contact while also providing a source of charge carriers through the generation of nitrogen vacancies.[24] This is in addition to the increased O-vacancies present within the defect regions at the base of the GaN LED material stack. The combination of the two factors (presence of nitrogen vacancies and oxygen vacancies) provides for a higher concentration n-type region near the source regions of the device.

5.1.3 PDMS inter-layer dielectric

PDMS, mixed in 10:1 (Part A: Part B) by weight was spun onto both samples. The relatively viscous PDMS planarizes across the wafer, removing the height difference caused by the nanowires. The planarized PDMS enables a controlled and linear etch back while still completely covering the base of the nanowire. After curing through an extended hot-plate bake for 11 minutes at 90°C, the PDMS was etched back through a CF_4/O_2 Reactive Ion Etch (RIE). The fluorine radicals aid in etching the Si complexes within PDMS while the oxygen aids in reacting with the organic, and carbon compounds within the PDMS. Continuous checks of the height of the nanowires were recorded once the nanowire tips were revealed in order to ensure that nearly half

of the u-GaN region was uncovered. In total, 17 1-minute cycles of the PDMS dry etch was done to reach a sufficient depth. Figure 5.6 shows the PDMS etch back observed from the 12th cycle in 2 cycle steps up until the 16th cycle. As observed, the tips are just visible after 12 cycles and the PDMS continues to etch back to reveal more of the nanowires through additional cycles.

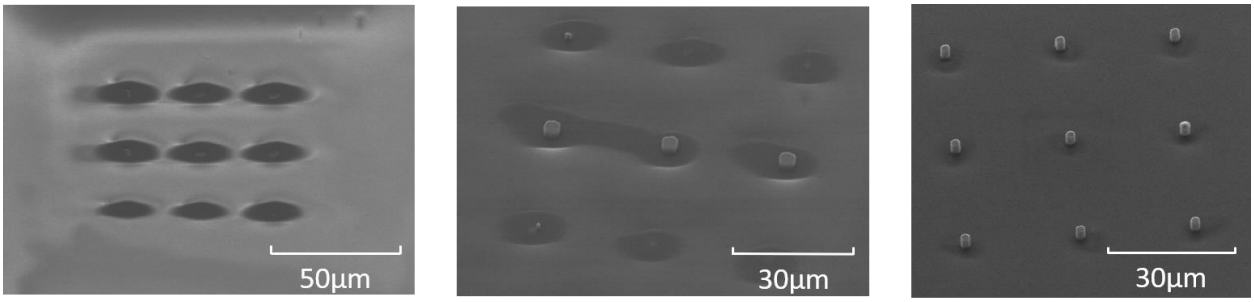


Figure 5.6: SEM images of 3x3 array through PDMS etch back cycles. (a) 12 cycles, (b) 14 cycles, and (c) at 16 cycles

5.1.4 ALD Deposition and Etch

After the PDMS etch back was completed to reveal sufficient depth within the u-GaN region, 3 nm of Al_2O_3 was deposited, followed by 10 nm of HfO_2 and 15 nm of Al_2O_3 all done at 200°C through atomic layer deposition (ALD). The same deposition conditions and recipes were used for both samples and followed the same conditions utilized during initial work involving Si capacitors shown previously.

Photoresist (AZ-1512) was coated over both samples after deposition. Photoresist, when spun on, coats and reaches the tips of the wires. Lithography and development of large pad regions

covering source regions where the dielectric layers were to be etched away was done. A low power, high pressure O_2 RIE was used to etch back the photoresist from the tips of the wires. Figure 5.7 shows the process described. Figure 5.7 (a) shows the originally coated photoresist completely over the sample, Figure 5.7 (b) shows the photoresist after lithography and development and Figure 5.7 (c) shows the photoresist being etched back to reveal the tips of the nanowires. This allows the deposited layers covering the tips of the wires to be etched back without photoresist. A CF_4-based RIE dry etch was used to etch back the deposited dielectric layers. 6 1-minute etch cycles were done to ensure complete etching of the $Al_2O_3/HfO_2/Al_2O_3$ dielectric stack in all exposed areas.

Figure 5.8 shows an SEM image of a nanowire after the dielectric layers were etched completely and the photoresist was removed. There is a definitive "lip" that shows the region above which the dielectric layers were etched to expose the Ni cap layer.

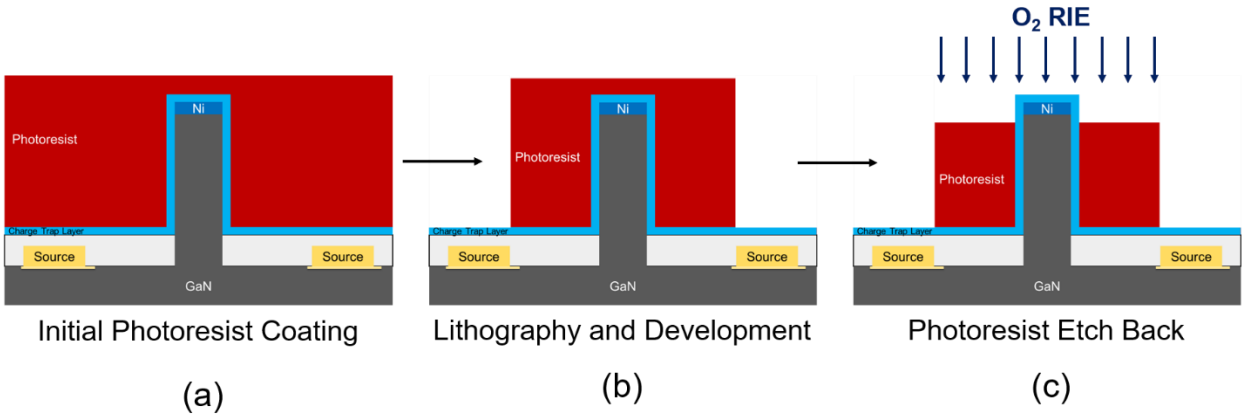


Figure 5.7: Schematic flow of photoresist patterning and etch back to define charge trap layer etch

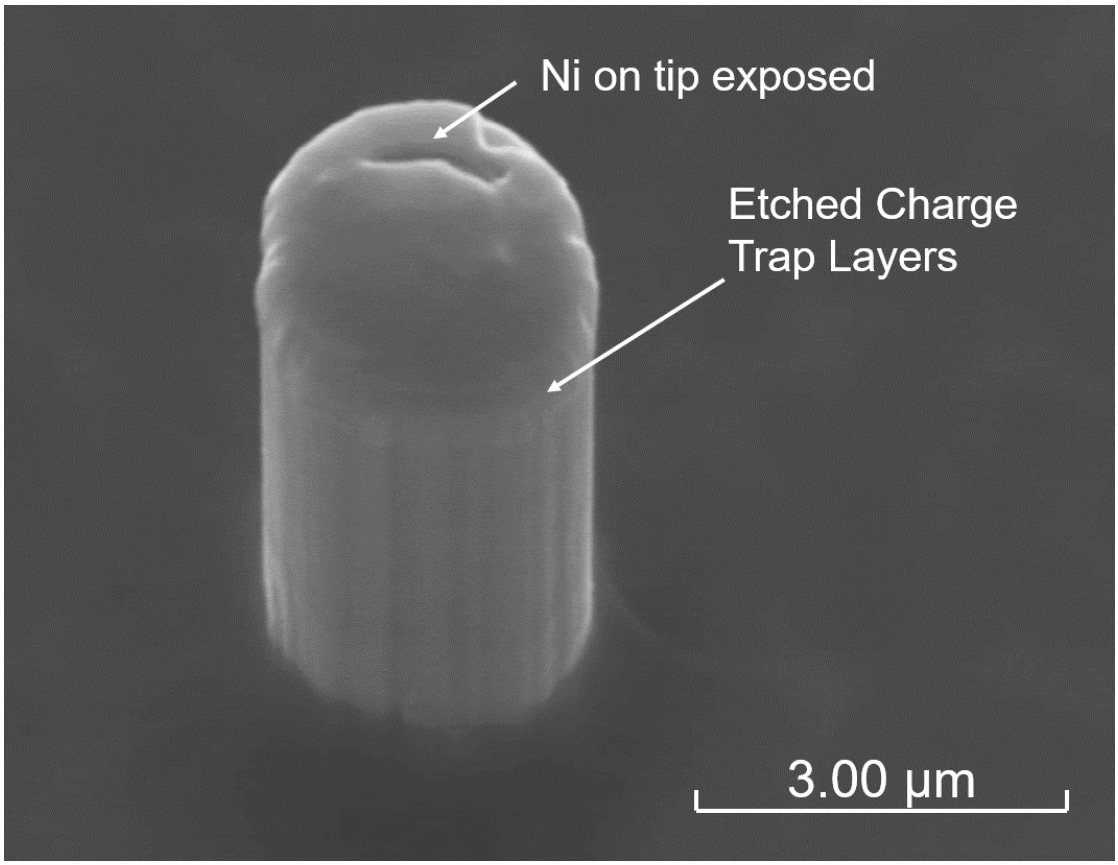


Figure 5.8: SEM image of nanowire with etched charge trap layer. Ridge/change in color visible signifying CTL etch.

5.1.5 Gate Metal

After the dielectric layers were etched, the photoresist was stripped, and gate metal regions were defined through a lift-off process. Ni was deposited as the gate metal through a directional thermal evaporation. The directional nature of the evaporation is extremely important since any continuous side-wall deposition up a nanowire will result in the drain and gate regions shorting together. 80 nm of Ni was evaporated on Sample 1 while nearly 95 nm was evaporated onto Sample 2. The thickness of the deposited metal dictates the overall gate length of the transistor. While a

thicker gate metal will be beneficial for electrical performance, there is a greater likelihood that it could result in a continuous metal film over the sidewalls. The directionality achieved is a combination of the alignment of the sample over the boat due line-of-sight nature of thermal evaporation, and the ability of Ni, when melted in a dimple boat, to agglomerate into an almost perfect, hemispherical shape that aids it in acting as a single point source during evaporation.

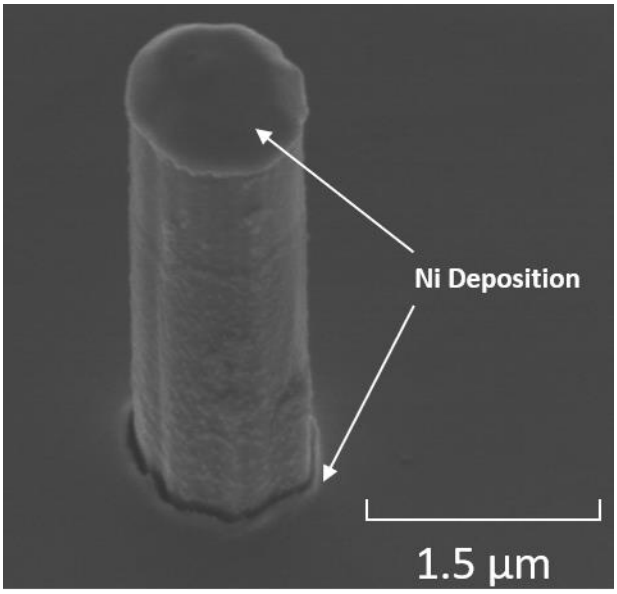


Figure 5.9: SEM image after gate metal deposition. Ni deposited on the base of the exposed nanowire and on nanowire tip

5.1.6 PDMS inter-layer dielectric

PDMS was again coated on both samples to completely cover the wires. PDMS, as mentioned previously, planarizes quite effectively even over large step-height differences. A RIE CF_4/O_2 plasms was used to etch back the PDMS. The etch was done to reveal just the tips of the nanowires. The tips of the nanowires still has Ni from the original patterning and definition of the

wires. Sample 1 had 14 1-minute etch back cycles to reveal the tips of the nanowires while Sample 2 had 13 1-minute etch cycles. It was found that Sample 2 had a slightly higher etch rate of PDMS as compared to Sample 1. This could be attributed to the differences in substrate size and therefore the relative amount of PDMS that needed to be etched back (and the overall thickness variation during processing from center-to-edge). Another possibility for this difference in etch rate could be due to the PDMS composition mixed and utilized for both samples.

5.1.7 Drain Metal

Drain regions were defined through lift-off once more followed by a Ni deposition through electron-beam evaporation. 40 nm of Ni was deposited conformally to ensure metal coverage was continuous over the tips of the wires and into the larger pad regions. A relatively thin Ni layer was utilized in this scenario to also enable observable light emission from the LEDs on the nanowires.

6. Electrical Results

Initial testing results are shown in this section. Figure 6.1 shows the family of curves (I_D-V_D) of a device tested with 4 wires on the double-side polished sample (Sample 2). The 4 wires are each 3μm in diameter. As shown, the results show similar electrical characteristics as a static induction transistor (SIT).[14], [26] The results also show gate control in that the drain current is modulated for a given drain voltage dependent on the gate voltage applied. Higher negative biases prove to show current flow limitation, signifying a channel with reduced carriers flowing through the nanowire vertically. Further reducing the gate voltage to more negative values would be expected to further limit current at a given drain voltage.

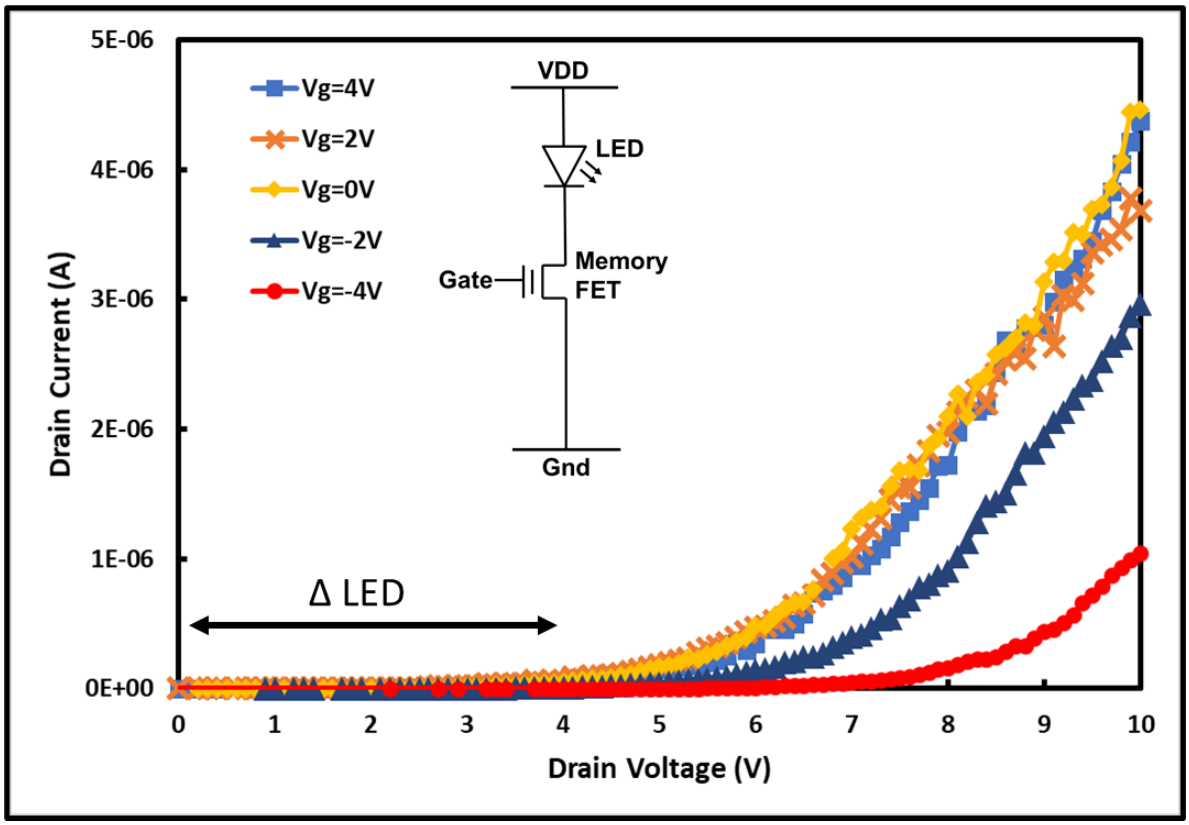


Figure 6.1: ID-VD Characteristics

Next, the memory characteristics of the device was also tested through I_D-V_G characteristics. The I_D-V_G characteristics are used to find the threshold voltage. A shift in the threshold voltage between the programmed and erased states signifies a functioning memory device. The initial I_D-V_G characteristics of the raw device was first measured from -4V to +4V of V_G with a drain voltage of 2V. The initial I_D-V_G test was followed by a +10V potential applied to the gate in order to trap electrons into the charge trap layer. I_D-V_G characteristics were again read from -4V to 4V of gate voltage. An erase was done through a -10V potential applied to the gate. I_D-V_G characteristics were again plotted. The +10V potential applied on the gate allows for electrons from the GaN nanowire to tunnel through the 3 nm Al_2O_3 layer to then be trapped within

the HfO_2. Figure 6.2 shows an overlay of the 3 plots. As shown, there is a threshold voltage shift observed between the initial state, programmed state and the erased state. The threshold voltage shift between the programmed and the erased state in this case was extracted to be around 2.5V. The threshold voltage shift here also closely correlates to the total memory window seen on the previously fabricated n-type Si capacitors for the same gate voltage sweep range of +/-10V, which was 2.44V. (Refer to Section 3.3.2).

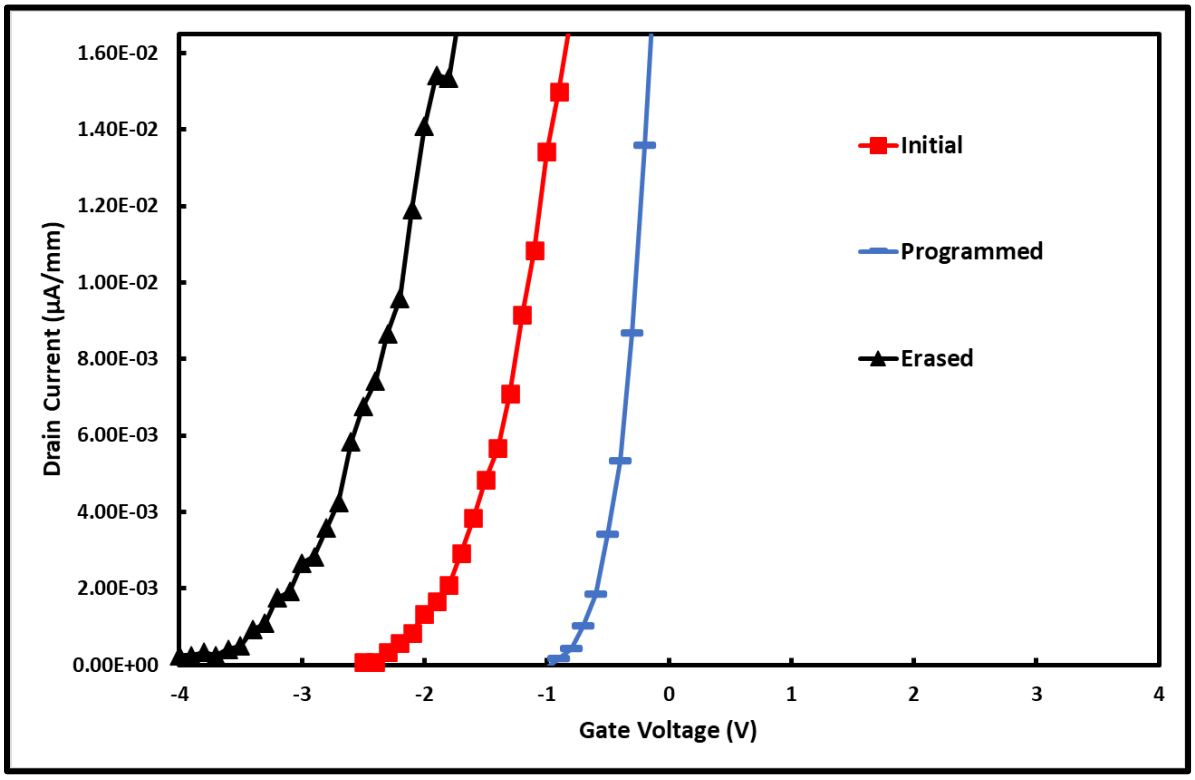


Figure 6.2: ID-VG of Initial, Programmed and Erased States

Figure 6.3 shows a microscope image of the LED lit during I_D-V_D electrical testing. An interesting phenomenon observed here is the blue-shift of the LED itself. While the initial LED structure was designed as a green LED, when fabricated into vertical nanowires at these

dimensions, there is a significant blue-shift. This has also been observed in literature as well.[30] The thin Ni drain deposited offers enough transparency to observe light emission through the tips of the nanowires. The blue-shift observed is a result of strain relief after nanowire formation within the lattice-mismatched InGaN/GaN MQW layers. The strong relaxation provides reduced piezoelectric polarization within the quantum wells. The reduction in the piezoelectric polarization leads to the light emitted being shifted to a higher energy (blue-shifted).

The results shown here are the first shown for a vertically integrated GaN nanowire memory device in series with an LED. The presented unique combination provides the basis for a number of prominent areas of application spaces and work. Low refresh rate micro-LED displays can leverage such an integration scheme and device to fabricate arrays. Such an integration scheme also provides a unique method to control brightness of individual nanowire LEDs. Results shown here also provide a basis for future possibilities of vertical GaN-nanowire non-volatile memory devices.

Figure 6.3:LED lit under microscope during testing

7. Process Development and Process Improvement

7.1 Re-metallization of nanowire tips

After the initial dry etch to form the tapered nanowires described in Section 5.1.1, the true height of the nanowires was difficult to find out due to the surrounding micro-masking on Sample 1. The heated KOH etch was done on the wires to clear the micro-masking to find the true height of the wires. It was observed that during this process, the Ni had significantly pulled back from the tips of the wires and had reduced in size. While this would not have been a significant issue for further processing, the true height of the wires defined was considerably lower than expected for the etch rate calculated. The overall etch rate of the sample (Sample 1) was significantly lower than the originally expected 600 nm/min. The reduced etch rate was due to increased micro-masking across the entire wafer. This meant that further dry etching would need to be done to get a taller wire. In this case, the Ni, no longer present over the complete surface of the wires, would no longer act as a hard mask and would result in an uneven step height for the nanowires.

Re-metallizing the tips of the wires was required for a further Cl_2-based dry etch. To re-metallize the tips, photoresist (MiR-701) was first spin-coated over the entirety of the sample. This was followed by a photoresist etch-back in an O_2-plasma for 1 min. to reveal the tips of the wires and the metal as shown in Figure 7.1 (a). Ni was then thermally deposited on the sample. The resist and the metal on top of the resist was then removed through an extended NMP soak.

Figure 7.2 (c) shows an SEM image of a wire that has been re-metallized and has gone through a second dry etch step. The step height clearly shows the delineation between the first and

second dry etch steps. After the second dry etch, Sample 1 was again etched to remove micro-masking and straighten the wire profiles in a heated KOH wet etch solution for 22 minutes.

While not all wires were successfully re-metallized a substantial percentage of the wires on the sample remained and continued through further fabrication steps.

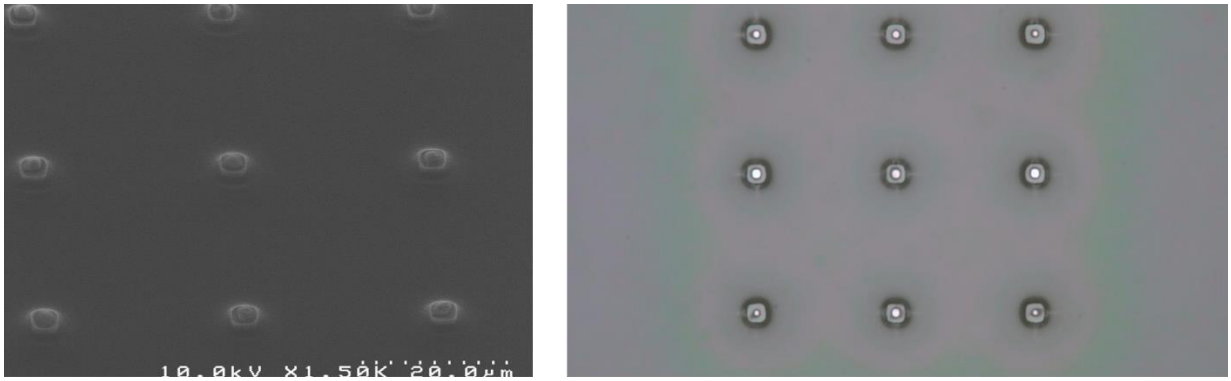


Figure 7.1: Ni metal etch pull-back issue (a) SEM image of wires with Ni tops and resist coating (b) Microscope image of Ni metal pull-back on wire tips

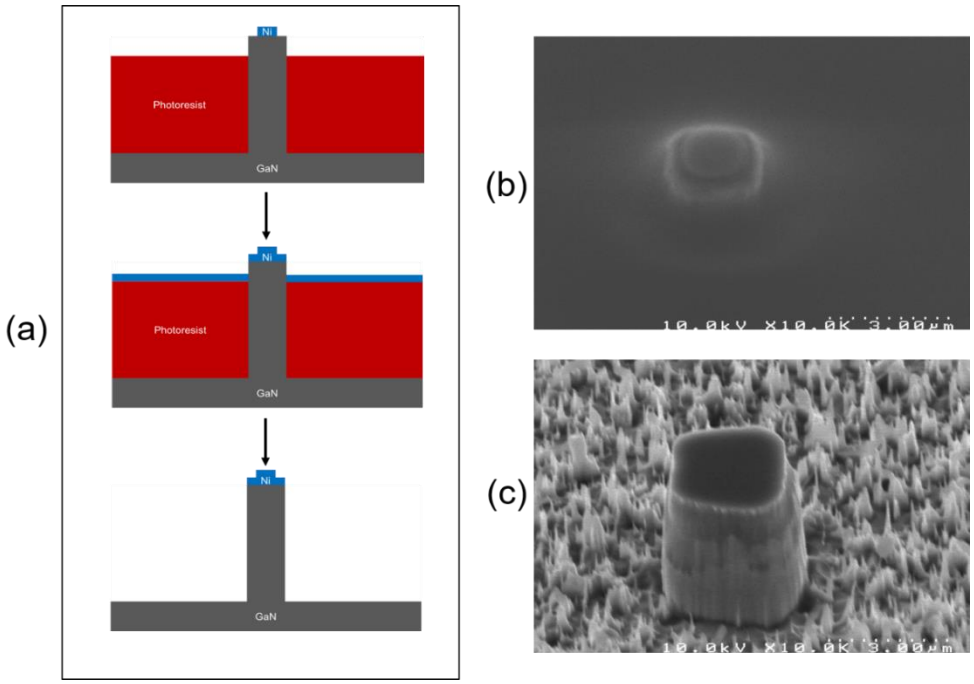


Figure 7.2: (a) Re-metallization process steps, (b) SEM image of nanowire tip with photoresist, (c) Second dry etch after re-metallization.

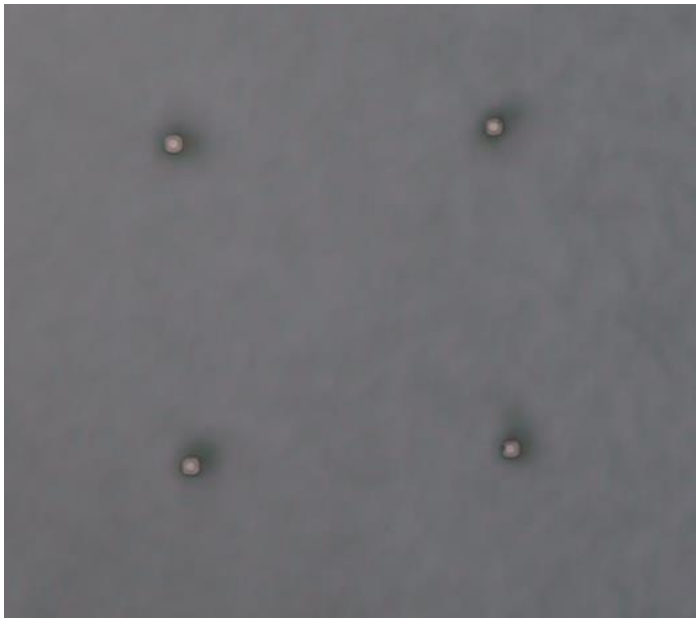


Figure 7.3: Microscope image of re-metallized tips.

7.2 Etching HfO_2 and Al_2O_3

A new HfO_2 and Al_2O_3 dry etch recipe was also developed and characterized. The etch recipe required a relatively low etch rate and extremely low damage to photoresist to prevent cross-linking. While wet-etching Al_2O_3 is possible, wet-etching HfO_2 is much harder and requires chemistry that would not be compatible with the previously deposited metal layers. A wet etch would also run the risk of delaminating the PDMS from the nanowires as well (or allowing etchant to remain within the space between the PDMS and the vertical GaN pillars). A Cl_2-based dry etch is also not possible in this instance since it would also etch the GaN nanowires. Instead, fluorine-based plasmas were investigated for an effective dry etch. Due to the relatively thin thicknesses of the films that needed to be etched, a dry-etch recipe that was capable of etching both films was preferred. This reduces any uncertainty associated with under-etching any of the layers.

Work in literature investigating etching HfO_2 films in a CF_4/Ar mixture in an inductively coupled plasma, suggested the need for a high DC bias voltage with a high forward RF power while at a relatively low process pressure. [31] It also showed the possibility to etch HfO_2 films with a pure CF_4 plasma as well. An RIE system was used in order to develop an etch recipe for HfO_2. Initial etch characterization was done visually on HfO_2 and Al_2O_3 films deposited with the ALD on Si pieces. Visual confirmation was obtained by observing the back side of the Si pieces. During deposition, the ALD system coats completely conformally and also deposits a thin ring of dielectric on the back of the wafers as well. The difference in refractive index of deposited and undeposited regions on the rough back-side of a Si piece is very visible. Separate Si pieces with 30 nm of Al_2O_3 and 15nm of HfO_2 were first put into a Trion Minilock RIE system with a pure

CF_4 plasma. After 4 1-minute cycles, both pieces showed a visually complete etch. Visually, very thin films appear transparent or completely clear. The visual confirmation was a simple confirmation that etching had indeed occurred without necessarily characterizing the etch.

Table 7.1 shows the recipe used on the Trion Minilock RIE for etching Al_2O_3 and HfO_2 films.

Table 7.1 : Recipe Details for Al_2O_3 and HfO_2 dry etch

Recipe Details	
Power	200 W
Pressure	15 mTorr
CF4	20 sccms
Time	60 sec/cycle

Si pieces were separately coated with 30 nm of Al_2O_3 and 30 nm of HfO_2 for further detailed characterization. The samples were measured using a variable angle spectroscopic ellipsometer (VASE) to find the etch rates. The samples were each measured after running 1-minute of the etch. Table 7.2 shows the measurements and mean-square error of the resultant fit used in the measurement given from the VASE. Initial thickness measurements were found to have a higher mean square error (MSE), and as the thicknesses reduced through multiple cycles, the

MSE also reduced considerably. This suggests that thicker values measured on the VASE are less accurate and the etch rates derived from the values obtained in further cycles are likely to be more accurate.

Table 7.2: Etch rate data and calculations for HfO_2 and Al_2O_3 films

	Cycle	**Thickness (nm)**	**MSE of Fit**	**Etch Rate (nm/min)**
HfO_2	0	34.06	123.00	
	1	26.10	63.45	7.96
	2	19.80	39.03	6.30
	3	13.50	19.84	6.30
	4	7.20	6.28	6.30
			Etch Rate Determined	**6.3 nm/min**
	Cycle	**Thickness (nm)**	**MSE of Fit**	**Etch Rate (nm/min)**
Al_2O_3	0	32.54	109.20	
	1	24.83	31.45	7.72
	2	17.42	4.41	7.41
	3	11.29	5.67	6.12
	4	3.77	6.78	7.53
			Etch Rate Determined	**7 nm/min**

Figure 7.4 shows the etch rate calculated per cycle for Al_2O_3 and the MSE for each measurement plotted on the secondary axis. While the MSE drops significantly after the first etch cycle, the etch rate is still varies between 6nm/min and 7.5nm/min. The variation here is still extremely small and can be taken into account when etching Al_2O_3 films with an over-etch to account for such minute differences. Figure 7.5 shows the etch rate calculated per cycle for HfO_2 and the MSE for each measurement plotted on the secondary axis. The MSE consistently drops as the HfO_2 is thinned. The reduction in the MSE also aids in improving the validity of the etch rate consistently obtained. A consistent etch rate of 6.3nm/min was obtained for HfO_2 when using the recipe developed.

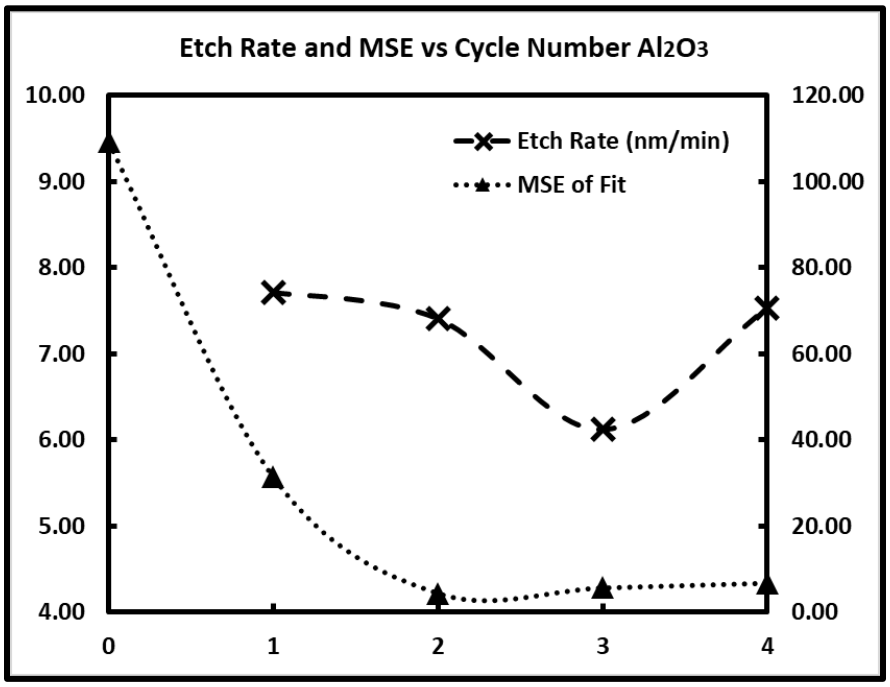


Figure 7.4: Etch rate and MSE per cycle of Al_2O_3

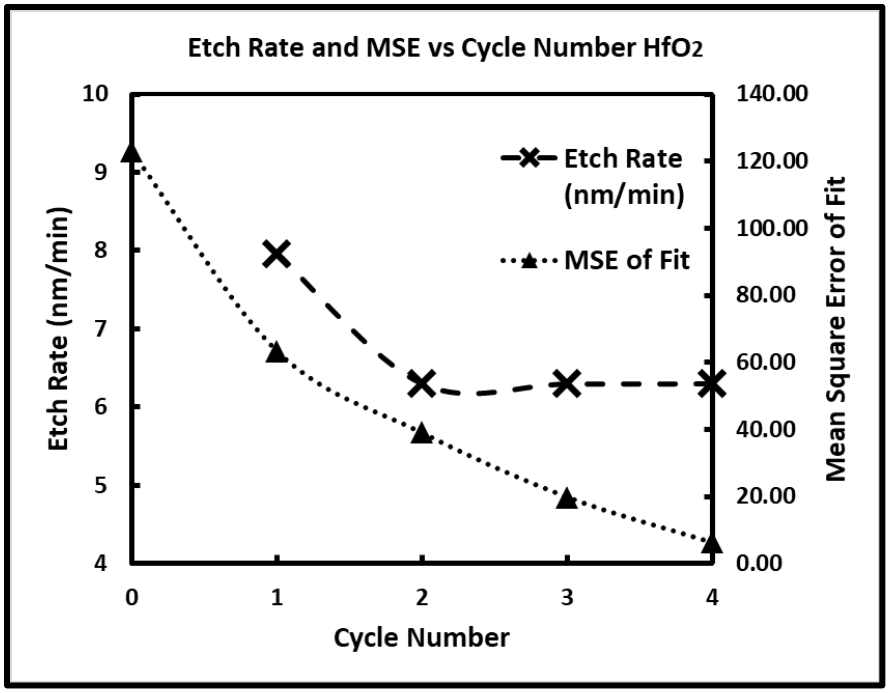
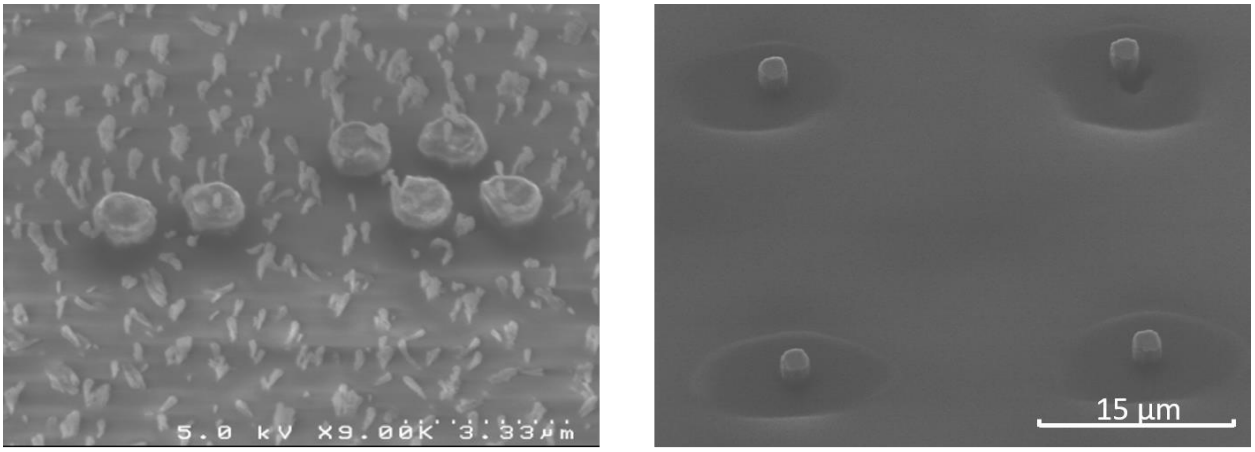


Figure 7.5: Etch rate and MSE per cycle of HfO_2

7.3 PDMS Etch Back

While there was an existing recipe for a PDMS etch back, after extended processing, a large amount of surface build-up and increased surface roughness would necessitate a 10:1 BOE HF dip to remove buildup of rough oxide-rich clusters for nearly 30 seconds when etching through large amounts of PDMS. The surface build-up and increased roughness was observed to be exaggerated after etching for 2 or 3 minutes continuously. The etch rate of the PDMS was also observed to increase when etching for elongated periods of time. A key factor that is thought to contribute to these effects is heat developed during the etch. To mitigate and minimize these effects, it was decided to etch in 1-minute cycles with 2-minute breaks. While the 2-minute breaks could have been optimized further for faster processing, this method of cycling proved effective

in keeping a nearly pristine PDMS surface with no build-up and minimal surface roughness. This also prevented the need to use acid that had previously also shown to aid in delaminating the PDMS from the GaN nanowire surfaces.



(a) (b)

Figure 7.6: (a) Particle build up during extended PDMS etching [Image courtesy of Dr. Matthew Hartensveld] (b) No observable particle build up with improved process

As Figure 7.6 (a) shows, there is evidence of considerable build up around the wires after an extended 3-minute PDMS etch. Figure 7.6 (b) shows the surface with wire tips revealed after 14 cycles of 1-minute etch steps with 2-minute breaks. The PDMS shows no signs of particle build up or increased surface roughness and continues to remain completely smooth. It is therefore quite evident that increased heat during extended etches causes the increased particle build up. Another method to possibly mitigate this would be to actively cool the substrate and bond the GaN-on-sapphire wafer to a thermally conductive carrier wafer for improved thermal contact instead. The presented process improvement in etching back PDMS was significant in that no acidic wet

chemistry was required to fabricate the devices which reduced the likelihood of any underlying metal from being etched away.

8. Methods for Further Scaling

8.1 Motivation and Background

A factor that would need to be addressed in terms of overall device performance for the device presented above would be in shrinking the nanowire dimensions. This shrinking would need to be reliable and controllable. At much smaller wire diameters and heights, the etch rate for continued shrinking would need to be slower. (The smaller the wire is, for the same etch rate, the faster the diameter will shrink) Smaller diameters (on the 10 nm scale) for the devices presented above would enable a number of key overall performance improvements. Figure 8.1 shows a GaN nanowire etched down from 150 nm in diameter down to 20 nm in diameter through a heated KOH etch solution for 70 minutes. Continued etching of such a nanowire to even smaller diameters without a self-limiting process would lead to either complete etching of the wires themselves or an insufficient etch with an added variation in wire diameters across a sample.

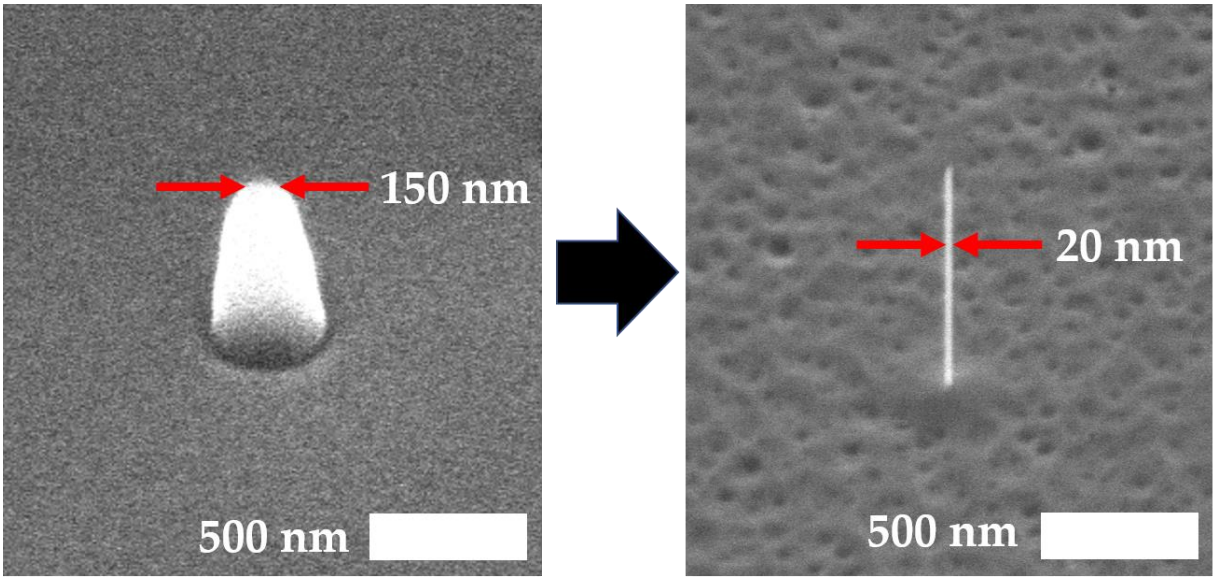


Figure 8.1: GaN nanowire etched from 150 nm diameter to 20 nm diameter through KOH wet etch [32]

For the devices presented and realized above, the smaller diameters would enable greater amount of gate control since the gate will actively be able to pinch the channel off. This would also greatly improve the overall leakage current. A completely pinched-off channel will prevent any current flow through the core/center of the wire.

Smaller wire diameters have also been shown to shift threshold voltages in a positive direction. This is especially attractive since it would shift the currently presented depletion-mode devices into enhancement-mode devices.

This leads to the motivation of investigating and analyzing novel etching techniques. One such technique studied here is digital etching. Digital etching is essentially a self-limiting etch technique.[33]–[36] What this means is, once a few layers of a material (in this case GaN) are taken off, no more subsequent layers are further etched. Work in literature has shown digital

etching of AlGaN layers as a low-damage, controllable etch technique for gate-recessing in high-electron mobility transistors (HEMTs).[34], [35]

In digital etching, an O_2-plasma is used to oxidize GaN to form Ga_2O_3. The N_2 formed during this oxidation is typically pumped away. The Ga_2O_3 formed is then removed through a reaction with HCl. [37]

$$4GaN + 3O_2 \rightarrow 2Ga_2O_3 + 2N_2 \qquad \textit{Equation 8-1}$$

$$Ga_2O_3 + 6HCl \rightarrow 2GaCl_3 + 3H_2O \qquad \textit{Equation 8-2}$$

This method theoretically allows for a controllable etch rate of GaN since the oxidation of the GaN surface is dependent on the RF bias power in an ICP system to determine the depth to which O-radicals can penetrate and react. The HCl in this instance allows a self-limiting process since GaN does not react with it. This effect has been reported and is quite apparent on the c-plane due to the alternating nature of Ga and N atoms.[37] However, this effect may be quite different for planes where Ga and N atoms are both exposed to the plasma and wet chemistry simultaneously. It is therefore possible that the m-planes and a-planes of GaN may be affected in a significantly different manner during this cyclic process compared to the c-plane. This work will be a first attempt in trying to characterize the effects of such an etch mechanism on the vertical surfaces of GaN.

8.2 Process Flow and Method

A labelled grid on GaN-on-sapphire samples was formed using a metal lift-off process with Ni. This allowed easy recognition of the same nanowire regions being imaged and measured before, during and after cyclic processing. 150nm silica spheres were diluted with DI water from a concentrated suspension and then coated on samples to deposit sparsely dispersed spheres over the GaN surface. A PlasmaTherm APEX ICP system was used for the initial nanowire formation using the silica spheres as an etch mask, using 10sccm of Cl_2, 40 sccm of Ar, an ICP power of 500W with a bias power of 225W at 5mTorr. The resulting nanowires were then etched further in a heated KOH solution for 15 minutes at 80°C. The KOH solution was made through diluting 10ml AZ400K, which has 2% wt. concentration of KOH, with 15ml of DI water. The heated KOH solution also etches the SiO_2 spheres on the surfaces of the nanowires at the same time, thereby exposing the GaN c-plane on the tips of the nanowires.

Select locations over the total sample area were imaged with a MIRA3 TESCAN SEM in 15 different locations. 4 cycles were completed and imaged in the same exact locations to note specific differences in height, width and general shape of the nanowires. A further 6 cycles were again done to note if differences were linear, predictable, and consistent. A single cycle consisted of a 5-minute run in the ICP with 40sccm of O_2 with a 75W bias power and an ICP power of 450W at 8mTorr pressure followed by a 90 second dip in 6.7 wt.% HCl solution.

Figure 8.2 shows the overall process flow summarized to form the nanowires and one cycle of the digital etch.

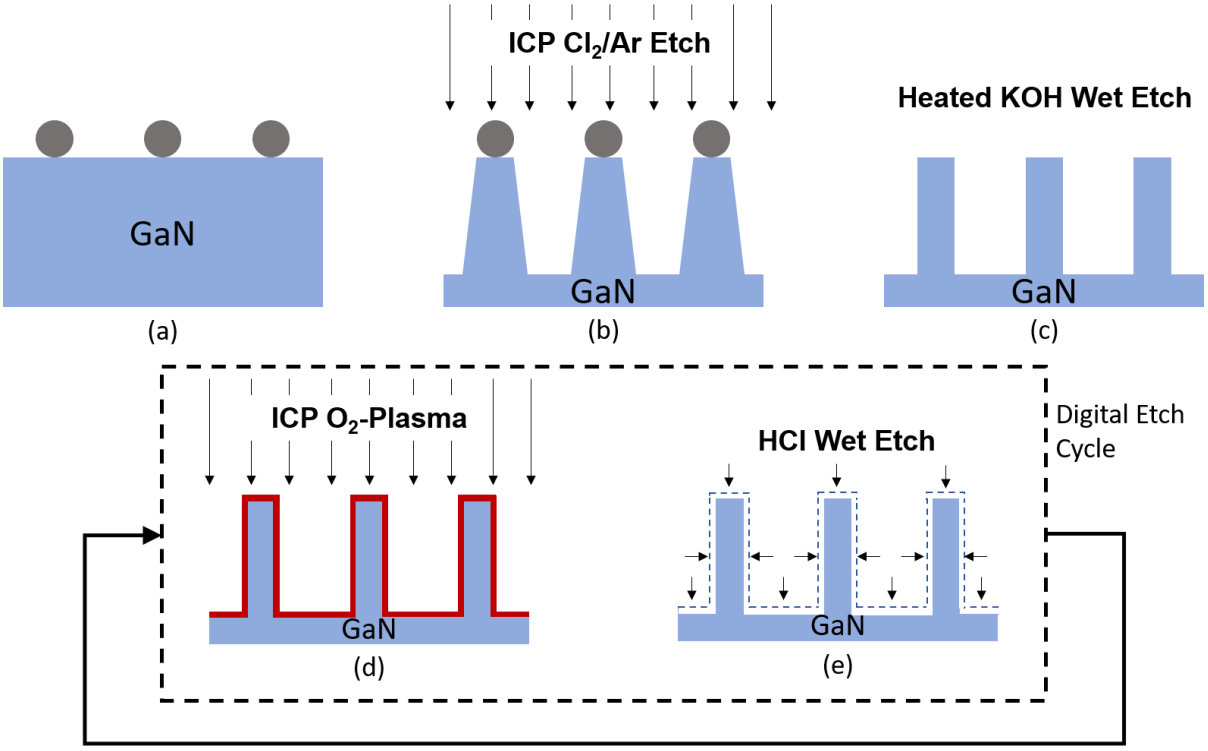


Figure 8.2: Digital Etch Process Flow

8.3 Results and Discussion

The heights and widths of the nanowires were measured before the first cycle, after 4 cycles, and after 10 cycles. SEM images at the same locations were taken and analyzed to measure the average height and average width of the nanowires.

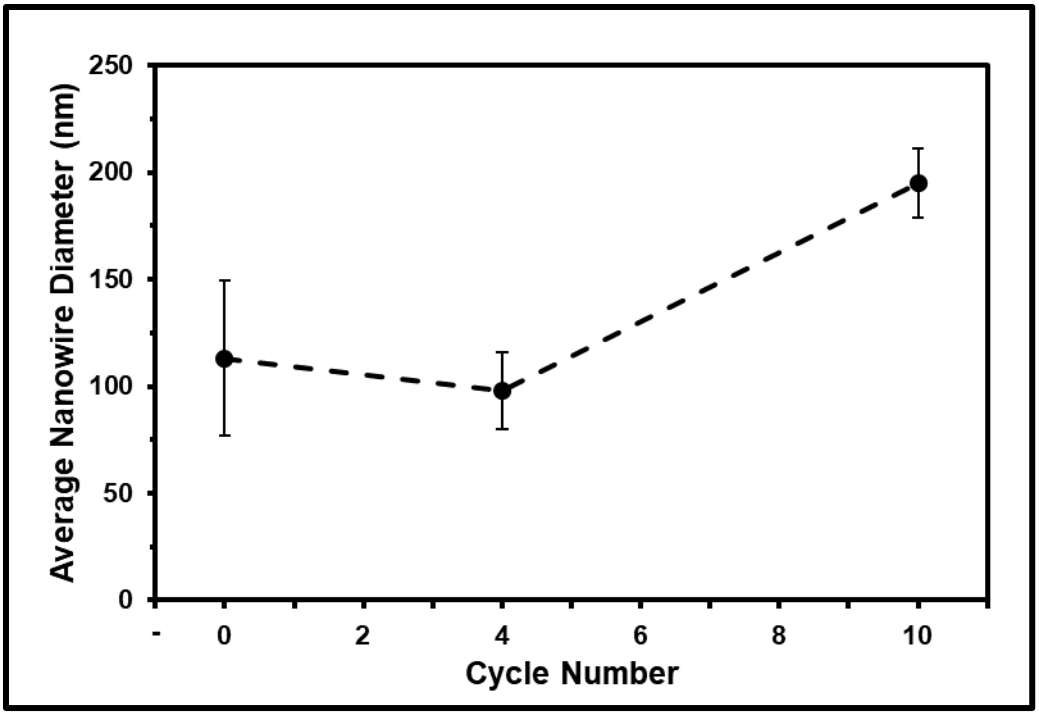


Figure 8.3: Average Nanowire Diameter vs Cycle Number

Figure 8.3 shows the average diameter of the nanowires measured. Comparing the diameters before the 1st cycle with the average diameter after the 10th cycle, the average diameter increased by 72.7%. In those same cycles, the average height of the nanowires measured decreased by 18.0%. In the same number of cycles, it was noted that the standard deviation of the average nanowire diameter reduced from 36nm to 16nm. In terms of nanowire diameter, this shows a limiting factor being reached with increasing number of cycles.

The initial reduction followed by the net increase in nanowire diameter can be attributed to a combination of factors. The initial diameter decrease was most likely a result of consistent etching along sidewall surfaces where Ga_2O_3 had formed thin enough layers due to the oxygen plasma having a lesser effect along vertical planes compared to the tops of the nanowires. This

would therefore cause the HCl to etch off these layers of Ga_2O_3 completely. As cycles continued, the inconsistent vertical surface, where there are regions of exposed GaN and regions of exposed Ga_2O_3 may have caused an increased buildup of Ga_2O_3, which, due to the dilute HCl concentration and fairly vertical O_2 atom directionality would result in an increased build-up of Ga_2O_3 along the bases of the nanowire. This would further be compounded by O_2-plasma atoms bouncing off the GaN surface onto the bases of the nanowires causing the wires to increase in diameter at a much faster rate near the GaN planar surface as compared to the tip. The nanowire tips also have the increased effect of O_2-plasma being much more vertically directional even in an ICP system.

Another aspect to consider are the exposed crystal plane surfaces themselves. Prior to the cycles starting, it is known that the c-plane and the m-planes are exposed as a result of the original crystal growth, and the crystalline nature of the KOH wet etch. The surface of the c-plane contains alternating Ga-layers with N-layers, while the m-plane contains both Ga- and N- atoms simultaneously exposed. The O_2-plasma step would cause the initial reaction between exposed Ga-regions and oxygen radicals, while the N- atoms would form N_2 and would get pumped out of the chamber. Along the c-plane, in a planar structure, this would result in layers of Ga atoms forming Ga_2O_3 resulting in a controlled etching as evidenced in previous work of etching planar AlGaN. Along the m-planes and more vertical surfaces, this would result in uneven distribution of Ga_2O_3 forming along sidewalls. This would contribute to the build-up observed as well since Ga_2O_3 would unevenly form along sidewalls as compared to the c-plane.

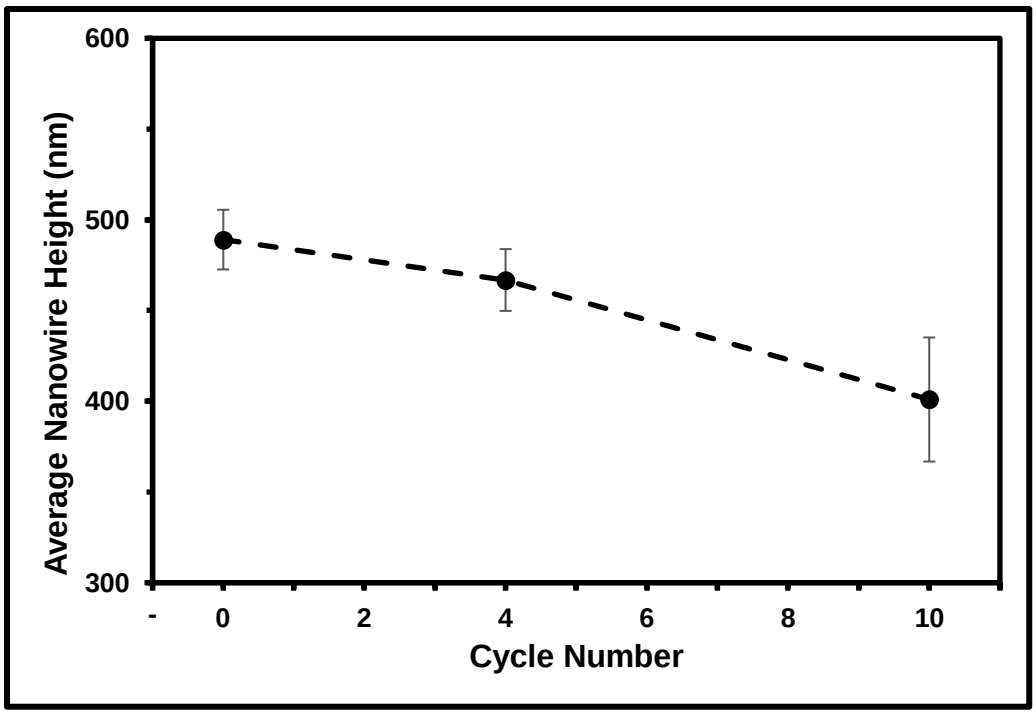


Figure 8.4: Average Nanowire Height vs Cycle Number

Figure 8.4 shows the average vertical height difference observed for all nanowires. From the results, it is estimated that the nanowires were etched vertically by 8.81nm per cycle. Taking into consideration the combination of reasons aforementioned, along with topographical differences at the tips of the nanowires, as the etch proceeded, the etch rate was faster for the last 6 cycles as compared to the first 4 cycles. While the nanowires started with a flat c-plane on its surface, once the c-plane was etched away, and the nanowires formed rounded tips, it resulted in much faster etching due to more exposed sites with greater Ga- atoms available for further reaction with incoming O-radicals. This, in addition to the majority of O-atoms bombarding the nanowires vertically, possibly resulted in faster, and more pronounced vertical etching.

Figure 8.5 (a), (b) and (c) shows a set of SEM images of the same nanowire on the sample taken prior to digital etching, after 4 cycles and after 10 cycles respectively.

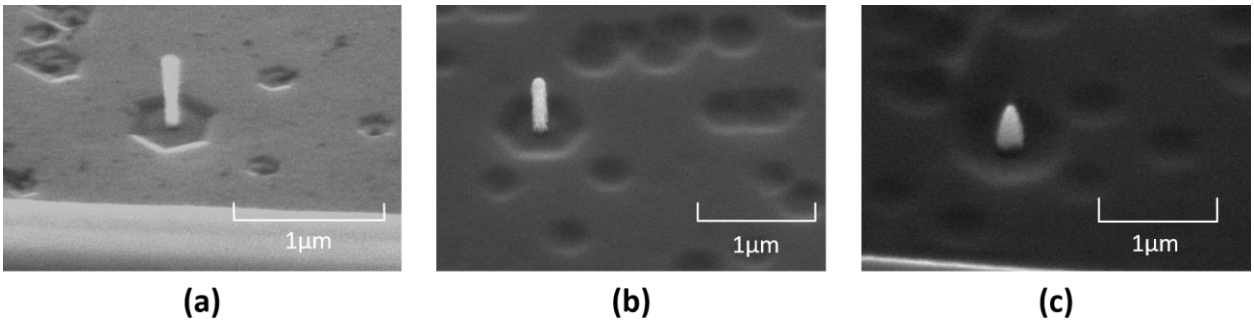


Figure 8.5: (a) Nanowire prior to digital etch, (b) Nanowire after 4 cycles, (c) Nanowire after 10 cycles

8.4 Summary

A novel etch technique to controllably shrink nanowire diameters was investigated. The etch characteristics along the vertical surfaces of GaN was characterized. While the nanowires shrunk in height vertically with this technique, the diameter showed a net increase. This was attributed to a continuously increased build-up of Ga_2O_3 along the vertical sidewalls. For further work investigating this etch technique for further shrinking, stronger HCl concentrations and longer HCl etch times seem to be viable paths. Other avenues to investigate would be to lower the overall directionality of the O_2-plasma used for initial oxidation.

9. Conclusion and Future Work

A novel GaN-based vertical memory device integrated with an LED has been proposed and demonstrated for the first time in this work. Unique methods to shrink nanowires further controllably were also investigated. Effects of the etching technique along the vertical surfaces of GaN wires were investigated for the first time. A high-κ dielectric memory stack was verified and characterized to operate with both n-type and p-type Si at RIT for the first time. The stack was selected for its high possibility of working and integrating well with the GaN material system and with the vertical, gate-all-around architecture proposed. Unique processes were also developed to metallize tips of nanowires without the need for lithography. Processes were also developed to dry-etch HfO_2 and Al_2O_3 dielectrics in a fluorine-based plasma. Improvements were made to existing processes, especially a key etch-back process step for PDMS.

Initial electrical testing of the fabricated device was done and showed evidence of a working memory device and a working LED. A threshold voltage shift of 2.5V was found for a +/-10V program and erase on the devices tested.

Investigating digital etching techniques showed an almost steady etch rate vertically for an exposed nanowire while an overall increase in diameter was observed. This was attributed to Ga_2O_3 possibly being built up along sidewalls without insufficient wet etching to completely remove the Ga_2O_3 along sidewalls.

Based off the work presented, multiple areas can further be explored. One is investigating the memory stacks with alternative high-κ dielectric materials and stacks. Just within this area and

field, several combinations and tests can be investigated and verified through making capacitors on Si. This has direct applications within current high-κ charge-trap memory devices. Investigation into combinations utilizing Al_2O_3, HfO_2, ZrO_2, TiO_2 all done through ALD techniques can yield a wide variety of memory and performance characterization. Further work could investigate the effects of utilizing multiple layers stacked together within the charge trap layer to widen the overall memory window, or the effects of annealing in different ambient conditions to aid in widening or suppressing memory windows. Supporting this work, still further areas of work would be to investigate etching and processing techniques with the different dielectric materials investigated. Apart from charge trap flash memory, alternative types of memory, such as ferroelectric memory could be investigated for faster read/write times, longer retention times, and even lower power consumption.

Other work would involve possibly fabricating the device realized here at even smaller scales. This would improve the overall leakage current and also shift the threshold voltage to the right (more positive threshold voltage). Scaling up multiple arrays of the memory devices integrated with the LEDs would also be worth investigating. Schemes and mechanisms to read, write and erase addressable arrays with integrated memory devices would yield improvement in multiple areas within current micro-LED displays. Avenues to integrate memory devices with power devices or high-frequency devices are also extremely interesting topics worth exploring.

Further testing and detailed investigation into the memory and retention characteristics of the devices fabricated would also be hugely beneficial. Temperature tests, write/erase efficiency, and write/erase speed testing along with long-term retention characteristics could all be performed to further quantify and characterize the devices realized in this work.

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