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Advanced III-Nitride LEDs for Display Applications

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Advanced III-Nitride LEDs for Display Applications

by

Matthew T. Hartensveld

A dissertation submitted in partial fulfillment of the requirements
for the degree of Doctorate of Philosophy in Microsystems Engineering

Microsystems Engineering Program
Kate Gleason College of Engineering

Rochester Institute of Technology
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Committee Approval:

We, the undersigned committee members, certify that we have advised and/or supervised the candidate on the work described in this dissertation. We further certify that we have reviewed the dissertation manuscript and approve it in partial fulfillment of the requirements of the degree of Doctor of Philosophy in Microsystems Engineering.

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ABSTRACT

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Dissertation Title: Advanced III-Nitride LEDs for Display Applications

Gallium Nitride (GaN) light emitting diodes (LEDs) are viewed as the next generation of display technology as a replacement for both liquid crystal displays (LCDs) and organic light emitting diode (OLED) displays. GaN based LEDs offer immense improvements in terms of efficiency, reliability, and resolution as compared to these conventional display technologies. New device opportunities are presented with the advent of LED displays, however there are a number of key challenges that also need to be addressed. Displays rely upon transistors in order to individually control the brightness of each color in a pixel. LED displays are no different, though there are no straightforward ways to pair transistors with LEDs. Furthermore, LEDs still leave room for improvement, suffering from poor p-type activation, single color emission, and inflexibility. Though with the promise of GaN LEDs, new integration approaches are realized here to overcome these limitations.

To address the challenge of transistors and LEDs, an innovative integration between LEDs and field effect transistors (FETs) has been demonstrated. The integrated LED-FET devices lead to dramatic increases in resolution, substantial decreases in processing steps, and considerable area savings. Device and simulation results are presented, with further scaling optimizations outlined.

The idea of full color integration has been a challenge for LEDs, where often multiple material systems are combined in order to realize these displays. Multiple materials translate to higher costs and lower resolution, as separate fabrication is performed to create these LEDs and then transfer the LEDs together. Monolithic approaches have been pursued, though necessitate the use of rare-earth materials. Instead, the structure of the LED is exploited in order to create the full range of LED colors from red to blue in a simple, efficient, monolithic format to demonstrate multi-color μ-LEDs.

Several novel devices and integration schemes are also presented that expand upon the existing device applications. Work developing a novel nanowire lift-off mechanism is presented which allows for both substrate reuse, as well as flexible devices. A capacitor-LED integration mechanism is demonstrated to enhance hole activation and utilization. AC operating LEDs are demonstrated through tunneling. Integration of high-power devices are additionally investigated for driving higher power LEDs. Together these breakthroughs provide a pathway for LED displays and beyond.

ACKNOWLEDGMENTS

The people who made a difference through scientific study, who changed the world, were the ones who not only had a dream, but had the courage to pursue it. “No individual has any right to come into the world and go out of it without leaving behind him distinct and legitimate reasons for having passed through it.” –George Washington Carver.

Through repairing xbox 360s as a freshman, to then starting a xbox repair company, which led to creating a garage cleanroom, I have had support from my family. A hands-on heavy equipment mechanic father and a creative art teacher mother provided me with the attributes that attributed to my creativity. Using limited resources, I was able to forge innovation by having a DIY attitude, which led to seeing problems from different angles. I always have them to thank for their support, conversations, and insight.

I enrolled at RIT for their Microelectronics Program, excited to embark using their cleanroom, especially as a freshman. I then grew interested in LED fabrication my second year following an REU at UCSB. Dr. Zhang was starting and establishing LED research at RIT at the time and welcomed me into her group to participate in further research. Dr. Zhang has always been open to new ideas, providing me with insightful suggestions and feedback. Her openness to novel ideas allowed me the freedom to develop revolutionary techniques and devices, for this I will always be thankful.

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I want to thank my committee, Dr. Mohseni, Dr. Hubbard, and Dr. Ni for joining me on this journey. I also have great respect for each of these men and they are by far some of the best faculty at RIT. They are experts in their respective areas of microelectronics. I thank them for their insight and feedback on the various stages of my PhD.

Having great colleagues who have become great friends is one of my highlights at RIT: Yu Kee Ooi, Cheng Liu, Bryan Melanson, Gildas Ouin, Vijaygopal Thirupakuzi Vangipuram, and Matthew Seitz. I truly appreciate their insight when bouncing concepts off them, creating new project ideas with them, and developing new devices together. They are always willing to help in the lab and make the time more enjoyable.

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TABLE OF CONTENTS

Chapter 1

INTRODUCTION AND BACKGROUND

1.1 Overview of Introduction and Background Chapter

The technological advent of LEDs has been a recent achievement made possible by the breakthrough in p-type dopant activation by Shuji Nakamura, making the first blue LEDs in the early 1990s [1]. Blue LEDs have significance, as optical down-conversion with yellow phosphors is used in order to covert blue light into white light. Since that time, research has evolved to include GaN LEDs emitting across the visible spectrum and into the UV [2-4]. GaN possess a wide energy bandgap of 3.4 eV which can be increased though incorporation of aluminum, or decreased with the addition of indium. The ability to tune the direct bandgap of GaN allow for color tuning for different device utilizations. GaN LEDs find widespread commercial use for numerous lighting applications and have extensive manufacturing infrastructure in place [5-6].

Meanwhile, current display technology is reaching its practical limitations as the liquid crystals and OLEDs that make up conventional displays are struggling to be reduced further in size and suffer from relatively poor performance. In response, inorganic LEDs are being pursued as the next generation of display technology due to higher efficiencies (70% vs. 5- 7%), high reliability, and the ability to be manufactured at the nanoscale [6]. GaN LEDs have the same and expanded benefits over OLEDs without the same processing drawbacks, such as sensitivity to the environment [7]. Making use of the solid-state nature of GaN, the device sizes are only limited to the size of atoms instead of polymers, and GaN LEDs benefit from standard semiconductor manufacturing processes. Major tech and display companies such as Google, Apple, Facebook, Samsung, and LG are all pursing the technology due to the inherent benefits recently made possible.

However, pairing the well-established LEDs with the controlling transistors has been the key challenge. There are a number of integration approaches explored that need to be developed and further improvements made in order to realize LED based displays. This topic is an ongoing challenge, as conventional thin film transistors (TFTs) are problematic to integrate [6]. LEDs also suffer performance limitations from poor p-type activation that adds resistive losses to devices [8]. Poor light extraction efficiency (LEE) is common with LEDs due to the high refractive index of 2.5 vs. 1 of air [9]. The work here addresses these issues in novel ways and introduces original device applications stemming from the work.

- **Driving Circuitry**

Conventionally LEDs have been fabricated from a separate materials system to the controlling transistors, making integration potentially challenging. Though there are critical reasons why LEDs need to utilize transistors in order to realize even moderate resolution displays.

Displays are arrays of individual pixels where each pixel can be further divided into three sub-pixels that compose a red, green, and blue emitter. There are three categories of display sub-pixels which can be fabricated, either a passive matrix, quasi-active, or active matrix.

- **Passive matrix**

The passive matrix is the simplest and most straightforward to design, though consumes the most power and presents limits on the number of pixels. The technology is still utilized on small screens, or screens with a low pixel density due to the simplistic design with lower cost. A basic example of a passive matrix is illustrated in Fig. 1, showing two rows and two columns that would be repeated multiple times.

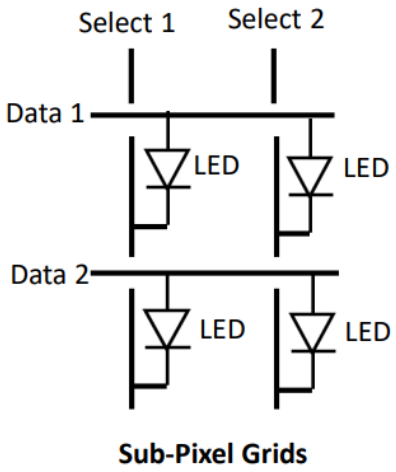

Fig. 1. 2x2 Passive matrix LED array.

To turn on an LED one row is selected by applying a positive bias, while a negative bias (or ground) is applied to a selected column. The non-selected rows and columns remains off, with the selected LED only turning on for a short time. The selected LEDs receive a large current spike to produce a high level of brightness, as illustrated in Fig. 2(a) [10]. Subsequent rows are selected

with corresponding columns to turn on additional LEDs as shown in Fig. 2(b) to complete an image [11]. The stepped approach to create an image has to be utilized, as if not, unwanted LEDs turn on, as can be determined if the perceived image of Fig.2(b) is created in a single step. These steps between selected LEDs is done faster than the human eye can perceive, where the brightness pulse is averaged across the frame by the human eye. Where the observer only interprets the combination of each rapid step [11].

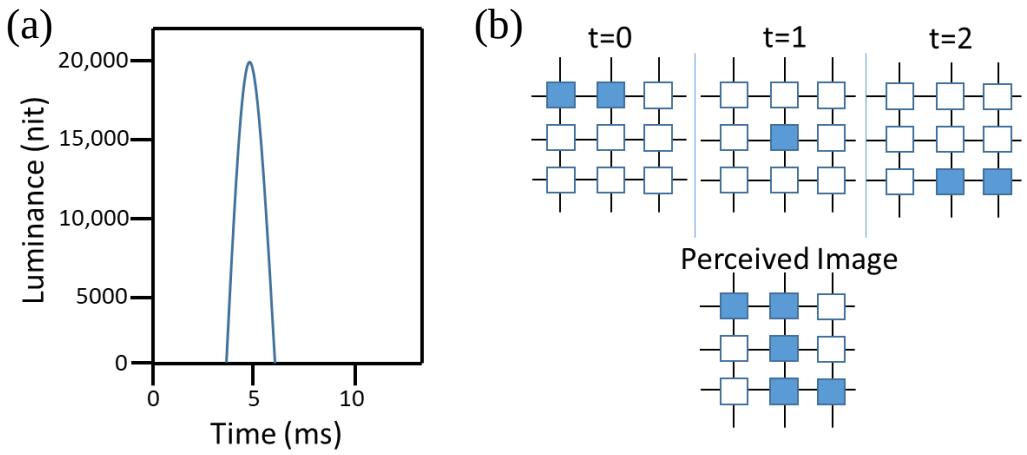

Fig. 2. (a) Passive matrix luminance spike, (b) Image creation through pixel driving.

The concept in a passive matrix is relatively straight forward to implement, though there are a number of problems that exist and are exacerbated with larger displays. The large current spike applied in a passive matrix has a high current density of greater than 10 A/cm^2 [12]. The efficiency of LEDs typically peaks between 1-10 A/cm^2 and degrades, a problem known as the efficiency droop [13]. LEDs are also known for higher leakage levels compared to transistors, that when connected together in a large matrix lead to significant parasitic losses [11]. Each pixel must be regularly supplied by current pulses, as the LEDs themselves are unable to hold the charge state. Furthermore, LEDs can also have a high capacitance, that add together when multiple LEDs are

connected in series, leading to RC delays [11, 14]. Due to these issues, as the number of pixels in the display increases, the display becomes less feasible.

- **Quasi-active matrix**

Use of an additional transistor can help mitigate the problems of a passive matrix, and is commonly known as a quasi/semi-active matrix [14]. Transistors have a lower level of leakage compared with LEDs, that can lead to less parasitic current for LEDs in the off-state [14]. Higher contrast and higher pixel density displays are able to be achieved compared with passive matrix displays. An example of a quasi-active matrix is shown in Fig. 3. Different design iterations can be utilized, putting the transistor either before or after the LED for isolation.

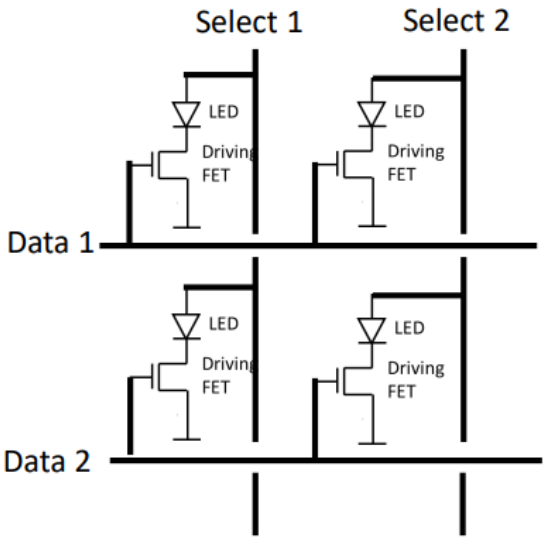

Fig. 3. 2x2 quasi/semi-active matrix with LED in series with the transistor.

- **Active matrix**

The active matrix display type is the most complex design, provides the highest performance, and is the most widely commercialized [11]. The most basic construction consists of

2 transistors and 1 capacitor, known as the 2T1C design, schematically shown in Fig. 4(a) in the n-type metal oxide semiconductor field effect transistor (NMOS) configuration. A pass transistor is connected to the row and column of the matrix and is utilized to charge up the storage capacitor Cs. The capacitor holds the voltage on the gate of the driving transistor which determines the current flow through the LED. The low leakage of the transistors and capacitor lead to charge storage, which can maintain the frame over a passive or quasi-active matrix. Instead of the NMOS configuration most µ-LEDs employ a p-type metal oxide semiconductor field effect transistor (PMOS) configuration [15]. The use of a PMOS configuration is commonly employed to µ-LEDs commonly utilizing flip-chip bonding with silicon and a common n-type layer with individually addressable p-type regions. The PMOS configuration is shown in Fig. 4(b), where capacitor is referenced to the supply voltage and the position of the LED and driving transistor are swapped [15]. Though more common, the PMOS configuration suffers from worse performance due to the lower hole mobility in transistors relative to the electron mobility and correspondingly larger sizes due to lower current driving capability [11].

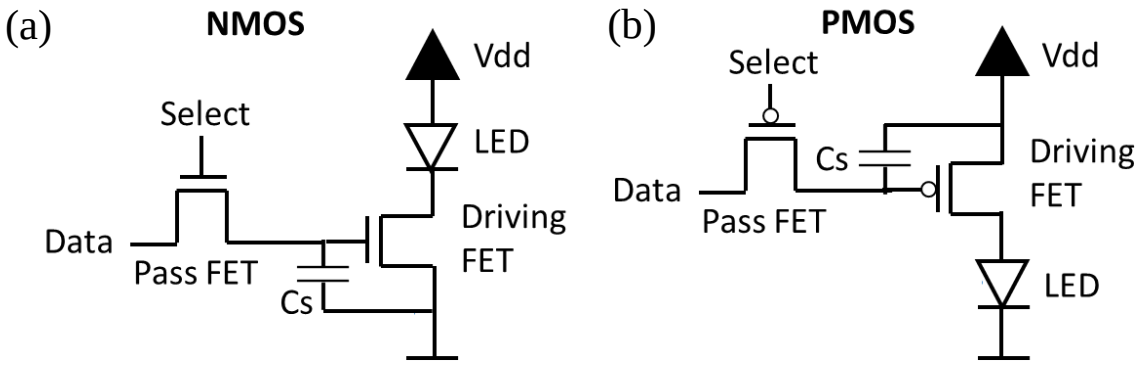

Fig. 4. (a) NMOS 2T1C configuration, (b) PMOS 2T1C configuration.

The basic 2T1C active matrix configuration is often expanded upon due to the variation in the threshold voltage that exists in particularly the driving transistor when making use of TFTs.

The basic sub-pixel circuit can contain greater than transistors when TFTs are utilizing, consuming a significant area, trying to compensate for threshold voltage shifts that arise during the crystallization process or due to aging effects [16].

The active matrix displays, due to the charge storage nature, does not necessitate the use of current spikes and instead uniform illumination can be utilized, Fig. 5(a). As the luminance is applied throughout the frame, the current density can be decreased, leading to higher LED efficiency. The steady state nature of the luminance also makes the display appear brighter and sharper to the observer over a passive or quasi-active matrix. The addressability of an active matrix can be similar to a passive, though the LEDs stay on, more accurately creating the perceived image as shown by Fig. 5(b).

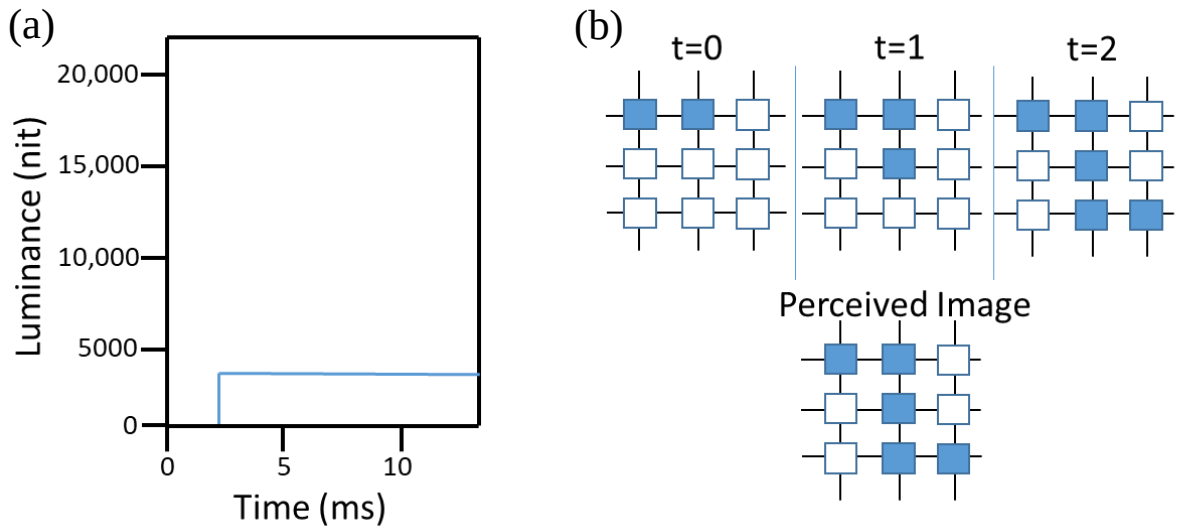

Fig. 5. (a) Active matrix uniform luminance, (b) Imaging formation with active matrix.

Due to the voltage controlled current flow provided by the driving transistor, increased grayscale levels can be achieved, creating better color accuracy. The separation of the LED from the rows and a columns of the matrix lead to fast switching for high refresh rates. Even though the

active matrix represents a more complex integration process, there are significant benefits that make this technology the mainstay of modern displays.

- **External control circuitry**

Regardless of passive, quasi-active, or active matrix utilization, the display itself is a matrix. Up to thousands of rows and columns make up high resolution displays, though the data input in done in a serial not parallel format. Shift registers are typically employed as the external control circuits to convert from the serial input to a parallel output to drive the rows are columns of the display. Latch circuits are also utilized follow the shift registers to select between sub-pixels for color. An overview of external control circuitry with the display is shown with the 2T1C configuration used as the sub-pixels in Fig. 6. Typically, greater demand is placed on the column drivers operating in the MHz, which connect to the drain of the pass transistors, in order to offer additional pulse width modulation (PWM) control [17]. Constraints on the row drivers are a bit more relaxed, operating at kHz speeds, in order to select the individual sub-pixels by addressing the gate of the pass transistor.

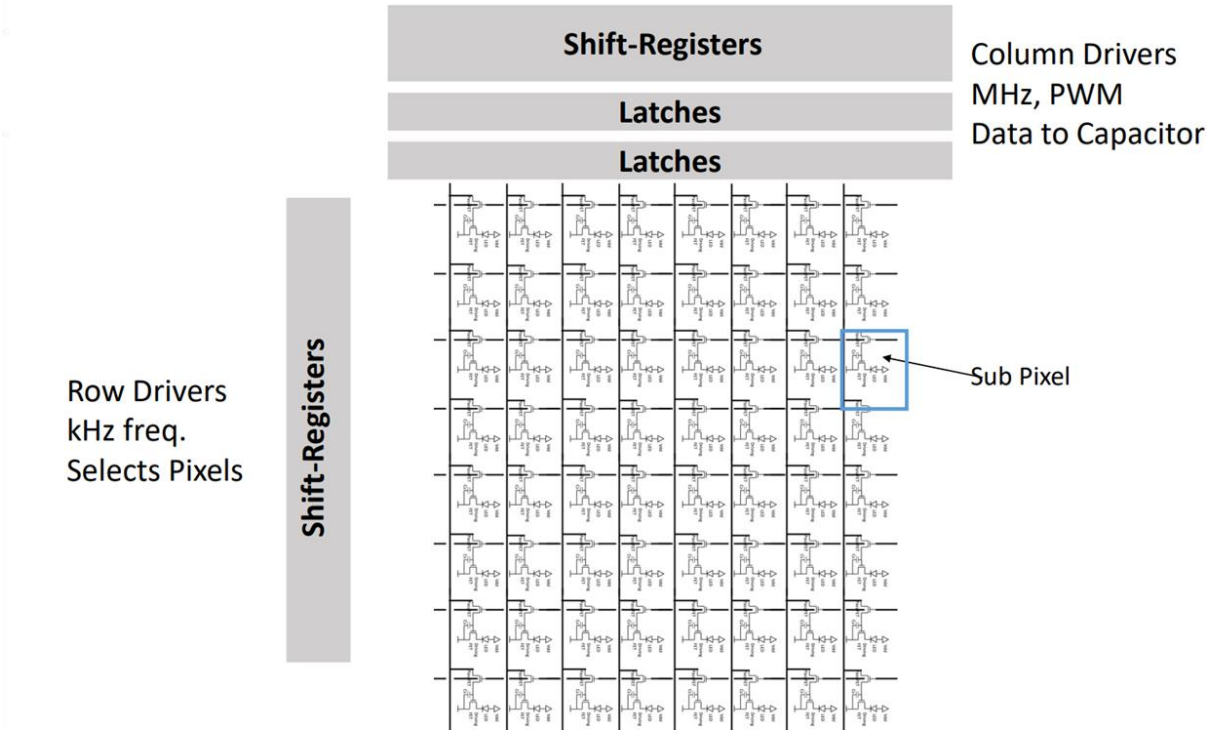

Fig. 6. External control circuitry for driving a display matrix.

The shift-registers can be further dissected to identify the composure of flip-flop circuits, shown in Fig. 7. The flip-flops offer a power efficient and rapid way to transfer from a serial input to parallel output. Though these logic gates that make up the flip-flop circuits can be further un-abstracted to reveal the individual complementary metal oxide semiconductor field effect transistor (CMOS) configuration of the transistors.

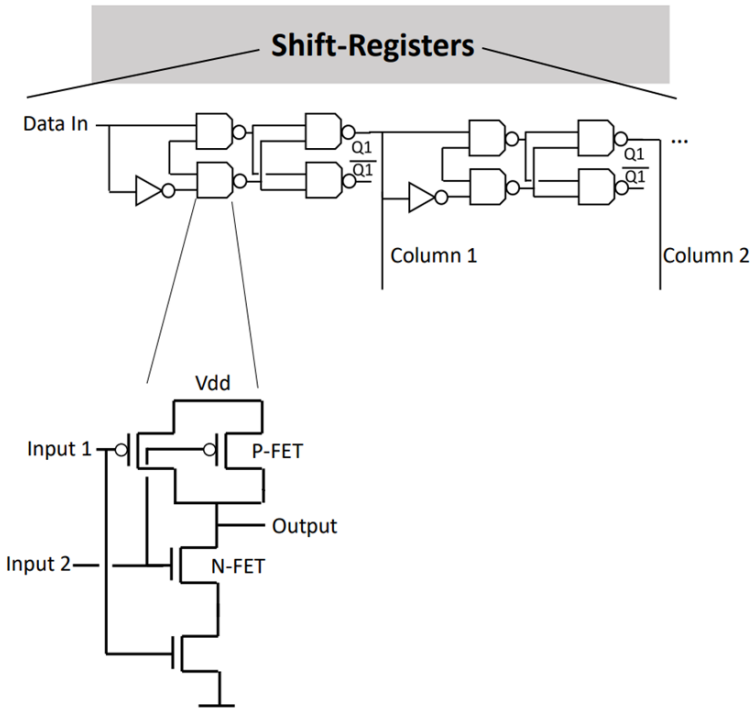

Fig. 7. Shift registers composed of flip-flop circuits, composed of CMOS transistors.

Due to the difficulty in implementing CMOS TFTs and the comparatively poor performance, silicon transistors are more commonly used instead. To pair the two diverse technologies, ribbon cable connections can be utilized to connect with a silicon controller located on a separate PCB for smaller displays. Though as the number of rows and columns increases, external PCBs are no longer a viable approach. Instead, an alternative approach takes single millimeter sized silicon chips with a large number of outputs, and bonds them to metal lines formed on the glass, as shown in Fig. 8. Multiple silicon chips can be placed in series as the display density is increased. Though ultimately, the separate fabrication leads to increased costs and is not viable for small high resolution displays. An approach is needed to integrate the control circuitry with the sub-pixel transistors for compact size and high performance.

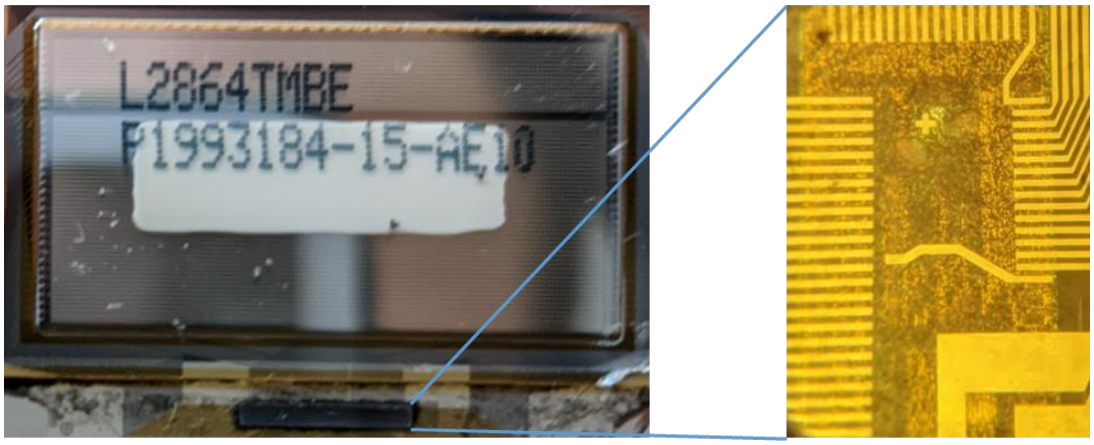

Fig. 8. OLED display with external control circuitry integrated through silicon chip on glass.

1.2 Current State of the Art LED Transistor-Integration

Works on developing LED displays, or µ-LED displays, are ultimately centered on the integration between the LEDs and their controlling transistors to create active matrix displays. To fabricate these displays there are two categories: monolithic integration or pick and place. Monolithic integration creates the transistors on the same substrate that the LEDs are fabricated on. Pick and place involves separately manufacturing the LEDs and transferring the LEDs on a host substrate with pre-fabricated transistors.

- **Monolithic Integration**

The conventional monolithic integration approach connects transistors and capacitors to LEDs in a lateral orientation. The transistors commonly paired with LEDs take the form of high electron mobility transistors (HEMTs), U-shaped metal oxide semiconductor field effect

transistors (UMOSFET), or TFTs [18-20]. These LED-FET combinations are shown below in Fig. 9-11.

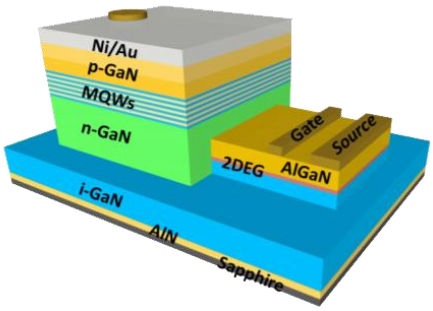

Fig. 9. Integration of LED and HEMT ©2018 IEEE, Reprinted with permission [18].

The HEMT-LED integration makes use of the existing works on GaN HEMTs. Where GaN HEMTs are utilized for high frequency switches in military application, and high power transistors in commercial power converters. In the approach of Fig. 9, convention LEDs are grown, then etched down to the intrinsic GaN (i-GaN) buffer region. Following the etch, selective area growth (SAG) can be done in order to grow AlGaN on top of i-GaN, positioned next to the LED. Final metallization steps can be done to from the source, gate, and p-type contacts. The AlGaN-GaN layers from a two-dimensional electron gas (2DEG) which provide the current path in the transistor. Current flows from the p-contact, through the LED to the n-type layer, then through the HEMT to the source contact. While the approach of Fig. 9 controls an LED, there are a number of problems with the device. The outlined fabrication process requires regrowth of the AlGaN layer which degrades device performance and is a significant increase in cost. Having the lateral layout for the device also consumes LED display area which is now dedicated to integration with the HEMT.

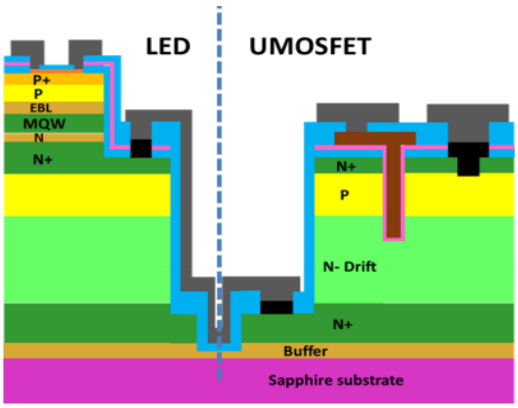

Fig. 10. Monolithic integration of LED with UMOSFET ©2019 John Wiley and Sons, Reprinted with permission [19].

Integration of the UMOSFET and LED is shown in Fig. 10. In this approach a single growth step is utilized, growing the LED on top of the UMOSFET structure. The LED areas are selectively masked off, with dry etching steps used in order to uncover regions for the UMOSFET. The UMOSFET is a type of vertical power MOSFET which makes use of a trench design which supports higher voltage operation in a smaller area. Here a polysilicon gate is utilized to from a conductive path between the n+ and n- drift regions. Current then flows through a metal line over to the n+ region of the LED. While the UMOSFET-LED integration approach does not rely on regrowth, the surface quality of the UMOSFET device can be degraded by the dry etching steps, leading to poor performance. The differences in layer heights between the UMOSFET and LED necessitate the need for a metal connection between the two devices. Having a metal connection introduces resistive losses in the form of both contact resistance and the resistance of the metal layer. A similar problem is found for the UMOSFET-LED as for the HEMT-LED, in that these approaches consume area which would otherwise be utilized for LED integration.

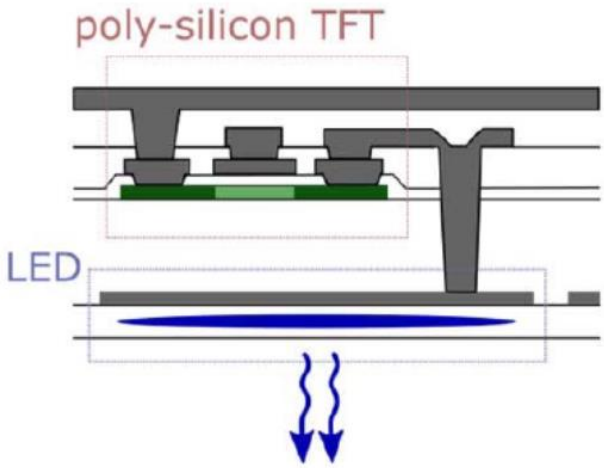

Fig. 11. Integration of LED and TFT ©2017 John Wiley and Sons, Reprinted with permission [20].

Fabrication of TFTs on top of LEDs is another conventional approach being pursued, Fig. 11 illustrates the combination. Conventional LEDs are fabricated which include a mesa structure with top and bottom contacts. A dielectric layer is deposited on top of the LED to separate the devices. Then a thin layer of polysilicon is deposited on top of the dielectric. Patterning and etching steps follow the deposition in order to both pattern the polysilicon for the TFT, and to etch through the dielectric to make contact to the LED. Ion-implantation is performed in order to form the source and drain regions for the TFT. Metal interconnects are formed between the LED and source of the TFT, followed by a gate dielectric and gate metal deposition as a final etching step. TFTs are conventional devices which are used in both OLED and LCD displays. TFTs, however, are still several microns in size and suffer from poor electron mobility. Similar to the UMOSFET integration, TFTs require metal interconnects to connect the transistor to the LED, with the same disadvantages.

- **Pick and Place**

The pick and place approach, as the name implies, involves the physical transfer of multiple LEDs unto a host substrate. Monolithic approaches offer parallel processing though rely on color conversion to down-convert blue into green and red. Instead, pick and place methods rely upon the separate fabrication of blue LED, green LED, red LED, and TFT wafers. Alternative LED materials can also be used such as GaAs in place of GaN for red LEDs, which currently have higher efficiency. Once these wafers are fabricated the blue, green, and red LED wafers are diced and transferred to a wafer containing TFT arrays. The process for the transferring is illustrated in Fig. 12.

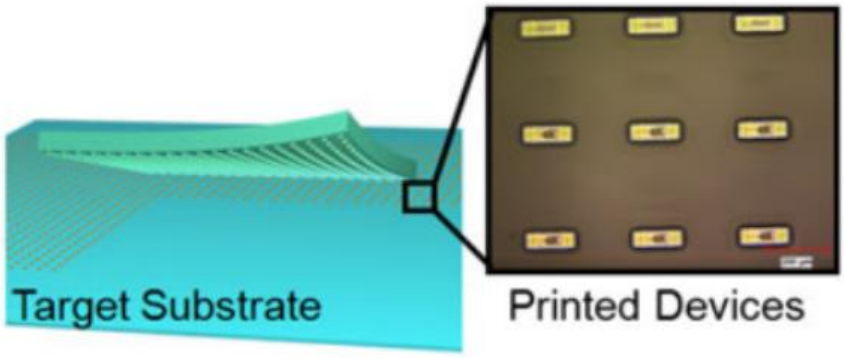

Fig. 12. Pick and place of LEDs ©2017 John Wiley and Sons, Reprinted with permission [21].

The semiconductor industry already relies upon pick and place tools for moving diced chips to packages. The pick and place process works well for low resolution displays, however for higher resolution displays issues arise. A 4K display contains ~25 million pixels which would conventionally take days to fabricate a single display. Various efforts have been made in order to bring the processing time down to make the fabrication cost effective.

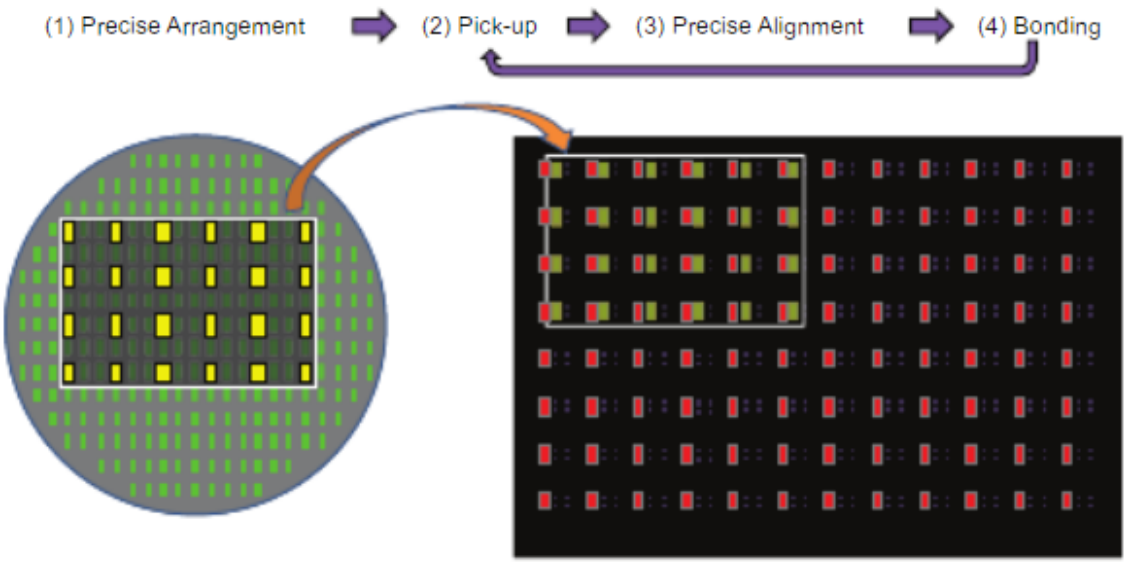

Fig. 13. µTP from host wafer ©2020 John Wiley and Sons, Reprinted with permission [22].

One method being pursued is the use of micro-transfer-printing (µTP). In µTP a Polydimethylsiloxane (PDMS) stamp is utilized, in conjunction with undercut LEDs, to remove LEDs in parallel and place them on a host substrate, Fig. 12-13. Depending on the speed at which the stamp and material make contact, device can either be picked up or placed [22-23]. In this method, LEDs from each color can be picked up and placed on the TFT array, with alignment possible due to the transparent nature of PDMS. Extra processing must be utilized in this approach to achieve an undercut structure for each type of LED in order to be successfully peeled off. The approach here also relies on over three times the manufacturing to create LEDs of each color along with the TFT arrays separately. Due to the contact lithography nature of the transfer, the alignment accuracy of the LEDs is limited to several microns. Yield is also a limiting issue, due to the inability to pick the transferred LEDs back up if inaccurately placed or damaged. Manufacturers have instead had to rely on redundancy, placing double the number of pixels and control circuitry, in order to compensate for potential losses.

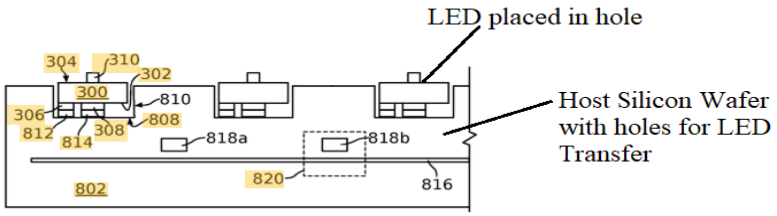

Fig. 14. Water flow method for LED transfer [24].

Another method for reducing the pick and place transfer time involves use of a release and transfer method in water. Analogous to the infant shape-in-hole game, the method here fabricated different sized LEDs to fit inside like-sized holes on a silicon wafer with transistors. The presented method of parallel transfer is shown by Fig. 14. LEDs are undercut and ultrasonicated to remove the LEDs from the host substrates and to get them into water. After the LEDs are in the water, the original host substrates are removed and a silicon wafer with corresponding openings can be inserted. The water containing the LEDs is washed over the surface of the silicon wafer repeatedly in order to transfer the LEDs into the holes in the silicon wafer. The silicon wafer contains silicon transistor circuitry in order to then drive the transferred LEDs. The approach here will achieve parallel transfer of LEDs, however, yield is not perfect. LEDs being transferred in liquid can flip or rotate in the silicon wafer openings which lead to non-functional LEDs. Careful inspection of Fig. 6 can reveal there are several dead pixels in the image.

- **Vertical Integration Approach**

Novel to this work, vertical integration is introduced in the realization of a nanowire GaN gate-all-around (GAA) FET is monolithically integrated at the base of a nanowire InGaN/GaN LED for the first time. The device is shown schematically in Fig. 15. The nanowire FET makes

use of the u-GaN layer common to InGaN/GaN LED growth. The vertical integration allows individual nanowire LEDs to be addressed with none of the issues experienced by previous approaches. Ti is deposited at the base of the wire and annealed to induce nitrogen vacancies which act as donors [25-26]. The Ti annealing combined with the higher conductivity of the initial buffer layer [27-29] creates a bottom n-type region. The generated bottom n-type region at the base of the wire, combined with the u-GaN layer and the n-type GaN from LED, make an n-i-n structure for a FET.

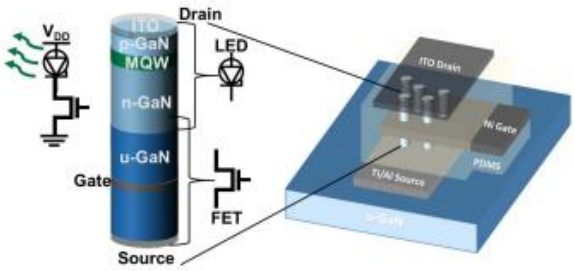

Fig. 15. Schematic of the vertical GaN nanowire LEDs with the nanowire FETs, inset showing a single wire and series connection [30].

The initial nanowire FET chosen to be integrated with the nanowire LED is the static induction transistor (SIT). Multiple types of FETs such as the conventional metal oxide semiconductor field effect transistor (MOSFET) can alternatively be integrated. The SIT though is a straightforward vertical power device that offers easier manufacturing without need for atomic layer deposition (ALD) [31–34]. A schottky gate is used to modulate the depletion region in the nanowire in order to pinch off current. Triode-like curves are produced in the SIT device due the short gate length [31–34]. The presented work offers an advantageous alternative approach to integrate nanowire LEDs with nanowire FETs for displays without sacrificing display area or performance. The presented approach makes use of a top-down etch in order to form the nanowires. The top-down approach allows for use of conventional LED wafers in order to readily

integrate LEDs with FETs. Previous works have demonstrated the ability to fabricate multiple-color nanowire LEDs, which are needed for displays, through top-down approaches [35]. Top-down approaches leverage existing fabrication facilities for large scale device manufacturing. Alternatively, a bottom-up growth technique can be utilized to grow unique colored nanowires [36]. The nanowire growth techniques utilize methods such as molecular beam epitaxy (MBE), which has limitations for large scale manufacturing due to single-wafer growth and uniformity issues [36]. Nevertheless, the presented device fabrication to introduce LEDs and FETs can similarly be accomplished through both top-down and bottom-up created nanowires. The work introduces a novel engineering of the base layers for transistor fabrication.

1.3 Conventional Current Spreading Approaches

GaN suffers from poor p-type doping due to a high hole activation energy of the magnesium (Mg) dopant. Mg has a high activation energy of ~112 meV, compared to ~40-50 meV for silicon dopants, where complete ionization can not be assumed [37]. To calculate the number of ionized acceptors, Eq. 1 can be utilized.

$$Na^{-} = \frac{N_V}{2}\left(\frac{e^{\left(\frac{-(E_a - E_V)}{kT}\right)}}{1 + \frac{N_v}{4N_a} * e^{\left(\frac{-(E_a - E_V)}{kT}\right)}}\right)$$

Eq. 1. Concentration of ionized acceptors.

$$\rho = \frac{1}{qp\mu_p}$$

Eq. 2. Resistivity of a p-type semiconductor.

The density of states for the valance band (N_V) of GaN is equal to $1.8*10^{19}$ cm^{-3}, the activation energy (E_a-E_v) is 112 meV, kT at room temperature is 0.0259, and the assumed doping concentration is 10^{19} cm^{-3}. Plugging in these values show the ionized dopant concentration, which can contribute to conduction, is $1.19*10^{17}$ cm^{-3}. Only 1.19% of the total dopant is electrically active, generating holes, at room temperatures. The low doping leads to high resistivity of the p-type layer by Eq. 2. In Eq. 2, q is the electron charge of $1.6*10^{-19}$ C, p is the calculated ionized p-type dopant of $1.19*10^{17}$ cm^{-3}, while μ_p is the hole mobility of ~10 $cm^2V^{-1}s^{-1}$ [38]. Plugging these values into Eq. 2 yields a high resistivity of 5.25 Ω*cm. In contrast, a p-type silicon region can achieve high doping of 10^{21} cm^{-3} with a low resistivity on the order of 0.0001 Ω*cm.

This highly resistive p-type layer necessitates the use of a current spreading layer to minimize the effects of current crowding [39]. Various current spreading approaches have been employed such as current blocking layers [40-41], indium tin oxide (ITO) thin films [42-43], and thin metal films [44-45]. Current spreading layers must be sufficiently transparent to avoid reflecting and/or absorbing the light emitted from the LED. Additionally, the geometry of the ohmic p-contact and the current spreading layer must be designed to optimize the electrical performance and LEE of the LED. Design of a current spreading layer must also consider the resistivity and thickness of the conductive material used in order to further optimize the electrical performance and LEE of the device.

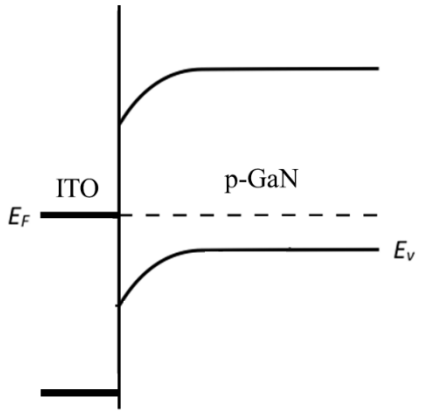

Fig. 16. Band alignment between ITO and p-GaN.

ITO is a commonly used current spreading method, as ITO can achieve over 90% transparency to visible light [46]. ITO can act as a transparent current spreading layer due to the wide bandgap of 4 eV and high n-type doping [46]. Many commercial devices make use of ITO as a transparent conductive film due to these properties. However, for LEDs ITO forms an undesirable Schottky contact to p-type GaN due to the band alignment, Fig. 16. The n-type ITO is also put into reverse bias with respect to the p-GaN, having tunneling current dominate, and leads to a high contact resistance [46].

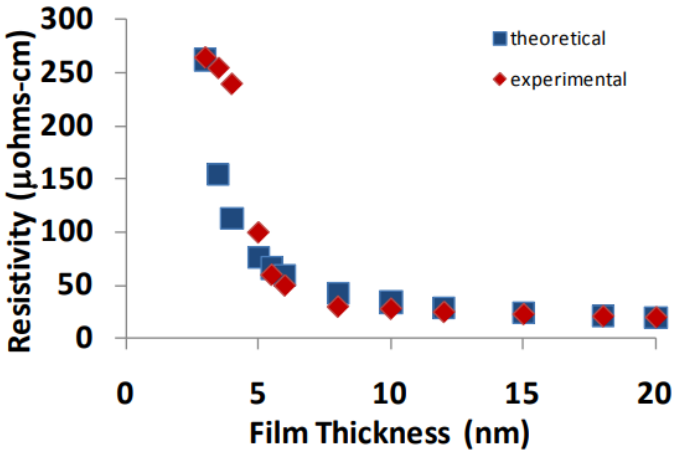

Fig. 17. Metal resistivity vs. thickness ©2011 Springer, Reprinted with permission [47].

Nickel (Ni), in contrast to ITO, provides an ohmic contact to p-GaN and is the conventional p-contact metal. Works employ single nanometer thin layers of Ni to act as a transparent current spreading layer for LEDs. Thin metal layers have high transparency to both visible and UV wavelengths. The drawback of this approach is that thin metal layers are difficult to make continuous and suffer from high resistivity. As the thickness of a metal is scaled down to single nanometers, the resistivity dramatically increases, Fig. 17. The increase in resistivity limits the potential gains of a thin metallic current spreading layer.

- **Novel Current Spreading Approach**

To resolve these issues, a novel integration method is investigated in this work which enables current spreading without the resistive losses and trade-offs suffered by other approaches. Here, a capacitor is utilized as the current spreading layer for the first time. The capacitor is operated similarly to the gate of a FET in order to modulate charge accumulation or depletion. Integrating a capacitor with a transparent conductive top plate allows for the benefits of high transmissivity with materials such as ITO, without the drawback of energy band misalignment or high resistivity [46-47]. The choice of dielectric and transparent metal for the capacitor can also enable both increased LEE by grading the refractive index, along with surface passivation to reduce radiative recombination.

A schematic of a conventional GaN LED with the integrated current spreading capacitor is shown in Fig. 18(a). The fabrication process is compatible with most conventional LED processes, adding a capacitor as a final step. The device functions by applying a positive bias to the capacitor which bends the energy bands in the p-GaN to repels holes from the surface, Fig 18(b). The holes are pushed from remote areas towards the p-type contact and also towards the multiple quantum

well (MQW) active region to enable increased electron-hole recombination. Depleting the holes from these unused regions allows them to be utilized by the device, which boosts the internal quantum efficiency (IQE) of the LED, in turn enhancing the external quantum efficiency (EQE).

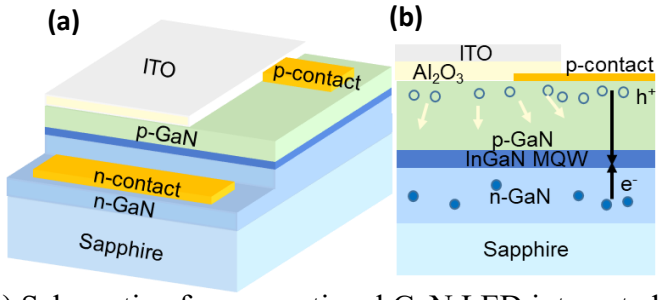

Fig. 18. (a) Schematic of a conventional GaN LED integrated with a current spreading capacitor, (b) Positive bias capacitor repelling holes. [48]

Alternatively, applying a negative bias to the capacitor accumulates holes near the surface of the LED. Accumulation of holes under the capacitor pulls holes away from both the p-type contact and MQW region, generating the opposite effect. Negative voltage leads to a slight decrease in IQE when compared to the case of zero capacitor bias, as remote holes do not play a large role in conduction at low applied bias

Introduction of this novel capacitor layer to a fabricated LED allows for increased performance with no added energy consumption, as the capacitor has negligible leakage current. New integration schemes can also be utilized to further boost LED performance and add new materials which would otherwise reduce device performance. The described capacitor layer requires only a single additional mask level following fabrication of a conventional LED.

1.4 LED Light Extraction and Efficiency Improvements

LEDs suffer from poor light extraction efficiency due to the high refractive index of 2.5 vs. air of ~1. Snell's law, Eq. 3(a), can be used to calculate the critical angle, Eq. 3(b). Plugging in 1 for n_2 and 2.5 for n_1 gives a critical angle of 23.6º. Photons emitted inside this 23.6º cone escape the LED, while those at higher angles than the critical angle are internally reflected back inside the LED.

$$\text{(a) } n_1 sin\theta_1 = n_2 sin\theta_z$$

$$\text{(b) } \theta_c = sin^{-1}(\frac{n_2}{n_1})$$

Eq. 3 (a) Snell's law, (b) critical angle calculation.

The total fraction of light that is emitted into the escape cone can also be calculated through finding the surface area of the spherical cone with radius r, Eq. 4.

$$\text{Area}=\int dA = \int_{\theta=0}^{\theta_c} 2\pi r^2(1 - cos\theta_c)$$

Eq. 4. Surface of a spherical cone with radius r.

Assuming the photons are emitted from a point source with a total power of P_s, the output power can be expressed as Eq. 5.

$$P_{escape} = P_s \frac{2\pi r^2(1 - cos\theta_c)}{4\pi r^2} = \frac{1}{2}(1 - cos\theta_c)$$

Eq. 5. Photons of escaped light.

The critical angle of the GaN LEDs is small so that when the cosine term is expanded into a power series the higher order terms can be ignored, yielding Eq. 6.

$$\frac{P_{escape}}{P_s} \approx \frac{1}{4}\frac{n_2^2}{n_1^2}$$

Eq. 6. Ratio of emitted photons to generated photons.

Plugging in the refractive index for GaN and for air, it is found that only ~4% of the photons generated by the device can escape. This is a significant issue for GaN LEDs as the total EQE is drastically reduced.

There are, however, a number of methods to boost the LEE for LEDs. These approaches fall not two categories: either grading the refractive index to widen the escape cone, or modifying the surface geometry.

A common method for grading the refractive index is the use of a flip-chip LED design. GaN LEDs are conventionally grown on sapphire as a low-cost substrate. Sapphire has a lower refractive index than GaN of 1.8, allowing a larger escape cone. For flip-chip devices, the LED is rotated upside down and bonded to a host package as shown in Fig. 19. The grading of 2.5 to 1.8 to 1 allows for 8%> of the light to escape from the LED. Additionally, in the flip-chip design, the p-GaN contact can be engineered to be highly reflective, allowing for increased efficiency of the generated light out of the device. Further optimization of the flip-chip LEDs can be accomplished through the use of adding an SiO_2 coating on top of the sapphire, which has a refractive index of 1.5. Use of SiO_2 allows higher efficiencies of 11%> LEE. Unfortunately, numerous deposition steps can lead to increased costs for LED production.

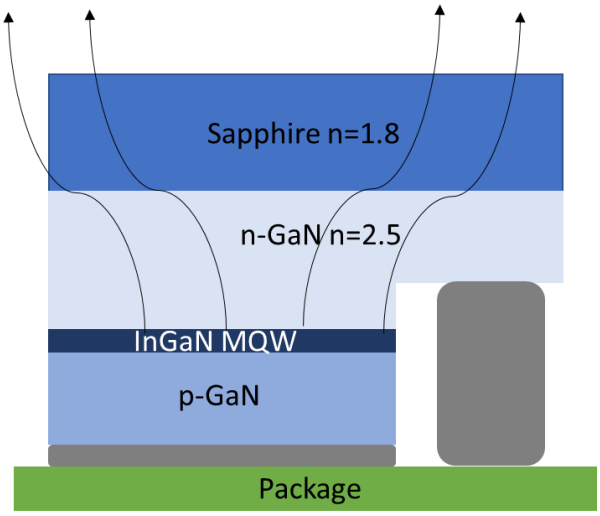

Fig. 19. Flip-chip LED design.

Modification of the surface geometry can expand upon the results achieved through grading the refractive index. Surface texturing is a common approach to introduce roughness of the p-GaN in order to scatter light [9]. Roughness can be introduced through the use of either wet etching or dry etching to create periodic or random structures, Fig. 20 [9]. These microstructures scatter the light, widening the escape cone to boost light extraction [9]. Surface texturing, while increasing light extraction, can lead to surface states which degrade electrical performance of the LEDs [49].

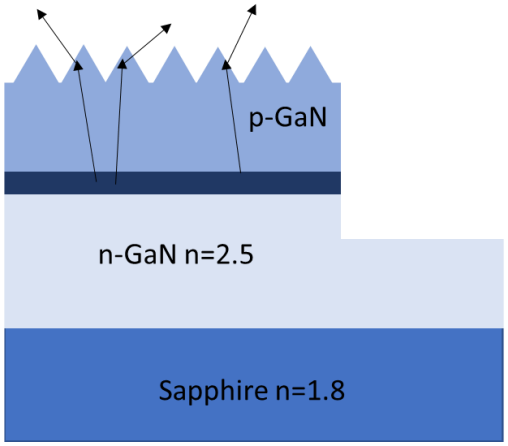

Fig. 20. Surface textured p-GaN LED.

- **Nanowire Optimization Approach**

Both the refractive index grading and surface modification of LEDs can be costly solutions to achieve small gains in light extraction efficiency. Instead, Nanowire LEDs provide a large boost in terms of IQE and LEE due to strain relaxation and geometry, respectively [50]. Methods such as surface texturing lead to multiple reflections, increases chances of reabsorption, before the emission of light, Fig. 21. Alternatively, nanowires have 100% light emission when the light is radially emitting from the QW, which leads to greatly increased LEE.

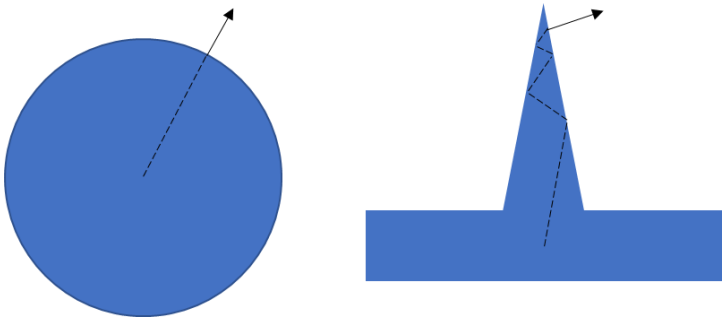

Fig. 21. Nanowire vs. triangle light extraction.

The formation of vertical nanowire LEDs has been optimized through a top down etching approach. Dry etching combined with wet etching approaches allowing tailoring of both the nanowire diameter and design. Crystallographic wet etching with KOH based chemistry has been studied in order to form nanowire LEDs for a variety of applications, Fig. 22.

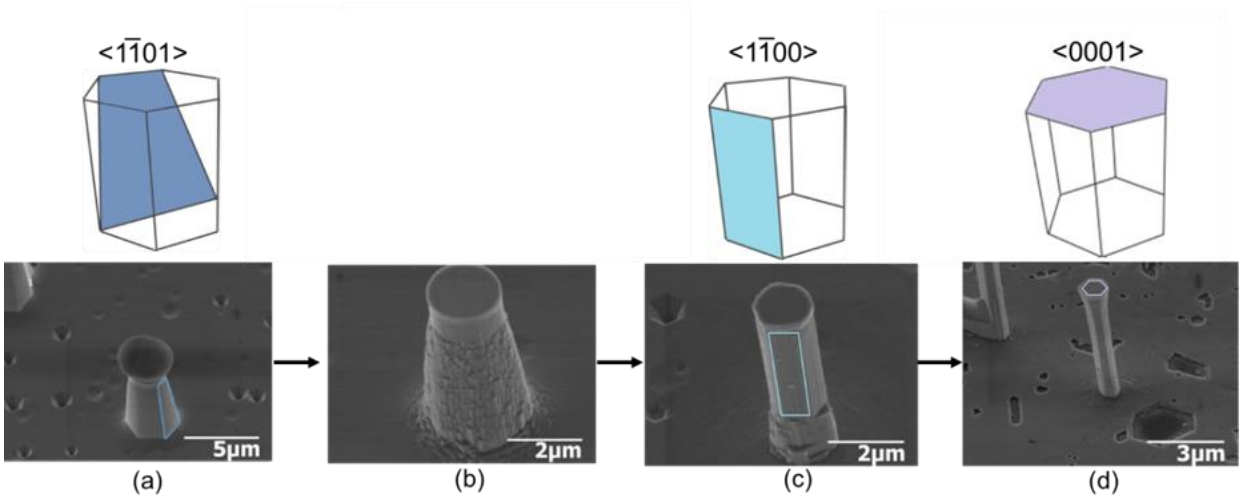

Fig. 22. GaN KOH etching with pertinent crystal planes (a) initial wire shape following the <1$\bar{1}$01> plane (b) <1$\bar{1}$01> plane etch (c) <1$\bar{1}$00> plane uncovered (d) <1$\bar{1}$01> plane etch with <0001> surface unetched. [51].

1.5 Flexible GaN Devices

GaN LEDs deliver high performance commercial lighting and offer the possibilities of further integration mechanisms. GaN is conventionally a ridged crystal which does not bend or flex, and cracks upon excessive torque. LEDs, however, can be made at the micron or nanoscale, and while individual LEDs are not flexible, they can be used with a flexible substrate. Having flexible, efficient, LEDs allows a number of novel applications to be realized for both the commercial and medical fields. The issue is in the removal of LEDs off of the ridged host substrate.

LEDs grown on silicon offer novel possibilities compared with conventional growth on sapphire substrates. <111> type wafers are used for GaN growth on Si in order to growth the GaN wurtzite structure on the diamond lattice of Si. After growth, a dry etch can be used to etch down through the GaN in order to reach the Si underneath. Hydroxyl based chemistry such as KOH can be applied through a wet etch to rapidly target the <110> plane of the Si over the GaN, Fig. 23. The GaN can effectively be released from the substrate and placed unto a flexible host. Researchers

such John Rogers from the University of Illinois have applied this technique and transferred the LEDs through a PDMS stamping method, Fig. 23.

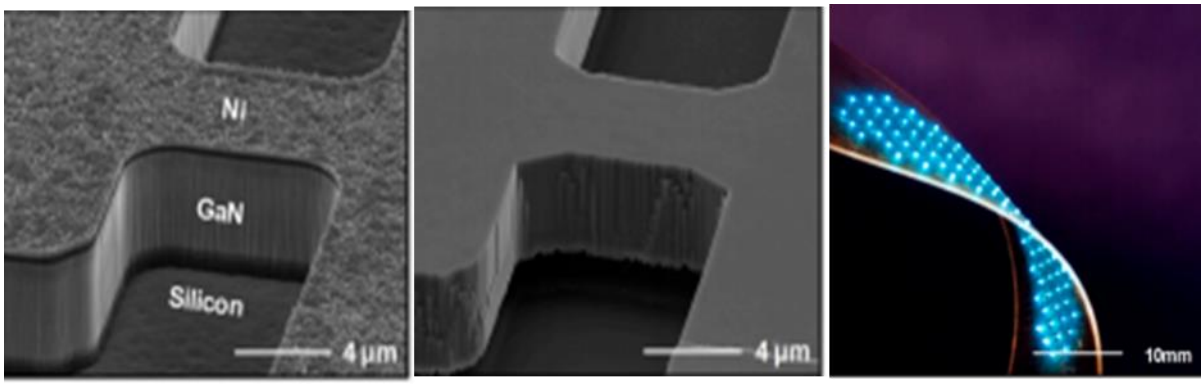

Fig. 23. GaN LED wet etch release and transfer method, ©2011 PNAS, Reprinted with permission [52].

While the presented method, Fig. 23, provides a way to transfer large scale LEDs, there are notable limits. As the LEDs are each ridged devices, the pitch has to be balanced such that density is a trade-off for flexibility. Nanowire LEDs have greatly improved performance over planar LEDs, though are incompatible with the presented technique. Nanowires LEDs are vertical structures, which do not lend to the pick and place method, due to the lack of structural support once placed. Making use of nanowire devices also lends to increased flexibility and density, as each device occupies a smaller lateral area.

Attempts have been made in order to develop a flexible nanowire LEDs, Fig. 24 [53]. In the presented approach, 30 µm tall core shell nanowires are grown with PDMS coating between the nanowires. The wires and PDMS are then mechanically exfoliated from the growth substrate and placed on a flexible host substrate. The layer of PDMS provides the wires the flexible, mechanical, support layer to keep the wires upright upon removal. Use of the PDMS also allows the devices to contact both the top and bottom of the wires which correspond to the p-type and n-type regions, respectively. The obstacle with the presented approach is that the wires have to be

grown 30 µm tall, and that pieces of the wires are left upon mechanical exfoliation. Growth of wires 30 µm tall is needed as the PDMS layer has to be thick enough to be mechanically stable during removal. Bottom-up growth, especially for tall wires, is a large expense which prevents the presented approach from being manufacturable. Instead, another solution is needed to bring flexible nanowire LEDs to scale.

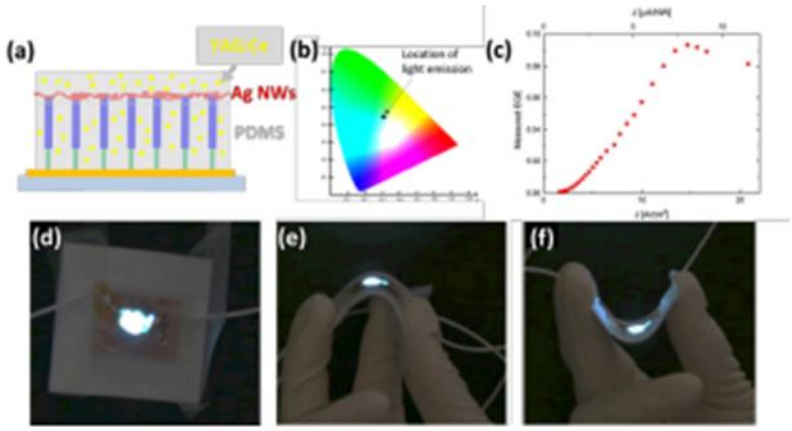

Fig. 24. Flexible Nanowire LED with integrated phosphors, ©2017 RSC, Reprinted with permission [53].

- **Novel Peeling Approach**

Lessons learned from the two techniques are applied in order to present a novel solution to achieve flexible GaN nanowire LEDs. Growth of GaN on Si with a KOH based wet etch is similarly done to undercut the structure. Here, however, the Si is just undercut and not fully removed in order to still provide structural stability, Fig. 25. PDMS is also used for the filling layer, though coating the PDMS and etching back just to reveal the wire tips. ITO is coated and patterned in order to provide a transparent top contact to the LED. In this approach, a thicker PDMS layer is then coated for added mechanical stability. The PDMS layer is released from the Si using a KOH etch to peel away the edges, for the first time. The sample is mounted to a host

substrate following peeling, with added etching to reveal the bottom GaN section of the nanowire, under the AlN layer. Metallization is then performed in order to make contact to the back of the device. A final etching step is done in order to remove the top mechanical support layer of PDMS. Following the presented approach leads to dense, flexible, nanowire LEDs can be fabricated. Distinct to this approach, shorter wires with heights of ~4 µm can be removed. These novel nanowire devices can be readily utilized for boundless device applications.

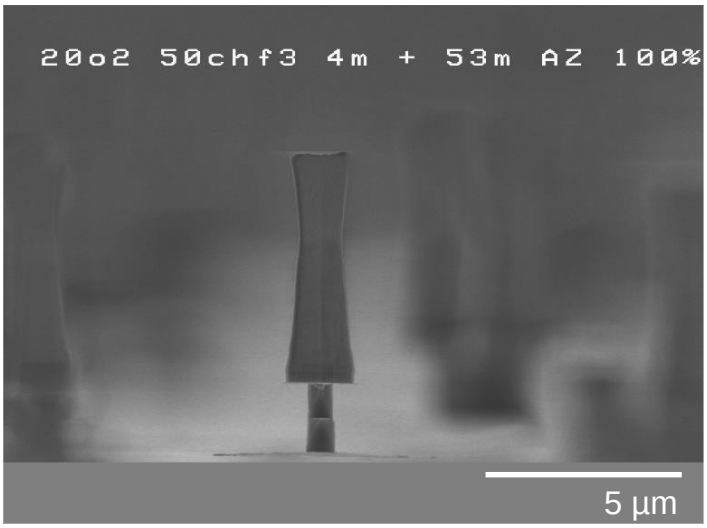

Fig. 25. GaN nanowire with undercut Si nanowire.

Chapter 2

FABRICATION APPROACHES

2.1 Overview of Fabrication Approaches Chapter

The introduction chapter outlined several issues and purposed solutions in order to optimize LEDs for display applications. To realize these solutions a number of building blocks need to be developed in which devices can be built. Fundamental processes such as dry and wet etches, film depositions, resist patterning, and more must be each optimized for GaN processing. Standard Si and gallium arsenide (GaAs) processes in commonplace in the RIT semiconductor micro-fabrication lab (SMFL), though GaN is new to the facility. Novel processes and method are also introduced in this chapter in order to realize devices in the constraints of the current facilities. Wafer level testing of devices are performed for all devices. Software simulations through Silvaco Atlas and Athena are utilized to better understand device behaviors and predict results.

2.2 Planarizing Dielectric Processing

GaN nanowires formed through a top down approach are vertical devices for reasons of both processing and increased density. Multiple vertical levels must be fabricated in order to realize a number of nanowire-based devices such as LEDs or nanowire FETs. Conventional approaches coat multiple metal-insulating layers in succession, leading to devices with rough topography [54]. Advanced semiconductor processes do not tolerate topology, as there is a small window for the depth-of-focus in advanced lithography tools. Instead, a planar layer by layer process is purposed and utilized for these vertical devices. In the presented scheme, layers of directionally deposited metal are put down, with a planarizing dielectric used as a spacer. There are several critical constraints put on the planarizing dielectric in order to fabricate these vertical GaN devices. The dielectric must be able to withstand aggressive solvents used in photoresist lift-off processes, have uniform thickness with the nanowires, be able to be dry etched, have a coating thickness of several microns, and be optically transparent for LEDs. These aforementioned constraints eliminate most common dielectric materials.

- **BCB Tests**

A commonly utilized dielectric which is used as a planarizing dielectric coatings is benzo cyclobutene (BCB). BCB can be coated several microns thick and will not be removed in solvents after a baking step. Tests were conducted with nanowires in order to judge the quality. Dow Cyclotene 4000 series BCB was utilized for these experiments. The BCB was pipetted unto the sample and then spun at 500 rpm for 5 seconds with a 2 second ramp, followed by 4000 rpm for 60s with a 2 second ramp. The BCB was then baked on a hotplate for 10 min at 140ºC, then moved

to an oven for 1 hour at 250 ºC in an N_2 environment. The BCB was found to overcoat 4 µm tall nanowire structures. A reactive ion etch (RIE) recipe was developed with the conditions of 300 mT, 50W, with 80 sccm O_2, and 20 scccm SF_6 for an etch rate of ~380nm/min. During the etch-back process it was found that the coating on the surface was very non-uniform. Fig. 26(a) shows the non-uniformity in the wire arrays, with microns of BCB remaining, while outside the array wires are fully cleared. The non-uniformity is entirely attributed to the coating process, as the 10 µm spacing of the wires would not lead to any aspect ratio dependent etching. These nanowire devices have a slight negative slope, where the diameter is smaller at the base of the wire then at the top. During the dry etch it is found that there are voids around the nanowires due to the poor coating of BCB, Fig. 26(b). Once again, the effect of the void is attributed to the coating instead of the dry etch, as a directional dry etch would be shadowed by a negative slope, leading to a decrease instead of an increase in etch rate. Having non-uniform layer coatings and voids along the nanowires would lead to metal layers of the devices shorting together, killing devices. For these reasons BCB is found not to be a good choice for a dielectric spacer.

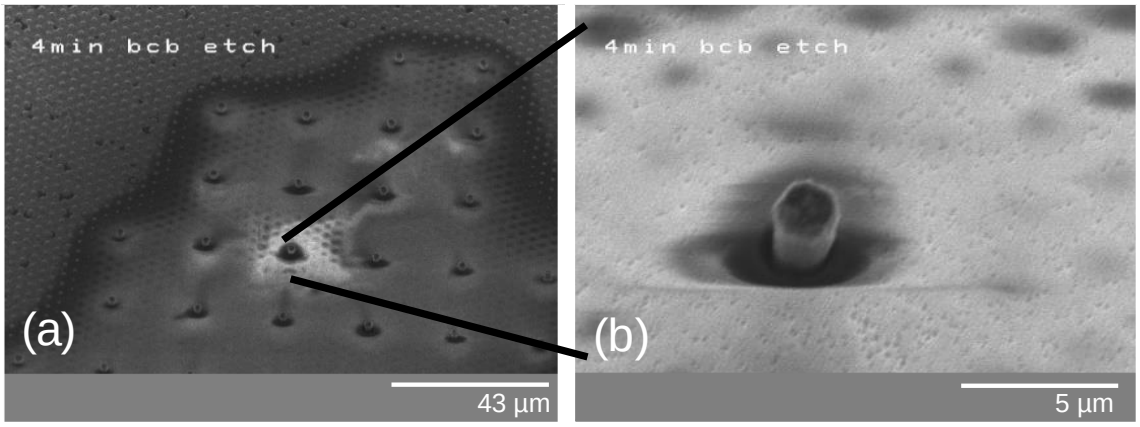

Fig. 26. (a) BCB non-uniformity, (b) BCB etch showing voids around the wire.

- **SiO_2 Dielectric Tests**

SiO_2 is another commonly used dielectric in order to planarize structures due to the resistance of solvent removal. Spin-on-glass can be used which contains silica that is diluted in a solvent for spin coating. SiO_2 provides isolation for many semiconductor devices and the ability to spin-coat allows for planarization, unlike chemical vapor deposition (CVD) processes. The CVD process available makes use of the tetraethyl orthosilicate (TEOS) precursor for SiO_2 depositions. CVD is expected to uniformly coat the surface of the material, including the sidewalls. A metal pattern, several hundred nanometers in thickness was tested with a 4 µm coating of SiO_2 to try to planarize the surface. Shown in Fig. 27 it was found that the height differences were maintained or amplified, and that planarization did not occur.

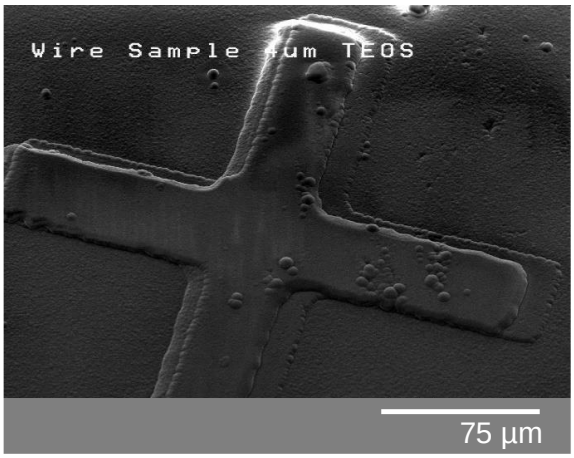

Fig. 27. SiO_2 CVD deposition.

Honeywell T12B was available and utilized to test spin-on-glass, as CVD was found to be a poor choice. Test samples of Si were utilized to judge the thickness of the coatings, along with nanowire samples. A nanospec spectrometer provided thickness measurements based on the refractive index of SiO_2. After the spin-on-glass was pipetted unto the sample spin-coating was performed. A first spreading step of 500 rpm, a ramp of 1 second, and a time of 3 seconds was

done for each coating step. RPMs of 1000, 3000, and 4000 were each tested with a ramp rate of 1 second and a dwell time of 30s. After coating the samples were baked at 250ºC for 5 minutes, with increased time finding no change in thickness. The corresponding thicknesses measured to be 1.16 µm, 880 nm, and 750 nm respectively. The coating on the nanowire samples was examined to find that the spin-on-glass coated up the nanowires, leading to a non-uniform topology shown by Fig. 28.

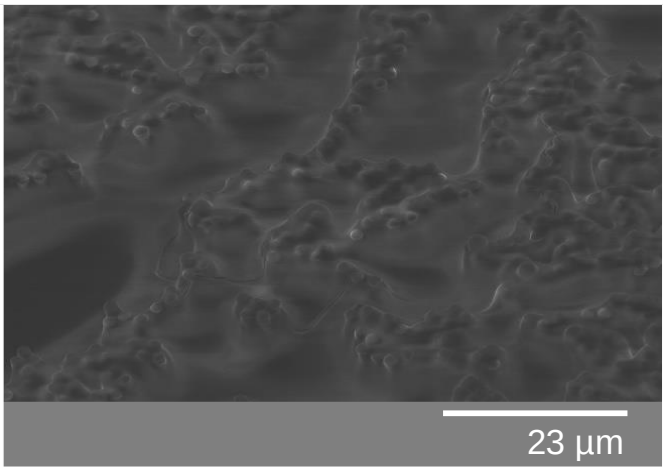

Fig. 28. Spin-on SiO2 non-uniform coating.

To achieve a planar coating, a subsequent layer or a thicker layer was needed. A dual coating of spin-on-glass was tested to provide increased thickness without sacrificing uniformity. The 1000 rpm coating was repeated twice, this time providing a planar surface coating. Shown by Fig. 29, the coating on the sample was uniform, however widespread cracking resulted from the stress of the dual coating. The cracks persisted deep into the nanowire arrays and could lead to device layers shorting. To minimize film stress a lower baking temperature of 100ºC for 5 mins was tried with the dual coating approach. The lower baking temperature was found to not remove surface bonds, which made the surface hydrophobic, preventing subsequent coatings. Use of an O_2 plasma was found to modify the surface, turning it hydrophilic, for successfully added coatings. Slight cracking was found around the edges of the sample, though not on the same scale as the

higher temperature tests. Due to the concerns though about higher temperature processing on the film stress, spin-on-glass was found to be a non-ideal dielectric.

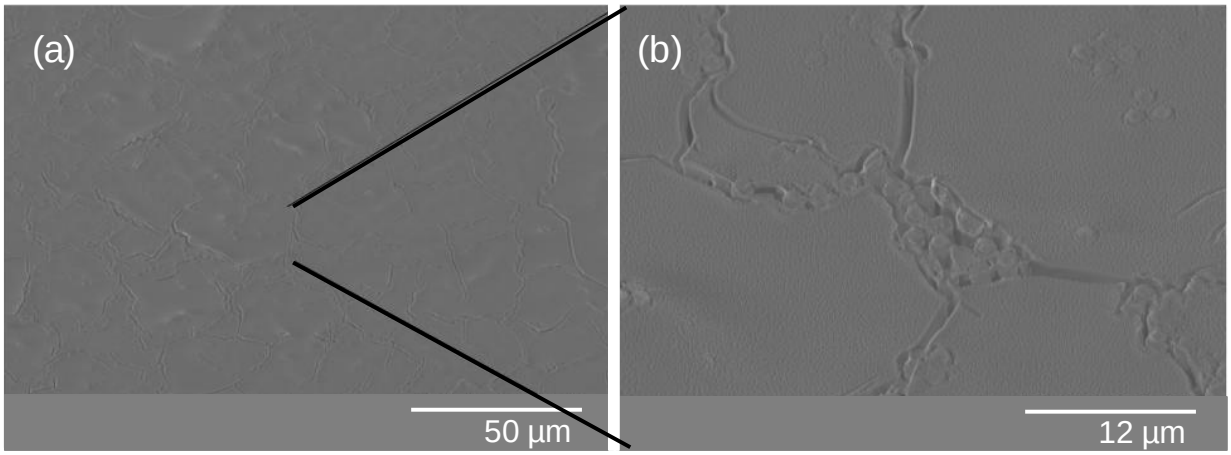

Fig. 29. Dual coated Spin-on-SiO2 uniform coating with cracking.

- **PDMS dielectric coatings**

PDMS is widely used for microfluidic devices to make micro-channels with a thick coating, though a casting approach. PDMS is a polymer which contains a silica backbone which makes it resistant to most chemical etches. PDMS is also optically transparent, widely available, and flexible. For these reasons PDMS was investigated for use as a dielectric spacer layer. The dielectric comes as a two-part solution, a base resin and curing agent which are mixed together by weight ratios. Conventionally a 10:1 base resin to curing agent is utilized, with increased curing agent later found to give poor uniformity. Once mixed together the solution forms bubbles, which negatively impact the coating. To remove the bubbles either degassing with a vacuum system or use of a centrifuge is used. In these experiments a centrifuge is chosen due to the ease of processing. The samples are spun at 3000 rpm for 3 minutes in order to fully remove the bubbles. Coating must be done within a few hours to prevent hardening of the mixed PDMS film. PDMS is a very viscous liquid and is evenly spread out before spin coating. To achieve a uniform thin

film of PDMS a spin coating recipe of 5000 rpm for 120 seconds was developed. A fast ramp rate of 1 second was used, finding ramp rate as the main factor to control the formation of an edge bead. The corresponding recipe yields a thickness of 7.1 µm and uniformly coats the surface, planarizing the nanowires. A bake of 11 minutes at 90ºC is found to be optimal, as too high temperatures or time lead to excess cross-linking.

Dry etching of the PDMS is to be carefully managed as to balance heat, and gas flows. Since PDMS is a polymer with a silica backbone, only dry etching can remove the film. Both fluorine-based chemistry and oxygen are utilized in order to both remove the silica and organic parts, respectively. Due to the incorporation of oxygen, only metal hard masks can be used for patterning as a resist mask would be rapidly etched away. The developed recipe uses 20 sccm O_2, 40 CF_4, at 275 W, and 100 mT. The initial etch rate for the first ~3 minutes is found to be ~0.4 µm/min, as the PDMS forms a skin when exposed to the air. After ~3 minutes of etching, the etch rate is found to increase to ~1.1 µm/min. Heat is a big concern in the etching chamber, and delays of several minutes were put in place after every ~3 minutes of etching. Excessive heating can cross-link the PDMS which builds up polymers which can be impossible to remove.

The gas ratio of the dry etch is also important to control. Increases in the O_2 flow lead to a buildup of silica particles on the surface, as more organics are removed., Fig. 30(a). In contrast, increased CF_4 flow leads to a buildup of polymer due to the lack of O_2, Fig. 30(b). Buildup of silica is preferred as polymers can be difficult to remove. Despite the difficulties with dry etching, PDMS has excellent wet etching resistance to most chemistries.

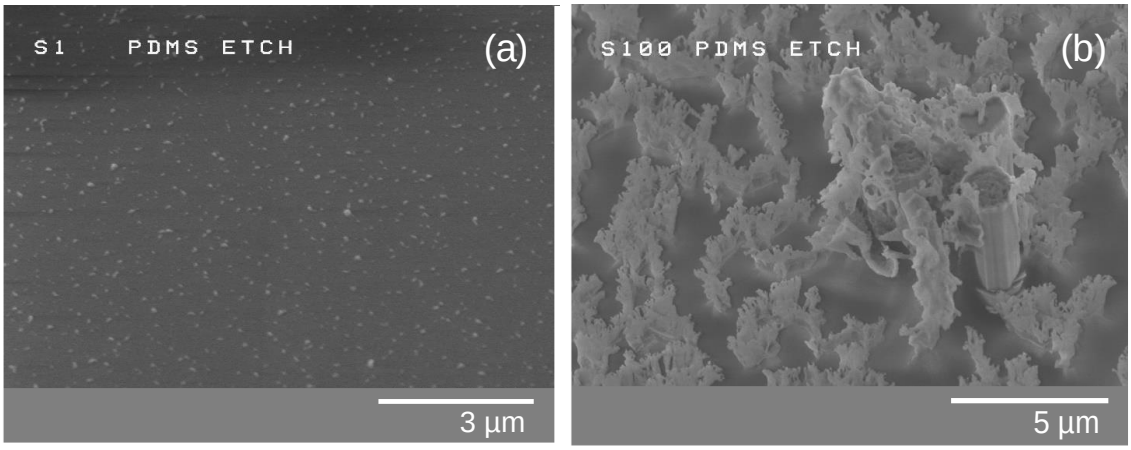

Fig. 30. (a) Silica surface buildup from O_2 rich conditions, (b) polymer buildup from CF_4 rich conditions.

Nanowire etching tests are performed making use of the overcoat provided by the PDMS. The PDMS surface is found to be planar regardless of nanowire positions, for tested nanowire heights up to 7 µm. Samples were processed for the etch on a 6" silicon carrier coated with aluminum. The carrier wafer coated with aluminum helps to maximize etching rates, where the CF_4 is not consumed by the silicon. Dry etching of the nanowires proceeds with included cooling delays for the PDMS. When the PDMS film height is close to reaching the tips of the nanowires, the surface of the PDMS darkens. The darkening of the dielectric is due to the electrons from the beam being transported away due to the close presence of the nanowire. Careful attention to the surface contrast is a good indicator of the etch time left. Precision in the dry etch is critical, as top-down LEDs are axial in nature, over-etching leads to electrical shorting of the p-type and n-type regions. Post etch results are shown by Fig. 31(a), where a slight build-up and redeposition occurring. Silica is found to be at the surface of the PDMS, with redeposition also occurring on the nanowire. Leaving the silica at the surface can lead to poor performance of the top contact. To remove the silica, sample are placed in 10:1 buffered oxide etch (BOE) for ~10 minutes to etch

away the redeposition and surface silica. The results from surface cleaning are shown in Fig. 31(b), where the PDMS has not been attacked, and the surface is planar to the nanowire.

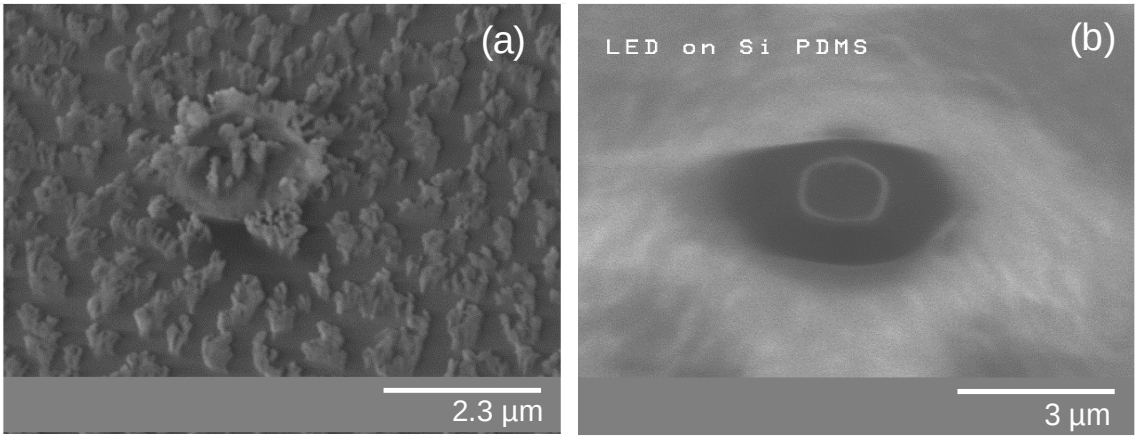

Fig. 31. (a) Post-etch buildup of silica, (b) BOE etch removal of silica, with nanowire tip exposed.

Deeper etches can be required for the formation of devices such as nanowire transistors, which require a gate level to be located at ~half of the wire height. Additional etching tests performed show thin layers below 1 µm can be generated across the sample using PDMS. No voids are found along the nanowire, with negligible height differences, Fig. 32.

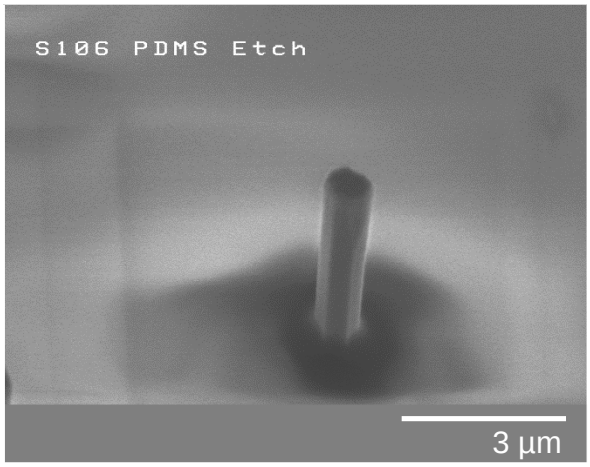

Fig. 32. PDMS film etched back to less than 1 µm.

To evaluate film quality towards harsh solvents, a metal lift-off process was performed. The PDMS surface was first treated with an O_2 plasma in order to convert the hydrophobic surface to hydrophilic for the resist coating. LOR 5A was coated on the sample and baked at 170°C for 5 minutes. HPR 504 photoresist is then coated on top of the LOR, and baked for 1 minute at 100°C. The photoresist is exposed and developed to achieve an undercut profile. Nickel is thermally evaporated coating the top of the nanowires, the top of the photoresist, and the exposed PDMS. The strong solvent, N-Methyl-2-pyrrolidone (NMP), is utilized for several hours to release resist and the metal. Results of the lift-off show the PDMS as unaffected, along with the metal uniformly coating the PDMS which was exposed, Fig. 33. Achieving a crack free, planar film, with no voids, and is capability with solvents, makes PDMS a good choice as an interlayer dielectric.

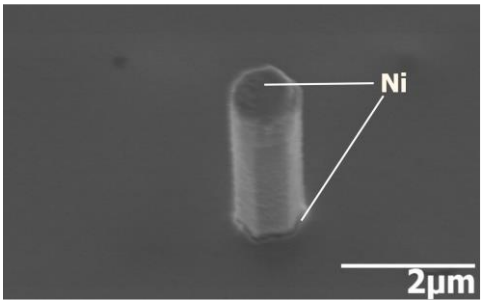

Fig. 33. PDMS film etched back to less than 1 µm.

- **Photoresist dielectric coating**

Photoresists are widely available solutions for the high-resolution patterning of nanostructures. There are many different varieties of photoresist tailored to different applications and coating thicknesses. Most photoresists are optimized for highly uniform coatings of features and this work here investigates the use of photoresist as a dielectric spacer. AZ MIR 701 photoresist is selected for this work, as the coating can be optimized for several microns. A dense nanowire sample with diameters of ~350 nm and heights of ~2 µm was chosen and coated with

701. A two-step coating recipe of 500 rpm, ramp 1 second, dwell 1 second, then 3000 rpm, ramp 1 second, and dwell 30 seconds was done. The resist coating was approximately planar to the nanowire tips. A key requirement of the spacer dielectric is insolubility in harsh solvents such as NMP, though conventionally photoresists are stripped with these same solvents. In order to address the resistance to solvents, the sample was baked for 39 minutes at 250°C, Fig. 34(a). The high baking temperature cross-links the photoresist film to prevent removal in solvents. To test the resistance to solvent removal, the photoresist baked sample was left in NMP for a period of 6 hours. The NMP was found to have no effect on the sample, as shown by Fig. 34(b).

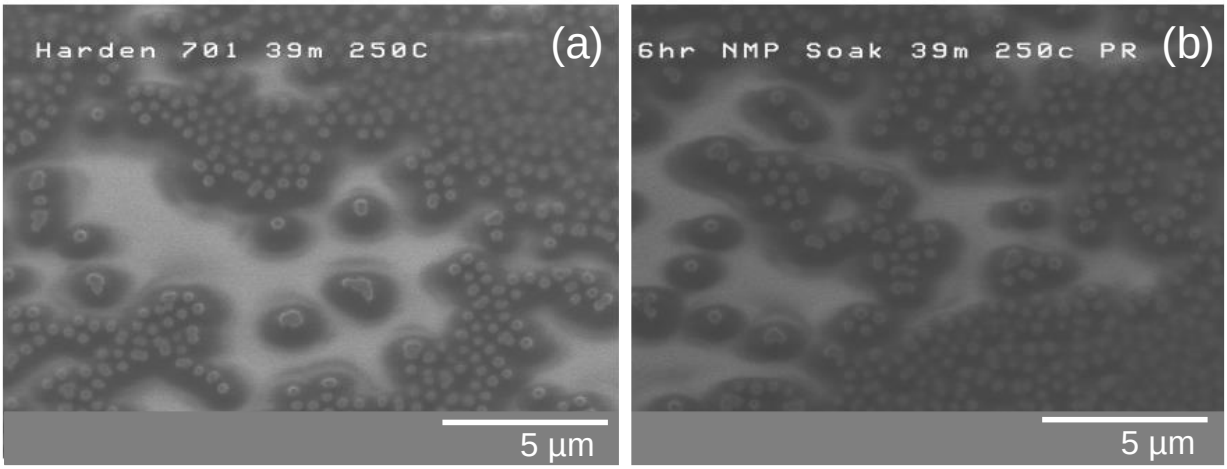

Fig. 34. (a) 701 coated sample baked for 39 minutes at 250ºC, (b) baked sample after 6 hour exposure to NMP.

Denser nanowire arrays with high aspect-ratios, however, exhibit different coating behaviors. Nanowires with heights of ~ 7 µm, diameters of ~2 µm, and spacing of ~1 µm were coated with 701 photoresist to study planarization. These wire arrays show a poor coating, with areas in the arrays left entirely uncoated, Fig. 35. In the areas of the array with photoresist, the resist is seen to only coat the tops of the wires, leaving voids below the wire tips, Fig. 35. Therefore, photoresist is not well suited to planarize dense, high aspect ratio, nanowire arrays.

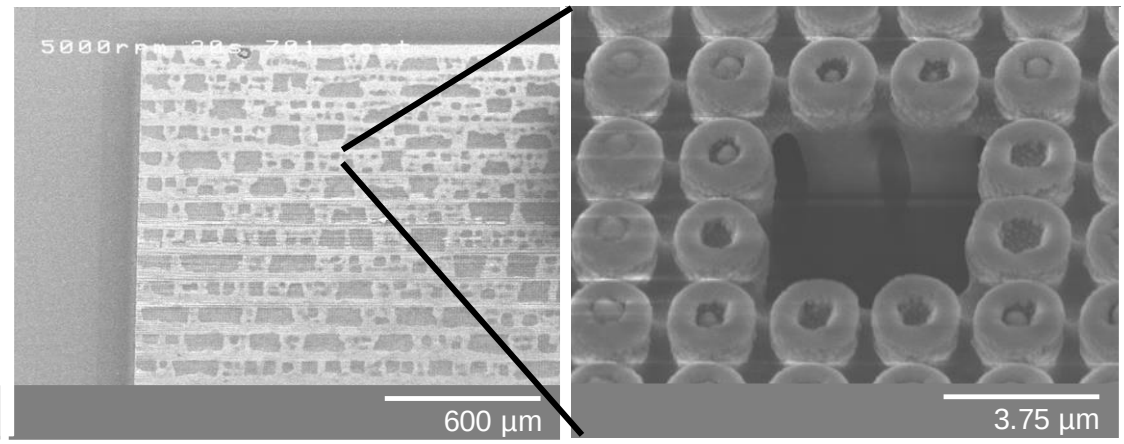

Fig. 35. Uneven photoresist coating on dense high aspect-ratio nanowire arrays.

Conventionally GaN devices utilize all topside contacts, due to the non-conductive substrates. As such, during the final process steps contact cuts are made through the dielectric layer to reach the buried metal layers. After the baking step the photoresist can no longer be removed through conventional solvents and dry etching is to be utilized. To etch the photoresist, use of an O_2 plasma has been found to successfully remove the cross-linked photoresist. Similarly, a hard mask is to be utilized for a patterned etch, as the masking photoresist would also be removed. Photoresist represents an alternative process to PDMS dielectrics, though is unable to be coated in dense arrays and absorbs in the blue/UV regime. Additional work is planned to be conducted to further study the possibilities of a photoresist dielectric.

2.3 Photolithography Patterning

Semiconductor devices rely on advanced photolithography in order to create nanoscale patterns. In photolithography, photoresist is coated and used as the light sensitivity medium for patterning, which upon development reveals the pattern. There are multiple methods and tools through which pattern transfer can occur. Contact lithography is the earliest method for

photolithography pattern transfer, where a chrome photomask with the etched design is placed either in contact or proximity to the wafer. The limit of contact lithography is the inability to produce submicron features due to the near field Fresnel diffraction. The wafer is never in perfect contact with the substrate due to debris and non-uniformities. Projection lithography is the primary technology used in commercial semiconductor products. Projection lithography makes use of a mask separate from the wafer, with a number of lens elements to scale and transfer the pattern into the photoresist film. While projection lithography has key advantages for production, it is not well suited to research and development work due to the cost of mask production.

Alternatively, direct write systems such as electron beam lithography or laser direct writing, provide pattern transfer without photomasks. Direct write systems are series systems, in that the beam is scanned across the surface to create the pattern. Increased flexibility is offered in these systems for prototyping, with the drawback of slow speeds.

- **Heidelberg Laser Direct Writing**

The RIT SMFL facility possess a Heidelberg DWL 66+ laser writing system. The Heidelberg takes a mask file in GDSII format and uses a 405nm laser in order to expose the photoresist. The tool has two different write heads available, the 20mm for features as small as 4 µm, and the 4mm that can go down to 0.8 µm. The difference 20mm write head can write features faster than the 4mm write head due to the larger laser spot size. Staff in the RIT SMFL make use of the tool for writing masks, though users had not used the system to achieve submicron features. Development work had to be done in order to develop a process to achieve micron to submicron patterns for nanowire devices.

The conventional mask writing process on the Heidelberg made use of pre-coated AZ 1505 photoresist. The chrome masks were purchased with this coating and no AZ 1505 was available for separate coatings in the SMFL. For these tests, LOR with AZ MIR 701 photoresist were coated onto GaN wafers for a thickness of 1.1 µm. Due to height limitation in the tool, 2" wafers or small pieces were mounted to a mask with water. While the water held the samples in place, water will do nothing to remove the wafer bow that inherently exists. When aiming to pattern nanoscale features small variations in the height lead to large changes is dose. This can be seen from Fig. 36, looking at the critical dimension (CD) vs. focus.

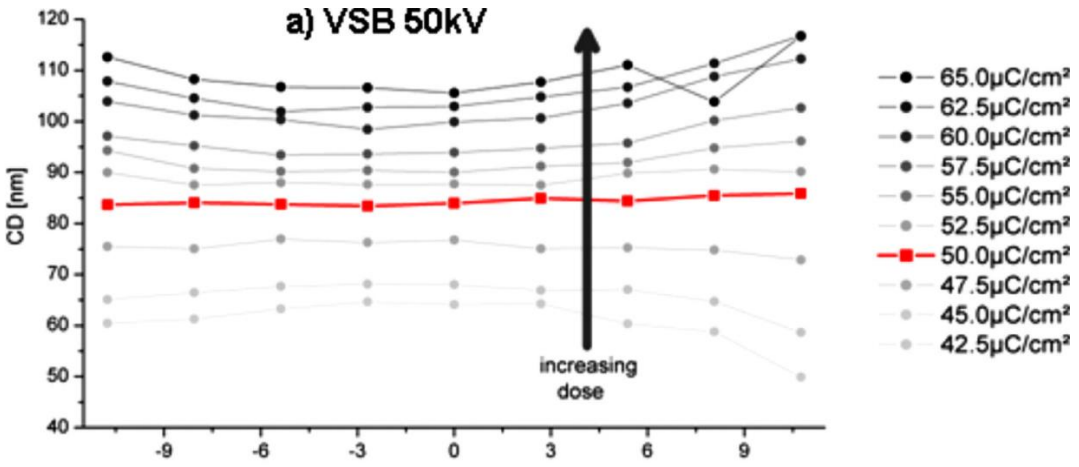

Fig. 36. CD vs. Focus curves ©2009 AIP Publishing, Reprinted with permission. [55]

When trying the standard water mounting technique, the results lead to severe non-uniformity, that is demonstrated in Fig. 37. The write head tries to focus, though due to the changes in the wafer, as the beam scans the left side CD is almost double that of the right side.

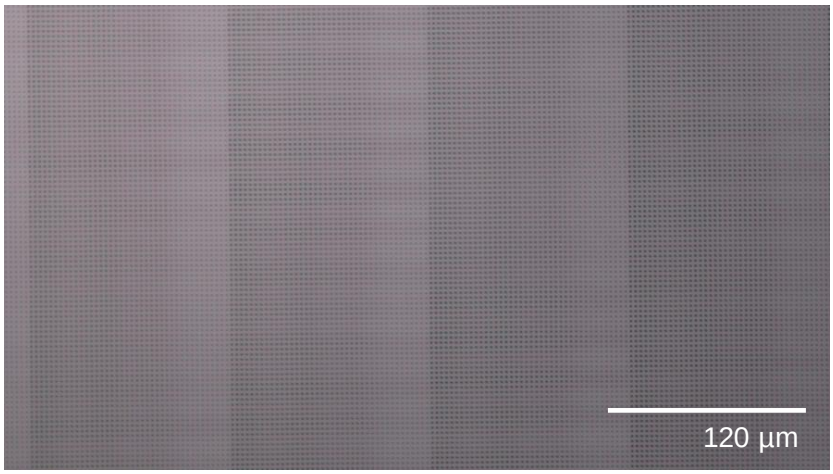

Fig. 37 Variation in laser stripe width due to poor focus.

In order to solve this issue, a piece of precision engineer plastic was utilized as a spacer. Vacuum holes were drilled which mated up to the stage, and high grit sandpaper was used after the drilling to remove and height differences, Fig. 38. The design is optimized for a 2” wafer, though smaller pieces can be used when placed in the center and the rest of the vacuum holes covered are covered by silicon. Only pieces bigger than 1 cm can be processed due to the pneumatic focus.

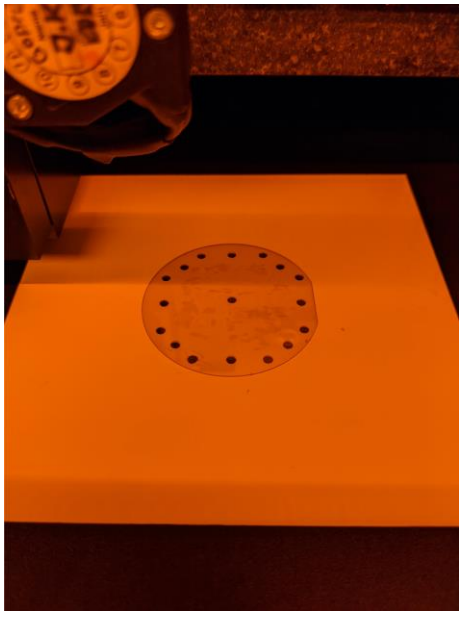

Fig. 38 Engineered plastic spacer with vacuum openings for 2” wafer.

Use of the plastic spacer allows the wafer to be pulled down with the stage vacuum in order to correct for wafer bow. The results show a remarkable improvement, where lithography was previously almost impossible to perform. The patterns instead are very uniform across the stripe width and wafer, Fig. 39.

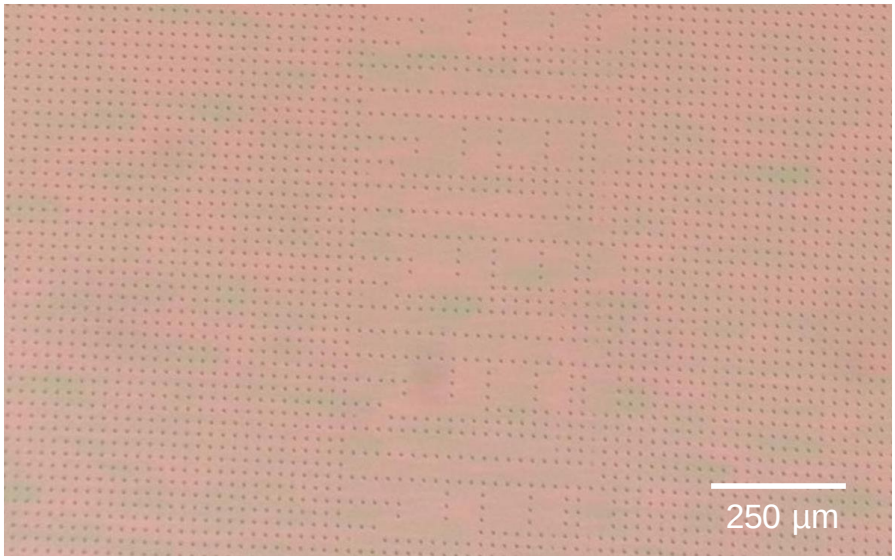

Fig. 39 Improved pattern uniformity with use of the plastic spacer and vacuum.

Through continued use of the tool, it is found that focus and dose and change over time, particularly if the tool is idle for a period of time. Many direct write systems, such as e-beam lithography have similar behavior. Tests with photoresist between writes on the 4mm write head vs. the 20 mm write head were studied. The general process of record on the 4mm makes use of the 25% laser filter due the smaller spot size of the laser, leading to a higher dose. Taking an exposure job from the 4mm to the 20mm, it is found that the focus is the same though the dose is ~2.5x higher with use of no filter. Of separate note, the 4mm write head was found to incapable of processing clear-field patterns, with significant non-uniformity across the wafer, not corresponding to focus variation.

- **GCA GaN Patterning**

The RIT SMFL facility possess a 6800B DSW wafer stepper, which is a g-line (436 nm) exposure system. Work has been previously done on pieces, though years ago, and no work had been done to develop an exposure system with GaN. To start the stage offsets were calculated for the first time for a 2” wafer, in order to center the array to the wafer. The calculated offsets are 0.25 for the X and 12.25 for the Y, making use of the 4” wafer parameters and switch position. Next focus exposure matrix (FEM) tests were performed making use of a high resolution test mask with various clear field and dark field features. It was determined that a time of 0.5 seconds was best of AZ1512 resist, and 1.2s for AZ701. Due to the low NA of 0.28, the system has a large depth of focus (DOF). The focus in the FEM was varied from +25um to -25um with little observable effect, though +25 resolved smaller 1 µm features the best, Fig. 40.

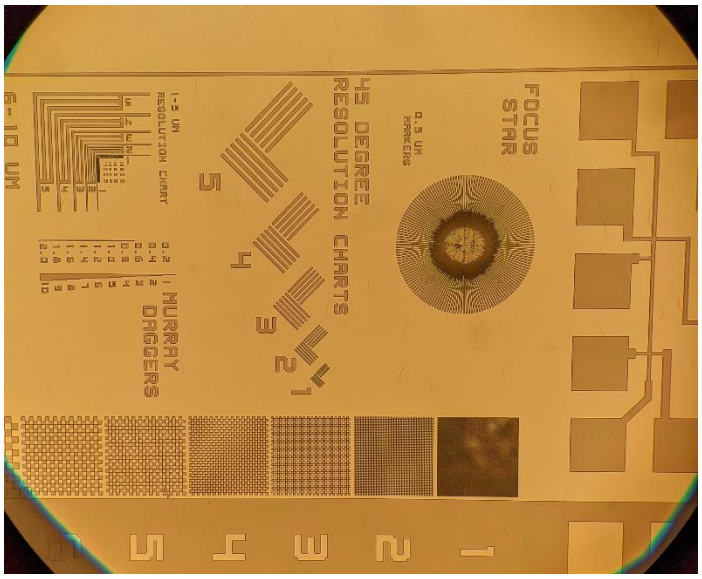

Fig. 40 Test Die with best results of 0.5s exposure and +25µm focus.

Variations in exposure can be very drastic for high contrast photoresist, such as AZ1512. Fig. 41(a) shows the exposure time of 0.4s in AZ1512 and 0.5s in Fig. 42(b). Small changes are

highlighted with the resist close to being fully cleared. Rings from where the vacuum pulls on the wafer can be seen, where these slight differences are amplified.

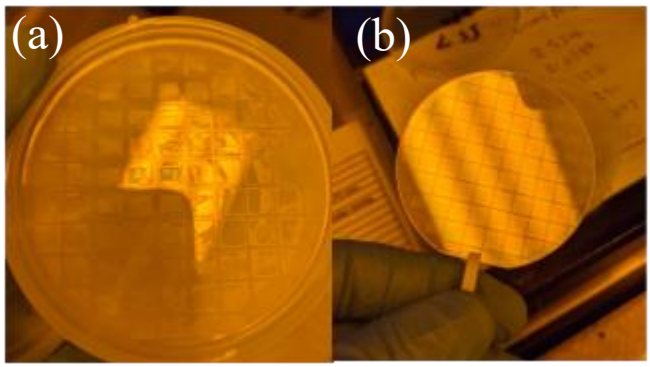

Fig. 41. (a) 0.4s exposure, (b) 0.5s exposure in AZ1512.

Alignment is a key challenge on the GCA system, where positions on the Heidelberg patterned mask are not as straightforward as they should be. Many users utilize older legacy masks/patterns, or use of external companies for mask fabrication. The Heidelberg laser mask job positions the center of each design +/- 2 cm in the x or the y direction for a four pattern design. These 2 cm offsets are programmed into the job file, and added to the position of where the alignment mark should be. It was found however, that the system is roughly off by 1 mm in the +y direction relative to the wafer stage. Despite these flaws, the GCA provides high quality pattern of features ~1 µm in size.

- **Electron beam lithography**

Patterning with a direct write laser system is inherently limited by the exposing wavelength, with diffraction occurring as the features as scaled down. Compared with visible or UV light, electrons have much smaller wavelengths of 1.23 nm. Making use of electrons for patterning over optical lithography allows the realization of single nanometer sized devices. Electron beam (e-beam) lithography functions in a similar serial manner to laser direct write

systems, though with more complex elements, slower write times, and increased cost. The e-beam system is analogous to a SEM operating at higher accelerating voltages. Conventional photoresists used in optically lithography can not be used for e-beam lithography, as the acid generation process is too inaccurate. Instead, plastic coatings such as poly(methyl methacrylate) (PMMA) are selected, as upon exposure, the bonds are broken which can be developed away.

Initial development work to make nanoscale e-beam patterns for nanowire devices was conducted at Brookhaven National Labs on a JEOL JBX-6300FS system. The test layout contained features from 300 nm down to 60 nm in size, with various pitches. Due to the variations in both size and pitch, proximity correction was performed with Beamer in order to deliver optimal doses to each region. E-beam lithography is more sensitive to factors such as pitch compared to conventional photolithography, as electrons can travel through the material to modify the dose in different regions.

PMMA-A6 was first coated unto the samples at 3000 rpm for thickness of 300 nm and then baked for 3 minutes at 180ºC. PMMA-A4 was coated on top at 3000 rpm for a thickness of 200 nm, and then baked at 180ºC for 3 minutes. PMMA-A6 has higher sensitivity to the exposure compared with PMMA-A4 which leads to an undercut structure, Fig. 42. The dual coating replicates the LOR-photoresist combination, though at the nanoscale.

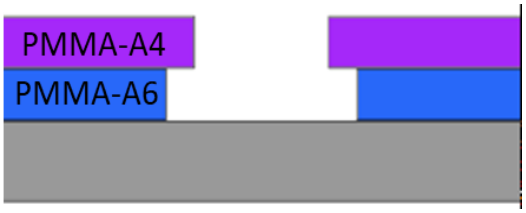

Fig. 42. Dual coating of PMMA-A6 and PMMA-A4 after exposure and development.

To increase exposure speeds, a larger beam current of 8nA was utilized. The smallest feature sizes of 60 nm, large by e-beam standards, allowed for the larger beam current. To

determine the baseline dose, from which the proximity correction is based, a 3x3 exposure array was patterned with does from 750 uC to 1950 uC. Development occurred after exposure for 2 minutes in 1:3 MIBK:IPA, followed by a rinse in IPA. Unlike conventional lithography, solvents are used for development rather than a strong base. From the exposure tests, a baseline dose of 1250 uC was found to produce the best results. Subsequent exposures were run under the 1250 uC baseline dose, with similar development conditions. Samples were patterned with three die in each corner of the 2" wafer. Write times for these devices averaged ~1 hour per wafer. Green and blue LEDs grown on sapphire were patterned, along with blue LEDs grown on silicon. The patterning results post-develop are shown in Fig. 43 for features from 300 nm down to 70 nm with the same scale bar. The smaller 60 nm features were a sparse pattern which proved difficult to locate under SEM.

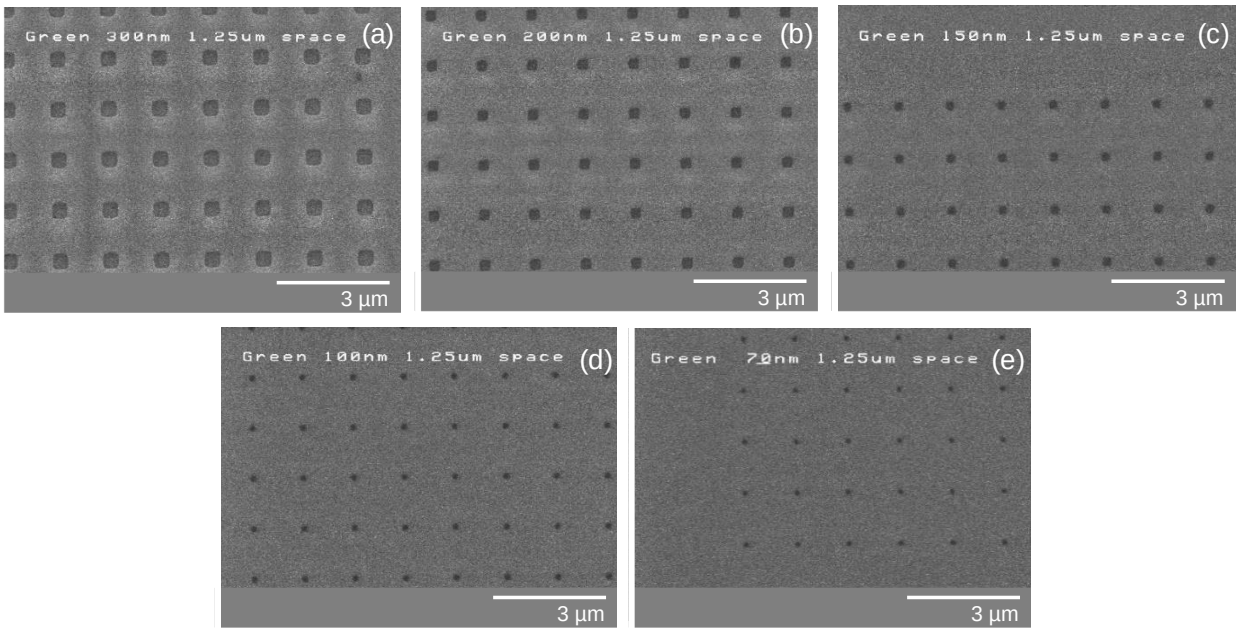

Fig. 43. (a) 300 nm e-beam patterned dots, (b) 200 nm e-beam patterned dots, (c) 150 nm e-beam patterned dots, (d) 100 nm e-beam patterned dots, (e) 70 nm e-beam patterned dots

- **Metal lift-off**

Once the patterns are formed either through optical or e-beam lithography, a metal lift-off is utilized in order to form the critical layers of the devices. GaN devices make common use of Ni for the p-type ohmic contact and an intricate Ti/Al/Ni/Au metallization from the n-type contact [56]. Use of these metals necessitates the use of lift-off processes as Ni can not practically be dry etched, and there is not a single process that can etch a four metal stack. Lift-off with photoresist provides a way to accomplish the patterning of these materials through a stencil-like approach. Conventionally a dual layer coating is utilized with the bottom layer have a faster dissolution rate in the developer compared to the top layer. An undercut is therefore created which prevents continuous metal formation upon deposition, and later allows solvents to dissolve the resist stack, lifting off the metal.

To form ordered nanowire arrays for LED display applications, Ni is deposited and lifted-off to both form the hard mask for the dry etch and the ohmic p-type contact. Two methods of Ni deposition were tested based on the tools available, either e-beam deposition or thermal evaporation. The e-beam deposition tool makes use of an electron gun in order to heat a crucible containing the metal. The sample is positioned at a ~45^{o} angle and rotated to provide a more conformal coating. In contrast, the thermal evaporator runs current through a tungsten boat with the metal wire, while the sample is positioned perpendicular to the boat. Both systems were pumped below 5E-7 torr in order to lower the metaling temperature of the Ni, as Ni requires high temperatures in order to evaporate.

Use of the e-beam deposition system, with the rotating planetarium introduces a slight angular component to the point-source deposition. Much of the metal is deposited perpendicular to the pattern with slight sidewall depositions. Through this method, 350nm of Ni are deposited

and lifted-off. The post lift-off results of the Ni dots are shown by Fig. 44(a). The angular component of the deposition leads to a thin metal ring around the base of each Ni dot. Sidewall coating of structures is possible through angular deposition, though for use of hard making an etch, the ring which forms is detrimental. The nanowire dry etch is anisotropic in nature in order to form vertical nanowires. During the dry etch, the thin ring around each dot is quickly etched away, while the bulk of the Ni dot remains. Loss of the thin ring leads to surface roughness along the nanowire which is shown by Fig. 44(b). Surface roughness of the nanowire can lead to additional leakage and act as a platform for metal deposition which can short the device.

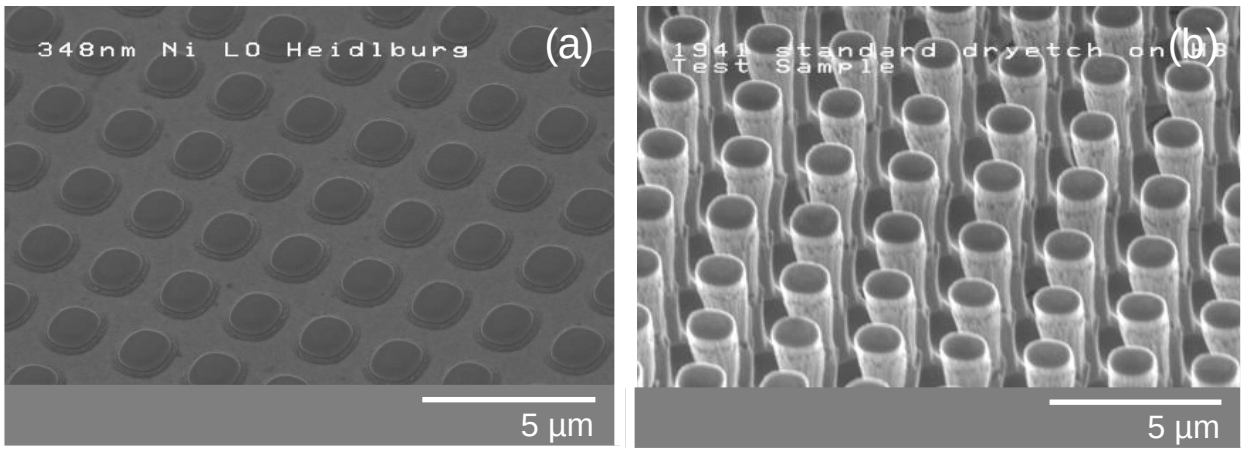

Fig. 44. (a) 1 µm Ni dots formed through e-beam deposition, (b) post nanowire etch results.

Thermal evaporator of Ni makes use of high melting temperature metals such as tungsten or molybdenum as carriers in order to melt the Ni through electrical heating. Low voltage and high current flow allow for the rapid heating of the carrier boat to melt the metals. The thermal evaporator utilized for these tests was a CVC bell jar evaporator. The system makes use of a flat platen, making the wafers perpendicular to the evaporating metal. Use of a flat platen minimize any angular deposition. The boats for the evaporator were tungsten coated in alumina, with a circular pocket for the metal. Use of the alumina prevented alloying of the deposited metal and the

tungsten boat. Use of this type of metal boat also modifies the profile of the metal deposition, where the behavior is more closely related to a cosine function than a circular point source [57]. The cosine behavior reduces angular deposition further and reduces sensitivity to positioning the samples perfectly over the boat. 275 nm of Ni was thermally evaporated unto the samples and lifted-off through the use of NMP. The CVC thermal evaporator led to added sample heating over the e-beam evaporator due to the differences in the thermal mass of the metal platen. The slight increase in heat led to residual film stress of the Ni on the photoresist which aided in lift-off.

The profile of the thermally evaporated metal looked distinctly different compared to the e-beam evaporated sample, Fig. 45(a). There is no clear angular deposition on the thermally evaporated sample, with the metal thickness narrowing as the deposition proceeded. The narrowing of the metal that occurs is due to the deposited metal pinching off the photoresist opening as the deposition proceeds. The faint pattern around the Ni present in Fig. 45(a) is due to excessive undercut of the LOR in this sample. Following lift-off, the sample was anisotropically etched in order to form the vertical GaN nanowires, Fig. 45(b). The profile of the nanowire post etch is shown to be far smoother compared to the results from the e-beam deposition. Less metal pull-back occurs in the case of thermal evaporation due to the distinct profile. The nanowire etch is seen to round the deposited metal, though the Ni still acts as an effective mask leading to a smooth etch.

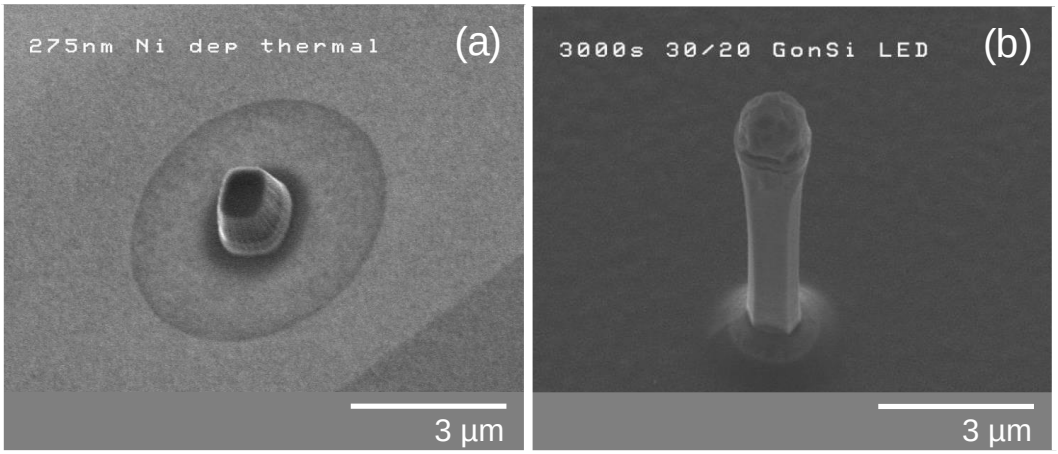

Fig. 45. (a) 1 µm Ni dots formed through thermal evaporation, (b) post nanowire etch results.

Thermal evaporation is also necessary for the deposition of metal layers in vertical nanowire devices. Any angular deposition would short the distinct regions of the vertical nanowire devices. Directional deposition is needed and is made possible through the use of thermal evaporation. Tests are performed making use of vertical GaN nanowires and positioning the sample directly over the metal boat in order to best achieve direction deposition. To best study the direction deposition, the n-type four-layer metal stack was deposited. The n-type metal consists of 10 nm Ti, 140 nm Al, 30 nm Ni, and 100 nm Ag. The CVC thermal evaporator has a rotating carousel which allows four metals to deposited during a single pump-down. Results of the metal deposition are shown in Fig. 46. Metal is seen to be deposited only at the top of the nanowire and at the base of the structure. The textured surface is taken as evidence of metal deposition, while the smooth sidewalls of the nanowire show no sidewall deposition. On the nanowire tip the diameter is expanded a bit due to the metal deposition due to the same effect which makes the diameter smaller of the deposited Ni in Fig. 46. For the development of vertical nanowire devices, thermal evaporation provides advantages over e-beam evaporation due to the ability to directionally coat a wide range of metals.

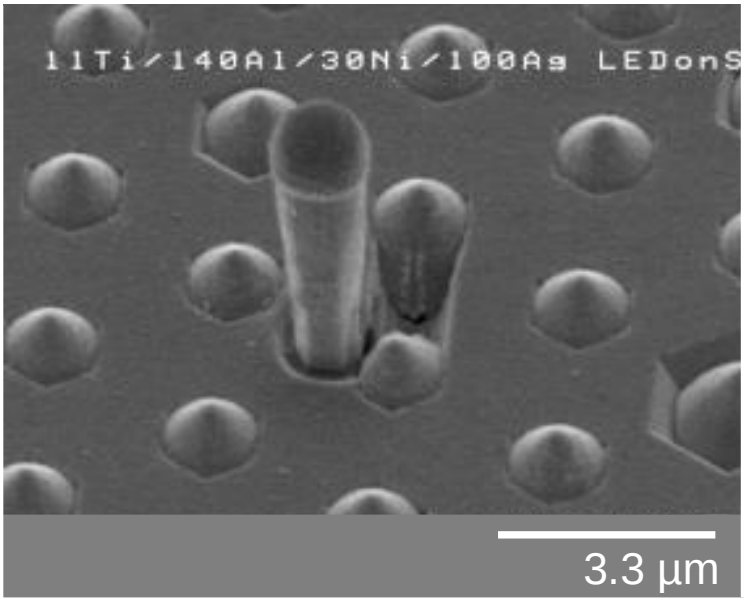

Fig. 46. Ti/Al/Ni/Ag thermal evaporation on a vertical nanowire.

2.4 Dry Etching and Wet Etching

To create arrays of high aspect ratio GaN nanowires, both the dry etching and wet etching are to be precisely optimized. GaN has a wurtzite, hexagonal, crystal structure compared to the diamond lattice of Si and other common semiconductors. KOH rapidly etches along the <100> plane of silicon and slowly etches the <111> direction leading to the formation of pyramidal etch pits in <100> type Si. When KOH etches GaN nanowires, the sloped $<1\bar{1}01>$ plane rapidly etches to form a perfectly vertical structure, Fig 22. The $<1\bar{1}00>$ planes that are the sidewalls of a perfectly vertical nanowire are more slowly etched to give diameter control. Meanwhile, the surface <0001> plane remains unetched. The KOH etching process can therefore take an etch which is not perfectly vertical and create nanowires that are perpendicular to the substrate. The drawback on the wet etching process is the etching time in order to tailor the nanowire geometry. Instead, having an etch that is approximately anisotropic reduces the total wet etching time. The dry etch making use of a Lam 4600 etcher has been optimized in order to achieve an anisotropic

etch for GaN nanowires, shown by Fig. 47. Details on the development of both the dry etch and the wet etching can be found from references [51, 58].

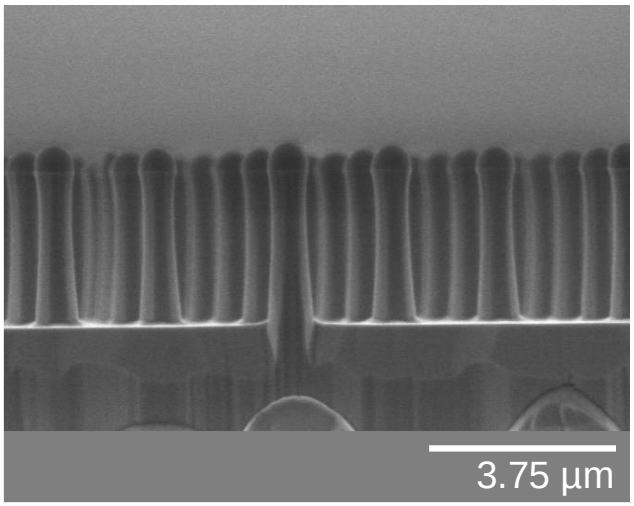

Fig. 47. Vertical GaN nanowire etch with Ni hard mask, photo credit: Bryan Melanson.

Inductively coupled plasma (ICP) is an alternative technique compared with RIE. Additionally, control over the etch in terms of remote plasma generation, allows for increased functionality. A Plasma-Them Apex ICP system was a utilized in order to study the etching differences between RIE and ICP for the formation of GaN nanowires. Samples were mounted to a glass carrier wafer with Santovac 5 vacuum grease for thermal conductivity. The ICP coil leads to higher ion fluxes to the wafer, creating more heat compared with a conventional RIE system. The ICP system also operates at lower base pressures of 10 mTorr and below, compared with RIE which operates at 30 mTorr or greater. Various parameters such as gas choice, gas ratio, gas flow, pressure, ICP power, and bias power were tested with the use of Ni dots for a hard mask. Forward bias power was power was found to be a key parameter in etch selectivity, while ICP power determined if the chemical nature of the etch dominated. Cl_2 and Ar were found to produce the most anisotropic profile, while BCl_3 greatly increased the base diameter relative to the top of the wire. Increasing flow rates and pressure was found to lead to a chemically dominated etch, with a

porous surface, shown by Fig. 48. The chemical etching regime is also seen to affect the Ni hard mask, potentially due to the added heat in the system. For these initial tests a flow of 40 sccm Cl2, 10 sccm Ar, 100W bias, 500W ICP at 5 mTorr was found to be optimal, Fig. 49. An etch rate of 600 nm/min with a selectivity >30:1 were recorded with Ni.

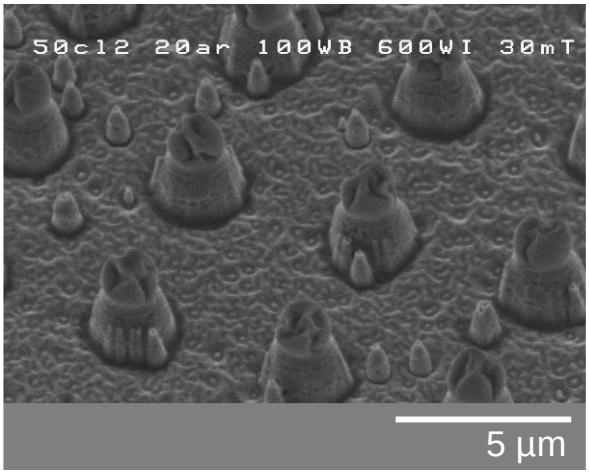

Fig. 48. 50 sccm Cl_2, 20 sccm Ar, at 30 mTorr porous etch.

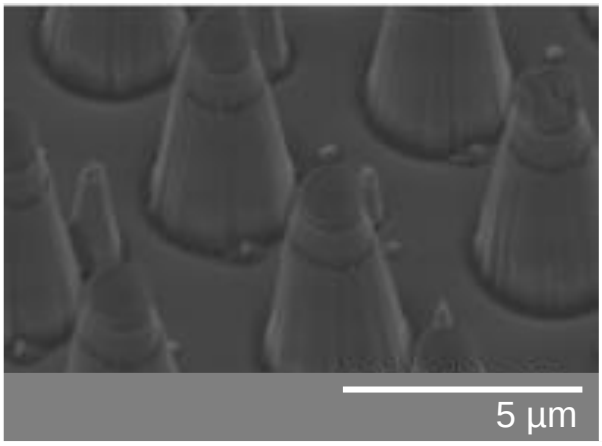

Fig. 49. 40 sccm Cl_2, 10 sccm Ar, at 5 mTorr etch.

Chamber conditioning was found to be critical, where after the system is opened or idle for a long period of time, the profile of the etched nanowires can change. Fig. 50(a) shows a nanowire etch after the tool had been opened up for service. After running the standard nanowire etch recipe

on a dummy wafer for 40 minutes, the nanowires go back to producing a nice vertical shape shown in Fig. 50(b). While KOH etching can take the initial tapered structure and form vertical nanowires, the extended wet etch time is not ideal, and instead it is preferred to condition the chamber.

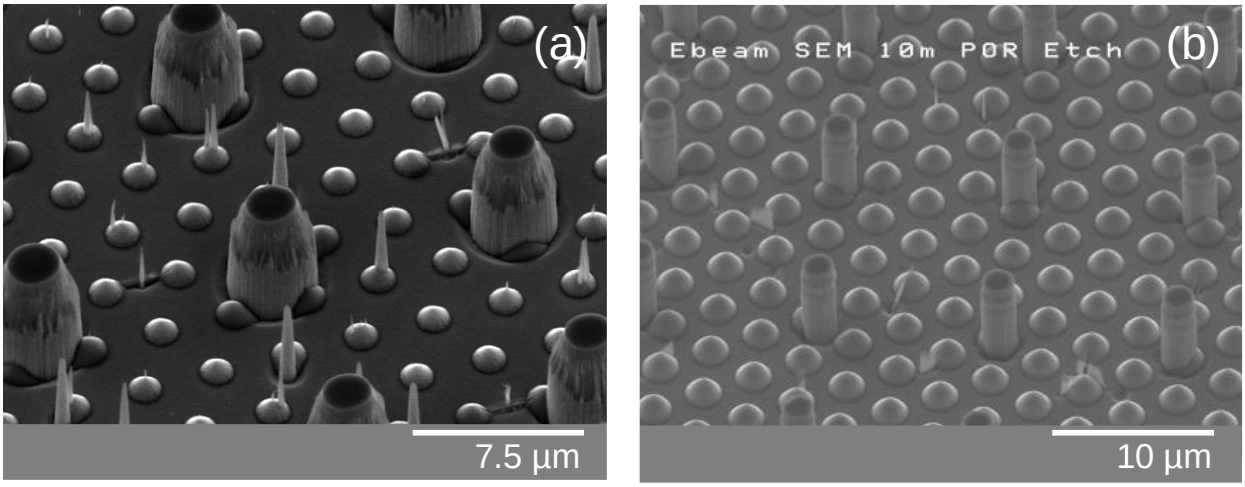

Fig. 50. (a) Unseasoned chamber, (b) seasoned chamber.

Making use of photoresist over Ni can be done for more shallow etches, such as for planar LED fabrication. Poor selectively of photoresist is found, where the selectively is ~1:1. The photoresist also partially cross-links due the high heat and chlorine based chemistry. Photoresist removal in solvents lead to a surface scum on devices which require use of an O_2 plasma clean or piranha etch.

The combined optimizations of both dry and wet etching opens the possibilities for new device fabrications. In order to fabricate flexible nanowire devise, the nanowires must be removed from the host substrate. GaN grown on Si is utilized for this purpose in order to target Si to GaN nanowire removal. The optimized anisotropic dry etch through the RIE [58], is employed is etch nanowires down into the Si substrate. Silica nanospheres are utilized initially for these test devices, where good selectivity exists. Samples are etched through the ~6 µm of GaN and ~1 µm into the Si substrate. Results from the etch are shown by Fig. 51, and show the smooth GaN nanowire in

contrast to the rough silicon surface. The dry etch has been optimized for the etching of GaN and leads to a tapered base upon etching silicon, due to the different dry etch mechanisms.

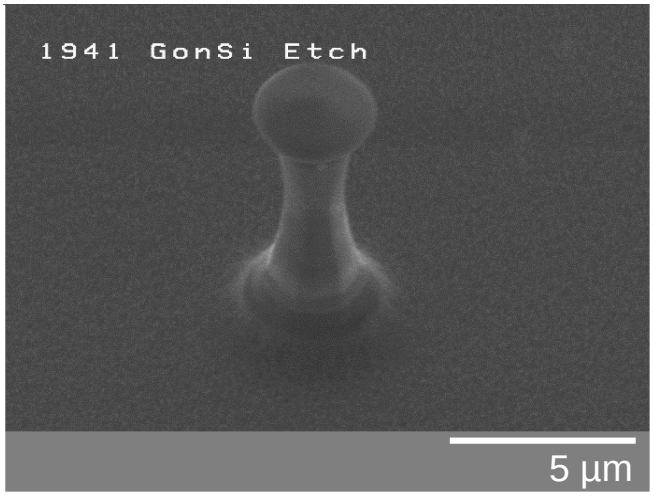

Fig. 51. Dry etch of GaN nanowire on Si.

The sphere is removed after the dry etch in BOE, in order to later make electrical contact to the top device. KOH etching is performed in order to etch the Si at the base of the nanowire. The silicon wafer is <111> type for GaN growth, which etches very slowly in KOH. GaN also etches in KOH, though very slowly at room temperatures. Therefore, the Si at the base of the wire is selectively targeted through the use of a room temperature KOH etch. Etching occurs transforming the sloped Si tapered base, into an anisotropic nanowire. Results from the etch can be seen from Fig. 52, showing the GaN wire on top of the silicon nanowire. The KOH etch reveals the <110> crystal plane of silicon which is vertical to the <111> plane. The diameter at the base of the nanowire had a total width of 5.275 µm, which has been reduced to 0.75 µm after a 53 minute etch in 100% AZ400K developer at room temperature. The etch rate is found to be ~85 nm/min.

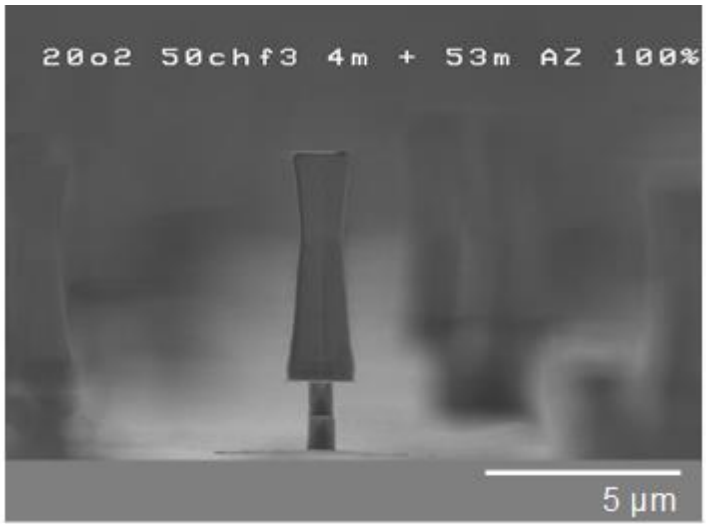

Fig. 52. Si nanowire base etch.

Care is to be taken when etching the Si nanowire base to prevent over etching. The diameter of the wire is to be a few hundred nanometers for GaN wire diameters of ~2 µm. The etched nanowire base aids in the mechanical release of the GaN nanowires though the later embedding in a flexible polymer. Over etching of the Si leads to nanowire collapse, due to the weight of the GaN wire, Fig. 53. Evident in Fig. 53, above the Si nanowire, is the thin AlN buffer layer which is utilized for GaN growth on Si. The AlN is resistant to the KOH etch over Si and GaN, and is not removed. The inherent properties of a chemical etch lead to slight non-uniformity in etching rate across the sample. The variations in etch rate limit the Si undercut diameter to several hundred nanometers in order to compensate for this effect. KOH etching of GaN-Si integrated nanowires provide novel device integration schemes, besides flexible electronics, which are being actively investigated.

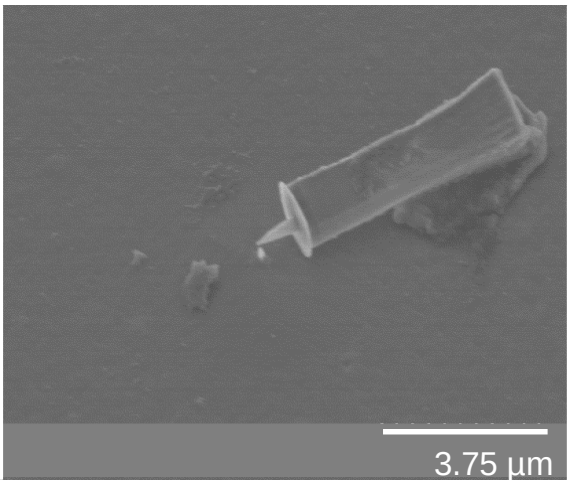

Fig. 53. Si nanowire base over etch.

2.5 Film Characterizations

Metal film and surface treatments are used in a variety of devices, though require application specific optimizations. GaN LEDs rely on ITO as a transparent conductive contact, though careful optimization is required to achieve low resistivity and compatibility with LED processing. Metal annealing is required to achieve low resistivity to GaN and processes have been developed in the RIT SMFL. The GaN surface and PDMS surfaces are natively hydrophobic and an O_2 plasma process has been developed in order to convert the surface to hydrophilic for process compatibility. Al_2O_3 is utilized a common dielectric in GaN devices and etches are developed for thin layers.

- **ITO Optimizations**

ITO is a transparent conductive film used in numerous display applications [34-35]. The ITO film has a wide bandgap of ~4 eV and is heavily n-type doped, allowing low resistivity and optically transparency [46]. The ITO deposition available in the RIT SMFL makes use of a

sputtering process in a CVC 601 system. The process of record for sputtering ITO uses 40 sccm Ar, at 5 mTorr, 180 W, with a pulse DC sputter at 1616ns. A pre-sputter is done for 15 minutes prior to the actual deposition in order to clean the target. The sputtering occurs with a deposition rate of 5.5 nm/min under these conditions. As deposited, the ITO on glass has high sheet resistance of ~ 10,000 ohm/■ and has low transmittance with a yellow hue. The yellow hue is an indication of excess indium and a lack of O_2 during the deposition. To increase the O_2, improving both the sheet resistance and transmission, the effects of annealing were tested. A hotplate in room air was chosen over a furnace, due to the rapid transfer of heat, allowing for quicker anneals. Tests at temperatures of 150°C and 250°C were tested with time durations of 10 minutes, with the sheet resistance taken through a four-point probe. Results for the sheet resistance are shown in Fig. 54, which show an initial drop with time and a leveling off for both temperature ranges. For the case of 150°C, there is an initial drop from 9300 Ω/■ to 4372 Ω/■ after 10 minutes, followed by a leveling off at ~ 3200 Ω/■ after 30 minutes. The 250°C anneal shows a similar drop off, going from 11300 Ω/■ down to 309 Ω/■ after 10 minutes, followed by leveling off at ~ 85 Ω/■ after 30 minutes. Increased temperatures allow different degrees of either crystallization and/or oxygen penetration into the film. Marginal further results are expected with further increases in temperature, though with diminishing returns.

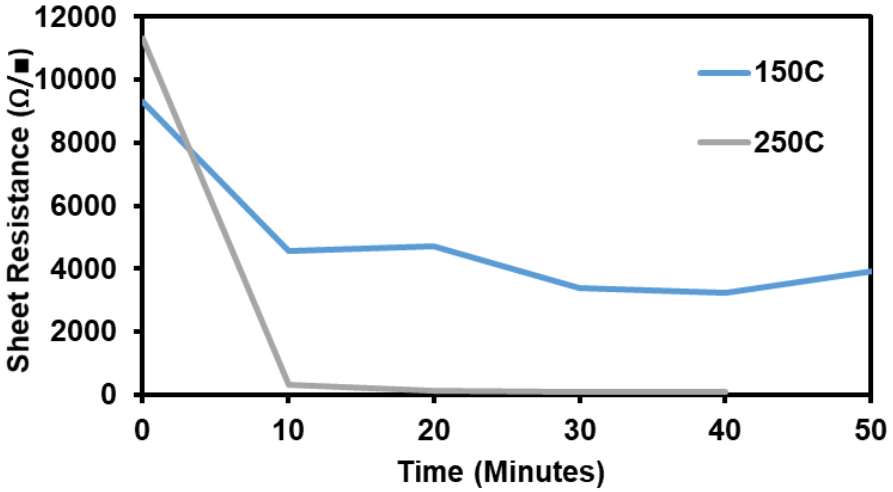

Fig. 54. ITO sheet resistance after anneals at 150°C and 250°C.

The as deposited ITO film exhibits low transmission with a yellow hue on a glass slide. Annealing at 150°C improved the sheet resistance of the film, though the optical properties remained the same, Fig. 54. Annealing at the higher temperature of 250°C showed booth a large decrease in the sheet resistance, and also an increase in optical transparency as by Fig. 55. Tests with higher temperatures should yield a further improvement in optical transparency.

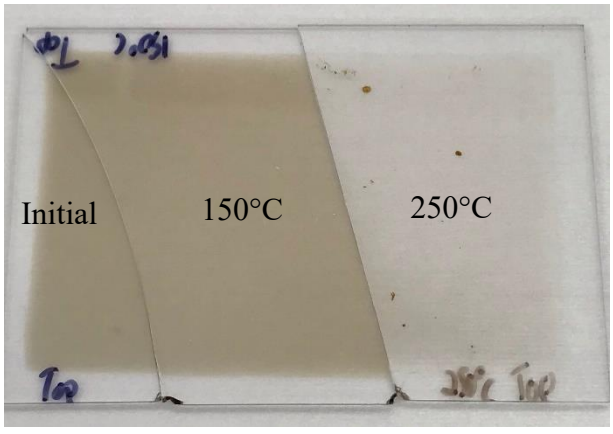

Fig. 55. ITO optical quality after anneals at 150°C and 250°C.

Having optimized the resistivity and optical properties of sputtered ITO, steps to characterize the etching were conducted. The as deposited ITO is amorphous in nature and readily etches in a variety of chemistries. In contrast annealed ITO is more resilient to etches, necessitating the etch patterning before annealing. Both unannealed and annealed ITO is resistant to fluorine based dry etches, showing only a low etch rate in chlorine based dry etches [59-60]. Etching of ITO is preferred over a lift-off process as sputtered material makes lift-off difficult, often tearing the metal even with a dual layer resist stack. The photoresist is coated on top of a planar film with etching to target the ITO. For certain device applications, ITO is patterned on top of an oxide film where both requiring patterning. BOE was found to etch both unannealed ITO along with the underlying oxide film in a single step. Before photoresist is coated the unannealed ITO was found to be hydrophilic and required an O_2 plasma treatment. Photoresist is then coated and patterned, with a hard bake at 140°C for 2 minutes. Etching in BOE resulted in a high etch rate of ~100 nm/min for the ITO film. In the etched regions, the post-etched sample showed a particles remaining on the surface, Fig. 56. These particles between the nanowires are assumed to be particles of indium on the surface of the wires. Extended etching in BOE can be utilized to remove the particles, though as the particles are discontinuous they are not impactful.

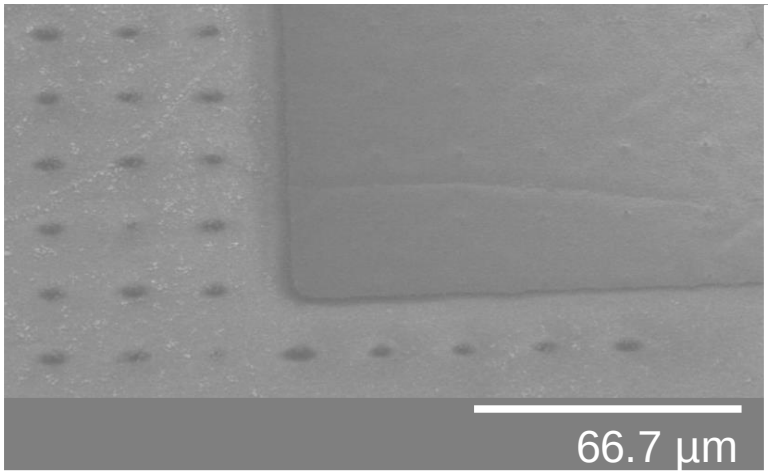

Fig. 56. 100nm of ITO etched in 10:1 BOE.

Tests with diluted HCl were also studied in order to have cleaner removal of indium from the substrates. 100 nm of ITO was coated on glass slides in order to study the effects of the etch. First LOR was coated 600 nm thick to act as an adhesion layer for the AZ1512 photoresist which was subsequently coated. Testing concentrations found 10 ml of HCl diluted in 40 ml of water to give a fast etch of ~300 nm/min, though minimal undercut and no resist lifting. To just the etch, the photoresist was mechanically removed to show a side by side effect, Fig. 57.

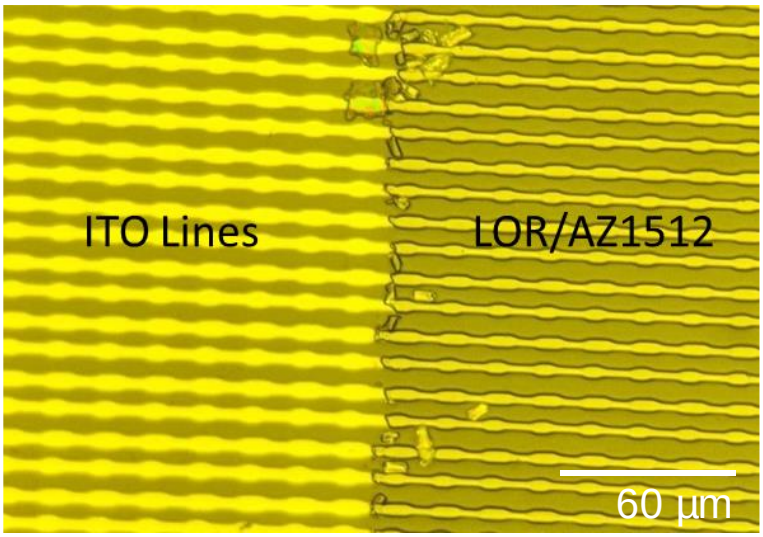

Fig. 57. 1:4 HCl 20 sec etch comparison.

Dry etching was also explored, though with more limited selectivity due to available gases. Hydrogen is often employed during ITO etches, though represented a more hazardous process. Instead it was found that sputtering with Ar provided great results with minimal undercut. Operating with 70 mT, 50 sccm Ar, and 200 W produced an etch rate of ~20 nm/min [60]. The results of the etch are shown in Fig. 58, again with the mechanical exfoliation of the LOR/AZ1512. While there is no risk of resist de-adhering in a dry etch, additional care must be taken as the Ar provides poor selectively to any underlying film.

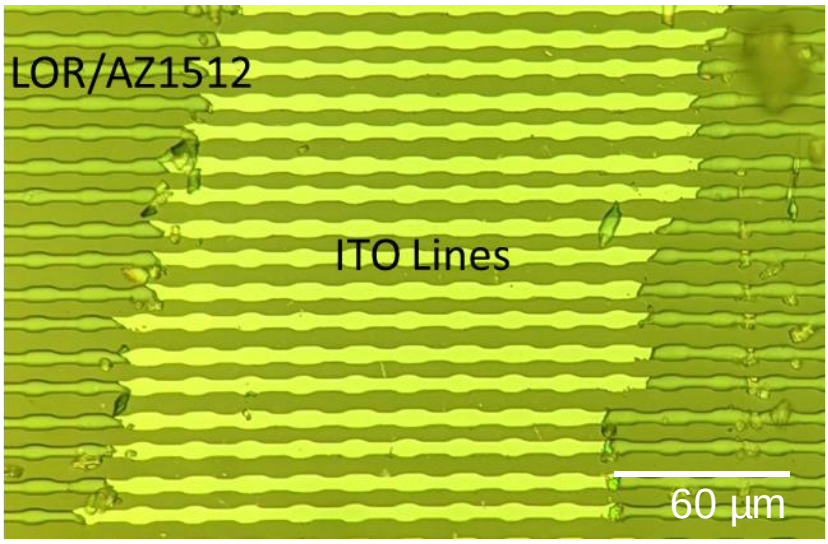

Fig. 58. ITO Ar etch comparison.

Once the sample is patterned, the annealing step can then be performed in order to both lower the sheet resistance and increase the optical transparency.

- **Metal Annealing**

To achieve a low resistive ohmic contact to GaN, both the n-type and p-type metals are annealed. Both annealing processes raise the effective doping leveling which allows for an ohmic contact through tunneling. For the n-type metal of GaN, a multi-metal film stack is utilized with each metal serving an important function. Ti, Al, Ni, Au is the conventional metal stack for the n-type metal. Titanium when annealed forms TiN from the GaN, generating nitrogen vacancies near the surface [25-26]. Nitrogen vacancies in GaN act as donors, which increase the effective doping in the n-type GaN leading to increase tunneling current. Aluminum bonds with titanium to form low resistive phases which lower the resistivity and help prevent against titanium oxidation. Gold form the top level which prevents oxidation of the contact, as gold is inert in air. Nickel is sandwiched between the Al and the Au and acts as a diffusion barrier, as the Au would otherwise

diffuse towards the GaN. The nickel diffusion barrier is necessary as Au form a midcap trap state which would degrade electrical performance. A high temperature of 850ºC for 30 seconds under a nitrogen ambient is conventionally utilized [56]. For the p-type ohmic contact to GaN nickel is utilized with an annealing process to generate nickel oxide. Nickel has a high work function of 5.5 eV, though for p-type GaN a schottky barrier is still present, though with a reduced height compared with other metals. In order to form an ohmic contact to p-type GaN, the Ni is annealed under an O_2 atmosphere. During the anneal the Ni becomes NiO which is a p-type semiconductor. Use of a p-type NiO aligns with p-type GaN in order to provide an ohmic contact.

Annealing processes exist in literature; however, these processes had not been developed in the RIT SMFL. Initial experiments were performed with GaN in order to determine the effects of the anneals. To test the n-type metal unintentionally doped GaN was utilized which has an effective n-type doping of ~5E16 cm^{-3}. Making ohmic contact to a lightly n-type doped semiconductor ensures ideal behavior for increased doping levels. A TLM structure was utilized with the metal layers thermally evaporated. In order to minimize expenses, silver was utilized instead of gold as the corrosion resistant coating. Ti/Al/Ni/Ag were evaporated and lifted-off to form the TLM structure with thickness corresponding to 10/150/30/100nm. The results from the TLM measurements are plotted in Fig. 59. A line is fit to the data for both the annealed and unannealed case with the equations recorded. The unannealed sample exhibited orders of magnitude higher resistance compared to the annealed sample, demonstrating the effects of nitrogen vacancy generation. The contact resistance is half the value of the y-intercept, as there are two contact pads. The unannealed sample showed a contact resistivity of 387 kΩ which would be detrimental to device performance. Annealing the sample reduces the contact resistance by 100x to a value of 3.5 kΩ. The annealed results are in line with the expected ohmic contact to

unintentionally doped GaN. Separately, Ti/Al with thicknesses of 20/10nm were deposited and similarly annealed. The Ti/Al results showed contact resistance values as low as 3.7 kΩ, though without the capping silver layer the results are expected to degrade overtime. Increasing the doping concentration is expected to dramatically lower the contact resistance, where higher n-type doping in common in most devices.

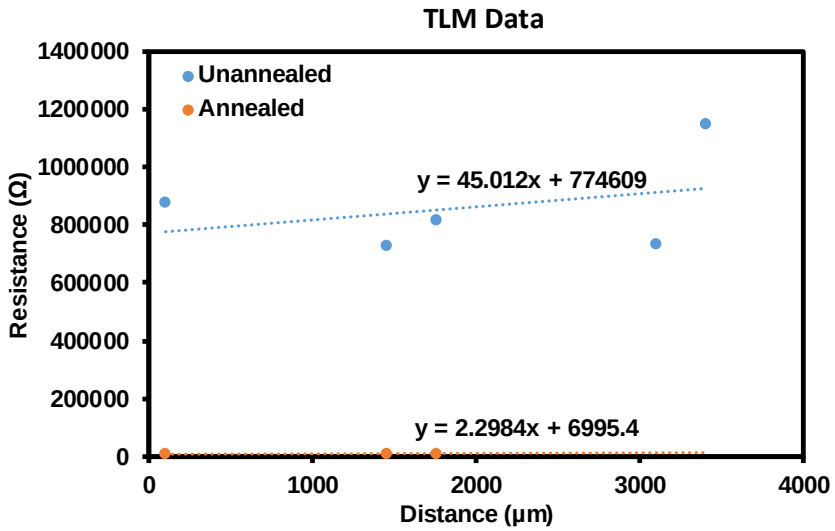

Fig. 59. Ti/Al/Ni/Ag unannealed vs. annealed TLM data.

These annealing results were applied to nanowire devices in order to study any differences during device fabrication. Ni is deposited as the first nanowire hard mask and the n-type metal is deposited both on top of the Ni and at the base of the nanowire. The Ni acts as the diffusion barrier against the metal during the n-type anneal, though film stress between the n-type metal and the nickel was recoded. Results for the as deposited n-type metal on the Ni nanowire tip are shown by Fig. 60(a). Following the anneal the metal on the Ni nanowire tip shows nanowires, compared to the planar metal on n-GaN, Fig. 60(b). For large scale structures such as the alignment marks which have a top layer of Ni, annealing of the n-type metal shows large scale delamination due to the film stress. For the majority of device applications, the effects of the stress are negligible.

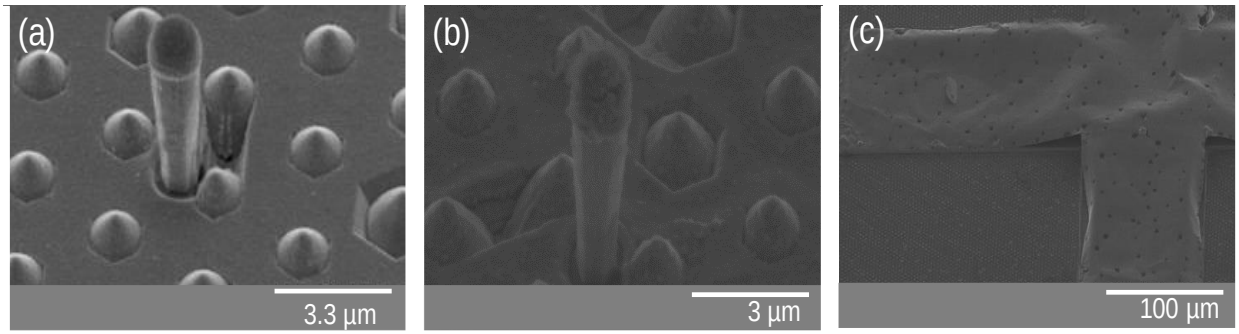

Fig. 60. (a) Deposited n-type metal, (b) annealed n-type metal showing whiskers on Ni, (c) large scale delamination of annealed n-type metal on Ni.

The p-type metal requires an anneal in O_2 in order to convert the surface Ni to NiO. The developed recipe utilizes an anneal at 500ºC for 120 seconds to convert the Ni into NiO. Further elevated temperatures in oxygen would degrade other metal contacts and potentially dope the device as O_2 acts as a donor in GaN. TLM results are planned to be conducted in the future to gauge the performance gains in contact resistivity. Al_2O_3 thin films are widely utilized in GaN devices as a gate dielectric or passivation layer due to the lower interface trap states for the film.

- **Al_2O_3 Optimizations**

Al_2O_3 thin films are widely utilized in GaN devices as a gate dielectric or passivation layer due to the lower interface trap states for the dielectric [61]. To controllably deposit thin films ALD is utilized for the deposition with Trimethylaluminum (TMA) and H_2O as the precursors, where the Al reacts with the O to form Al_2O_3 and the H reacts with the C to form hydrocarbon byproducts. The deposition rate through ALD is controlled at 1 Å/cycle at a temperature of 200°C. To characterize the films, the backside of silicon pieces was utilized, where the gas is depleted before fully reaching the center. A clear color distinction shown in Fig. 61 can be seen, where otherwise

alone this is a subtle change. These samples were combined with film that had the front side fully covered in Al_2O_3 in case of non-uniformity on the backside of the test pieces.

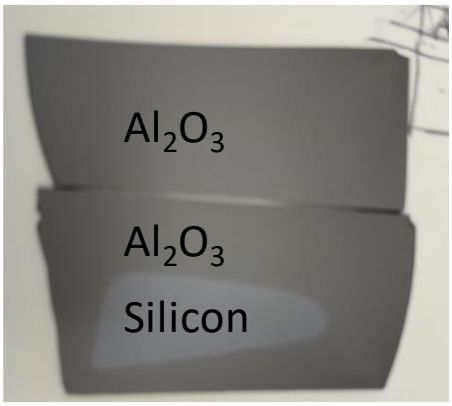

Fig. 61. 30nm Al_2O_3 color difference with silicon.

Wet etch tests were done making use of dilute HF in a 10:1 BOE solution. The etch was found to produce an etch rate of ~100 nm/min. Undercut can be a critical concern when dealing with small dimensions, which BOE is unable to accurately define. Instead characterization through a Cl_2 based ICP etch was performed. An etch of 10 mT, 32 sccm Cl_2, 8 sccm BCl_3, 5 sccm Ar, 75 W bias, 350 W ICP is utilized. The dry etch recipe is also known to etch GaN, while minimizing photoresist erosion. Making use of this recipe, an etch rate of ~125 nm/min is obtained, by observing the color change back to silicon in the viewport of the tool. It was experimentally found that that the etch rate on scaled features is a bit lower, and that if possible it is better to perform an over etch on samples.

- **Capacitor Particle Characterizations**

  Characterizations of particles induced through the course of semiconductor processing in

the RIT Semiconductor & Microsystems Fabrication Laboratory are characterized through a capacitor breakdown analysis technique. Lower than expected breakdown voltages and shorts were found to an unfortunate common place which has a negative impact on yield, particularly when engineering integrated device designs. Small samples also are more subject to environmental factors, as manual device handling and use of carrier wafers can cause an added impact. Humans are also a large cause of particles, where lack of proper attire from staff lead significant particle introduction into the environment. To quantify these issues, capacitors provide a good indicator, where optical particle counters may be unavailable or incompatible. Fabricating arrays of capacitors on die and recording the breakdown voltage tells details about the particles. Fig. 62 show a plot of cumulative percent failure vs. the breakdown voltage for capacitors, where two distinct populations are observed. The intrinsic population signifies normal wear out of the capacitor, related to the intrinsic dielectric properties, where defects do not play a role. The extrinsic population are due to particles which cause a tailed distribution and fail early. Known good processes and wafers should have little to no extrinsic capacitors, as particle counts are minimized.

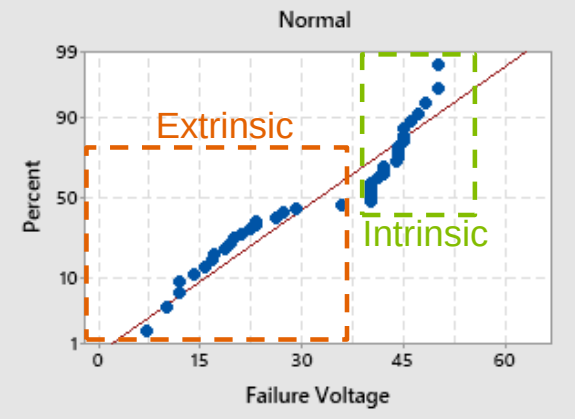

Fig. 62 Cumulative % failure vs. breakdown voltage for capacitors.

In order to get an initial gauge on small particles formed on the surface through device fabrication, LEDs were fabricated, and capacitors were formed on the unutilized n-GaN surface. Following conventional LED fabrication, the sample was cleaned in an O_2 plasma in order to attempt to remove small organics from the surface. 30nm of Al_2O_3 was deposited through ALD, which produces a higher quality dielectric film. Lifted-off Ni was deposited with an e-beam evaporator, minimizing dielectric damage, to a thickness of 30nm. Damage to the dielectric or a poor-quality dielectric would result in a negative shift to the intrinsic population. Following Ni deposition, the dielectric was patterned through with a 10:1 BOE wet etch. Many different capacitor designs were formed, though the smaller 30 µm x 70 µm capacitors were chosen for testing, as shown in Fig. 63. These are relatively small capacitors which have an area of only 2,100 μm^2.

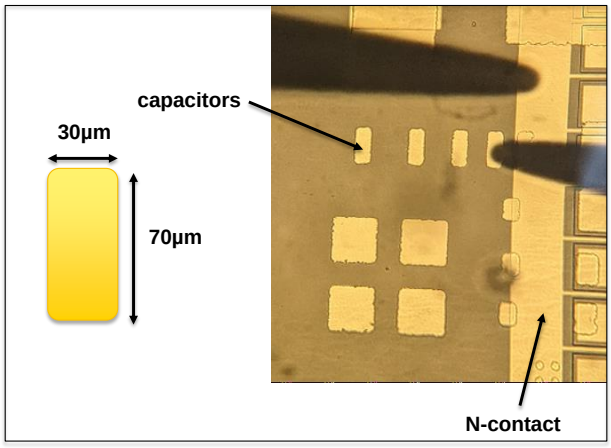

Fig. 63. Capacitors fabricated on LED substrate.

Capacitors fail gradually due to trap induced tunneling, thermionic emission, and/or Fowler-Nordheim tunneling before an eventually shorting of the dielectric. As such the point of breakdown can be a bit arbitrary. Here capacitor failure is determined at a current flow of 10 nA, as shown by the grey line in Fig. 64. Ideally capacitors should show a slow breakdown, sustaining

high voltages before failure. Where a ‘bad’ early failing capacitor is shown in orange in Fig. 64, while a ‘good’ capacitor is shown by blue in Fig. 64.

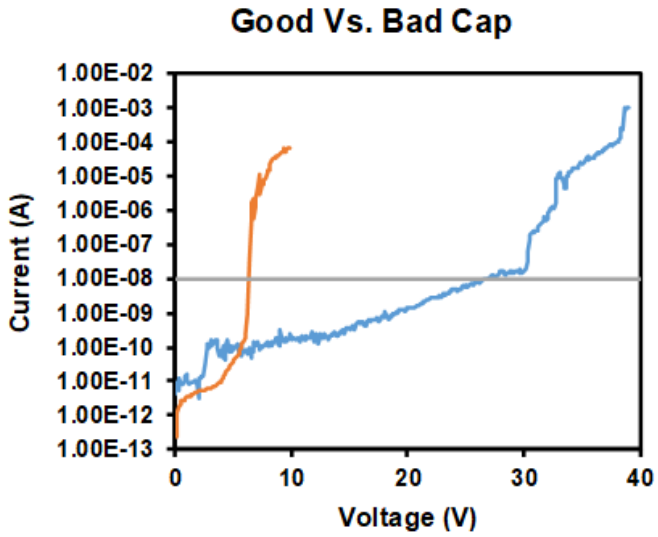

Fig. 64. Capacitor current vs. voltage characteristics with failure current.

Over 80 capacitors where individually tested to breakdown, avoiding areas with obvious external damage. A positive bias was placed on the top capacitor plate, while a negative bias is placed on the cathode which is connected to the n-type GaN layer beneath the dielectric. The cumulative percent failure vs. breakdown voltage are plotted in Fig. 65. It can be seen from these results in Fig. 65 that there is only an extrinsic region. Where the intrinsic region is expected to potentially fall around 45 V. Defects dominate these capacitors, where it seems they are all impacted by particles. Poor capacitor results due to high numbers of particles directly impact device yield results. A clean environment is incredibly important in order to maintain low particle count numbers. Use of cleans represent a temporary fix to much larger more systematic problems that can exist in an unclean facility.

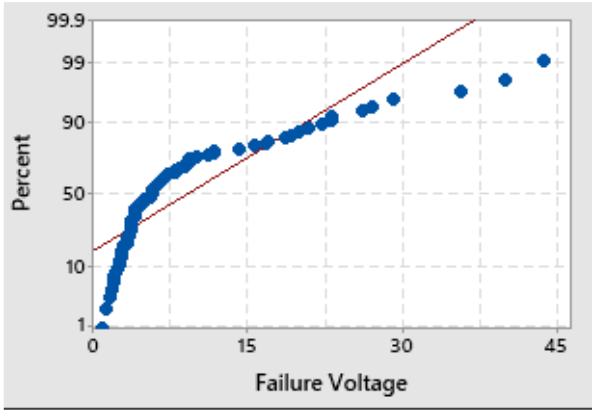

Fig. 65. Measured cumulative percent failure vs. failure voltage for 2,100 μm^2 capacitors.

The measured breakdown results can also be utilized to extract the size of the largest particle which caused the failure. Making use of Eq. 7, with a linear distribution across the electric field the defect size can be calculated [62]. Where V_{br} is the measured breakdown, T_d is the thinned dielectric thickness, V_{bri} is the intrinsic breakdown voltage, and T_i is the intrinsic thickness. Where the particle size is calculated from T_i - T_d.

$$T_d = \frac{V_{br}}{V_{bri}/T_i}$$

Equation 7. Thinned dielectric thickness due to particle [62].

Eq. 7 is applied to all the measured capacitors, creating a histogram of the largest particles causing the failures, as shown in Fig. 66. There are many particles >25 nm which are leading the early or instant failures. Future work should focus on the source of such particles. This technique is recommended to be applied to individual tools and areas of the RIT cleanroom in order to identify and solve problem areas. Existing known particle generators are also recommended to be addressed such as staff and compressed air gun filters.

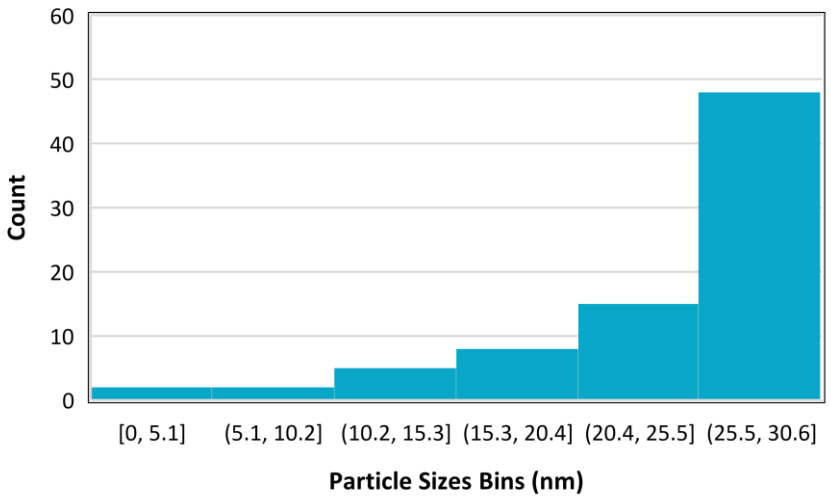

Fig. 66. Histogram of largest particles which cause early capacitor failure.

- **Activation of buried p-GaN**

P-type doping in GaN makes use of Mg acceptors which provide free holes to the material. During growth of p-GaN in an MOCVD, the Mg becomes passivated with hydrogen, due to the byproducts of the precursors, forming Mg-H complexes [63-64]. With the Mg bonded to H, there are no free holes contributed to the material system, rendering the layer to revert to the n-type background doping concentration [63-64]. These complexes can be broken at temperatures above 600ºC, where activation is normally done directly after growth. The position of the p-type GaN is conventionally located at the top, as the last layer, due to differences in growth temperatures with n-GaN. When the p-type layer is instead grown as a lower layer, it is reported that the buried p-GaN is not able to be activated after growth [63]. The hydrogen is found to have difficulty diffusing through the n-GaN due to a lower diffusivity, and that the built-in electric field from an n-type layer (or unintentionally doped n-type layer) grown on p-GaN repels the positively charged hydrogen [63]. Buried p-type GaN layers are of interest for vertically integrated LED-FET and

other MOSFET devices which rely on vertical p-n junctions. Previous reports have investigated the activation step after etching, where hydrogen instead diffuses out the sides of the structure [63-64]. This work is expanded upon in order to optimize the buried p-type activation. On a sapphire substrate a 500 nm GaN buffer layer is grown, followed by 1 µm of n-GaN (10^{18} cm^{-3}), 500 nm of p-GaN (10^{19} cm^{-3}), 200 nm of n-GaN (10^{18} cm^{-3}), InGaN-GaN MQWs, and 200 nm of p-GaN (10^{19} cm^{-3}). The structure is shown in Fig. 67, with the top p-GaN layer activated after growth.

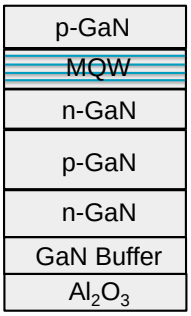

Fig. 67. Growth structure of buried p-GaN layer.

In order to investigate the activation of the buried p-GaN, selective etching is down in order to remove the top p-GaN and MQW region, then selectively define the n-GaN layer. The structure then is utilized in order to fabricate an NMOS transistor, shown in Fig. 68.

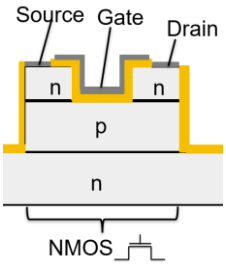

Fig. 68. NMOS transistor fabricated from buried n-GaN and p-GaN layers.

It has been found that without the added activation step, the NMOS devices are unable to turn-off, due to the then continuous n-type layer. Fig. 69(a-b) showcases the case of a planar NMOS device with separate p-type activation. Fig. 69(a) shows the family of curves, where the

gate can modulate the resistance through the gate, either accumulating electrons to form a channel, or repelling them from the surface to increase resistance. Fig. 69(b) further shows this effect, where the gate has very weak to little control, never fully being able to pinch off or further turn-on.

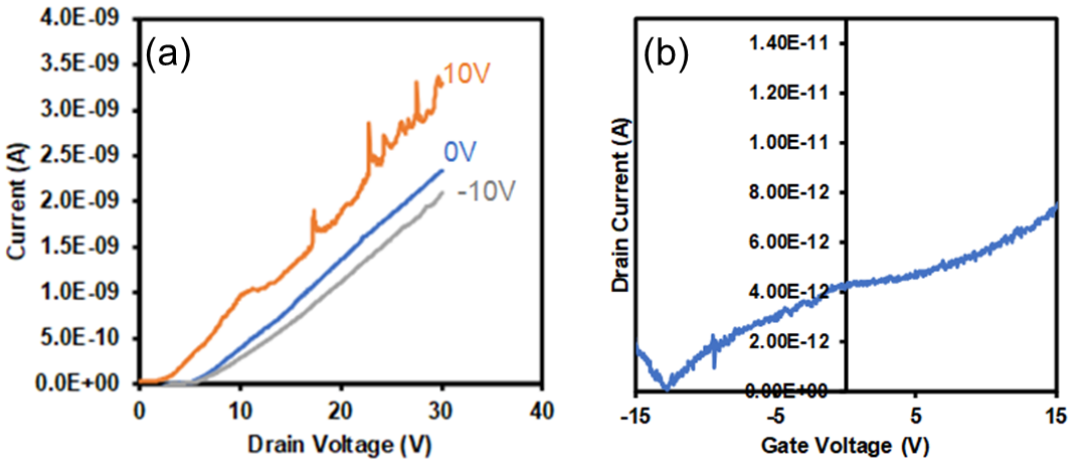

Fig. 69. (a)NMOS family of curves with no middle p-type activation, (b) current on-off characteristics with no middle p-type activation.

To further confirm the expected behavior with regards to activation of the buried p-type region, Silvaco Atlas simulations were performed. The p-type region was replaced with an n-type region of the same thickness, having a doping of 10^{16} cm^{-3}. The doping level is expected to be around this value due to nitrogen vacancies induced during the growth which act as donors. Fig. 70(a) show cases the family of curves going from 0 to 10 V, while Fig. 70(b) shows the current on-off characteristics with the inability to pinch off. These results are in close match to the experimental results obtained in Fig. 70(a-b).

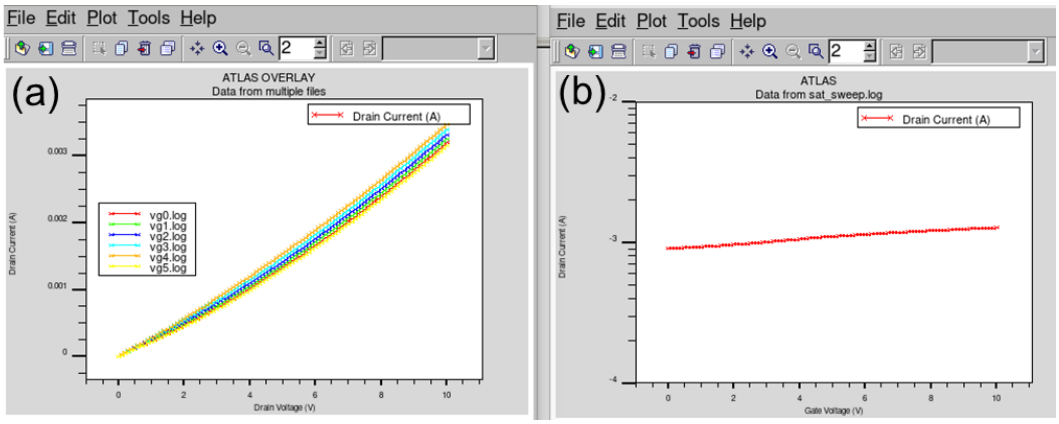

Fig. 70. (a)Simulated family of curves for NMOS device without p-type activation, (b)simulated on-off characteristics for NMOS without p-type activation.

Activation and optimization of the buried p-GaN was then performed on a separately fabricated sample. Repeated etches to the above transistor process were done, creating similar structures. An anneal at 725ºC for 30 minutes in an O_2 atmosphere is performed, where the sample is on a Silicon carrier wafer to act as a hotplate. Making use of an O_2 atmosphere for p-type activation is found to hydrogen extraction, forming H_2O vapor [65]. Diodes were formed to ensure rectification and low leakage currents to check for proper activation. Diode dimensions were 20 x 40 µm with a top metal contact size of 7 µm. Fig. 71(a-b) exhibits the linear and log current-voltage characteristics for the fabricated diodes, respectively. The linear I-V in Fig. 71(a) shows a turn on of ~2.75 V, a bit below the magnitude of the bandgap, which is in-line with what is expected from a GaN diodes [1]. The log I-V in Fig. 71(b) shows a low leakage level under 10^{-10} A at -5 V, indicating most or all of the hydrogen is liberated. These results can be utilized in order to realize vertically integrated transistors through a single growth step, lower costs and increasing yields over implant or regrowth methods.

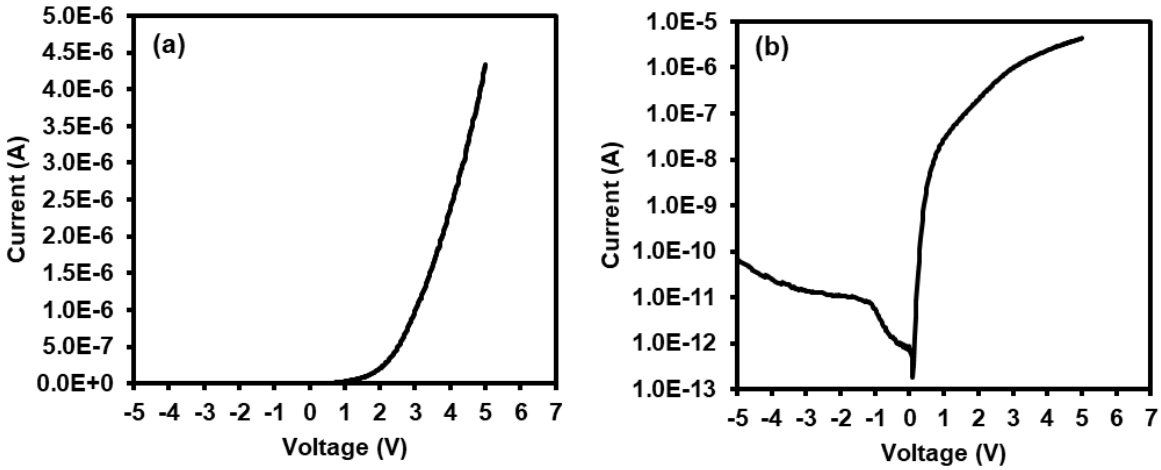

Fig. 71. (a) Linear I-V of diode after buried p-type activation, (b)Log I-V of diode after buried p-type activation.

Chapter 3

MONOLITHIC TRANSISTOR INTEGRATION

3.1 Overview of Monolithic Transistor Integration

This chapter featured a number of novel devices, focusing on integration between GaN LED and transistors in a monolithic format. These devices address the fundamental challenges of GaN LEDs and power devices in novel ways, introducing new concepts and designs. The section here explores in detail each of these breakthrough devices with the dedication of sub-sections. Both theoretical and measured results are presented for these projects and the future directions are discussed.

3.2 GaN Nanowire Static Induction Transistor

Gallium Nitride based semiconductors are emerging materials for power electronics and LEDs. The development of high-efficiency LEDs and micro-LEDs (μLEDs) are opening doors for a number of important applications such as backlight for liquid crystal display [66], visible light communication with light modulation up to several hundred MHz [67-68], as well as display system for Augmented Reality (AR) and Virtual Reality (VR) technologies [69-70]. To enable these novel applications, voltage-controlled μLEDs [18, 71-72] are highly desirable for simplified control loop and flexible driver circuit design compared to Si-CMOS controlled LEDs [73]. Therefore, there is a strong motivation on exploring potential promising electronic candidates based on the same material system that can be integrated with such μLEDs to achieve voltage-controlled component.

To fulfill this goal, AlGaN/GaN High Electron Mobility Transistors (HEMTs) have been investigated to be laterally integrated with InGaN/GaN LEDs due to low on-resistance and faster switching speed [18, 71]. However, there are several key challenges with the HEMT-LED lateral integration: 1) most of the integration schemes require complex growth techniques such as selective epi removal or selective area growth [18, 71] which often leads to leakage through the shared GaN buffer layer; 2) the lateral configuration leads to interconnect parasitics; and 3) scaling and heat dissipation are limited. To solve these issues, GaN-based vertical transistors will be of great interest to investigate.

A transistor which fits into these fabrication requirements is the Static Induction Transistor (SIT). The SIT is a vertical power device which was invented in the 1970s and is conventionally utilized in Si, SiC, and GaAs materials [32-33]. A GaN fin SIT has been realized recently through

a self-aligned process shown by Fig. 72. [34]. Use of a fin design inherently leads to worse electrostatic gate control as compared to a gate-all-around nanowire.

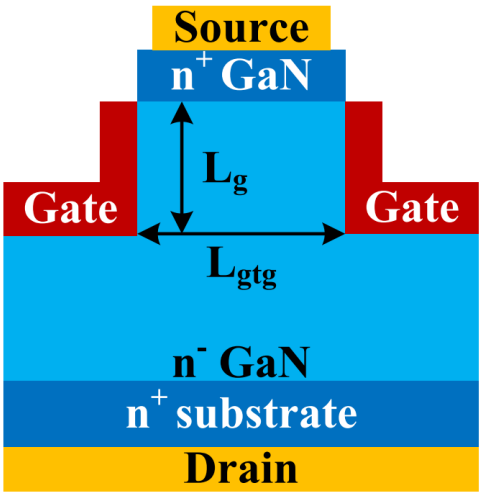

Fig. 72. GaN fin SIT design ©2007 IEEE, Reprinted with permission [34].

The SIT can be compared to a Metal Semiconductor Field Effect Transistor (MESFET), though with important differences. In an SIT the structure of the gate is very small and does not extend close to the source or drain, as is typical in a MESFET. Additionally, current flows vertically in an SIT with no need for a semi-insulting layer commonly used in MESFETs. The sidewalls of the SIT confine the carriers instead of confinement by a semi-insulating layer. Due to the short gate length, punch-through occurs in the device to produce triode-like curves, in contrast to the pentode-like curves of a MESFET. These triode-like curves can be optimal for high current devices such as driving LEDs, as there is no saturation region such as a MESFET or HEMT.

The SIT is a normally ‘on’ device similar to the HEMTs investigated for use with LEDs [18, 71]. In the SIT the gate forms a depletion region, due to the work function of the metal gate forming a schottky contact. The applied gate bias is utilized to modulate the depletion width in the

channel region. Correspondingly, a reverse bias extends the depletion region pinching-off the current flow. Conversely, applying a forward bias to the gate shrinks the depletion region increasing current flow. These concepts are visualized though Fig. 73, which plots the conduction band for a GaN nanowire SIT under 1 V forward bias. Modulation of the electron barrier height control the flow of forward current through the device. Given a fixed forward bias and no gate current, there are upper and lower bounds to the effect of current flow caused by the gate.

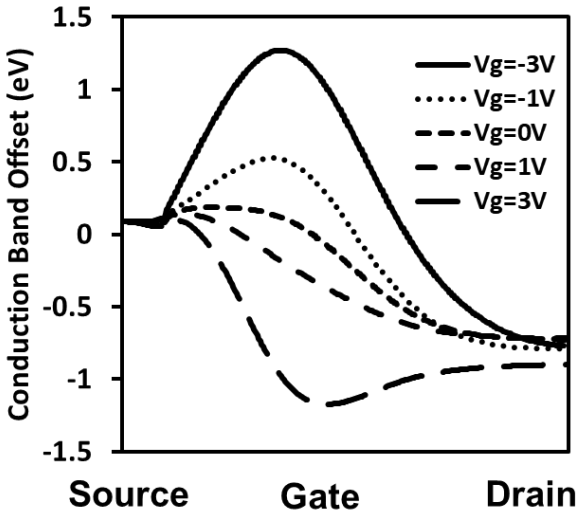

Fig. 73. GaN nanowire SIT conduction band under various gate biases with the drain voltage at 1V.

As the drain to source bias increases, the current can punch-through the pinched-off depletion regions caused by the gate, this allows current to flow again. In order to stem the punch-through current the gate must be further reverse biased [34]. This phenomenon is known as drain induced barrier lowering (DIBL) and is found is scaled transistors. The barrier caused by the gate is lowered because of the drain field penetrating towards the source region. The highly scaled gate length is not enough to block the field from the drain region, causing this effect. The conduction band of a nanowire SIT is plotted in Fig. 74 with a gate bias of -1 V and increasing drain biases.

The barrier height the electrons encounter is reduced through increasing drain biases, where a more negative gate bias is required to form a larger electron barrier to block current flow.

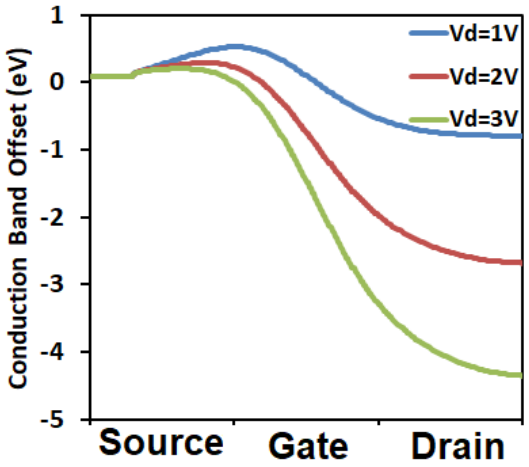

Fig. 74. GaN nanowire SIT conduction band with gate at -1V and increasing drain bias.

The use of a depletion region to control current flow is common in many power electronic applications. The SIT finds commercial use as a high speed switch for power electronics applications. The wide bandgap of GaN present promise to further extent the applications of the SIT to support even higher operating voltages at higher frequencies.

Vertical nanowire structures are chosen to fabricate the SIT due to the gate-all-around benefits for better control, combined with reduced surface area consumption for improved scaling and integration. The nanowire approach additionally allows for diameter scaling to further merge the gate depletion regions for the potential of normally 'off' operation. Unintentionally doped GaN (u-GaN), which is the common template of InGaN LEDs, is utilized to form the vertical wires to enable integration. For the source and drain of the nanowires, Ti is deposited and annealed to increase the doping on the top and bottom of the wires. A TiN layer is formed during the anneal which creates Nitrogen vacancies from the GaN [25-26]. These Nitrogen vacancies act as donors, creating highly n-type regions on the top and bottom of the wires that form an n-i-n structure. The

vertical GaN nanowire SIT will be suitable in enabling voltage-control, fast switching, seamless integration without interconnect parasitics, and better scaling for µLEDs.

Here, GaN nanowire SITs are proposed and fabricated, as illustrated schematically in Fig. 75. Several SITs are in parallel for ease of fabrication. A top down etch to form the nanowires, and a layer by layer fabrication process are utilized to build the complete structure. Layers of metal are put down with layers of dielectric, PDMS, in-between to create the separations. The final device is pictured in Fig. 65 showing the complete architecture with a cutaway view. The gate-all-around design creates a controllable depletion region shown as the solid black lines in cutaway of Fig. 75.

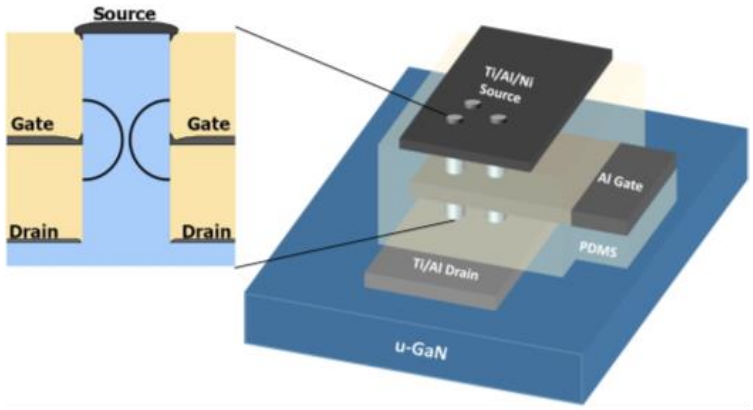

Fig. 75. Schematic of vertical GaN nanowire SIT combined with insert showing the depletion regions formed by the gate metal.

The proposed fabrication flow of the SIT is shown in Fig. 76 with corresponding SEM images. The starting material used for the SIT device was u-GaN grown on a sapphire substrate. The layer of u-GaN was 6.2 µm thick with a background n-type doping of low to mid 10^{16} cm^{-3}. Silica nanospheres with 700 nm in diameter were spin coated to provide the masking pattern for the nanowire etch [74]. These nanospheres form a closed packed hexagonal array which densely coat the surface. Use of nanospheres for the formation of nanowires removes the need and effort of costlier sub-micron photolithography. The coated spheres were then RIE etched with SF_6 and

O_2 in order to radially shrink the sphere diameter from 700 nm to 550 nm, which correspondingly shrinks wire diameter. The spheres provide the hard mask for the chlorine based RIE etch which forms the initial shape of the nanowires. The chlorine RIE etch operates at 150 W with a pressure of 65 mTorr, 30 sccm of Cl_2, 25 sccm BCl_3, 2 sccm $CHCl_3$, and 30 sccm of Ar. After the chlorine RIE etch, the nanowires are treated in KOH in order to both shrink the diameter and remove surface damage from the dry etch [51]. The use of KOH additionally takes the non-uniformities from the dry etch process, to form completely vertical nanowires [51]. Fig. 76(a) shows the results of the GaN nanowires following both the dry etch and wet etch with KOH. The nanowires height and diameter are measured as ~1.5 µm and ~350 nm, respectively. The spacing between the nanowires is ~350 nm. Smaller diameter wires can lead to positive threshold voltages as the depletion regions caused by the gate metal work function can form a complete barrier to prevent current flow.

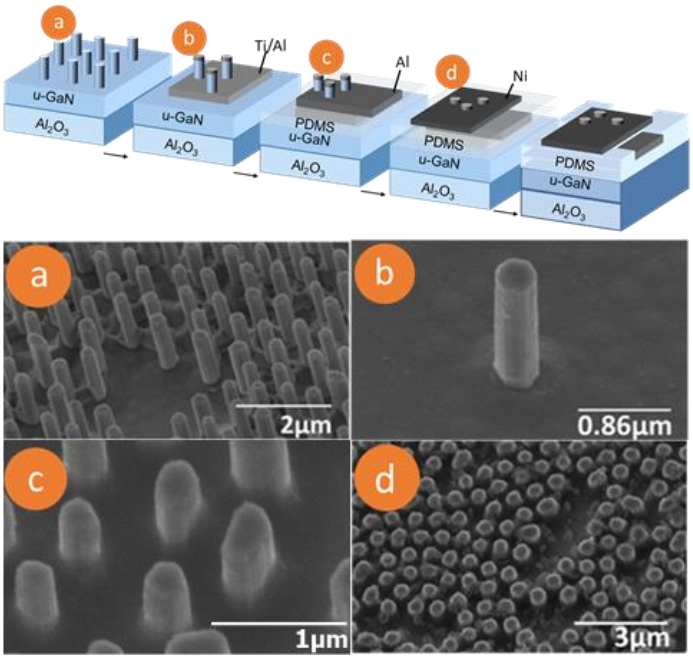

Fig. 76. (a) RIE and KOH Wet etch of nanowires, (b) Ti/Al metal evaporation and anneal, (c) PDMS coat with etch-back and 30nm Ni gate evaporation, (d) PDMS coat with etch-back and Ni top metal.

With the nanowires formed, 20 nm of Ti and 10 nm of Al are deposited through evaporation and lifted-off in order to form the source and drain. Fig. 76(b) shows the Ti/Al coating the top and base of the wire in an uncommonly sparse region. To ensure the top and bottom of the devices are coated with metal but not the sidewalls, the samples are placed flat directly above the source metal with no sample rotation during deposition. Use of the KOH wet etch is also critical to ensure the formation of vertical nanowires. The samples are then annealed in a two-step process, 10 min at 600ºC followed by 20 s at 900ºC in an N_2 atmosphere. The anneal causes nitrogen vacancies as TiN forms which creates an n-i-n structure in the nanowire [25-26].

Following the metal deposition, a layer of PDMS is spin-coated. PDMS is chosen as the inter-metal dielectric due to the property of resistance to chemical removal [75-76]. The PDMS is etched back through an RIE with SF_6 and O_2 to reveal half the wire height. During the PDMS etch back, the top metal is pulled back slightly, removing the slight overhang which could form during evaporation. 30 nm of Al is then evaporated and lifted-off to create the gate of the device, as shown in Fig. 76(c). The SEM image shown in Fig. 76(c) shows the nanowires after gate metal deposition, illustrating how the PDMS supports the metal and how the metal wraps around the wire forming a gate-all-around for better electrostatic control. Here the deposited metal thickness defines the SIT gate length instead of lithography due to the horizontal nature of the evaporation. With the gate metal deposited, another PDMS layer is spin-coated and etched back to expose the top tips of the nanowires. The top metal of 90 nm of Ni is then deposited and lifted-off in order create a contact for probing. A final patterning and PDMS etch step are performed to uncover the buried metal contacts for electrical testing, as shown in Fig. 76(d).

The presented process flow includes less complexities and better integration potential compared with alternative works on vertical GaN nanowire metal oxide semiconductor field effect

transistors (MOSFETs) [54, 77]. These nanowire MOSFETs typically rely on atomic layer deposition (ALD) to form a gate dielectric, combined with an added etch to remove the dielectric from the top and bottom of the nanowires. Sputtering is also used for the gate deposition which provides less control over the gate length [54, 77]. Use of u-GaN as a starting material for an SIT also opens door to many possible integration schemes for micro display.

Device characterizations are performed on the fabricated SITs. Devices of 150 μm^2 are fabricated which are composed of up to 1,600 wires. The electrical results for the family of curves are shown in Fig. 77(a) with the gate voltage varying from 5 V to -5 V. Current flows under no gate bias (V_g = 0 V), and can be pinched-off through a negative gate bias or increased by applying a positive gate bias. Similar trends are found in the 2D Silvaco simulations of a single nanowire SIT in Fig. 77(b). Note that drain current levels are lower from simulation which is due to the use of a single nanowire versus multiple nanowires in parallel from experiments. The non-linear and non-saturating behavior from both simulation and measurements are common to SITs. The effect is caused by punch-through due to the short 30 nm gate length. The SIT exhibits triode-like behavior, in contrast to pentode-like experienced by MESFETs and other devices due to punch-through.

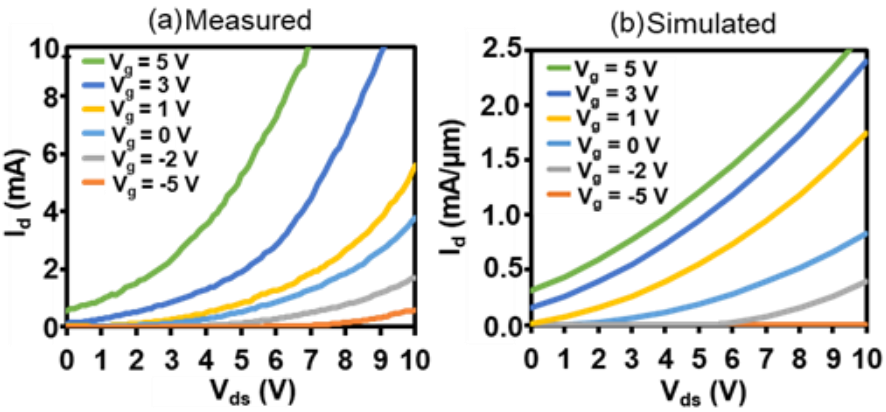

Fig. 77. (a) Measured SIT Family of Curves, (b) Silvaco Simulated single nanowire SIT Family of Curves.

Fig. 78(a) extracts the threshold voltage of 1.3 V at a drain voltage of 1 V from the linear drain current vs. gate voltage. Fig 78(b) shows the log drain current vs. gate voltage (I_d-V_g) behavior of the device. Looking at the on/off characteristics in Fig. 78(a), the device shows the ability to support moderate current with low leakage. The off current is at 5×10^{-11} A while the device on current reaches a level of 1×10^{-4} A showing an I_{on}/I_{off} of 2×10^{6}. The on to off ratio is promising for a preliminary device and the gate-all-around design shows an improvement over the GaN SIT fin designs which have an on/off ratio of 2.2×10^{3} [34]. The vertical current flow is fully pinched off by a reverse gate bias at -1 V, at a drain voltage of 1 V. A substhreshold slope (SS) of 126 mV/dec is extracted from the curve. This value is slightly higher than the ideal of 60 mV/dec due to slight variations in the nanowire diameters, where larger diameter nanowires in parallel require more negative voltage to fully pinch off. Measurements of the gate leakage are also recorded and shown in Fig. 78(c). The SIT device conventionally operates at low reverse biases on the gate to pinch off the channel. Schottky gates inherently suffer additional leakage compared with capacitive gates, as the further reverse bias allows electron tunneling from the metal. The SIT shows leakage current as low as 10^{-11} A at low negative voltages.

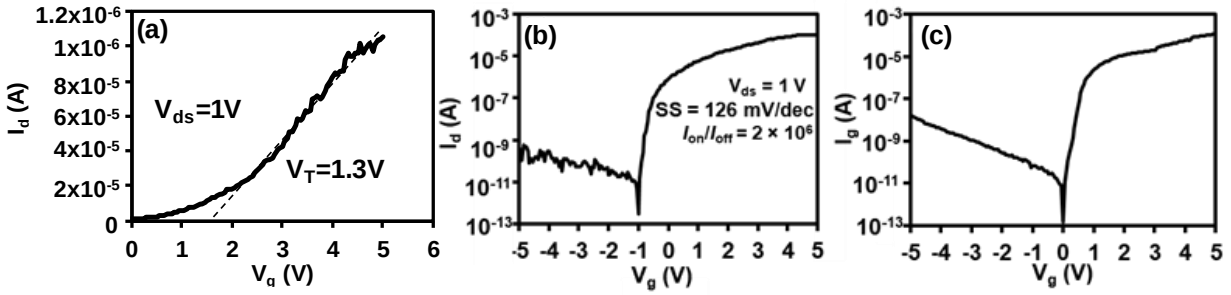

Fig. 78. (a) Threshold voltage extracted, (b) V_g vs. I_d curve showing the on and off current at V_{ds} = 1 V, and subthreshold slope (SS), (c) SIT schottky gate leakage.

In summary, GaN nanowire SITs were purposed and fabricated for the first time. These devices employ a top down nanowire formation combined with a layer-by-layer fabrication approach to form vertical structures. Use of u-GaN followed by annealing allows for the fabrication of an n-i-n structure, which has been demonstrated in device results for the first time. An Ion/Ioff ratio of 2 × 10^6 is obtained from these initial devices which is due to the gate-all-around design. These initial results demonstrated that vertical nanowire SITs by the use of u-GaN which is typically the template layer for LEDs will enable voltage-controlled components for new integration schemes and opportunities in micro display technology.

- **Future Device Directions**

The initial GaN nanowire SIT performs well compared to the GaN fin version of the SIT, due to the increase in gate control. There are however, further device improvements that can be made, along with future device applications. The device results demonstrated a high on-off ratio, however the device drive current can be further boosted while maintaining low off current. Implementing a grown n-type region on the nanowire base and nanowire tip would allow for

increased electron injection to support higher levels of current. Use of a grown n-type layer would also further reduce the contact resistance of the device, which would improve performance. In such a design the u-GaN nanowire would remain as the channel region in order to allow for current pinch-off at relatively low reverse biases. Shrinking the nanowire diameter to sub 200 nm would allow the device to operate in enhancement mode with a positive threshold voltage. As the diameter of the nanowire is scaled down, the depletion regions from the metal gate further merge and create a larger barrier to electron flow. The larger depletion barrier would additionally allow the devices to block high voltage levels before subsequent current punch-through. Similarly, increase the thickness of the gate region beyond 30 nm creates a large depletion barrier to support higher levels of voltage, though at the cost of switching speed delays. Future device designs would also greatly benefit from the fabrication of an ordered array of nanowires, instead of the random pattern through nanospheres lithography.

To judge the future performance of nanowire diameter reduction on threshold voltage, additional Silvaco Atlas simulations were performed. Wires of the same 1.5 μm height were simulated with a gate length of 50 nm. The device diameter was varied from 300 nm to 100 nm, keeping the other device parameters contestant. The device simulation was modeled after the process flow, replicating the metal depositions as demonstrated in Fig. 79.

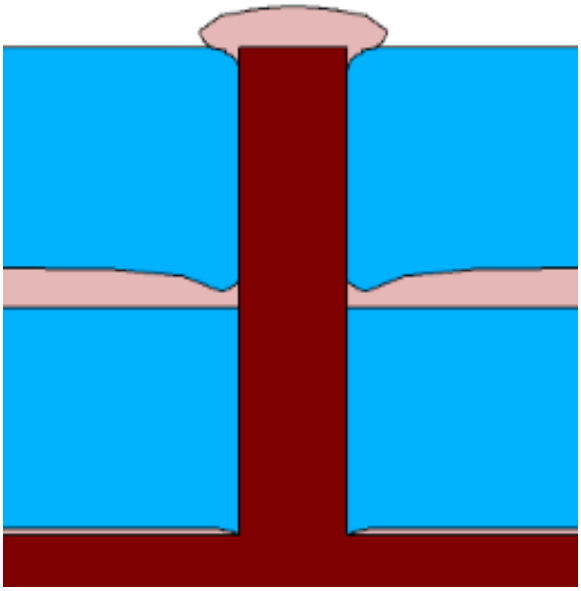

Fig. 79. Structure of simulated GaN nanowire with modeled thermal evaporation.

Results from the varied diameter simulation on the threshold voltage are shown in Fig. 80. The gate bias is varied from -4 V to +5 V with the drain held at 1 V and corresponding current recorded. The on current for each nanowire diameter is seen to saturate at ~3 V, as the on current for the device is determined by the source and drain doping. Similar current values result in the off state for the tested diameters, with a slight increase in current for larger diameters due to a lower electron barrier height for larger diameters. The threshold voltage is seen to move from the ~ -1 V value at 300 nm to ~ 0 V at 200 nm. Further reductions in diameter push the threshold voltage to a higher positive value. As the depletion regions formed by the metal provide a larger barrier to current flow, enhancement mode devices can be achieved.

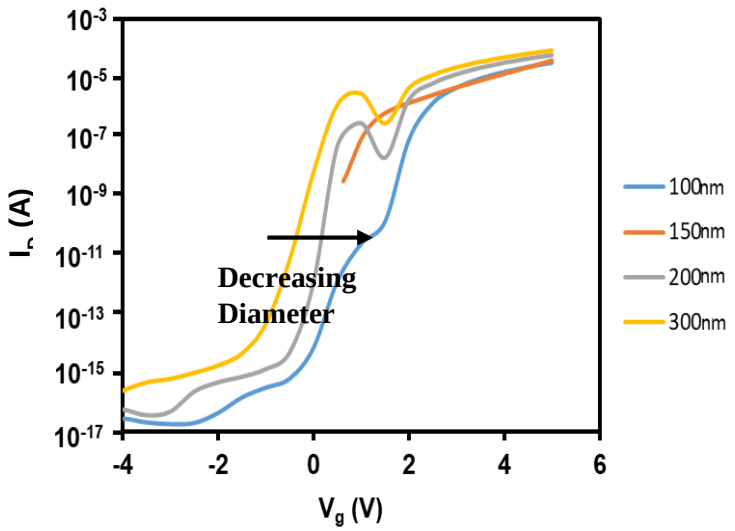

Fig. 80. I_d vs. V_g for various nanowire SIT diameters.

The use of the nanowire SIT can be applied in the power devices space to offer high blocking voltages with higher switching speeds compared to fin or planar designs due to the advantages in electrostatic control. Many conventional high voltage devices rely on a vertical structure with optimization of grown regions in order to achieve high device breakdowns. One example of this is from Y. Zhang et. al, who makes use of a fin structure on a grown GaN substrate [78]. The use of the backside drain contact allows for layer growth to determine the device breakdown voltage. A layer of lightly n-type doped GaN is grown ~8.5 µm in the example by Y. Zhang et. al, Fig. 81. In this example and in conventional power electronics, the lightly doped layer acts as a large resistor which can sustain the voltage drop. As the lightly doped layer is grown thicker, additional increases in breakdown voltage result though with the trade-off of increased on-resistance [79]. The fins at the top of the structure provide the gated control, as the current flows through the fins before reaching the bulk GaN regions. The fin power device with thick lightly n-type doping was able to support device breakdown levels of 1200 V. Use of just the fin for the device would only support breakdown levels of tens of volts, as resistance of the lightly doped GaN is critical. Swapping the fins design with nanowire SITs would allow both higher blocking

voltages and higher switching speeds due to the increased electrostatic control. A similar sub-200 nm nanowire diameter would be utilized to achieve enhancement mode operation. The planar design offer by the GaN SIT is also expected to reduce capacitance between the gate the source region, while offering additional integration schemes though the planar topology.

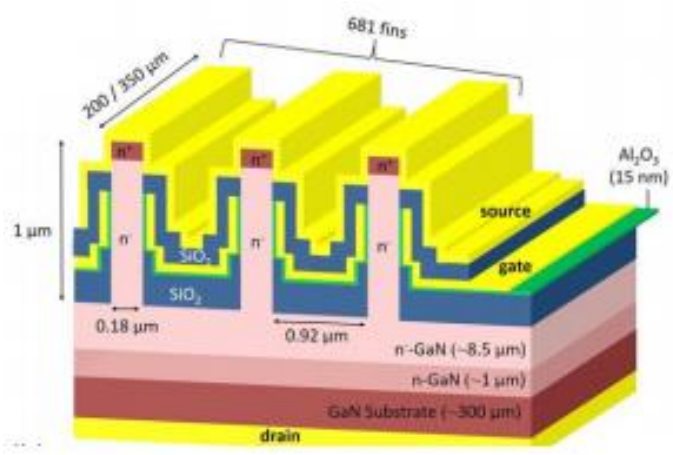

Fig. 81. GaN fin power device ©2018 IEEE, Reprinted with permission [78].

3.3 GaN Nanowire LED-FET Integration

Building upon the work to develop the GaN nanowire SIT, a novel SIT-LED integration scheme is investigated for display applications. The FET-LED work is necessary as current display technology is reaching limitations as the TFTs used for liquid crystal displays or solid state LEDs are struggling to be reduced in size [80-83]. The current TFT technology is limited by poor material properties, with an inability to achieve further increases in efficiencies [80-83]. To solve these issues and introduce the next generation of display technology, power electronics combined with LEDs based on GaN are being pursued [1, 84-85]. GaN based LEDs offer higher efficiencies of up to 80%, improved long-term reliability, and the ability to be manufactured at the nanoscale [86-88]. The emergence of micro-LEDs (µLEDs) and nanowire LEDs are opening doors to have LEDs

directly compose individual pixels, removing conversion losses [89-91]. A number of important display applications will be significantly improved such as virtual reality (VR) and augmented reality (AR), due to the efficiency, nanoscale pixels, and transparent nature of GaN LEDs. Both μLEDs and nanowire LEDs provide these solutions, though the persistent problem is the lack of integratable FETs in order to control these LEDs. To address the lack of integration there is potentially promising electronic candidates based on the same material system that can be integrated with such μLEDs to achieve the voltage-controlled component.

To provide the voltage control, AlGaN/GaN HMETs have been initially investigated to be laterally integrated with InGaN/GaN LEDs [71, 91]. The integration with the HEMT-LED presents a number of issues: 1) the presented integration makes use of etch back and high temperature regrowth [71, 91] which often leads to defect incorporation and added cost; 2) interconnects are required which introduce added resistance; and 3) LED display area is lost to the HEMTs. Alternative approaches include integration of TFTs with LEDs, though these displays are limited in both performance and scaling [92]. To address these issues, vertical GaN FETs are presented, removing the reliance on regrowth, eliminating interconnects, and erasing LED area consumption.

Novel to this work, a nanowire GaN gate-all-around (GAA) FET is monolithically integrated at the base of a nanowire InGaN/GaN LED for the first time. The nanowire FET makes use of the u-GaN layer common to InGaN/GaN LED growth. The vertical integration allows individual nanowire LEDs to be addressed with none of the issues experienced by previous approaches. Ti is deposited at the base of the wire and annealed to induce nitrogen vacancies which act as donors [25-26]. The Ti annealing combined with the higher conductivity of the initial buffer layer [93-95] creates a bottom n-type region. The generated bottom n-type region at the base of

the wire, combined with the u-GaN layer and the n-type GaN from LED, make an n-i-n structure for a FET.

The initial nanowire FET chosen to be integrated with the nanowire LED is the SIT. The pairing of the nanowire SIT and nanowire LED builds upon the developed work. Multiple types of FETs such as the conventional MOSFET can alternatively be integrated. The SIT though is a straightforward vertical power device that offers easier manufacturing without need for ALD [31-34]. A schottky gate is used to modulate the depletion region in the nanowire in order to pinch off current. Triode-like curves are produced in the SIT device due the short gate length [31-34]. This preliminary work offers an advantageous alternative approach to integrate nanowire LEDs with nanowire FETs for displays without sacrificing display area or performance.

For the first time GaN nanowire FETs have been vertically integrated with nanowire LEDs. The integration scheme has been both proposed and fabricated, shown by Fig. 82. Avoiding the need for advanced lithography, an average of 45 wires are fabricated in parallel for each device. A multilayer fabrication approach was utilized, forming the wires through a top-down dry etch, while the contacts are build up through dielectric and metal layers. Metal is evaporated to avoid sidewall coatings, with PDMS spin coated and etched back to provide the transparent spacers. Fig. 82 illustrates the nanowire FET and nanowire LED integration, with a single wire showing the series connection.

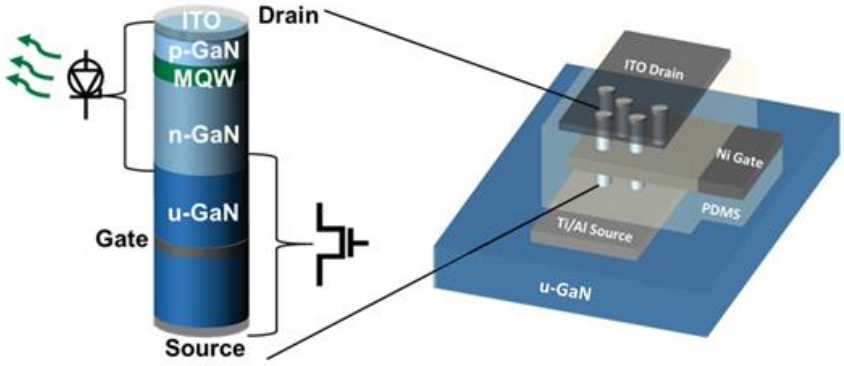

Fig. 82. Schematic of the vertical GaN nanowire LEDs with the nanowire FETs, insert showing a single wire. [30]

A conventional InGaN/GaN green LED on sapphire is used here which composes a 20 nm GaN buffer, ~3 µm of u-GaN (10^{16} cm^{-3} background doping), 3 µm of n-GaN, InGaN/GaN MQW 150 nm of p-GaN, and 1 nm of p-InGaN. Silica nanospheres with 3 µm diameter diluted in DI water are spin coated to provide a sparse coating to mask the nanowire etch [74]. Nanosphere lithography used in this initial work provided a cost-effectively alternative over conventional photolithography for patterning. The coated spheres are radially shrunk in 10:1 BOE from 3 µm to 1.6 µm, which correspondingly shrank the final nanowire diameter. SiO_2 spheres provide high selectivity over the chlorine RIE and set the wire diameter. The RIE etch recipe developed uses 225 W of power at a pressure of 65 mTorr, flowing 30 sccm of Cl_2 and 20 sccm of Ar. To remove etch damage from the RIE and further reduce the wire diameter, a KOH wet etch is performed [48, 58]. The KOH wet etching removes surface states which lead to non-radiative recombination, while also etching the wire to be perfectly vertical. Fig. 83(a) shows the results of the post KOH wet etched nanowire in the SEM. The dry etching created nanowire heights of 5.5 µm, with the KOH shrinking the diameters down to ~1 µm. The depletion regions formed by the schottky gate at this diameter are not enough to pinch-off the device under no gate bias. Similar results are found for the nanowire SIT at 350 nm diameters. Decreasing the nanowire diameter further can merge

these depletion regions providing normally off behavior, as demonstrated in Fig. 70 through the simulations of GaN nanowire SITs.

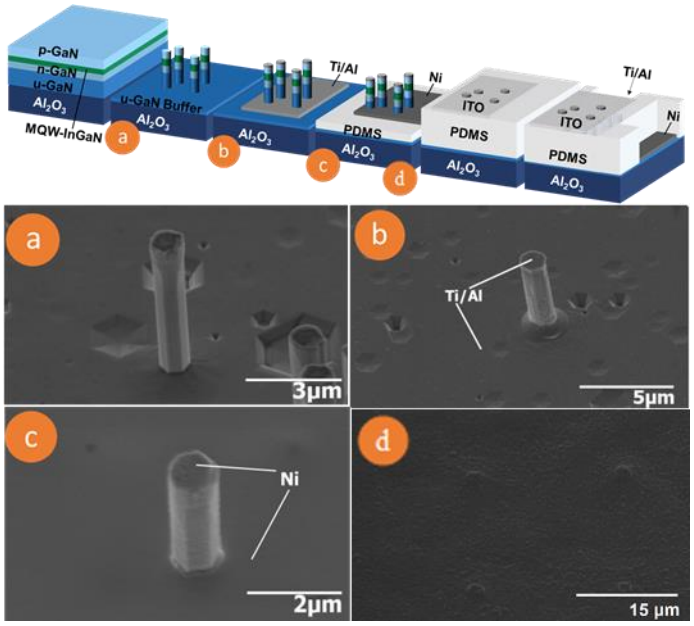

Fig. 83. (a) RIE and KOH etching of InGaN/GaN nanowires, (b) Evaporation and anneal of source and drain, (c) 40 nm Ni GAA on PDMS, (d) ITO deposited on nanowire tips [30].

Following the dry etch and KOH wet etch, 20 nm of Ti and 10 nm of capping Al are evaporated. Lift-off is performed in order to remove the metal, leaving Ti/Al on the tops and base of the wires which act as the source and drain, Fig. 83(b). An anneal is next done to cause the formation of nitrogen vacancies as TiN is formed [25-26]. The anneal is done at 600ºC for 10 min then 900ºC for 20 s. The anneal forms an n-type layer at the base of the nanowire, while the u-GaN buffer is the intrinsic region, and the n-type layer of the LED functions as the second n-type layer for the n-i-n structure. The n-type region of the LED functions as the drain of the transistor and supplies the LED with electrons for recombination.

PDMS is then spin coated which provides the spacer between the metal layers, and planarizes the surface. PDMS is optically transparent and will not be removed in common

chemistries such as developers [75, 96]. After spin coating, the PDMS is RIE etched with CF_4 and O_2 to reveal about half of the u-GaN region. For the gate metal, 40 nm of Ni is evaporated followed by lift-off, Fig. 83(c). Nickel is chosen due to the high metal work function, which provides an increased depletion region for the gate control. The gate metal forms a schottky GAA contact with wire, which can be seen in Fig. 83(c). Making use of a vertical FET with the presented process flow allows the gate length to be set by the metal thickness instead of conventionally lithography, where the fabrication of small gate length devices can be achieved.

Following the gate evaporation more PDMS is spin coated and etched to reveal the tops of the wires. To allow for light emission, ITO is utilized due to the high transparency. 80 nm of ITO is sputtered, followed by lift-off, Fig 83(d). Patterning and PDMS etching is done as a final step to uncover the gate and source contacts which have been buried.

Making use of a layered approach with evaporation allows for device planarization which is not present in previous works on vertical GaN MOSFETs [54, 77]. Previous works on vertical GaN nanowire devices also utilized ALD for the gate dielectric, with subsequent etches, which is not needed for a schottky gate [54, 77]. A sputtered gate has conventional been used, though evaporation here is found to provide the ability to fabricate small gate lengths [54, 77]. Use of thermal evaporation of the gate additionally prevents plasma damage which can occur due to sputtered gate metals [97].

Electrical measurements have been performed on the fabricated nanowire LEDs with integrated FETs. For ease of fabrication an average of 45 wires are in parallel to compose each device. First the I_D-V_D results are recorded with the gate bias set from 5 V to -10 V in 5 V steps, Fig. 84(a). For use of the SIT in this preliminary device, the 1 µm diameter for the wires is not small enough to pinch off current at (V_G = 0 V). Smaller wire diameters of sub 200 nm or use of a

p-type channel can be utilized in order to achieve enhancement mode operation. The SIT is conventionally a depletion mode device with negative gate biases used to pinch off current, or alternatively, positive gate biases to increase current. The triode-like results are the expected behavior for an SIT device [32-34, 74]. The I_{on}/I_{off} performance showing the drain current vs. gate voltage (I_D-V_G) is shown in Fig. 84(b) with a forward bias of 5 V. Due to the SIT, the device is in depletion mode, where the LEDs are "on" until switched off at a gate voltage of -2.2 V. The lower threshold voltage value is consistent with the larger diameter than the 350 nm SIT which showed a threshold voltage of -1 V. The device shows an I_{on}/I_{off} ratio of 2.9×10^4 at V_D of 5 V which is a 2.4x improvement over the HEMT-LED integration [71]. The gate leakage levels are recorded, shown by the inset of Fig. 84(b). Gate leakage as low as 10^{-12} A is seen for the device.

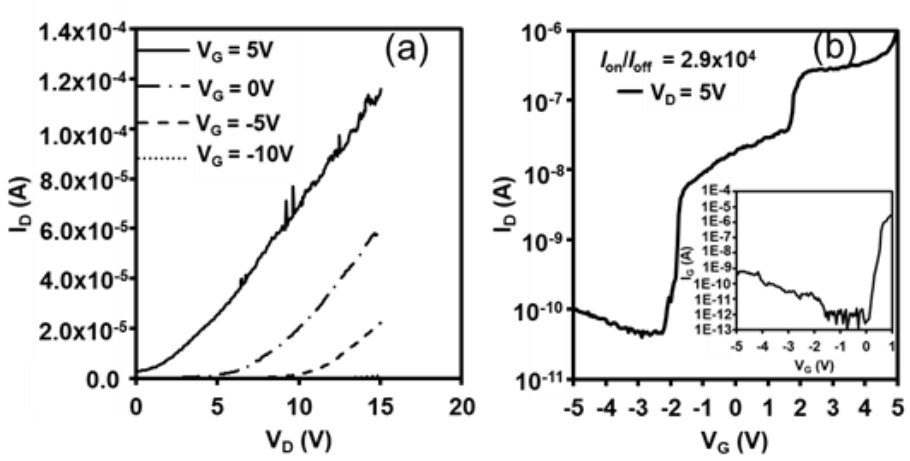

Fig. 84. (a) I_D vs. V_D with gate biases, (b) I_D vs. V_G at V_D =5V, inset: gate leakage V_G vs. I_G [30].

The step behavior observed in the I_D-V_G curve was though to initially indicates the presence of trap states [98], though additional analysis through Silvaco Atlas was performed. The device structure was replicated in Silvaco Athena to include the same parameters as the fabricated devices. When simulating the I_D vs. V_G behavior the same 'step' pattern was recorded and shown in Fig.

85(b) next to the measured curve of Fig 85(a). The curve is in contrast to the behaviors recorded and simulated for the nanowire SIT.

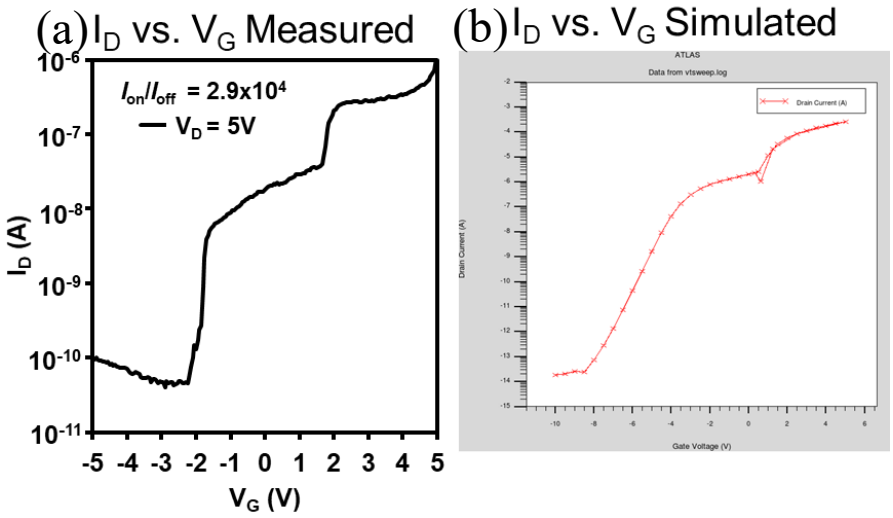

Fig. 85 (a) I_D vs. V_G measured at 5 V bias, (b) I_D vs. V_G at simulated at 5 V bias.

Two distinct curves appear to be overlaid on top of each other in order to provide the cumulative effect. These two distinct regions are identified in Fig. 86. Approximating the second curve in Fig. 86 down to the x-axis points to a value close to 0 V. Schottky diodes are known to have very small threshold voltages in the forward bias, where the nanowire LED-FET has a schottky gate. With positive threshold voltages the gate of the device is seen to turn on, providing increased drain current. The current from the gate is undesired and can be considered as leakage current in the device. The schottky gate should therefore not be driven in an excessive forward bias. The 'step' behavior has not been seen with the previous tests with the nanowire SIT which had a diameter of 350 nm.

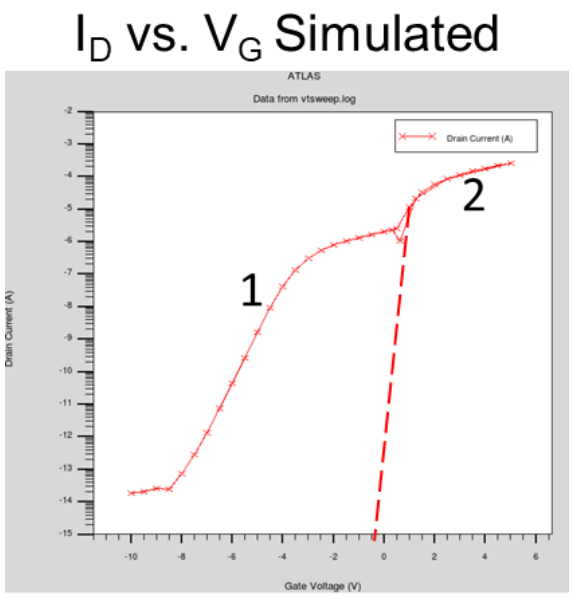

Fig. 86. I_D vs. V_G simulated nanowire LED-FET showing the two overlaid curves.

In order to investigate the gate turn-on with the nanowire SIT-LED vs. the nanowire SIT the conduction bands across the nanowire diameters were simulated through Silvaco Atlas. The simulation applied a 1 V forward bias, with a gate voltage of 3 V for both the SIT-LED and the SIT. The forward gate bias of 3 V is located in the second region of the curve in Fig 86, where the gate current is flowing in the nanowire SIT-LED. A horizontal cutline is taken from the gates, across the diameter of the nanowire for both devices. The conduction band for both devices is plotted showing the SIT-LED in Fig. 87(a), and the SIT in Fig. 87(b). For the larger nanowire diameter SIT-LED, the gate is seen to be 'on' with electron flow possible between the gate and the wire. Gate current flow is possible as there is no longer a schottky barrier present, Fig. 87(a). In contrast, the smaller diameter of the SIT is more depleted by the gate, due to increased merging of the depletion layers from the metal gate. The conduction bands from the 300 nm diameter SIT show a schottky barrier is still maintained at 3 V, which explains why the jump in current is not recorded. The depletion from the gate metal drops off to equilibrium in a conventional

semiconductor. In the case of both the 700 nm diameters and the 300 nm case, the center of the wire is not at equilibrium under no applied biases. As the depletion regions merge, the height of the energy bands rise in the center of the nanowire, with a larger increase for smaller diameters. This effect is how the smaller nanowire diameters are able to better stem gate turn-on.

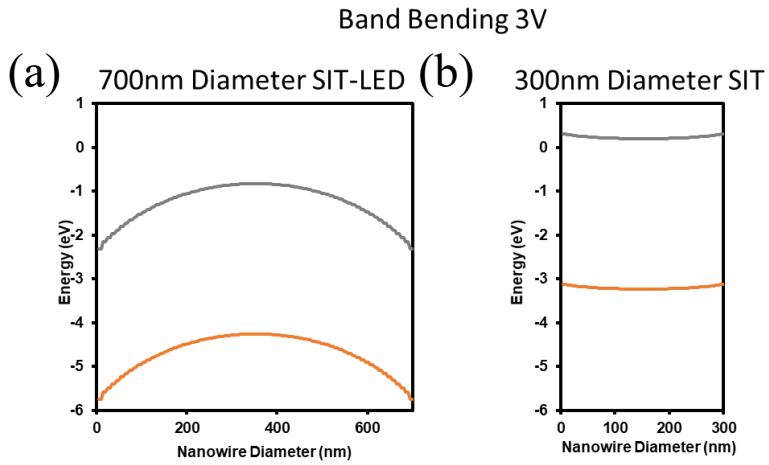

Fig. 87. (a) Energy bands across the gate region of a 700 nm diameter wire, (b) Energy bands across the gate region of a 300 nm diameter wire.

Fig. 88(a) shows the ~45 individual nanowires lighting up at 10 V. Due to the intentional sparse and random spin coated distribution, individual nanowires in close proximity show up brighter. Spin coating a close packed array or use of photolithography would allow high densities of wires. Electroluminescence (EL) measurements were performed to view the spectra under various gate biases for modulation, as shown in Fig. 88(b). A bias of 24 V was applied in order to drive the 45 nanowire LEDs to produce excess light for the detection setup. Under zero gate bias current flows in the SIT to turn "on" the LEDs. Increasing the gate bias creates additional current flow for the LED that correspondingly increases the brightness. Conversely, applying a negative gate bias extends the gate depletion regions to pinch off current flow. The LED brightness

decreases and turns “off” with negative gate biases. The LED is observed to fully turn off at a -10 V gate bias. These results match up with the recorded family of curves in Fig. 84(a).

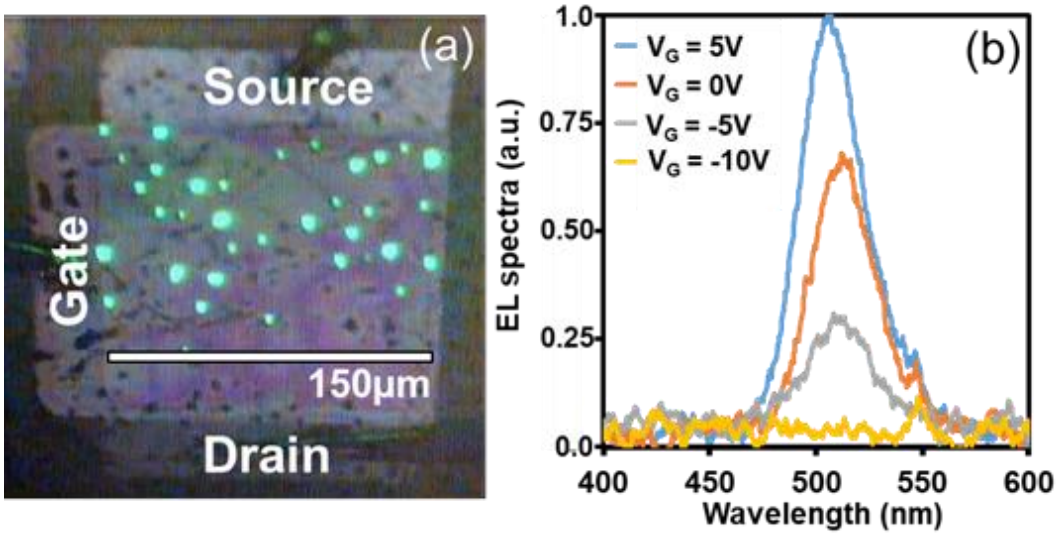

Fig. 88. (a) Nanowire LEDs with FETs lighting up (b) EL spectra with gate modulation [30].

Brighter spots appear in Fig. 88(a) showing the nanowires lighting up. These bright spots are due to the sparse and random nanowire coating. The largest spots are three individual wires in close proximity, while the smallest spots are isolated wires. The grouping of the nanowires can be seen in Fig. 89. During the sphere deposition process, the spheres often group close together due to the water evaporating during the spin-coating process. The spheres are shrunk through BOE and the wire diameters are reduced through the use of KOH. The wet etching processes provide adequate nanowire spacing even for the clusters of nanowires. A gate-all-around is still able to wrap around each nanowire to provide individual control.

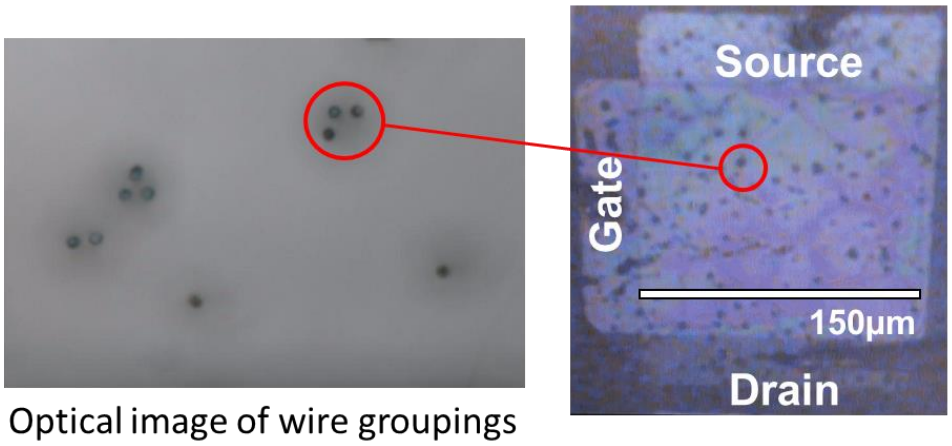

Fig. 89. Optical image of wire groupings with corresponding scaled out image of the device.

In summary, GaN-based nanowire FETs and nanowire LEDs were vertically integrated together for the first time. This novel integration makes use of the previously unused u-GaN layer to fabricate a GAA FET. Vertical integration allows for individually addressable nanowires for displays, removes the issue of lateral area consumption, and eliminates parasitic interconnects. As a preliminary demonstration, nanowire SITs are chosen to be integrated with the InGaN/GaN nanowire LEDs due to ease of fabrication. A planarized approach to fabrication is utilized making use of metal layers and transparent PDMS. Control over the nanowire LEDs is exhibited with classical SIT performance recorded. The nanowire LEDs can be modulated, turning off at -10 V. This work can open the door to next generation of GaN-based LED displays for electronics, VR, AR, and more.

3.4 GaN Monolithic Displays

µ-LED display technology represents a significant advancement in the display space [99-100]. µ-LED displays offer higher efficiency, longer lifetimes, and promises of higher resolution over existing technologies such as LCDs and OLED displays [100-103]. While LEDs for lighting

represent widespread commercial infrastructure which can be leveraged, there remains the issue of integration between these LEDs and the control circuitry [103]. Where conventionally LEDs are distinct from the common Si material system for integration with CMOS circuits or even with TFTs [99, 104]. TFTs which have had wide-scale adoption of LCD and OLED displays do not offer the level of performance necessary for μ-LED displays due to low motilities, threshold voltage variation, and added manufacturing costs [100-103]. Instead, many seek to directly bond individual μ-LEDs to a Si CMOS wafer to provide for both the peripheral control circuitry and transistors for active-matrix operation [100, 103]. While Si represents a mature, high performance material system, transfer techniques are not and continue to be plagued by yield, cost, and resolution issues. Instead, a novel fully monolithic approach is presented in which the GaN material system is utilized to both form the active-matrix elements and control circuitry. GaN itself offers high mobility, a key factor in transistors for displays, and already offers commercial high-power and high frequency devices [99, 104]. The GaN device and LED communities are largely separate with initial integration attempts adding cost and negatively impacting LED performance through high temperature processing [105]. Presented by Hartensveld and Zhang in 2019, was a novel integration mechanism in which field effect transistors (FETs) could readily be integrated with LEDs in a vertical format, without added growth steps [30]. The initial work is expanded upon here to offer additional device freedom, demonstrate active-matrix circuits, and integrate GaN based CMOS for peripheral control circuitry. An n-p-n structure is grown and incorporated beneath the LED, as shown in Fig 90.

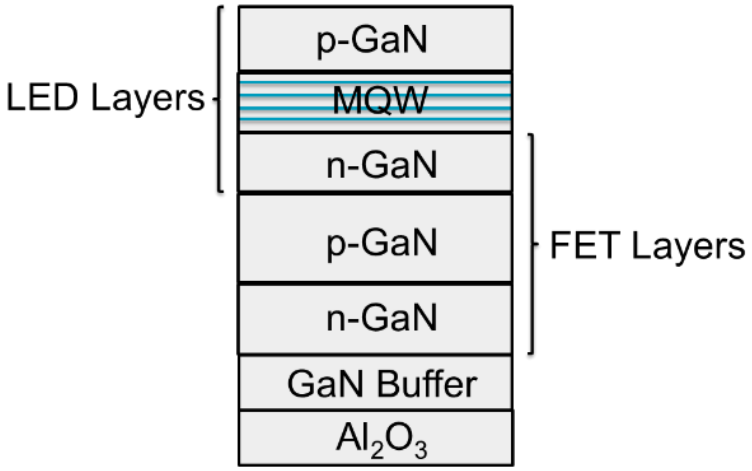

Fig. 90. Schematic of growth structure where the underlayers of the LED are modified to include an added p-type and n-type region.

The top p-type layer, MQW region, and top n-type layer make up the LED active layers. The top n-type layer, bottom middle p-type layer, and bottom n-type layer makes up FET layers for device fabrication. The top p-type layer to the bottom n-type layer represent a vertically integrated µLED-FET as shown in Fig. 91. The top n-type layer and middle p-type layer can be revealed through an etch, creating an NMOS FET, Fig. 91-92.

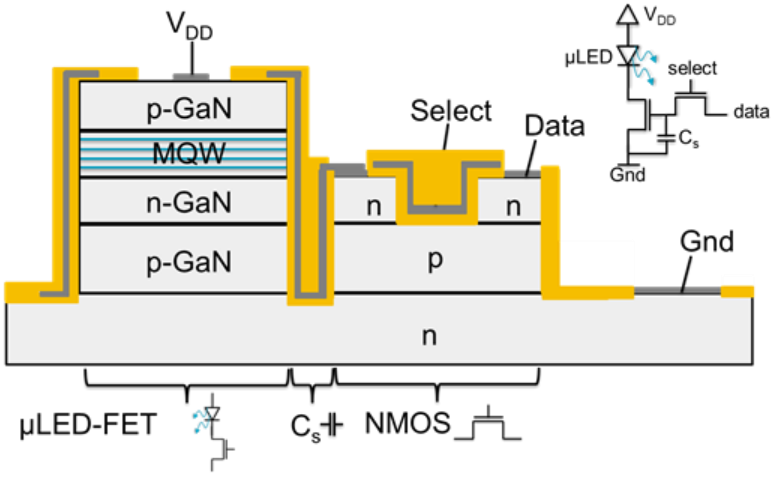

Fig. 91. Active matrix circuit with vertical µLED-FET in series, gate storage capacitor Cs, and planar NMOS pass transistor.

The middle p-type layer and bottom n-type layer, revealed through selective etching, can be used to form PMOS FETs, shown by Fig. 92. The active-matrix circuit shown by Fig. 91 represents a 2T1C configuration, where the circuit shown by the inset would represent each sub-pixel in a display matrix. Due to the single crystalline nature of GaN, it is expected that threshold voltage variations can be minimized, making the 2T1C configuration viable, over TFTs which often incorporate added threshold voltage compensating transistors [106]. Instead of the more common PMOS configuration, the NMOS design can be applied, as the vertical LED-FET design allows single addressability over the universal LED n-contact [107]. Due to the NMOS design with higher electron mobility, with corresponding higher drive current, the transistors can be made far smaller.

Outside of the display, the serial to parallel conversion circuits for driving the rows/columns of the display can be realized on chip through CMOS circuitry shown by Figure 92. The monolithic integration of GaN CMOS eliminates the need for external Si CMOS control chips, reducing processing steps, cost, and minimizing display thickness.

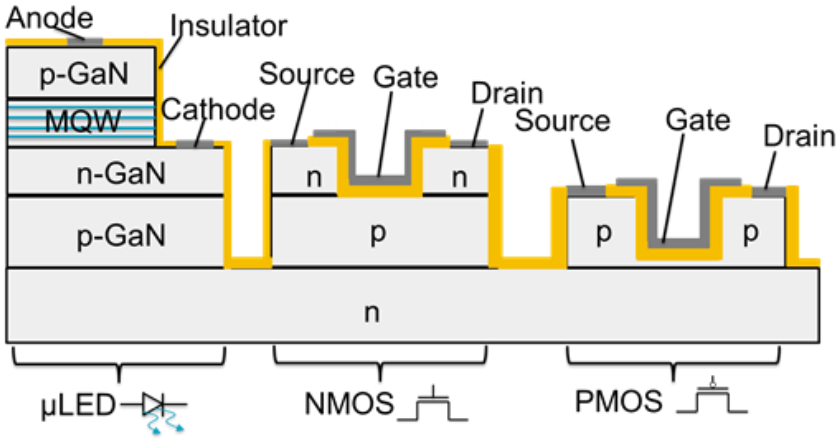

Fig. 92. Schematic of µLED, NMOS, and PMOS devices fabricated from the LED-npn structure, monolithically integrated together.

The integrated LED-FET structure is grown through conventional MOCVD on a sapphire substrate. A low temperature 20 nm GaN buffer region is grown, followed by 500 nm of u-GaN, 1 µm of n-GaN doped $10^{18}cm^{-3}$, 600 nm of p-GaN doped $10^{19}cm^{-3}$, 200 nm of n-GaN doped 10^{18} cm^{-3}, 8 periods of $In_{0.15}Ga_{0.85}N$-GaN MQWs, and 150 nm of p-GaN doped 10^{19} cm^{-3}. Photoresist masking is utilized with ICP etches in order to reveal the various layers. After etching, the samples underwent a hydroxyl based wet etch in order to remove damage formed by the etch [51]. Once the structure was formed the buried p-type layer had to be activated [63-64]. An anneal at 700°C in O_2 was done for 30 minutes to activate the Mg by removing the passivating hydrogen.

For the interlayer dielectric, 200 nm of SiO_2 is deposited through CVD. The deposited SiO_2 is then selectively etched where the gate dielectric is to be positioned, making use of a fluorine based dry etch. 30 nm of Al_2O_3 is then deposited through ALD, forming the gate dielectric. Ti with a Ni cap is then deposited through lift-off, forming the gates for both the NMOS and PMOS transistors. 200 nm more of SiO_2 is deposited through CVD, acting as an additional dielectric spacer. Contact cuts are made through the dielectric films for the anode, cathode, source, and drain regions through dry etching. ITO is conformally sputtered and then selectively etched, forming the contacts. A final contact cut is performed through a dry etch in order to uncover the buried pads for the gates.

Device characterizations are performed on the separate elements of the active-matrix circuit, and then the combined circuit. Where the presented results are from hero devices due to yield issues related to the lab cleanliness discussed in section 2.5. The fabricated NMOS devices had a gate length of 3 µm and a width of 5 µm. Electrical results are shown in Fig. 93(a-b). Fig. 93(a) showcases the current ratio with the threshold voltage as an inset. The threshold voltage was found to be ~0 V, due to a shallower etch depth in the channel region. An on-off current ratio of

~10^5 is recorded, with further improvements expected with thinned dielectric, reduced gate length, and edited metallization. A sub-threshold slops (SS) as low as 100 mV/dec was recorded from the gate on-off characteristics. Fig. 93(b) shows conventional FET performance, with increasing gate voltage leading to higher drain current levels with saturation. The electron mobility from the NMOS devices was found to be 292 $cm^2/V*s$. At 292 $cm^2/V*s$, the electron mobility is far higher than the single digit mobility of TFTs, leading to clear advantages for displays [102]. Further enhancements of mobility of expected to be obtained with optimization, due to the high electron mobility of GaN [108].

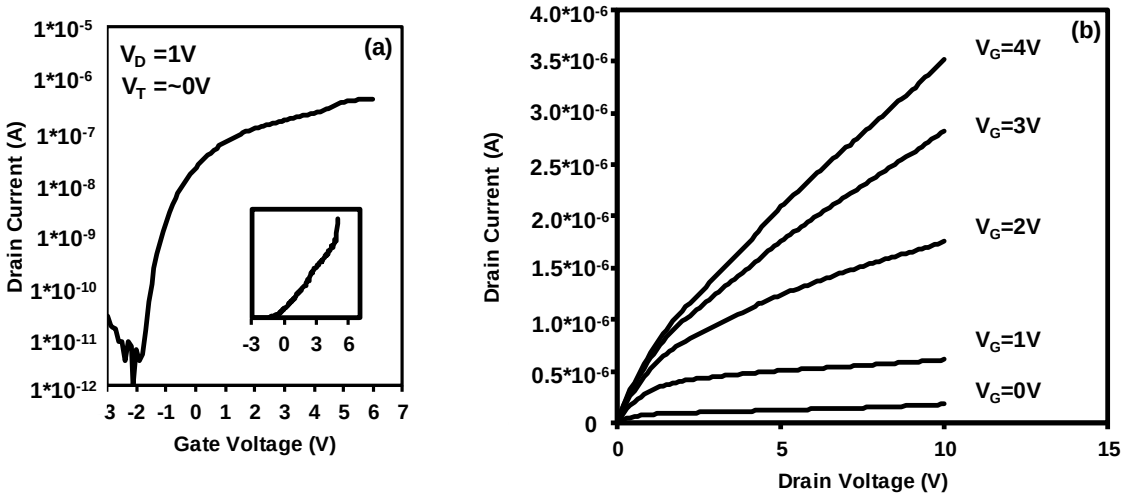

Fig. 93. (a)NMOS threshold voltage with inset showing on-off current ratio, (b)NMOS family of curves.

The fabricated PMOS devices fabricated had a gate length of 9 µm by a width of 9 µm. Results are shown in Fig. 94(a-b). Fig. 94(a) shows the threshold voltage at -3 V, due to the higher effective bottom n-type layer doping making up the channel region. The inset of Fig. 94(a) shows an on to off current ratio over 10^4. A slightly higher SS of 350 mV/dec is recorded for the PMOS device. Fig. 94(b) shows the family of curves, though due to slight gate misalignment making the

gate non-overlapping, the device shows dependence on the drain voltage to continue the channel region, bridging the gap. Gate control is still demonstrated for the device, modulating current flow.

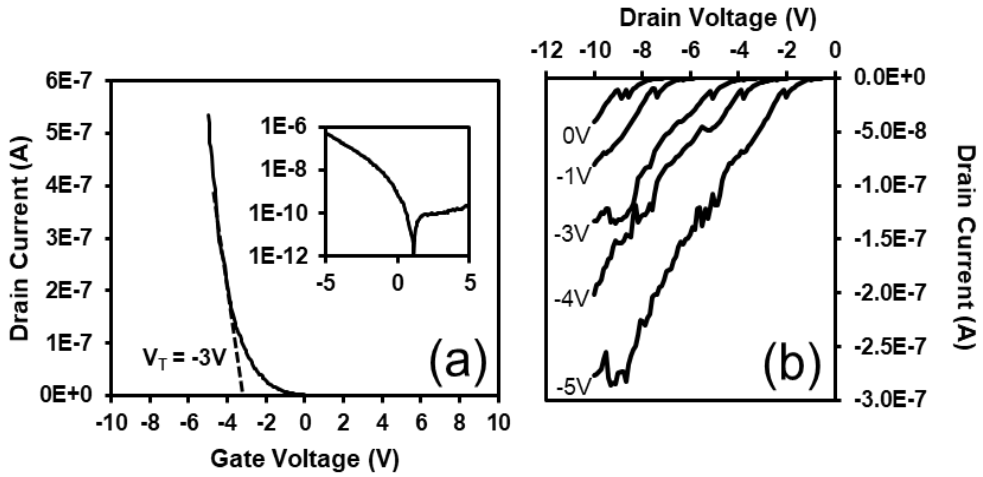

Fig. 94. (a)PMOS threshold voltage with inset showing on-off current ratio, (b)PMOS family of curves.

A standalone 20 μm^2 vertical µLED-FET with a height of 950 nm is shown in Fig. 95, where the gate wraps the sides of the structure. The FET controls current flow through the µLED, controlling the brightness, through a gate wrap around approach. Use of the n-p-n design allows for normally off performance and design freedom, where each vertical µLED-FET can be made at the nano or micro scale.

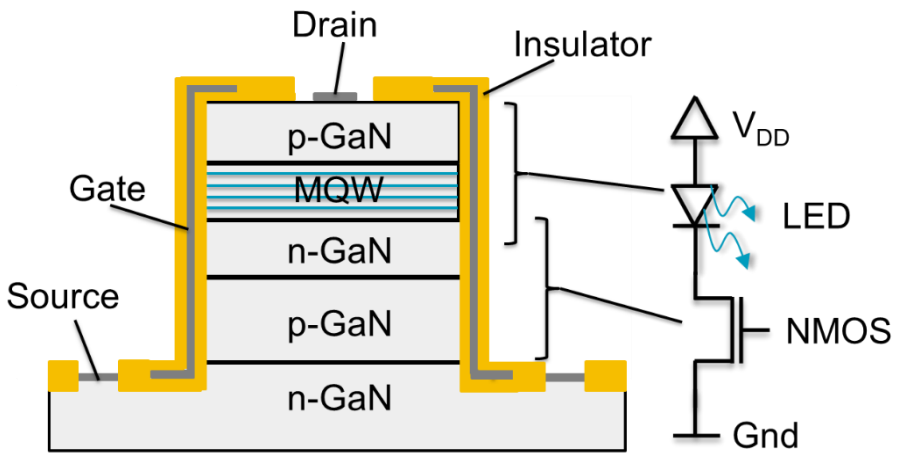

Fig. 95 Vertical µLED-FET in series with circuit diagram displayed.

Electrical results for the vertical µLED-FET are shown in Fig. 96(a-b). In Fig. 96(b) the threshold voltage is recorded at 1 V with an on-off current ratio of ~10^5, while the drain voltage is held at 2 V. The family of curves is recorded in Fig. 96(a) showing conventional transistor characteristics. The family of curves has a positive shift due to the built-in potential provided by the LED. Compared with the NMOS transistor, the higher threshold voltage could be attributed to the less interface charges, due to the formation of the oxide on the non-polar m-plane.

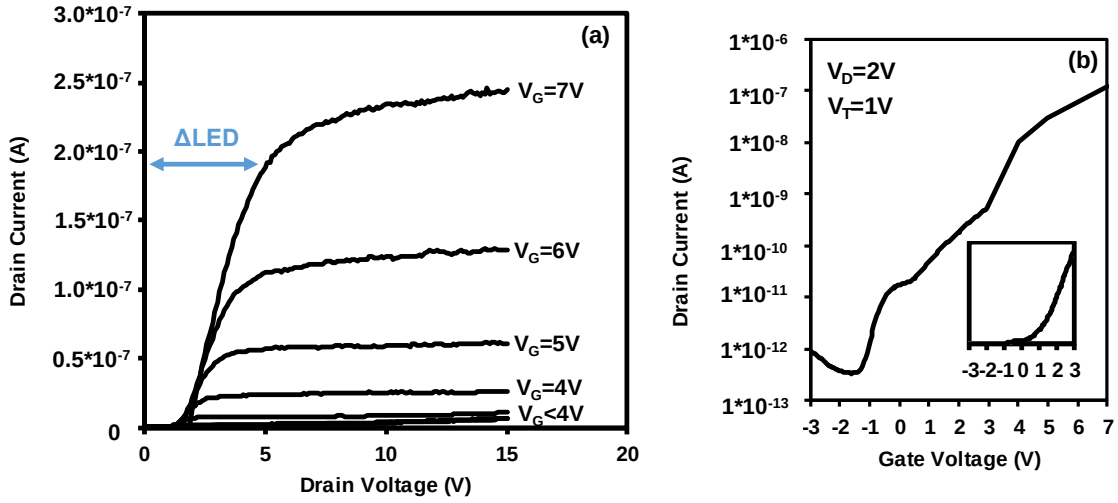

Fig. 96. (a)Family of curves for vertical µLED-FET, (b)turn-on characteristics and on-off current (inset) for the vertical µLED-FET ratio.

Optical power vs. gate voltage for emission at 440 nm is recorded for the vertical µLED-FET at a drain current of 10 V. Gate voltage control over the optical output is demonstrated in Fig. 97.

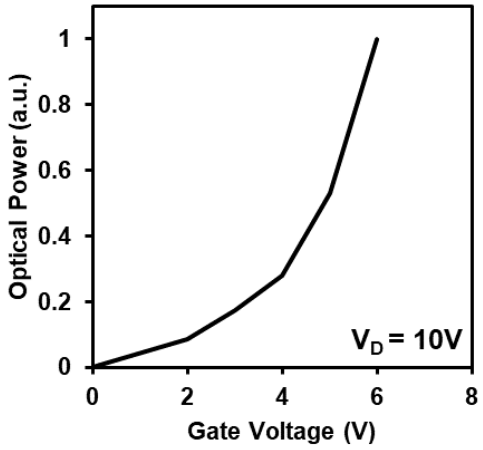

Fig. 97. Optical output power for the vertical µLED-FET vs. gate voltage.

Integration of both the vertical µLED-FET and planar NMOS transistor can be done in order to realize an active-matrix circuitry as shown in Fig. 91. Where the drain of the NMOS acts as the data line, while the gate of the NMOS acts as the select line. When a positive voltage is applied to both the select and data lines, capacitor C_s charges which also acts as the gate of the vertical µLED-FET to control current and corresponding intensity. Capacitor C_s is composed of the gate capacitance and is charged with reference to the grounded bottom n-type layer. The capacitor is also formed and spaced appropriately, such that the vertical n-p-n structure of the planar NMOS transistor is suppressed and does not turn-on. Optical intensity is shown vs. lateral distance is shown in Fig. 98 to both look at the directionality of the emitted light and demonstrate control with a constant select voltage and varied data voltage. The supply voltage is held at 10 V for the active matrix. Most of the light is generated around the p-contact and directed up vertically, as the gate metal minimizes cross-talk and directs light upwards.

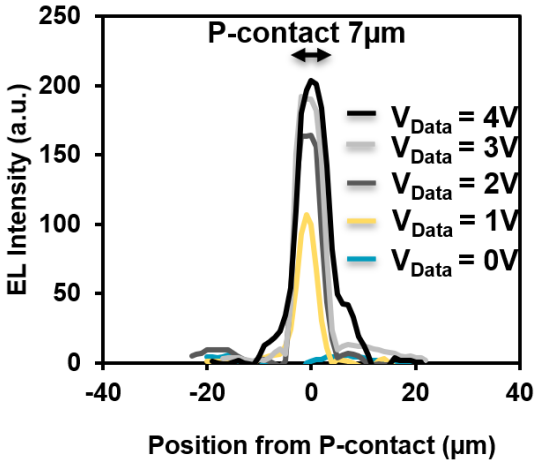

Fig. 98. Optical spreading with varied data voltage of active-matrix circuit.

This work can be directly applied and expanded upon to create fully monolithic GaN based displays. Fig. 99 shows an array formed with multiple active-matrix circuits integrated together. In Fig. 99 a single column is addressed in order to light up the µLEDs. The gates of the planar access transistors form the rows, while the drain of the access transistors form the columns. Each row and column can be connected to the GaN CMOS row/column drivers to provide the serial to parallel conversion.

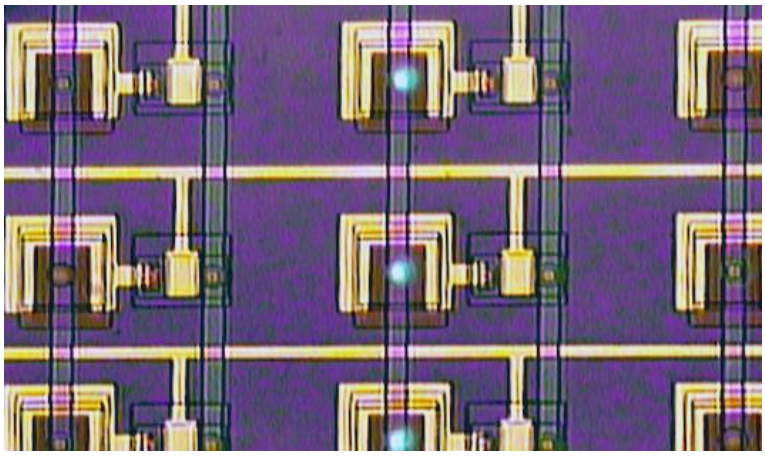

Fig. 99. Active-matrix µLED driving circuitry.

In summary, an active-matrix circuit has been monolithically demonstrated in GaN. Novel vertical integration has been proposed and demonstrated, making use of underlying layer of the LED. The vertical μLED-FET allows for greater size independence, enhancement mode operation, and minimization of cross talk, achieves an on-off current ratio of 10^5. The FET layers can then be utilized for the introduction of planar transistors, demonstrating comparatively high mobility of 292 cm2/V*s. PMOS devices demonstrated gate control and an on-off ratio of 10^4. These results represent a breakthrough for high performance and high resolution μLED displays.

Chapter 4

LED IMPROVEMENTS AND INTEGRATION

4.1 Overview of LED Improvements and Integration Chapter

This chapter focuses on novel improvements to the basic structure of the LED along with novel ways in which these LEDs can be integrated. Capacitor integration is demonstrated on p-GaN to lead to enhanced hole injection, flexible nanowires are demonstrated for improved performance and integration, color changing LEDs are demonstrated, and AC operating LEDs are produced. Each device is explored in separate sub-sections, with both the theoretical and measured results presented for these projects.

4.2 GaN Electrostatic Field Effect Light-Emitting Diode

- **Blue EFELED**

LEDs based on GaN materials provide efficient lighting for a variety of applications including display technologies [109-113], commercial lighting [114-116], and emerging applications such as visible light communication [117-118]. However, these wide bandgap semiconductors suffer from poor p-type dopant activation at room temperature, due to activation energies of 170 meV [119]. The lack of a low activation energy p-dopant leads to high resistance in the p-GaN layer with a low doping density, limiting the performance of GaN-based LEDs. This highly resistive p-type layer necessitates the use of either a current spreading layer or use of polarization doping [119-124]. In this work, additional energy band bending presents a third option for improved p-type doping.

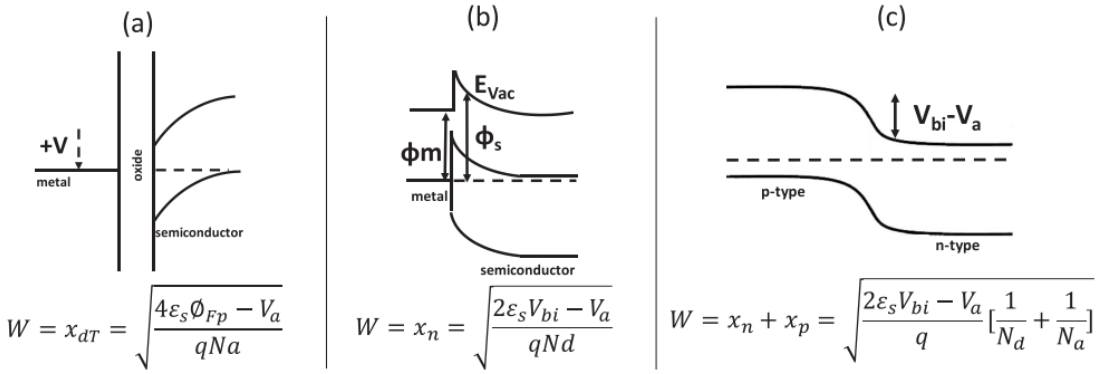

Fig. 100. (a) Capacitor band bending with depletion width equation, (b) metal-semiconductor Schottky contact with depletion width equation, (c) p-n junction with depletion width calculator.

Typical for semiconductor devices, energy band bending through depletion width (W) modulation occurs from an applied capacitor bias (Fig. 100(a)), metal semiconductor work function differences (Fig. 100(b)), or a direct applied voltage to a semiconductor p-n junction (Fig. 100(c)). In the first case, voltages applied to the metal plate of a capacitor bend the energy bands

to accumulate or deplete charges, Fig. 100(a). Fig. 100(a) includes the corresponding W that can be formed by the capacitor on the p-type GaN, where ε_s is the permittivity of the semiconductor, $\emptyset_{Fp}$ is the surface potential, V_a is the applied bias, q is the electron charge, and N_a is the p-type doping [125]. Secondly, metal on a semiconductor can cause band bending through differences between the metal work function and the position of the fermi-level, Fig. 100(b). Here, the band bending and corresponding W equation in Fig. 100(b) are based on the doping and built-in potential (V_{bi}), where the V_{bi} here depends on the work function of the metal and semiconductor [125]. The third case is applying a voltage V_a to a p-n junction, that modulates W to allow for current flow, Fig.100(c). In this work, additional energy band bending is accomplished through an applied capacitor bias on top of an InGaN/GaN LED to aim for significantly improved efficiency.

Note that the LED p-contact already creates band bending, as shown in Fig. 101 with a basic p-n junction under forward bias. Current flows through the device with holes being resupplied by the p-contact after they recombine [126]. The persistent issue, however, is that the band bending is localized around the p-contact and not the entire p-type layer which leads to inefficient hole supply to the active region [120]. In conventional LEDs, the p-contact area is minimized to allow for light extraction, where much of the p-type layer experiences significantly less band bending with the holes not contributing to current flow.

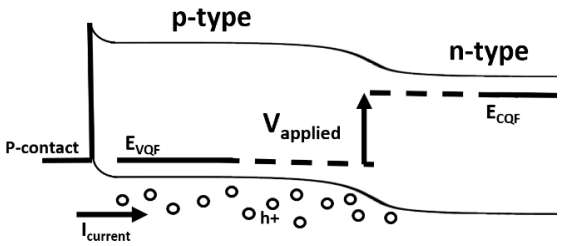

Fig. 101. Forward biased p-n junction with p-type highlighted showing current injection.

The proposed use of a capacitor on top of the conventional InGaN/GaN LED, however, can serve to create additional energy bending to modulate holes for the first time. The capacitor is without the constraints of high resistivity and optical absorption from the use of a metal current spreading layer. The physics of using a capacitor layer for accumulation or depletion of charges through band bending is analogous to the gate bias of a FET [127-128]. Integration of a capacitor can allow for additional utilization of band bending to aid in hole injection, while the p-contact still acts to forward bias the diode and as the steady-state source of holes.

Novel in this work, a capacitor layer is integrated on top of an InGaN/GaN LED in order to demonstrate the advantages in p-type doping, as shown in Figs. 102(a-b) through the optical and SEM images. The capacitor is operated similarly to the gate of a FET in order to modulate charge accumulation or depletion. An ITO layer is used as the top plate, as integrating a capacitor with a transparent conductor allows for the benefits of high optical transmission. Use of the capacitor eliminates the higher resistivity of ITO on p-type GaN [129], as current does not flow through the ITO layer. Instead, charges are accumulated on the top plate ITO, in order to cause the field effect band bending in the p-GaN, Fig. 102(c). The choice of dielectric and transparent metal for the capacitor can also enable both increased LEE by grading the refractive index, along with surface passivation to reduce non-radiative recombination.

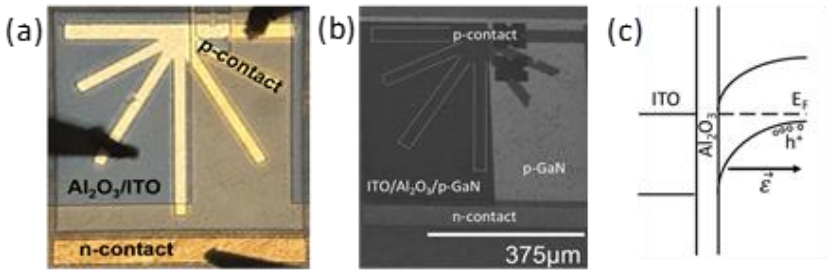

Fig. 102. (a) Fabricated Al_2O_3/ITO capacitor on top of conventional LED, (b) SEM at 45° of EFELED, (c) ITO/Al_2O_3/GaN vertical cutline showing a positive capacitor bias repelling holes.

This EFELED functions by applying a positive bias to the capacitor which bends the energy bands in the p-GaN to repel holes from the surface, as shown in Fig. 102(c). As mentioned earlier, the EFELED takes the concepts of charge transport from FETs, though applies this in a novel way. Instead of hole build up, the holes under the capacitor are transported towards the MQW region to enable increased electron-hole recombination.

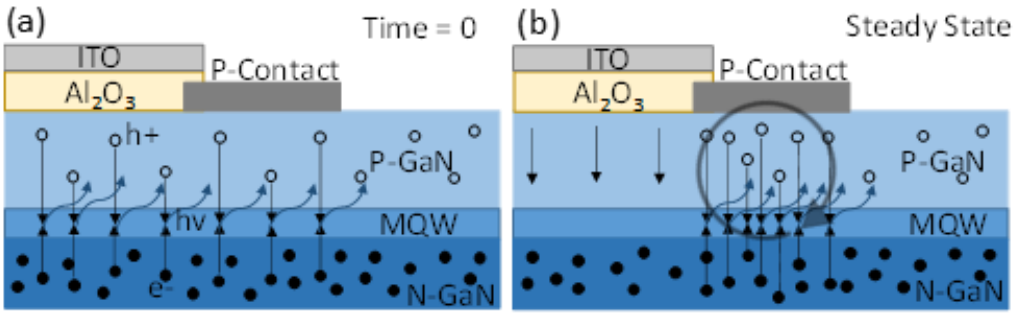

Fig. 103. (a) Positively biased p-contact and capacitor during initial conditions showing hole transport, (b) steady state hole injection with additional holes from capacitor region.

The advantage of the EFELED device is primarily from making use of holes further away from the p-contact which are not conventionally utilized in photon generation. Holes in the p-GaN exist uniformly throughout the layer, though only a few holes around the p-contact participate in conduction, especially with a low forward bias. In the EFELED at an initial time of 0 seconds, the electric field from a positive capacitor bias pushes holes away from the capacitor down towards the MQW region to recombine, as shown in Fig. 103(a). After these holes in the MQW recombine, they have to be resupplied due to charge neutrality. As virtually no current flows through the capacitor, holes are resupplied in steady state from the p-contact as shown by Fig. 103(b). The area under the capacitor becomes depleted, while the area under the p-contact becomes effectively heavily p-type doped. Holes that were under the capacitor are now effectively located around the p-contact, which can be any part of the p-contact. Supply of these additional holes to the p-contact

increases photon generation significantly in the device. Depleting the holes from these unused regions located away from the p-contact allows them to be utilized by the EFELED, which boosts the IQE of the LED, in turn enhancing the EQE.

The secondary effect leading to further enhancement is the Frenkel-Poole field ionization. The use of a capacitor with an independently applied electric field to the surface can lead to a reduced ionization energy for holes. Band bending in the valence band can lead to a reduced barrier height for holes, leading to higher rates of ionization [130-133]. Increased numbers of holes further improve the device performance. The electric field lines created by the p-contact and capacitor are shown by Fig. 104(a). Alternatively, applying a negative bias to the capacitor has the opposite effect as holes accumulate near the surface of the LED. A negative capacitor bias points the electric field towards the surface, as holes from the edge of the p-contact are pulled towards the capacitor instead of recombining in the MQW, as shown in Fig. 104(b). Therefore, there is a slight decrease in light emission and an increase in resistivity in this case. The remote holes away from the p-contact remain unused, as is the case for no capacitor bias. Both the effects of a negative or positive capacitor bias are more dramatic at higher forward LED voltages, as hole injection increases.

Introduction of this novel capacitor layer to a fabricated LED allows for increased performance with no added energy consumption, as the capacitor has a negligible leakage current of nanoamps. Alternative integration schemes can also be utilized to further boost performance of LEDs with various wavelengths based on wide bandgap materials.

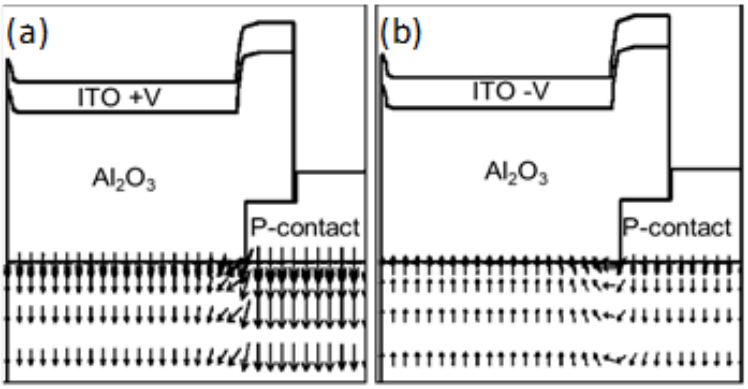

Fig. 104. (a) EFELED Silvaco Atlas simulated positively biased capacitor, (b) negatively biased capacitor.

Here, capacitors were fabricated on top of conventional planar InGaN/GaN LEDs as shown in Fig. 102(a). The devices have a mesa size of 500 μm^2 with a bar n-contact and half-star p-contact. The capacitor occupies an area 200 µm x 250 µm on the p-GaN, approximate half of the LED. A conventional InGaN/GaN blue LED on a sapphire substrate is used which is composed of 2.5 µm n-GaN, 6 InGaN/GaN MQWs with 2.5 nm thick wells, and 300 nm of Mg-doped p-GaN. The p-doping concentration is uniform and at a level of low 10^{17} cm^{-3}. Photoresist is patterned as the mask to form the mesa structure. A chlorine based RIE is used to etch the mesa structure in a Lam 4600 RIE system. The chamber pressure was 100 mTorr with 125 W RF power, 25 sccm BCl3, 30 sccm Cl_2, 20 sccm Ar, and 8 sccm $CHCl_3$. Following the etch and photoresist strip, the n-contact is patterned using metal lift-off. Thermal evaporation is used to deposit 35 nm of Ti and 150 nm of Au to form the n-type contact. The p-contact is then patterned through lift-off, using 36 nm and 150 nm of thermally evaporated Ni and Au, respectively. Both contacts were as deposited with no thermal annealing step. To form the capacitor dielectric, 30 nm of Al_2O_3 is deposited using ALD. A 70 nm ITO film is then sputtered at low power on top of the Al_2O_3 to form the transparent electrode for the capacitor. Photoresist is patterned to mask the capacitor, and a 10:1 BOE wet etch

is used to remove both the Al_2O_3 and the ITO in a single step. Following the removal of the photoresist, the ITO layer is then annealed at 250°C for 30 minutes on a hotplate.

To demonstrate the EFELED, electrical and optical characterizations of the fabricated devices were conducted and compared with simulation results. In this design, the capacitor is biased independently with respect to the grounded n-type contact. Having the capacitor independent allows modulation separate from the performance of the LED. Note that in alternative designs, the capacitor can be driven in parallel with the diode, sharing a common contact for simple integration with existing LEDs without using a three-terminal driver.

The I-V characteristics of the fabricated devices were measured under various capacitor biases ranging from 10 V to -5 V. As can be seen in Fig. 105(a), applying a positive bias to the capacitor greatly increases the current of the device going from 0.4 mA with no capacitor bias to 5.6 mA with 10 V on the capacitor. The current can be modulated, with higher capacitor biases leading to greater current flow. The I-V curve under negative applied bias appears similar to the 0 V reference, with a slight reduction as p-contact voltage increases. The applied capacitor field steals holes around the edges of the p-contact which take away from the forward conduction, leading to the current reduction. As the applied LED forward bias is increased, more holes are needed, though a negative capacitor bias further limits the holes which can be supplied. Applying a positive bias to the capacitor increases current flow of the LED through the utilization of additional holes, exhibiting the primary advantage of the EFELED. The increase in current is due to the increased holes providing a highly p-type pathway under the p-contact of the device. Silvaco Atlas simulation results from the devices are shown in Fig. 105(b), which are similar to the measured electrical results. Here, positive capacitor biases improve device current, and negative capacitor biases lower device current. The measured capacitor leakage current at each voltage for

a reference device is recorded in Fig. 105(c), showing a negligible leakage current of 9 nA on average through the tested voltages. The small capacitor leakage shows that the enhancement is due to the band bending from the capacitor on the p-type region, not leakage current.

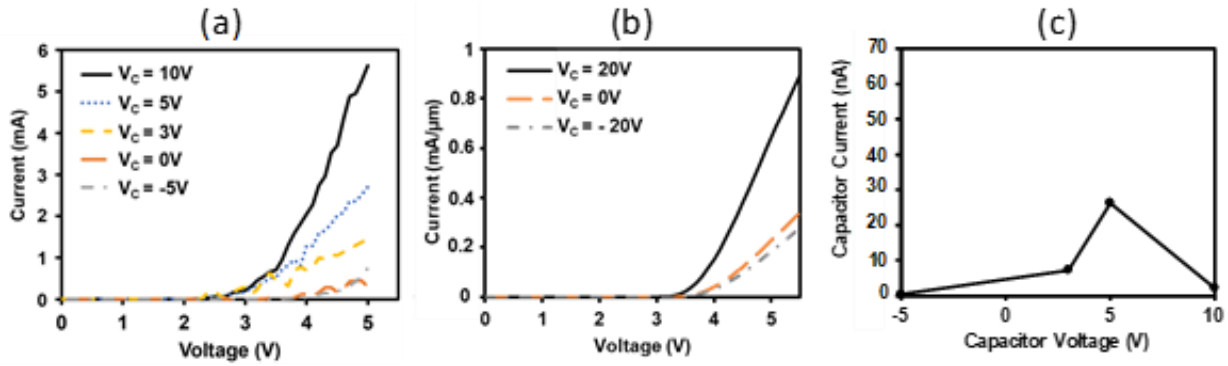

Fig. 105. (a) Measured I-V characteristics with varying capacitor bias, (b) Silvaco Athena simulated I-V curves with different capacitor biases, (c) capacitor leakage under tested biases.

Near-field images of the LEDs under different capacitor biases are taken and shown in Fig. 106. The LED is driven at 3.9 V, while the capacitor voltage is tested at 0 V, 10 V, and -5 V. At 10 V applied to the capacitor the increased utilization of holes allows for greater recombination with the plentiful number of electrons in order to emit more light. Note that the stronger luminescence spans across the whole device which is not limited to just the capacitor region. This observation is consistent with the physics that holes are reinjected by the p-contact. As the p-contact fingers span across the device, the whole device is seen to be brighter due to the higher hole concentration. As a negative bias of -5 V is applied to the capacitor, holes accumulate under the capacitor and cannot be utilized for conduction. The light output in this state is seen to decrease, with only the area near the furthest edge from the capacitor emitting light. This is due to the accumulation region from the capacitor extending well beyond the patterned dimensions due to the light p-type doping. The recorded results in Fig. 89. are consistent with measured and simulated

electrical characteristics. The use of the capacitor through hole depletion or accumulation has been discovered to be an effective way to modulate brightness through voltage control.

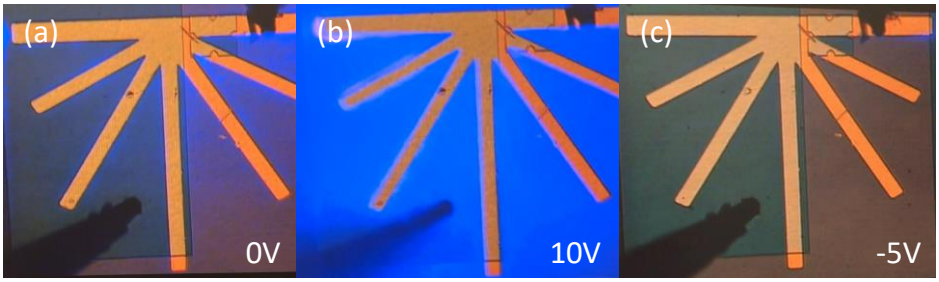

Fig. 106. LED biased at 3.9V with capacitor at (a) 0V, (b) 10V, (c) -5V.

EL measurements of the EFELEDs were also used to characterize the effects of the capacitor electrostatic field effect in order to further quantify the results. The EL spectra are plotted in Fig. 107(a) for various capacitor biases. During these EL measurements the p-contact is driven at 11 V for increased brightness, while the capacitor voltage is varied from 5 V to -5 V. Application of 5 V to the capacitor is shown to produce 127% enhancement in EL peak intensity. Applying a capacitor voltage of more than 5 V was observed to saturate the detector. Alternatively, if -5 V is applied a 33% decrease in EL peak intensity is observed, which is attributed to the aforementioned reduction of holes available for conduction, due to the positive surface charge accumulated by the capacitor. Tying back in with the results show in Fig. 106, it can be seen that the current dramatically increases with a positive capacitor bias and there is a slight decrease with the negative bias at higher driving voltages.

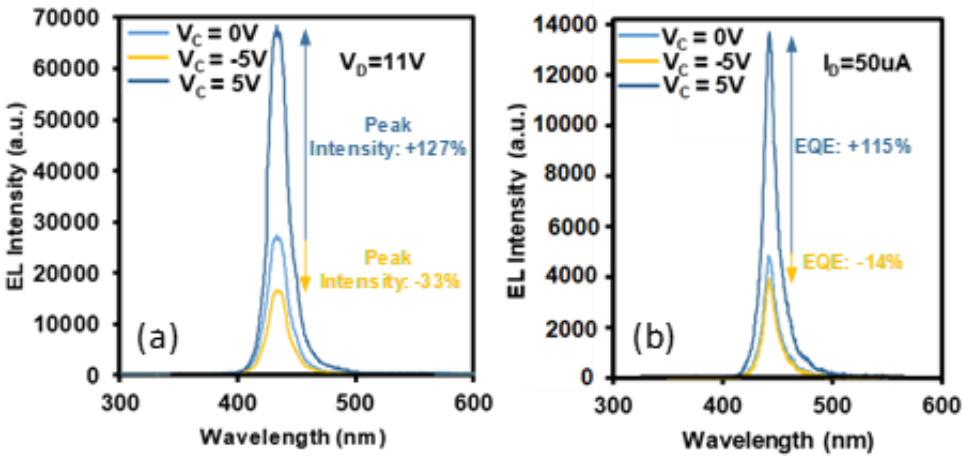

Fig. 107. (a) measured EL intensity with varying capacitor, (b) measured EQE with vary capacitor bias.

In order to compare the effects on EQE for the EFELEDs, EL measurements were taken at a constant current of 50 µA. The EL spectra are plotted in Fig. 107(b) with capacitor biases from -5 V to 5 V. To extract and compare the EQE, the integral of the curves are taken. With the application of 5 V applied to the capacitor, the EQE is dramatically increased by 115% compared to the conventional case of 0 V applied to the capacitor. These capacitors show virtually no leakage and the 50 µA is the total current supplied to the whole device. The increase is due to the greatly enhanced injection of holes into the MQW region due to the re-injection by the p-contact. More holes are effectively utilized by the device compared to the case with no capacitor bias. These results are consistent with those presented in Fig. 106, which show increasing the capacitor bias leads to higher current injection levels. Higher capacitor biases in excess of 5 V are expected to further improve this effect until the electric field intensity causes breakdown in the capacitor dielectric. Application of a -5 V to the capacitor is seen to have the opposite effect, with a slight 14% decrease in the EQE. The decrease observed is not as immense, as only the holes along the edge of the p-contact are captured by the capacitor, as shown by Fig. 104(b). The captured holes are unable to contribute to conduction, leading to a decrease in the light output.

The output power of the EFELED was collected and compared to the injection current in order to look at the efficiency droop under different capacitor bias. The efficiency droop is caused by either auger recombination of electrons or electron overflow into the p-GaN region, both leading to non-radiative recombination [133]. These identified causes each point back to the lack of holes relative to the number of electrons. As the EFELED leads to further hole utilization, the droop effect should be diminished. Results are collected under a capacitor biases of 5 V and 0 V while increasing the current density to the LED. Fig. 108, show the results of the tests with the wall plug efficiency (WPE) normalized. From these results, it is seen when applying 5 V to the capacitor the peak WPE occurs at a lower density. This finding is consistent with LEDs that experience less droop. At the highest tested current density of 14 A/cm^2 the case of 5 V applied shows only a ~40% droop, compared with the 0 V case where the device shows a droop of ~60%. Furthermore, the slope of the droop curve changes when 5 V is applied to the capacitor, which can lead to even still lower relative loss, when even higher current densities are considered. These results are consistent with other findings, showing that increase hole utilization helps improve device performance.

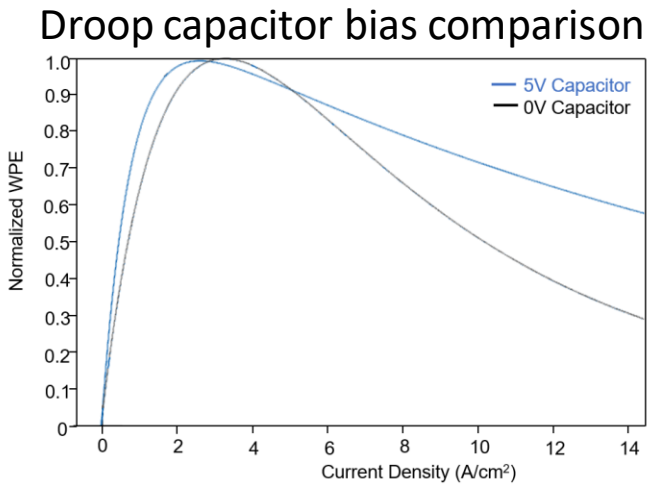

Fig. 108. LED WPE droop comparison for EFELED under different capacitor biases.

Integration of the described capacitor with an LED also improves LEE through grading of the refractive index. The higher refractive index of GaN (2.5) creates a narrow escape cone which traps much of the emitted light within the LED. The Al_2O_3 dielectric and ITO capacitor layers, which have refractive indices of 1.8 and 2 respectively, act to reduce Fresnel reflection in a manner similar to an antireflection (AR) coating, improving the LEE and overall EQE of the LED. Synopsys RSoft simulations were carried out finding that the use of 30 nm of Al_2O_3 with 70 nm of ITO provided a 6% improvement in LEE over a conventional LED. Further improvements in LEE were recorded as the ITO layer thins, finding 32% improvement in LEE for 30nm of Al_2O_3 and 50 nm of ITO. The Al_2O_3 layer also serves to passivate the p-GaN surface and reduce non-radiative surface recombination. The EFELED approach may allow a wider range of materials to be used, as attainment of ohmic contact between a current spreading layer and the p-GaN no longer needs to be considered. The technique could also be applied to solar cells to aid in charge separation.

In summary, integration of a capacitive layer with an InGaN/GaN LED to produce an electrostatic field effect is demonstrated for the first time to solve the inefficient p-doping for wide bandgap semiconductors. This novel EFELED makes use of an Al_2O_3 dielectric and ITO thin film on top of the p-type region of the LED. The electrostatic field produced by the capacitor enhances hole injection for p-GaN significantly, thus improving electrical and optical performances of the LED. An increase in current is observed by applying positive biases to the capacitor, which provides the electrostatic field to increase hole conduction. The integrated electrostatic field effect can also be used as a novel form of brightness control for LEDs in LiFi applications, through the modulation of capacitor voltages. EL results were also recorded, showing over 115% increase in EQE with a 5 V capacitor bias, and a 14% decrease in EQE with -5 V capacitor bias. LEE was

enhanced by 6% over a classical LED, with a pathway for higher enhancement. The fabrication of EFELED is compatible with most conventional LED processes, requiring only one additional mask level. Thus, this work shows promise to solve the fundamental issue of poor p-type doping for GaN, and could improve the performance of LEDs significantly for a wide range of wavelengths.

- **UV EFELED**

The AlGaN QW UV LEDs are being developed for applications such as virus sterilization, water purification, and medical treatments, as a replacement for mercury vapor lamps [134-137]. UV LEDs offer compact sizes, wavelength tuning, long lifetimes, and sustainability over mercury vapor lamps [134, 138]. Longer wavelength LEDs find widespread commercial use for lighting and display applications, highlighting the potential [138-139, 115]. However, UV LEDs struggle with poor EQE of typically less than 10% for wavelengths below 300 nm [134-136]. A main factor limiting the efficiency is the poor p-type doping of the wide bandgap AlGaN. Similar to the case of the blue EFELED, the problem of high ionization energy for the Mg p-type dopant is worsened. The ionization energy depends on the Al-content from the AlGaN material, which ranges from that of GaN at 170 meV to that of AlN at >500 meV [118-119, 140]. With the large p-type ionization energy, far less than 1% of the p-dopant is ionized in AlGaN. Due to the lack of available holes, a similar imbalance with the abundant electrons exists which limits photon generation. The lack of conducting holes in the p-type layer also leads to high resistance and degrades device performance. Currently, there are two approaches to address this issue: use of a current spreading layer or use of polarization doping [119-120]. Nevertheless, the use of a current spreading layer often leads to UV photon absorption issues, while the use of polarization doping requires precise

control of epitaxial growth of graded AlGaN layers. In this paper, a third method is introduced which is by the use of energy band bending.

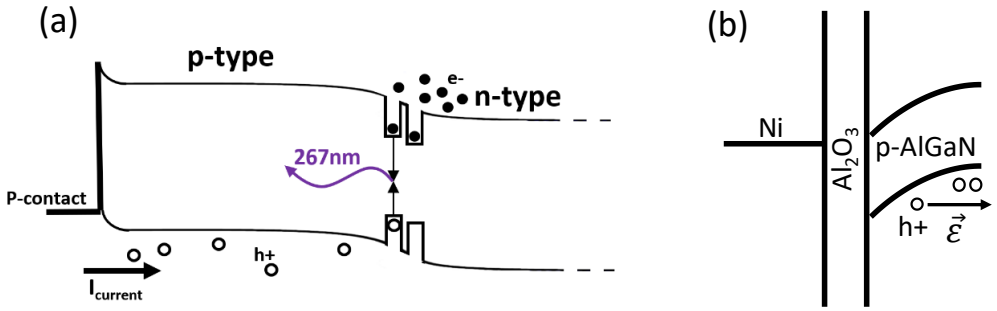

Fig. 109. (a) Forward biased LED showing steady state hole supply from the p-contact, (b) Positive bias to the Ni/Al2O3 capacitor causing energy band bending directing holes towards the MQW region.

Energy band bending is already utilized in LED devices, where a positive voltage applied to the p-contact with respect to the n-contact lowers the built-in potential allowing current to flow, Fig. 109(a). A steady state current of holes is provided by the p-contact to resupply holes that recombine in a forward biased LED. The issue, however, is that the band bending in a forward biased LED is localized around the p-contact [119]. As the distance from the p-contact increases, the band bending is reduced, limiting the injection of holes to produce light in these regions. The metal p-contact area cannot span the entire p-type region due to significant absorption issues, which degrades LEE. Thinner, optically transparent, conductors are commonly employed such as thin metal films, however, these thin films suffer from high resistance [141]. In order to apply additional band bending and to better utilize available holes, a capacitor is chosen while the p-contact still acts as the steady state source of holes.

Previous work has investigated the capacitor integration with InGaN/GaN visible LEDs showing EQE enhancements of 115%, this work is expanded upon here for UV LEDs [142]. Novel

to this work, the capacitor is integrated with the AlGaN material system, forming a UV EFELED. The operation of the capacitor is analogous to that of the gate in a FET, where charges can be attracted or repelled [143-144]. The width of the depletion region (W) where charges are attached or repelled can be found through Eq. 7, where ε_s is the permittivity of the semiconductor, $\emptyset_{Fp}$ is the surface potential, V_a is the applied bias, q is the electron charge, and Na is the p-type doping [145]. A thin layer of Ni is utilized as the optically transparent top plate of the capacitor, while a layer of Al_2O_3 is utilized as the dielectric, as shown in Fig. 109(b). The capacitor eliminates the resistance issue for thin metal current spreading layers, as virtually no current flows through the capacitor, and instead charges build up. Additionally, the Al_2O_3 thin film can serve to passivate surface states and enhance the LEE of the LED [146]. The performance increases by the UV EFELED are achieved by applying a positive bias to the capacitor in order to order to bend the bands further from the p-contact, repelling holes from the surface towards the MQW region to recombine.

$$W = x_{dT} = \sqrt{\frac{4\varepsilon_s \emptyset_{Fp} - V_a}{qN_a}}$$

Eq. 7. Width of the depletion region for a capacitor on a p-type semiconductor.

The same principal physics can be applied in the base of the UV EFELED as for the blue EFELED [129, 131-132, 147]. At an initial time, with the application of a positive bias to the capacitor, in addition to the p-contact, the energy bands further from the p-contact also bend, directing holes to the MQW region, as shown in Fig. 109(b) and Fig. 110(b). These holes modulated by the capacitor similarly recombine with electrons in the MQW region, as is the case with those from the p-contact, Fig. 110(a). Due to charge neutrality, these holes that recombine either radiatively or non-radiatively must be resupplied. The p-contact, as is the case in

conventional LEDs, is the steady and continuous source for holes, Fig. 110(c). The holes must be resupplied by the p-contact as the capacitor has negligible leakage current. Effectively in steady state, the areas under the capacitor become depleted, while the area under the p-contact gains these holes. These additional holes under the p-contact produce a highly conductive pathway and greatly enhance photon generation. Therefore, both the internal IQE and EQE are greatly enhanced by this novel method.

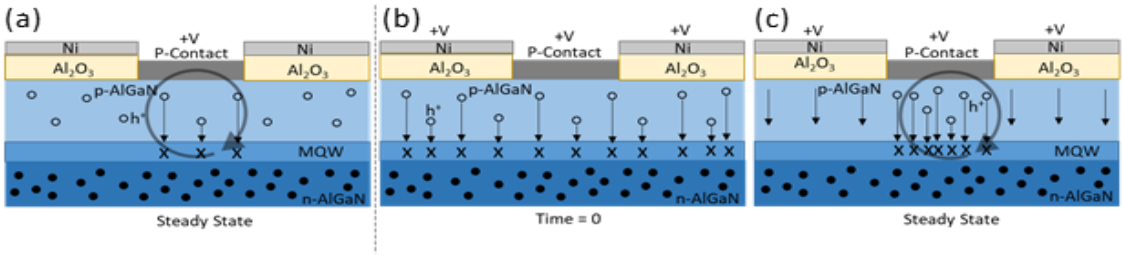

Fig. 110. (a) Positively biased p-contact under steady state showing path of holes, (b) positively biased p-contact and capacitor at initial time, (c) positively biased p-contact and capacitor under steady state showing path of holes.

The AlGaN UV LEDs emitting at 267 nm are grown through MOCVD on a sapphire substrate. A 1 µm AlN buffer layer is grown on the sapphire, followed by 2 µm of n-AlGaN, 75 nm of AlGaN-AlGaN MQWs, 20 nm of p-AlGaN as an electron blocking layer, 40nm of p-AlGaN, and then 160 nm of p-GaN. The mesa region is formed through the use of a chlorine plasma in a Lam 4600 reactive ion etcher with a photoresist hard mask. A 25/150/30/50 nm stack of Ti/Al/Ni/Ag was lifted off to form a common n-metal contact across the device. A 50 nm layer of Al_2O_3 was next deposited through ALD to form the dielectric for the capacitor. A 7 nm film of Ni was deposited and lifted off to act as the transparent top plate for the capacitor. The thin Ni film was also utilized as the hard mask with BOE to etch away the Al_2O_3 on the surface, leaving the film solely under the top capacitor plate. As a final step, a 50 nm coating of Ni was deposited to

form both the p-contact and a thicker metal pad to probe the capacitor plate. No annealing step was performed for the metal contacts. Integration of the capacitor only required the addition of one masking level to a conventional LED, or the same in the case of a current spreading LED. A schematic view of the fabricated device can be seen in Fig. 111.

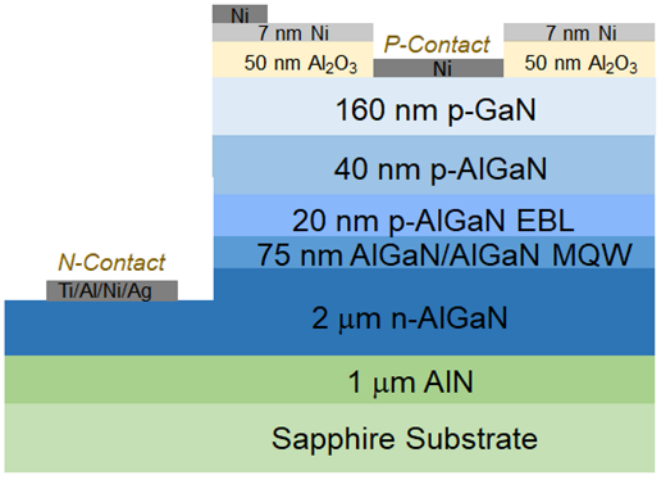

Fig. 111. Schematic cross section of fabricated UV EFELED device.

Four separate capacitor and p-contact designs were fabricated in order to optimize device performance. These designs are shown in Figs. 112(a-d) with an edge capacitor (design A), capacitor surrounding the central contact (design B), capacitor block with bar contact (design C), and capacitor block with edge contact (design D), respectively. These LED designs were fabricated to be 100 μm^2 in size. The devices had a contact area of 10 μm^2 for the p-contact and the capacitor, except for deign C with a contact area of 10 µm x 60 µm.

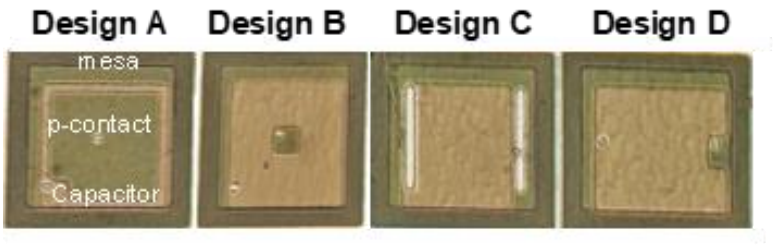

Fig. 112 UV EFELED fabricated designs (A-D) with differing capacitors and p-contacts.

Both electric and optical measurements were performed on the fabricated UV EFELED devices in order to explore the physics of band bending and the effect on hole injection. The integrated capacitor is biased independently in this design to allow for separate modulation apart from driving the LED. The capacitor contact can be shorted to the p-contact if the goal is a pure performance gain, separate from the novel ability to modulate photon generation.

The I-V characteristics were collected, with capacitor voltages varying from 20 V to -20 V, while the UV LED was driven at a forward voltage from 0 to 25 V. These voltages are higher in magnitude compared to the blue EFELED as the dielectric for the capacitor is thicker, and the AlGaN is far more resistive. As a representative example, I-V results of design C are shown in Fig. 113. From Fig 113, it can be seen that the application of a positive capacitor bias is seen to drastically increase the drive current by ~10x due to the utilization of additional holes. The increased hole concentration below the p-contact forms a far more conductive pathway for current transport. Under positive capacitor bias, Fig. 113 further shows the increased conduction leads to a lower turn-on voltage for the LED due to the greater hole concentration lowering the Schottky barrier formed by the p-contact. Capacitor leakage was recorded on average to be 9 pA from the tested capacitor voltages. This shows the drive current enhancement is due to the added band bending and not capacitor leakage. Opposite performance is seen in the case of a negative capacitor bias, with a reduction in the drive current of ~60%, Fig 113. The diode also has a higher turn-on voltage due to a fraction of the holes captured instead of participating in conduction. These results are consistent with those obtained on the blue EFELED, further show casing the expansive devices that can be improved utilizing this novel method.

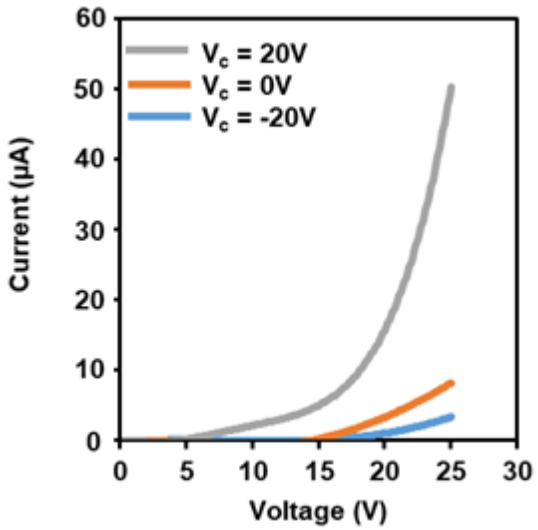

Fig. 113. I-V curves from UV EFELED design C showing performance.

Each of the tested capacitor designs showed a similar trend of enhancement with a positive capacitor bias and a decrease with a negative bias. In order to compare the four designs to best optimize the device performance, the I-V curves of each are recorded in Fig. 114. Here each capacitor voltage is held at 20 V to compare the current enhancement. It is clear that as the capacitor size increases the enhancement in drive current is greatly improved. Position and size of the p-contact are also important to the UV EFELED device efficiency. Location of the p-contact on the edge, as is the case of design D, leads to a lower drive current than design B for a similar capacitor area. Position of the contact near the edge can lead to surface recombination that can degrade current flow. Design C shows that a further gain in drive current is obtained by increasing the p-contact length from 10 μm to 60 μm. For larger p-contact sizes, the injected holes are not as confined and are able to better spread across the device, leading to lowered resistance. However, a larger p-contact leads to significant photon absorption. A future optimized design would call for a large capacitor with a thin p-contact metal in the middle that spans across the device, such as a star shaped contact with a surrounding capacitor.

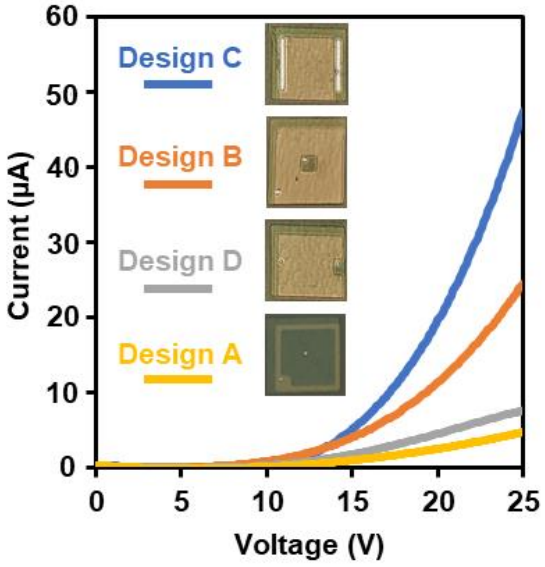

Fig. 114 I-V curves with designs (A-E) held at a capacitor bias of 20V.

Optical measurements through electroluminescence (EL) were taken in order to judge the optical performance of the device. The EL spectra are plotted in Fig. 115 for design C. Design C is selected as it was seen to have the best performance enhancement, seen by Fig. 114. To compare the peak EL intensity, Fig. 115(a), the capacitor is varied from 20 V to -20 V, while holding the drive voltage (V_D) constant at 15 V. With the application of 20 V to the capacitor the peak EL intensity is increased by 172%. The additional holes involved in conduction, which are the main limitation in UV LEDs, generates greater recombination with the plentiful electrons. In contrast, -20 V to the capacitor produces a decrease in peak EL intensity by 38% due to the captured holes from the capacitor.

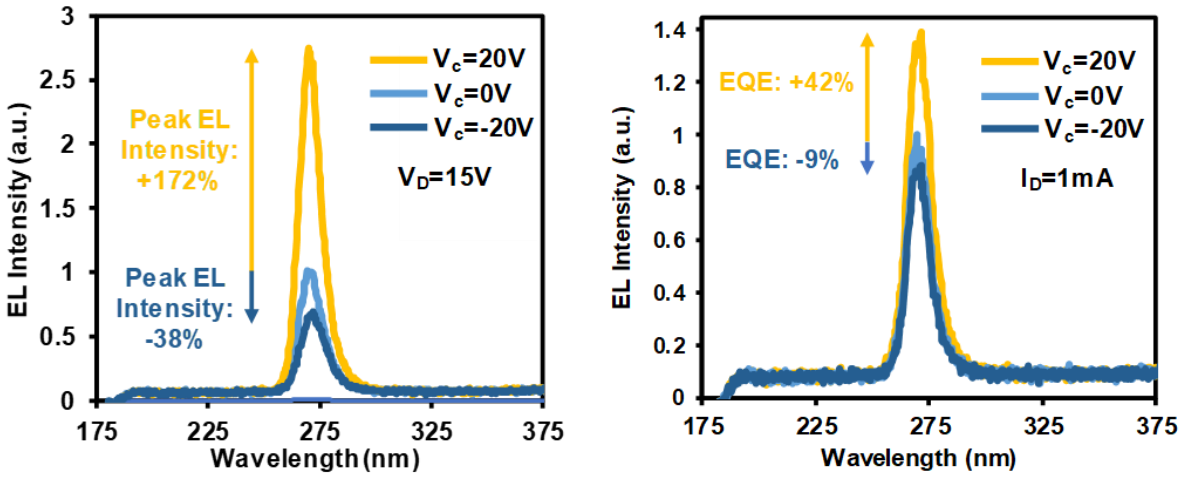

Fig. 115. (a) Measured EL intensity for varying capacitor biases at a forward voltage of 15 V, (b) measured EL intensity with varying capacitor biases at a constant current of 1 mA.

In order to compare the EQE of the UV EFELED, EL measurements are taken at a constant current of 1 mA. The corresponding EL spectra are recorded in Fig. 115(b) with the capacitor varied from 20 V to -20 V. The 1 mA is the total current to the whole device, including the capacitor, though the capacitor shows pA of leakage current. To extract the EQE, the integral of the curves are taken for each tested capacitor bias. At 20 V applied to the capacitor the relative EQE is seen to be dramatically increased by 42%, which greatly helps the commercial viability of UV LEDs. The boosted EQE represents a large improvement, though ultimately there are still limits due to the lack of holes in the material, where a larger EQE boost is obtained on the blue LED. Applying -20 V to the capacitor leads to the opposite of a slight decrease in the relative EQE of 9%. Increased positive or negative biases are expected to have a larger impact on EQE until the capacitor breaks down. Modulation of photon emission through the independent bias of the capacitor, presents a novel way to control the brightness of UV LEDs.

The work presented here introduces a capacitor-UV LED integration, known as a UV EFELED. The major limit of UV LEDs, the lack of p-type doping, is addressed through a novel solution. The UV EFELED makes use of an Al_2O_3 dielectric and thin transparent Ni film to form a capacitor on top of the p-type layer. An additional electrostatic field is produced by the capacitor in order to drive holes towards to the MQW to recombine and be recycled. Due to the capacitor with hole modulation, positive voltages lead to an increase in photon production and efficiency. The EQE was increased by a record 42% due to the capacitor integration. Capacitor integration also produces a novel means of brightness control with positive biases increasing photon generation, while negative biases limit generation through hole reduction. The fabrication of the UV EFELED is compatible with most conventional UV LED processes, requiring only one additional mask level. Thus, this work shows immense promise to address the limiting issue of poor p-type doping for AlGaN and therefore further the market viability.

- **Future Directions**

The integration of the capacitor on top of the p-type layer for the LED already represents a novel breakthrough, which can be applied to a number of additional devices. In theory the work can be expanded upon to include GaAs based LEDs. Interested enough, the work can be applied to solar cells to form an additional field to repel minority carriers to the respective sides to generate current. The dielectric choice of capacitors can also lead to additional interesting applications in terms of memory storage. Where commercial non-volatile memory makes use of silicon nitride traps for electron charge storage to lead to a prolonged threshold volt shift. These commercial dielectric stacks can similarly be applied here for display applications or use in visible light communication. This is initially invested by utilizing the charge trap states that exist near the

conduction band of Al_2O_3. Voltages of 5 V with different magnitudes are held on the top plate of the capacitor for several seconds then removed; testing is then performed on the LED by only applying a forward bias to the LED. Initial results are shown in Fig. 116, showing possible trap based storage.

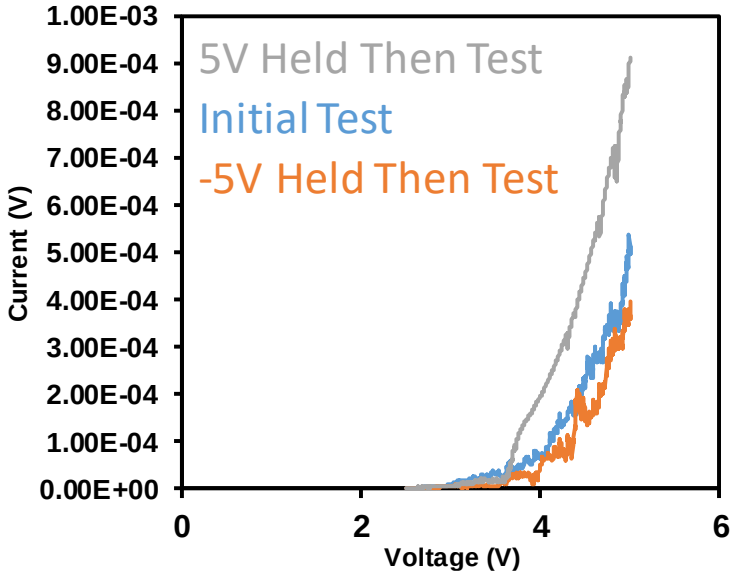

Fig.116 Initial charge storage due to oxide trap states in EFELED device.

4.3 Flexible Nanowire Devices

Nanowire GaN devices provide a number of novel devices as previously presented. These GaN devices contain all the necessary layers for the device in each nanowire. The host substrate for these devices only provides mechanical support after the nanowires are formed. There are novel possibilities and device integration schemes offered through the removal of LEDs from the host substrate. Flexible LEDs are a major goal, as though the performance of LEDs is superior to OLEDs, conventional LEDs can not bend or flex like OLEDs. Initial work has been demonstrated with the removal of planar LEDs from a silicon substrate, however density and efficiency are still

remaining issues [44]. Nanowire LEDs provide increased efficiency over conventional planar LEDs and can achieve higher densities. Preliminary work has been done embedding 30 µm tall nanowires in PDMS and mechanically exfoliating the structure through a razor blade [53]. The flexible nanowire work that exists currently is inadequate to address the goal of a flexible nanowire-based display.

- **GaN on Silicon Nanowire Peeling**

Presented here is the development of a novel nanowire peeling processes for top-down fabricated nanowires. Top-down fabricated nanowires provide a more manufacturable process for the development of large-scale flexible nanowire devices. GaN grown on silicon is utilized for this work to provide the Si undercut for GaN nanowire removal, demonstrated in Section 2.4. A 1 mm thick 2" Si wafer is utilized to minimize cracking of the GaN layers upon cooling from growth. AlN 300 nm thick is grown on top of the Si wafer, where a layer of Al is grown and nitridated in order to form AlN. GaN can not be directly grown on Si as the Ga dewets on the surface, while N_2 forms Si_3N_4 on the surface preventing grown. After the AlN layer is grown, a 600 nm downgraded layer of AlGaN is grown to grade the lattice constant up to GaN. 500 nm of u-GaN is grown, followed by 3.4 µm of n-GaN, 9 pairs of $In_{0.15}Ga_{0.85}N$ MQWs, 35 nm of p-$Al_{0.15}Ga_{0.85}N$ as the electron blocking layer, 60 nm of p-GaN, and 20 nm of p++ GaN. LOR and photoresist here coated and patterned in the Heidelberg direct write system, creating features of 1 µm in diameter, spaced by 19 µm. The increased spacing was utilized for the later contact lithography steps that followed. 250 nm of Ni was deposited and lifted-off to form the hard mask for the nanowire etch. A dry etch was utilized to form the nanowire structure down to the Si base. A 225 W, 30 sccm Cl_2, 20 sccm Ar, at 65 mT etch was utilized to anisotropically etch the wires. The initial shape of the nanowire

is recorded in Fig. 117. The GaN wires shows to be perfectly vertical, while the Si nanowire shows a significant taper. The planar surface of the Si is also seen as rough, due to the anisotropic chlorine etch. The dry etch process is optimized to achieve a vertical GaN wire, though the distinct material properties of Si lead to different etch profile.

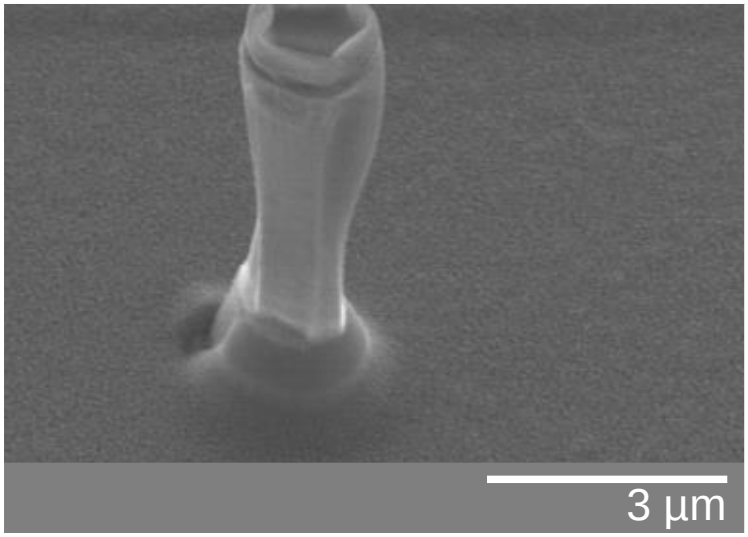

Fig. 117. LED nanowire on Si tapered nanowire, post dry etch.

Following the dry etch, the sample is immersed in KOH in order to etch the Si nanowire diameter. The diameter of the Si nanowire is reduced from ~1.2 µm to ~400 nm following the KOH wet etch, Fig. 118. The <111> surface of the Si is not target by the etch as the KOH etches this plane slowly. The sloped Si is seen to become perfectly vertical, matching with the <110> plane. The reduced diameter of the Si provides mechanical stability for the PDMS coating, while reducing the bonding strength of the nanowire to the Si surface.

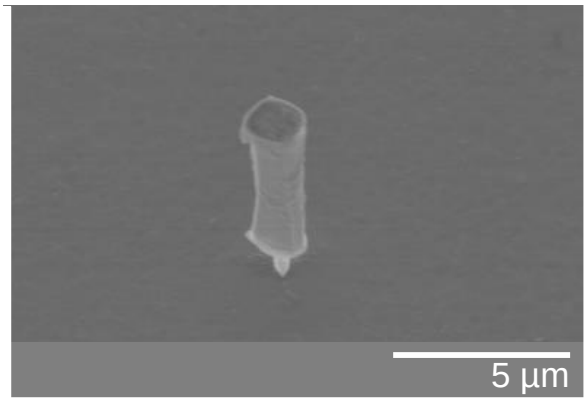

Fig. 118. LED nanowire with reduced Si nanowire diameter.

A 7 µm layer of PDMS is overcoated onto the nanowire array to provide planarization. The PDMS is etched back through use of a fluorine based RIE etch. Once the wire tips are revealed a BOE etch is performed in order to remove the build-up of silica on the surface of the PDMS. The post PDMS etch results are shown in Fig. 119.

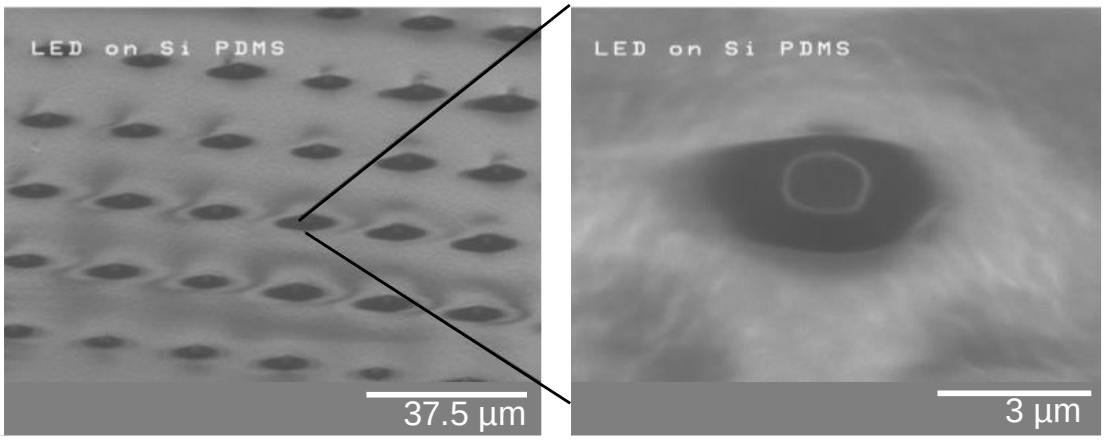

Fig. 119. LED nanowires embedded in PDMS.

A 100 nm layer of ITO is coated on top of the nanowires to from the top transparent contact. The ITO is patterned with a masking photoresist and etched for 1 minute in 10:1 BOE. The ITO deposition on the tips of the nanowire LEDs is seen in Fig. 120. The ITO was subsequently annealed for 30 minutes at 250ºC to improve both optical transparency and reduce resistance.

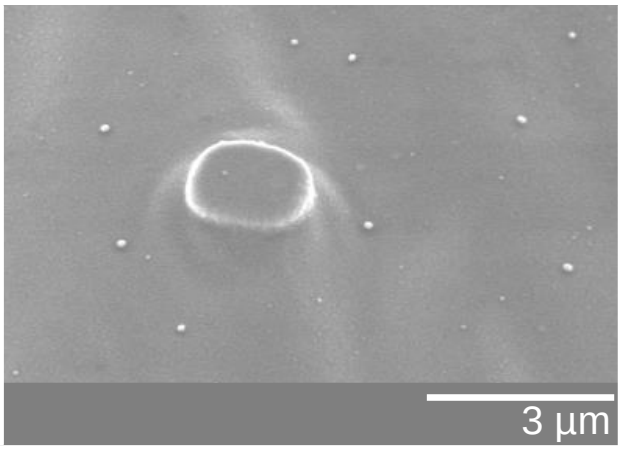

Fig. 120. ITO deposition on nanowire LED tip.

With the ITO top contact in place, a thicker 30 µm PDMS film is then coated on top of the sample following and O_2 plasma treatment. The thicker layer of PDMS was found to both provide mechanical support, while also keeping the underlying PMDS intact for subsequent steps. The thicker layer of PDMS is annealed at 90ºC for 1 hour in order to cross-link the thicker film. The sample is then immersed in KOH for a period of several days. The KOH was found to slowly peel the edges of the PDMS film from the host Si substrate. The KOH etch was found to not further etch the Si nanowire base for the majority of the sample, only releasing the edges. If only the thinned single layer PDMS is utilized, the KOH was found to be able to penetrate the film and etch the Si. The etched Si in a single PDMS layer led to the formation of bubble that would pop the PDMS film.

After the extended KOH etch to release the film edges from the Si substrate, the wires embedded in the PDMS can be easily peeled off. Fig. 121 demonstrates the peeling process, showing the smooth Si host substrate remaining. The film is ~40 µm thick where it is mechanically stable enough to be removed, though the film itself is still fragile. The removed PDMS film can easily fold or stretch, where care must be taken when handling. Use of either a temporary scotch tape backing or mounting on a 2” Si carrier wafer is utilized for further device processing.

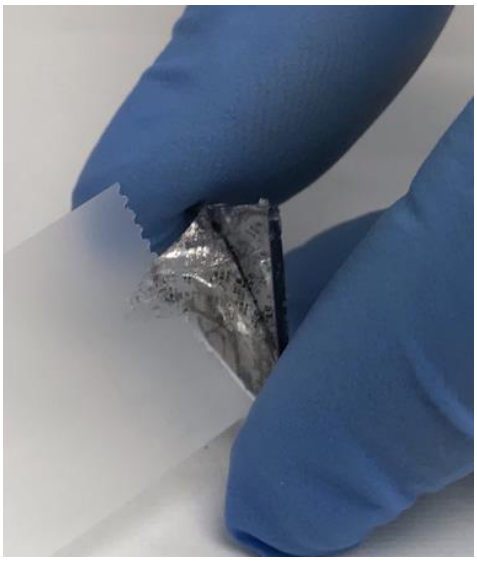

Fig. 121. Embedded GaN nanowires peeled from a Si substrate.

Once the PDMS with the embedded nanowires is mounted on a temporary substrate, the results from the peeling process are studied. The original Si host substrate is examined in order to study the KOH peeling process and the yield from nanowire removal. The original Si wafer is imaged in Fig. 122. The PDMS peeling process shows high yield, with no wires remaining on the host substrate. Leaving wires still attached to the Si substrate would translate into dead pixels for a flexible nanowire display. The Si base of the nanowires also do not appear targeted or etched through the extended KOH peeling step. The base also shows a snapping effect right at the interface between the Si nanowire and the GaN wire, due to the material differences. Leaving behind the Si nanowire is the ideal case as additional etching of the Si nanowire is no longer needed. Additional tests also have determined that the effects of the diameter shrining of the Si nanowire are not that critical, where only straightened Si sidewalls from the dry etch appear to aid in lift-off.

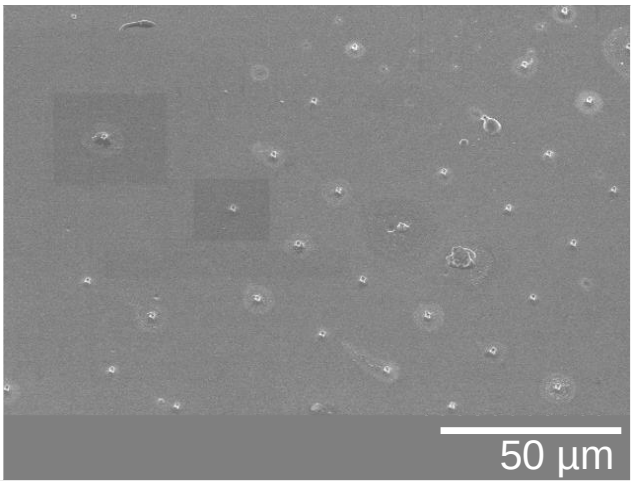

Fig. 122. Si host substrate following GaN nanowire removal.

The embedded nanowires in PDMS are also studied to ensure complete array removal. The results for the PDMS peeling are shown in Fig. 123. The nanowires appear as fully embedded in the PDMS film. Only the bottom surface of the nanowire is visible under SEM. Under an optical microscope the nanowires can be seen as dark dots in the PDMS film. The nanowire array positions are also kept intact with respect to the original spacing. The backside nanowire contact can not yet be made at this stage, as even with the Si base removal there remains the insulating AlN film. Etching of the PDMS must to done in order to revel a portion of the AlGaN under the AlN film in order to achieve an electrical contact.

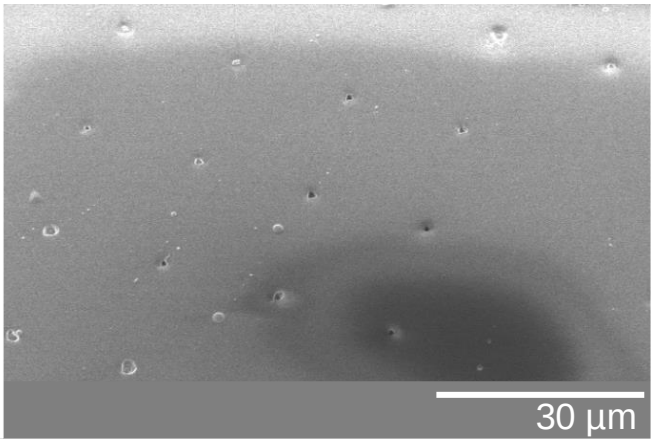

Fig. 123. GaN embedded nanowires in PDMS film.

Etching of the PDMS is performed on the post lifted-off film in order to both form an ohmic contact and also ensure the nanowires are still intact in the film. The post PDMS etching results are shown in Fig. 124. This particular sample has been over etched due to a theory of a slower PDMS etch rate post lift-off. The majority of the wires are almost fully uncovered from the PDMS, leaving only several hundred nanometers of PDMS left. As seen from Fig. 124, the wires are fully intact after the peeling and stretched of the PDMS film. The AlN layer is now positioned at the top of the nanowire, in Fig. 124. The Si nanowire is also seen to removed from the AlN layer during the peeling process.

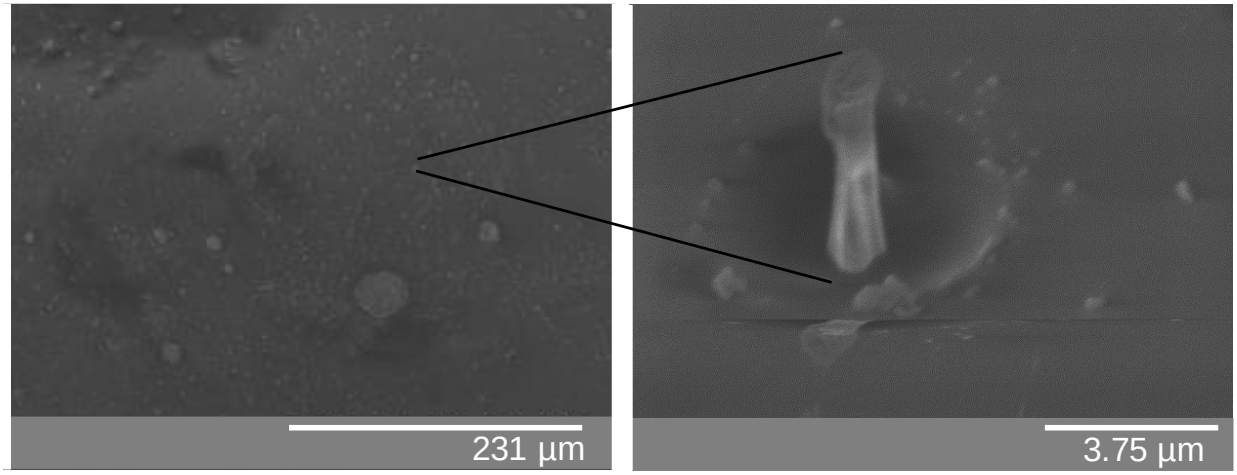

Fig. 124. Embedded GaN nanowires peeled from a Si substrate.

- **AlGaN DUV Nanowire Peeling**

The work is also expanded up for novel AlGaN DUV LEDs that show promise for use in applications such as water purification, pathogen neutralization, and medical treatments [134-138]. In contrast to mercury vapor arc lamps, DUV LEDs offer a small form factor, tunable emission wavelength, long lifetime, and environmental compatibility [134, 138]. DUV LEDs are usually fabricated as planar “mesa” devices due to the simplicity of this well-developed fabrication

process. Nanowire DUV LEDs, while more difficult to fabricate, offer higher LEE and improved IQE, which together produce significant enhancements in EQE. Nanowire LEDs fabricated using a bottom up growth approach can also offer large reductions in defect density through use of specialized growth substrates, further enhancing their IQEs when compared to planar LEDs [148]. Though nanowire LEDs have a number of beneficial properties, a reliable process to remove them from the growth substrate has not yet been developed, as it has for planar LEDs [149]. LEDs removed from the growth substrate offer new possibilities for displays and flexible electronics. Current published work on flexible nanowire LEDs typically involves embedding the nanowires in a flexible polymer for support, followed by mechanical exfoliation with a razor blade [150]. For this process to work, the nanowires must be grown to at least 20 µm tall, and even then this approach still suffers yield issues from the peeling process, making it non-deal scalable manufacturing [151]. This work presents a novel method of forming AlGaN nanowires with an inverse taper, which allows for more reliable release of nanowires from the substrate.

Hydroxyl-based chemistries are often used to wet etch GaN and remove dry etch induced damage, as the polar OH- ions in these solutions exhibit a unique selectivity against the non-polar planes in wurtzite GaN and AlInGaN allows [152]. Hydroxyl based chemistries also allow for formation of GaN structures and nanowires with perfectly vertical sidewalls [152]. These chemistries do not target Ga-polar surfaces, such as the c-plane (<0001>) of wurtzite GaN and AlInGaN alloys, instead rapidly etching the $<10\bar{1}1>$ plane until the $<10\bar{1}0>$ plane is revealed, which is then more slowly [153]. This phenomenon can be applied to transform a nanowire with a normal, cone-like taper formed through dry-etch into transformed into a cylinder with perfectly vertical sides, without reducing its height. However, this process is not well studied for UV and DUV LEDs, and existing research has not applied this wet etching process to high Al-content

AlGaN nanowire structures for extended etch times [154]. In this work, high Al-content AlGaN nanowires are etched in a hydroxyl-based solution for up to 70 minutes. Etch rates and sidewall angle dependence on etch time are investigated in order to better understand the physical mechanisms responsible for formation of the inverse taper profile which has been observed for the first time in high Al-content AlGaN nanowires.

In this work an AlGaN DUV LED epitaxial stack emitting at 267 nm was grown using MOCVD on a sapphire substrate with a Ga-polar c-plane orientation. The resulting epi-stack for is shown in Fig. 125. A Plasma-Therm Apex ICP reactive ion etcher was used to form the AlGaN nanowires, which were patterned by a 250 nm thick Ni etch mask. The gas flow rates for the dry etch were 40 sccm of Cl_2 and 10 sccm of Ar at a chamber pressure of 30 mtorr. An ICP plasma power of 500 W and a forward power of 225 W were used to produce the desired nanowire geometry. 40% AZ400K photoresist developer (2% KOH by weight) was used for the hydroxyl-based wet etch, and was held at 80˚C for the duration of each etch. A thick layer of PDMS was used to peel the nanowires from the substrate and transfer them for testing.

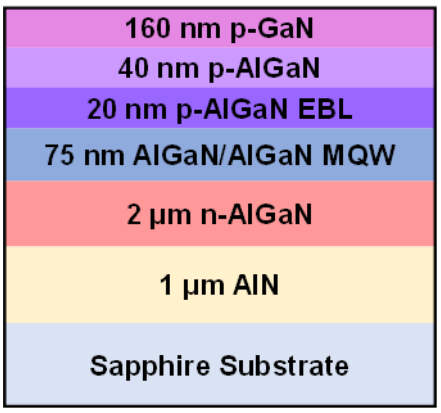

Fig. 125. DUV LED epitaxial layer stack.

The DUV wafer was first subjected to a solvent clean consisting of a 5 min immersion in acetone followed by a 5 min immersion in isopropyl alcohol, and a 5 min rinse in water. The wafer

was then coated with lift-off resist (LOR) and photoresist and patterning with 1 and 2 µm openings using laser direct write lithography. Ni was deposited with a thickness of ~250 nm and lifted-off, forming the Ni dots of the dry etch hard mask. Following hard mask patterning, nanowires with heights of ~1.5 µm were created with a Cl_2 plasma ICP dry etch. The initial nanowire etch profile produced by the ICP dry etch was approximately vertical. To study the effects of the AZ400K etching on the nanowires, 40% AZ400K in DI water at 80°C was chosen based on previous work with GaN LEDs which found this solution to produce smooth, vertical sidewalls in GaN nanostructures [152]. The wet etch was broken into steps, with SEM images taken after each step, in order to study the effects of etch time on the morphology of AlGaN nanowires. The sample was etched in the AZ400K solution for a total of 70 minutes with images taken at 5, 10, 20, 30, 50, and 70 min shown in Fig. 126. In stark contrast to work with visible nanowire LEDs, the DUV nanowires show a distinct undercut which increases with etch time, rather than maintaining a vertical sidewall profile independent of etch time. This undercut phenomenon was observed for multiple different samples with high Al-content. The etch is overtly crystallographic as evidenced by formation of a hexagonal axial cross section for all wires, but the selectivity of the wet etch against the various wurtzite crystal planes appears different for this high Al-content material. As with hydroxyl-based etching of GaN, the Ga-polar c-plane is unaffected by the etch. The wires do not increase in height as the etch progresses, and in instances where the Ni hard mask has lifted-off, the tops of the wires are not attacked by the etch chemistry. The Ga polar surface of the c-plane repels the hydroxyl groups, resulting in a negligibly slow etch rate, while the non-polar planes ($[10\bar{1}1]$) are readily etched.

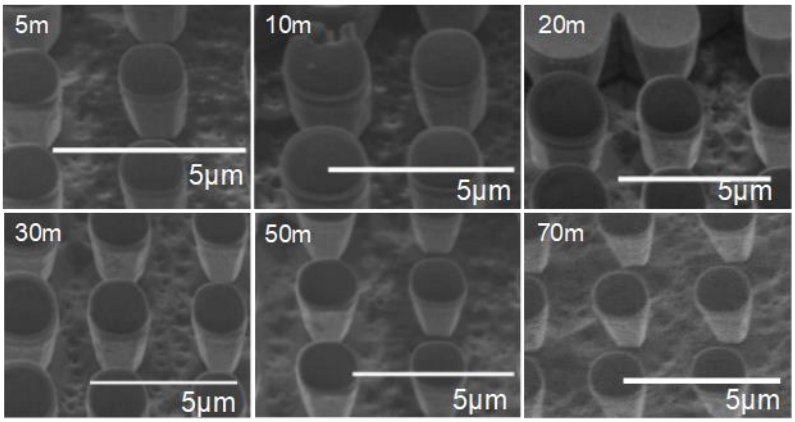

Fig. 126. SEM images of nanowires with top diameters of 2µm in 40% AZ400K at 80°C for between 5 min and 70 min.

The height, base diameter, and top diameter of the nanowires are used to find calculate the undercut angle. While the height and top diameter remain constant, the base diameter shrinks with increasing etch time. Fig. 127 displays the undercut angle as a function of etch. The undercut angle shows a semi-linear relationship with etch time, with an undercut angle of ~32°, realized followed a total of 70 min in the etch solution.

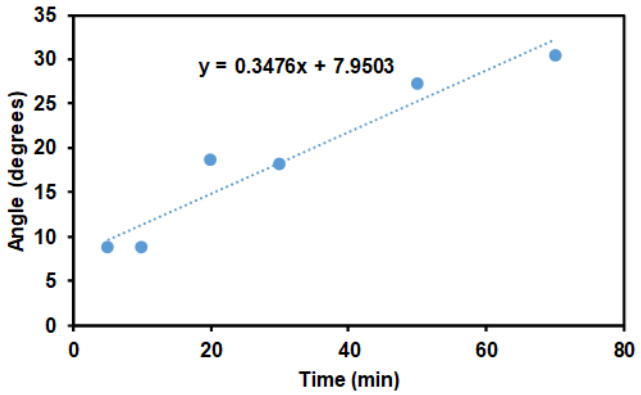

Fig. 127. Nanowire undercut angle as a function of etch time

Undercut angle was found to be independent of wire diameter for wires of the same height. As a result, wires with smaller top diameters appear to exhibit a larger undercut because the base diameter reduction caused by an undercut of any arbitrary angle accounts for a larger fraction of

their top diameter. Figs. 128(a) and 128(b) show nanowires following a 50 min etch with top diameters of 1.25 µm and 1 µm respectively. The undercut is more obvious for the smaller 1 µm wires, where the 50 min etch was sufficient to narrow the base diameter to a point, causing the wires to be "pinched off" and fall over.

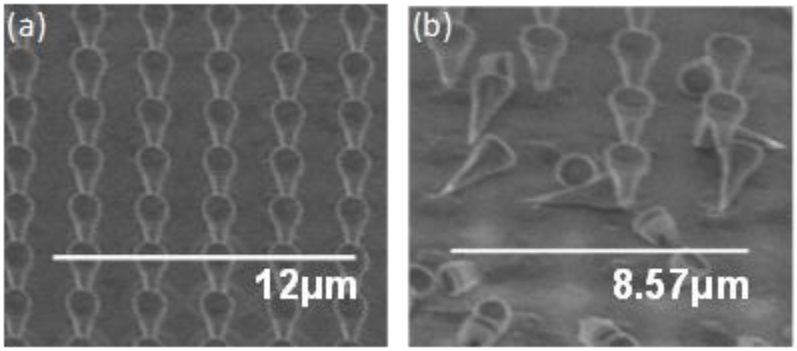

Fig. 128. (a) Nanowires with 1.25µm top diameters following 50min KOH etch, (b) nanowires with 1µm top diameters after 50min KOH etch.

The undercut and resulting inverse taper profile are caused by the polarity-selective nature of the hydroxyl based etch, with Ga polar surfaces repelling the hydroxyl groups while the N-polar, semi-polar, and non-polar planes are more easily etched. The relevant wurtzite crystal planes are shown in Fig. 129. The top surface of the nanowire is the Ga-polar <0001> plane (Fig. 129(a)), remains unaffected by the etch by repelling the hydroxyl groups in the etch solution. The ICP dry etch forms nanostructures with tapered sidewalls which expose the non-polar $<10\bar{1}0>$ plane. With conventional GaN LEDs an equal Ga:N ratio exists and a controlled etch peels back layers of this plane without altering the lithographically defined top diameter of the wire [153], allowing for formation of perfectly vertical sidewalls. The wet etch progresses according to a cavity model, which can be thought of as the inverse of growth [154-158]. Incorporation of the Al into the hexagonal crystal structure modifies the 1:1: Ga:N ratio, with Al atoms occupying Ga sites in the

crystal lattice. The hydroxyl-based etch must therefore overcome a larger energy barrier in order to remove Al atoms from the surface due to the Al-N covalent bond having a stronger binding energy (11.5 eV/atom) than the Ga-N covalent bond (8.9 eV/atom) [158]. In the case of AlGaN DUV nanowires it appears the initial plane approximation of the <10$\bar{1}$0> is etched to the <20$\bar{2}$1> towards the <10$\bar{1}$1> plane [157]. This novel inverse taper structure can be exploited to aid in removal of the nanowires from the underlying substrate.

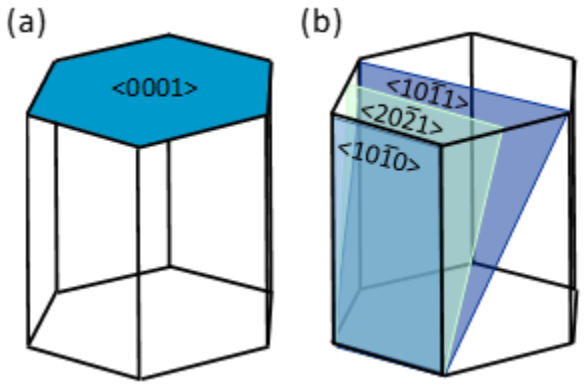

Fig. 129. (a) Wurtzite unit cell highlighting the <0001> surface, (b) highlighting relevant non-polar and semi-polar planes attached in AZ400K.

This novel nanowire morphology can be applied to aid in removal of nanowires from the substrate via a novel peeling process to enable flexible device applications. AlGaN nanowires with top diameters from 1.25 µm to 2 µm were subjected to a 70 min wet etch in 40% AZ400K at 80°C to produce an undercut of ~32°. Shrinking of the base diameter makes it easier to remove the wires from the substrate by reducing the cross-sectional area of the wire at the point at which it is mechanically separated from the substrate. In order to identify the prior location of the wires on the substrate following mechanical removal, a directional metal deposition is performed which leaves a circular “shadowed” area beneath the tapered wires. PDMS is used to remove the wires from the growth substrate due to its low cost, flexibility, and resistance to most wet and dry etch

chemistries. The PDMS is spin-coated onto the substrate and acts as both mechanical supporting layer for the nanowires as well as a flexible host substrate following removal of the wires from the growth substrate, as shown in Fig. 130.

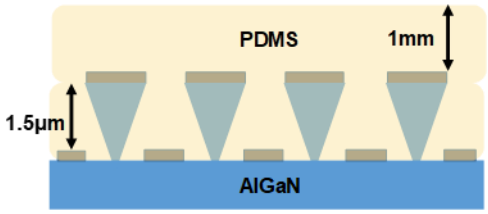

Fig. 130. Coated PDMS on the wet etched DUV nanowires.

After the PDMS is coated, the sample is cured at 90°C for 1 hour to increase the nanowire-PDMS adhesion and improve the mechanical stability of the PDMS film. The sample is then submerged in 100% AZ400K at room temperature to release the embedded nanowires from the host substrate. The AZ400K will not attack the PDMS or the AlGaN substrate, but slowly works its way along the interface between, delaminating the PDMS from the underlying AlGaN and further etching the bases of the nanowires. The narrow base diameters for the wires are further etched until the wires are nearly or completely removed from the underlying AlGaN. Were the nanowires not embedded in PDMS they would tip over onto the substrate, as shown in Fig. 128(b). The PMDS acts as a mechanical support layer, maintaining the orientation and relative positions of the nanowires. After the KOH etch is complete, the PDMS film can be peeled from the original substrate as shown in Fig. 131(a). The nanowires are completely removed from the host substrate by this process, with the openings in the metal film the only indication of their prior locations, as can be seen in Fig. 131(b). The bases of the removed nanowires can be seen sticking through bottom of the peeled PDMS film in Fig. 131(c). The peeled film exhibits exceptional flexibility despite containing thousands of rigid nanowires. Repeated flexing of the PDMS film does not

appear to disturb the location and orientation of the embedded nanowires or damage the nanowires in any way. AZ400K etching is found to be critically important for successful removal of the nanowires from the substrate. Without the extended AZ400K etch to delaminate the PDMS from the substrate and further reduce the base diameters of the nanowires, it is not possible to remove the nanowires using this method. The mechanical shear force applied to the wires by peeling the PDMS film from the substrate is not sufficient to break the wires off of the substrate. This novel AZ400K etching and PDMS peeling process enables removal of very short nanowires from the substrate without the damage incurred by conventional mechanical exfoliation techniques. As the nanowires are fully removed from the substrate without leaving broken stubs, it is possible that the expensive AlN growth substrate can be reused, reducing the overall cost of this process.

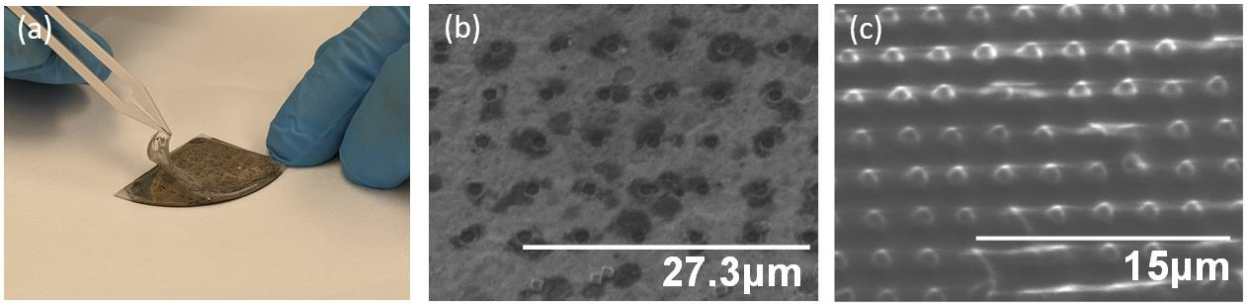

Fig. 131 (a) Peeling PDMS film with embedded wires, (b) surface of growth substrate showing metal at base of the wires, (c) backside of PDMS showing wires sticking out.

Optical characterization of the nanowires was performed before and after removal from the substrate in order to examine the effects of the peeling process on the light emission properties of the wires. Fig. 132 shows the PL spectra of the nanowires before and after the peeling process. Distinct emission at 292 nm is observed from the nanowires embedded in the PDMS host substrate, indicating that the nanowires are intact and confirming that the PDMS film is transparent to DUV light. In addition to its flexibility and chemical inertness, PDMS exhibits a low absorption

coefficient across the DUV emission range and an index of refraction of n=1.46 which aids light extraction from the nanowires [159]. A slight broadening of the emission spectrum and blue-shift of the peak emission wavelength is observed following removal of the nanowires from the substrate as shown in Fig. 132. Prior to removal, the nanowires showed a peak emission wavelength of 267 nm with a linewidth of 11 nm. Following removal from the substrate the nanowires show a peak emission wavelength of 292 nm and a linewidth of 36 nm. In addition to this 25 nm redshift and 25 nm increase in linewidth, the nanowires show a significant increase in longer wavelength emission following removal from the substrate. This can be longer wavelength emission can be attributed to measurement noise and luminescence of the PDMS film. Nanowires removed from their growth substrate are expected to show this behavior, with redshift and broadening of the emission peak caused by reduction of the quantum confined stark effect (QCSE) [160-161]. Lattice mismatch induced strain causes powerful piezoelectric polarization electric fields to develop in the QW active region which raise the electron and hole ground states further from their respect band edges, blue-shifting the emission wavelength of the primary exciton transition. Removal the nanowires from the substrate reduces this strain, reducing the internal electric fields in the QW and flattening the energy bands in the quantum wells, red-shifting and broadening the emission spectrum by moving the electron and hole ground states closer to their respective band edges. Once the nanowires are removed from the substrate they can either be transferred to an alternative substrate (and the PDMS removed via dry etch) or remain embedded in the PDMS which can act as a virtual, flexible substrate, enabling development flexible DUV LEDs.

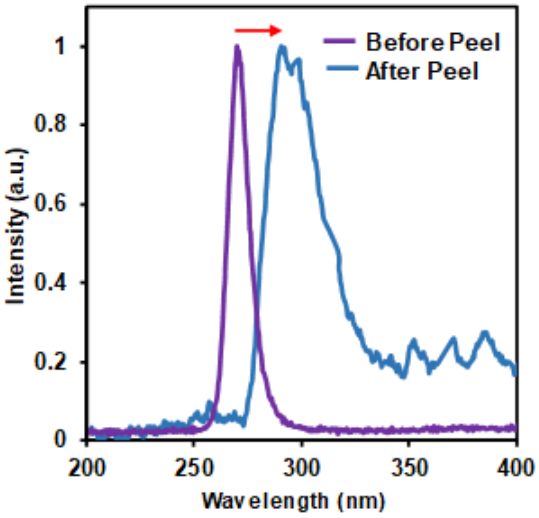

Fig. 132. PL spectra before and after substrate removal.

The work presented here introduces both a fabrication process which can be used to form high Al-content AlGaN nanowires with an inverse taper and a novel peeling process enabled by these nanowires which can be used to reliably remove them from the substrate. The time-dependent effects of a conventional hydroxyl based crystallographic wet etch on the morphology of high Al-content AlGaN nanowires, specifically the undercut angle, was studied. Undercut angles of ~32° were obtained after 70 min in 40% AZ400K at 80°C. The formation of this undercut can eventually lead to complete removal of the nanowires from the underlying substrate as the etch progresses. This undercut enables a unique PDMS peeling process capable of removing the nanowires from the growth substrate while maintaining their orientations and relative positions. Nanowires removed from the substrate and embedded in PDMS show a 25 nm redshift in peak emission wavelength due to a reduction of the QCSE through strain relaxation. Following further development, this novel nanowire peeling process could enable both unique flexible light emitting devices as well as high yield nanowire transfer processes.

- **Future Device Optimizations**

With these initial steps developed, flexible nanowire device can be readily manufactured. Future work is related to the realization of flexible device manufacturing. After successful peeling of the GaN nanowires followed by a quick etch of the PDMS, backside metallization can then be performed to contact the AlGaN portion of the nanowire. Sputtering is to be utilized for the backside metal connection to the nanowire, as conformal deposition is required to coat the sidewalls of the nanowire to avoid contact only to the AlN. After the backside of the nanowires is metalized the devices can be contacted for electrical testing. The issue, however, is that the top ITO contact is buried under 30 µm of PDMS. The initial process flow theorized is shown in Fig. 133, where the backside metal is put unto a host substrate and the PDMS is etched. Etching back of 30 µm is a slow process, where stopping the etch on the 6 µm PDMS film is difficult. Even if the etch is perfectly timed such that the etching is stopped once the ITO is uncovered, the thin layer of PDMS remaining is no longer mechanically stable. The flexibility of the resultant device is dependent on the flexibility of the host substrate. During the thick PDMS etch back, the loss of mechanical stability led to the film flexing during the plasma process that would lead to non-uniformities during the dry etch.

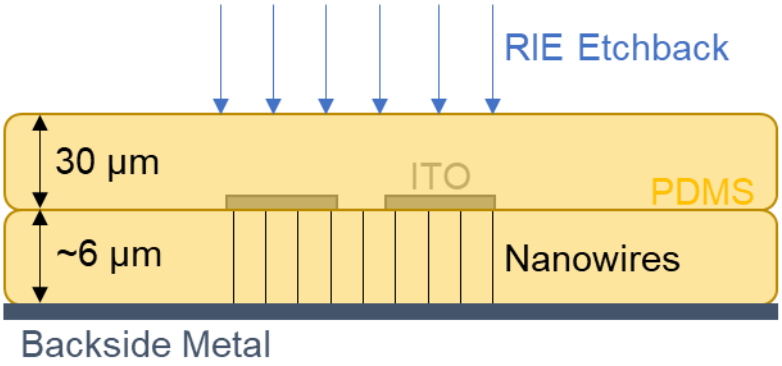

Fig. 133. Theorized initial process flow for GaN flexible nanowires.

Instead, a revised process flow is presented in Fig. 134. In this process flow, once the backside metal is patterned, photoresist is then coated and patterned to etch the backside metal such that only the backside metal remains over the devices. Aluminum as a choice for the backside metal would provide a hard mask for a fluorine based dry etch. A PDMS dry etch of the thinner ~ 6 µm film is then formed in order to etch down to the ITO film. In contrast to the previous approach, an over etch in this design is tolerable. The thicker PDMS film is maintained, allowing for the flexible nature of the device to be maintained. As 30 µm of PDMS no longer requires etching, the top layer of PDMS can be made thicker for increased mechanical stability. Light in this presented process flow would be backside emitted through the thicker PDMS film. As PDMS has high optical transparency, there would be little absorption. The refractive index of PDMS has a value of 1.4, while the GaN nanowires have a value of 2.5. Grading of the refractive index through these materials should significantly aid in the light extraction from the device. The backside metal can also serve as a mirror, reflecting photons back towards the PDMS and out of the device. The only concern with the presented process flow is that the peeled PDMS after backside metallization should be made flat for even photoresist coating. Increased top layer thickness of PDMS can be utilized for added mechanical stability for this step. Flexible nanowire device can provide a number of both novel applications, as well as improve upon the existing applications for flexible planar LEDs.

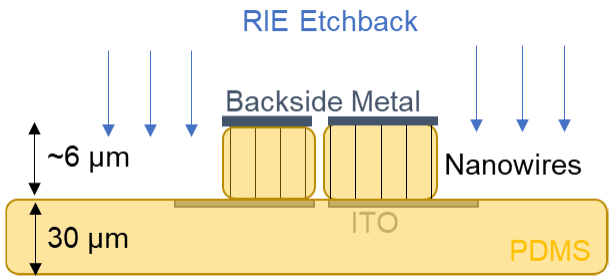

Fig. 134. Theorized improved process flow for GaN flexible nanowires.

4.4 Color change LEDs

Regardless of the type of µLED display, red, green, and blue colors are each needed. These three primary colors can be utilized with color mixing to create any color of the visible spectrum. While black matrix material is filled in around each µLED to provide true black when the pixel is off [162]. The conventional pick-and-place approach to µLED displays relies on the separate fabrication of wafers each with a single LED color [21]. With separate InGaN/GaN LED wafers for blue and green, and GaAs based wafers for red. The separate colors mean increased fabrication costs and increased complexity to ingrate these three different types of LEDs. Monolithic integration for µLED displays instead relies on the use of color converters such as QDs or nanophosphors, to convert higher energy blue into green and red [163]. Use of color converters allows for a single LED material system, and correspondingly lower manufacturing costs. Though color converters do not have 100% conversion efficiency and can lead to lost performance. There are also concerns with the volume of color converted needed, as µLED size further decreases. The ideal solution would be to implement a monolithic architecture for lower cost and higher performance, yet still have all three LED colors.

Research groups have recognized the importance of monolithically integrating all three LED colors and there have been recent works on the topic. For the III-N materials system, the wavelength of emission is determined through the indium % in the InGaN/GaN MQWs. Blue LEDs are ~10% indium, green LEDs ~20%, red LEDs ~40%. The research challenge has been incorporating > 20% indium. Indium concentration for red emission reaches solubility limits at GaN growth temperatures, along with issues of high lattice strain [164]. The low temperatures needed to increase solubility lead to numerous point defects, and self-segregation [164]. Initial attempts to incorporate high indium concentrations have then lead to poor EQE and a large internal

band bending caused by strain [168]. Nanowire growth shows the potential to form multi-color LEDs, through tailoring the diameter of the nanowires to incorporate different levels of indium [165]. Nanowires allow for greater indium incorporation due to the strain relief and edited growth mode, where larger diameter wires incorporate more indium [166]. Though only axial and not radial nanowires can be utilized, due to the worse solubility of indium with non-polar planes. Bottom-up growth represents yield issues and a general incompatibility with current semiconductor processes or architecture. The promise of low defect densities in nanowires is also not readily realized. Alternatively, there has also been work done introducing europium (Eu) into the lattice which acts as an optical mid-gap state [167]. Comparatively high efficiency is achieved over high planar indium incorporation, though still remains lower than desired [167]. Multi-color growth can be done to form blue, then green, then Eu-doped red LEDs on top of each other, where selective etching is used to fabricate full color. Eu remains a rare element, that is questionable in terms of large-scale manufacturing and performance.

Each of the available options creates some level of sacrifice which is non-ideal for large scale commercial manufacturing. Instead, monolithic multi-color LEDs are investigated and demonstrated without increased planar indium or Eu doping. Bias voltage and corresponding current modulate the LED emission from ~640 nm down to ~425 nm, spanning the visible spectrum, Fig. 135.

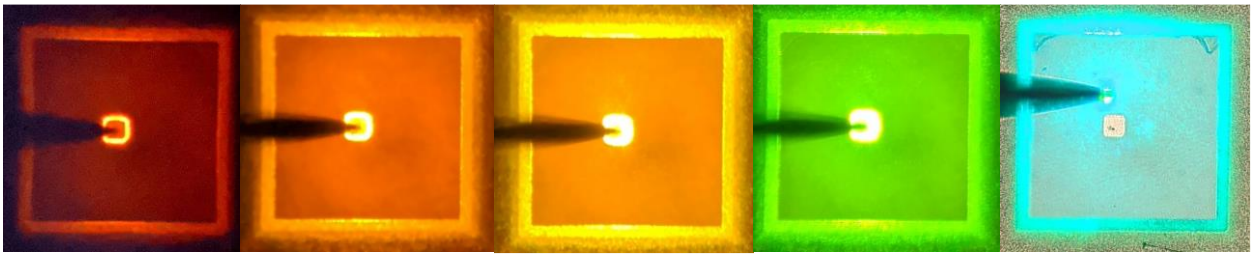

Fig. 135. Single GaN LED showing color change with applied bias and current.

A reverse engineering investigation is performed in order to determine the mechanism behind multi-color emission that was discovered from material thought to be a conventional green LED. Where the mechanism can be understood and exploited in future devices. For fabrication, the LEDs were defined with a photoresist hard mask and ICP etching to a depth of 445 nm. Standard n-type metallization was done through lift-off, depositing Ti/Al/Ni/Ag 10/150/30/100 nm. The p-type contact was deposited through lift-off, making use of a 30 nm film of Ni. Testing of these LEDs reveals a current density dependence on color emission, instead of the expected green color emission. Conventional green LEDs are shown to have relatively stable emission from low to medium current densities, with a slight shift and dual peak formed a high current density due to population of the first excited state [169]. The provided growth stack for the green LED is shown in Fig. 136.

Fig. 136. Provided green LED layer stack.

The color shift is shown by the EL data in Fig. 137 for a 40 µm LED. At low bias corresponding low current density, the red emission is observed at a peak of ~640 nm and a FWHM of ~50 nm. As the current increase, emission shifts to higher energy, seeing the color shift from

red to amber, orange, yellow, green, and blue. The corresponding current to achieve the various colors are listed in Fig. 137. Increased current corresponds to a change in brightness for the sample, where the blue has much stronger intensity than red. Interestingly, the FWHM seems to be relatively constant at ~50 nm, and the emission curves do not seem to strongly overlap, where the blue and red emission are distinct. The blue emission is achieved through both shifting the main peak to higher energies, and through the generation of a secondary peak at 425 nm.

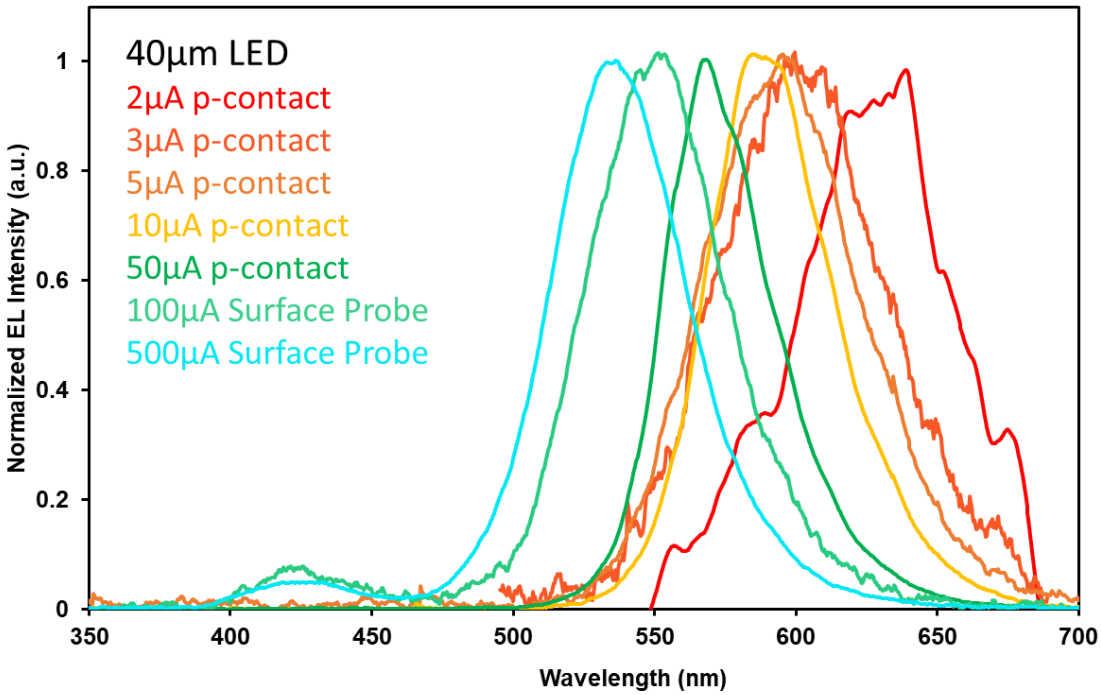

Fig. 137. Single 40 µm LED EL spectra vs. applied current and corresponding band bending.

Even though blue emits more strongly than green or red, this effect can be compensated for with tailoring the sizes and number of the individual LEDs. The important aspect is the total efficiency of emission from these colors. The relative EQE is extracted for each emitted color and corresponding current, listed in Fig. 138 for a 500 μm^2 LED. The peak EQE is at ~200 µA, corresponding to green emission, where these LEDs were thought to conventionally emit at. At low current of ~15 µA for red emission, the EQE is at a lower, but viable, relative EQE of ~20%.

At high current above 200 µA for blue emission, the efficiency drops in part due to efficiency droop. Though Fig. 138 only account for the primary emission peak, and at higher current the second peak appears which would lead to slightly higher EQE values.

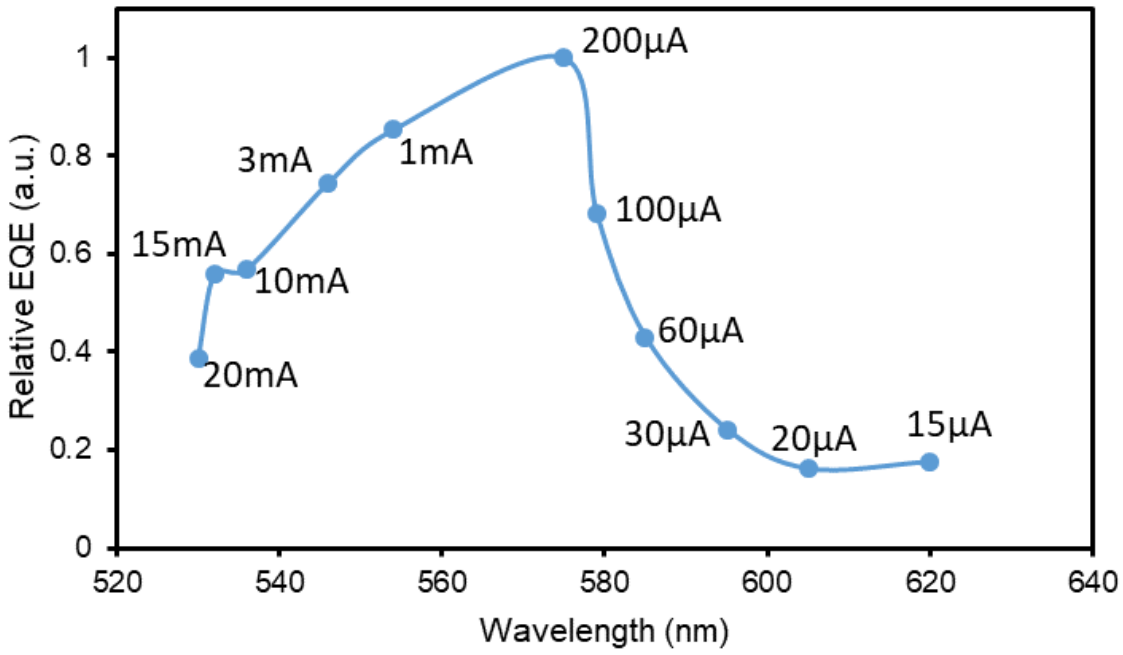

Fig. 138. Relative EQE vs. wavelength at various currents for a 500 µm^2 LED.

The raw current to the device does not fully capture the phenomena, where it is better expressed in terms of current density. Different sized LEDs were tested, making use of the same driving current of 10 µA. Results from these size tests are shown in Fig. 139, with Fig. 139(a) showing the near field microscope images and Fig. 139(b) showing the normalized EL intensity. Several key points can be drawn from the presented data. First, the current density is higher in smaller devices compared to larger LEDs. This leads to a blue shift, where the 40 µm^2 LEDs emit yellow light, while larger 500 µm^2 emit red. The two smaller LED sizes of 40 µm^2 and 75 µm^2 share approximately the same current density and have similar contact sizes, leading to similar emission. The second key finding is that sizes greater than 200 µm^2 saturate with red emission

peaks at ~640 nm. Where the optical step causing the emission leads to an energy of 1.94 eV and does not emit into the infrared.

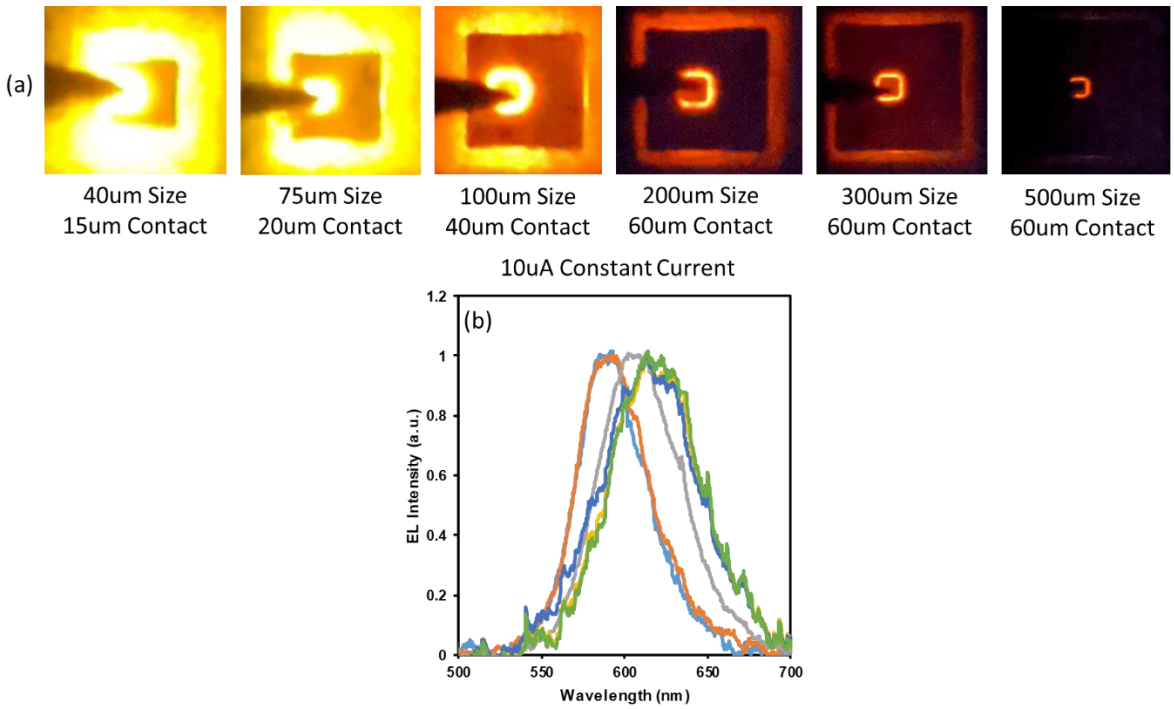

Fig. 139. (a) Near-field images of color change with current density, (b) corresponding EL spectra for a fixed current of 10 µA.

Comparison between the color change LED and a conventional green LEDs is done at low (15 µA) and medium (200 µA) current levels using near field imaging to compare emission characteristics. Fig. 140 shows the results with the low current on the right and medium current level on the left for each. In the conventional green LED case at both injection levels there appears to be decent current spreading with stable green emission. There are dots that appear brighter in each case, where these correspond to indium clusters, where there is a slight increase of indium leading to a lower turn-on voltage in these spots [169]. Similar slight indium fluctuations can be observed in the color change LED under medium current injection, though such spots are not visible at low injection. Where it can be thought that the planar InGaN MQWs are generating the green emission similar to a standard LED, though the mechanism behind the red emission is

distinct. The color change LED also exhibits worse current spreading, with most light generated around the central p-contact, with emission also observed escaping out the sides. Both p-type contacts rely on a simple Ni deposition which makes a slight schottky contact to the p-type GaN.

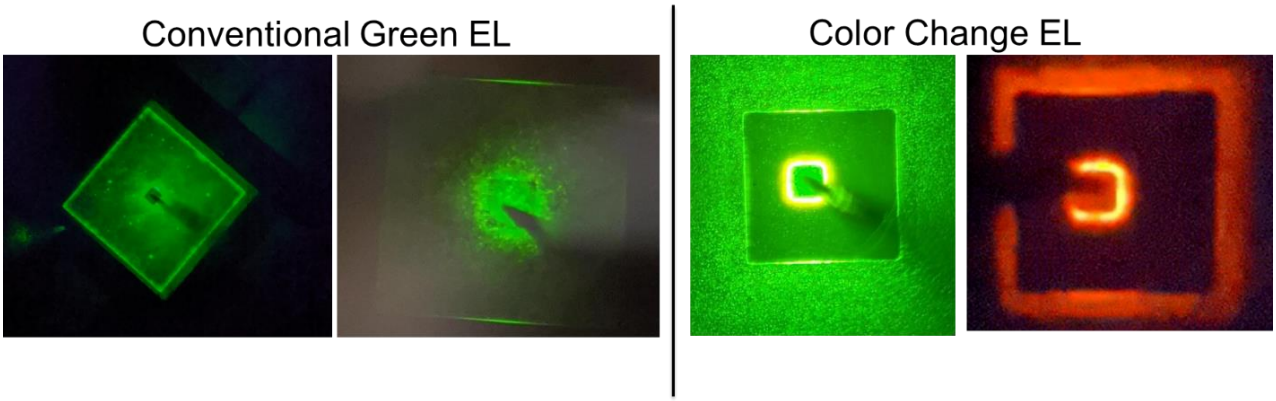

Fig. 140. Near field optical images of convention and color change green LEDs at differing currents.

To further look at the performance of the color change LEDs, electrical characterization is presented in Fig. 141 (a-b). Fig. 141(a) shows the log of the current vs. voltage for the color change LED, where conventional operation is recorded. Fig. 141(b) records the linear I-V, where a turn-on voltage is recorded at ~2.4 V. The turn-on voltage is around what is expected from a green LED, where the turn-on voltage is expected to be around the bandgap energy. The p-type contact is also not annealed, which could lead to an additional voltage drop experienced by the structure. The electrical characterization does not show excessive leakage or results which would be unexpected from an InGaN/GaN green LED.

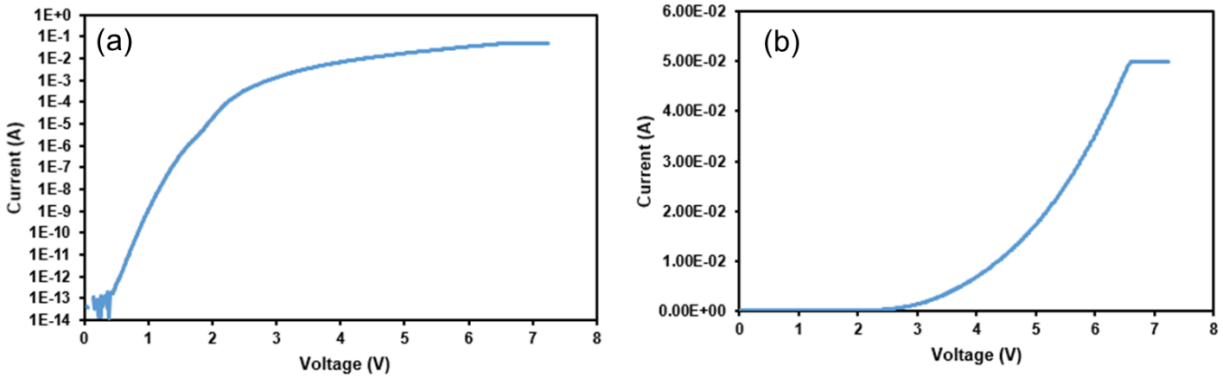

Fig. 141. (a)Log I-V for color change LED, (b)Linear I-V for color change LED, both from 200 μm^2 device.

Besides the electrical results, the optical aspect of the color changing nature, however, differed significantly from the expected behavior of a conventional LED, with findings not seen or previously reported. Photoluminescence (PL) measurements were taken of the sample in order to get an initial idea of the origin of the multi-color emission. A 325 nm UV light source was utilized for photoexcitation, with the emission collected at a 45^o angle from the sample. Results of the PL measurements are shown in Fig. 142 with a reference conventional green LED. The reference green LED shows a much narrower full width at half maximum (FWHM) of ~30 nm, in comparison the color change LED has a wider FWHM of ~100 nm. Peak emission wavelengths are also different between the two samples, with the green LED at 525 nm and the color change at 560 nm. Similar to the high current results in Fig. 137, Fig. 142 shows that the color change LED has an additional peak at 425 nm while the green LED does not.

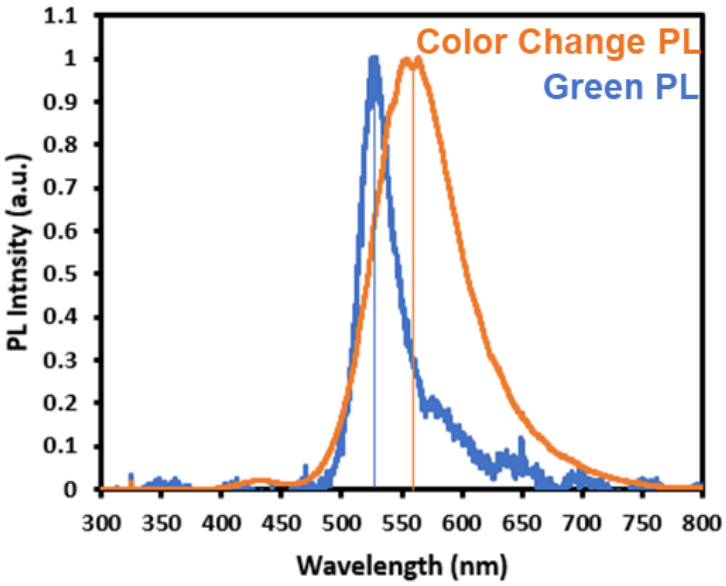

Fig. 142. PL intensity of color change LED and reference green LED.

For further reference, a conventional green LED grown on double side polished (DSP) sapphire is studied with PL. Both frontside and backside optical pumping is performed and shown in Fig. 143. When standard frontside optical pumping is done, a narrow line width green emission peak is observed, like Fig. 142. However, when the backside is optically pumped, a broad peak is collected, just like the color change LED, though with the absence of the 425 nm peak. The backside pumping is thought to optically excite defects that exist in the initial growth near the GaN-sapphire interface.

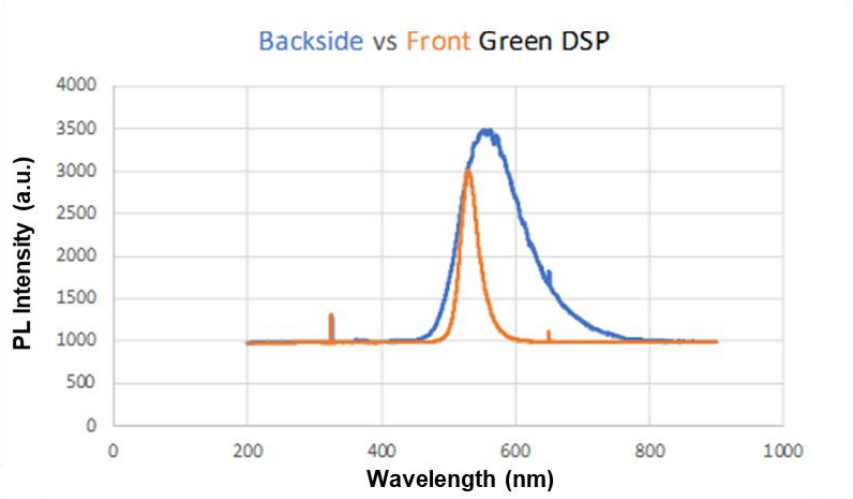

Fig. 143. PL intensity backside and front side pumped green LED on DSP sapphire.

The spread of the emission and peak wavelength recall the yellow (YL) band emission common to standalone GaN films. The YL peak is commonly thought to be caused by vacancies, particularly Ga vacancies [170]. This theory is consistent with the recorded results in Fig. 143. As further evidence, an additional PL spectrum is taken for a u-GaN film. Each of these recorded spectra are plotted together with a reference curve from literature in Fig. 144 [170].

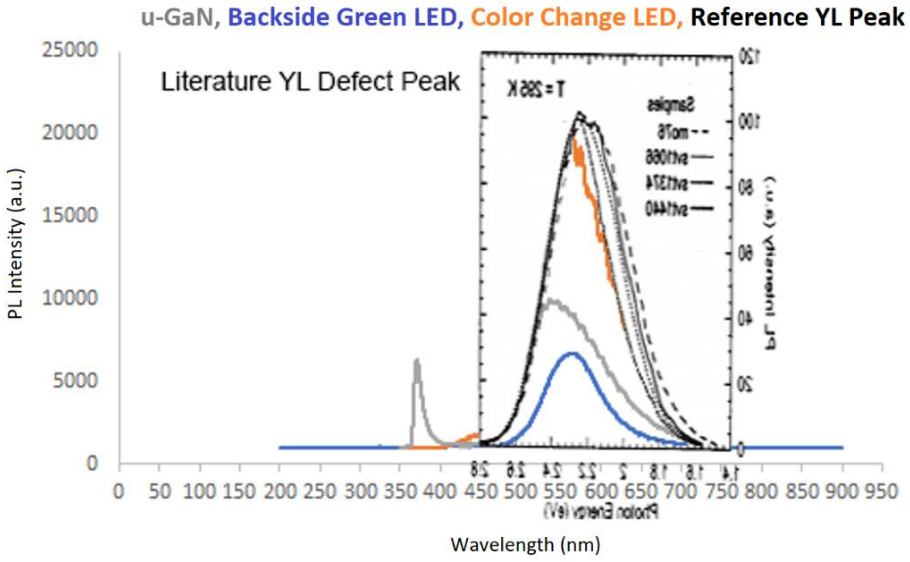

Fig. 144. PL intensity of u-GaN, backside green LED, color change led, and referenced YL peak.

Optical recombination states from the defect band leading to emission can be further broken up into three sub-bands, the red (RL) band, the YL band, and the green (GL) band [171], Fig. 145. Commonly the entire defect peak band is referred to as the YL band given the dominance, though these sub-bands are very important to distinguish here. These bands have debated causes with the RL band being attributed to a dep level acceptor, the YL band attributed to Ga vacancies, and GL band attributed to mid-gap states [170]. Conventionally these peaks only appear in PL measurements of u-GaN where recombination occurs in the GaN, in a full LED structures the recombination occurs in the MQW region. Once electrons and holes are generated, thermally or optically, they eventually recombine radiatively or non-radiatively after a certain time. With a layer of just u-GaN, electrons and holes populate mid-gap states and recombine, leading to the optical defect band shown in Fig. 144. In an LED structure with a forward bias, these electrons and holes diffused into the MQW region to recombine, leading to a dominant emission profile. Where the lifetime of electrons and holes are long enough to diffuse into the wells, rather than recombining in the GaN. There are few instances of EL injection of these bands. One publication by Lee et al., utilizes a p-n junction grown on top of an LED to modify carrier injection, which produced a similar broad defect spectrum [172]. Holes in GaN have a low diffusivity, where it was found that there was recombination occurring in the defect band of GaN, alongside emission from the MQW region [172].

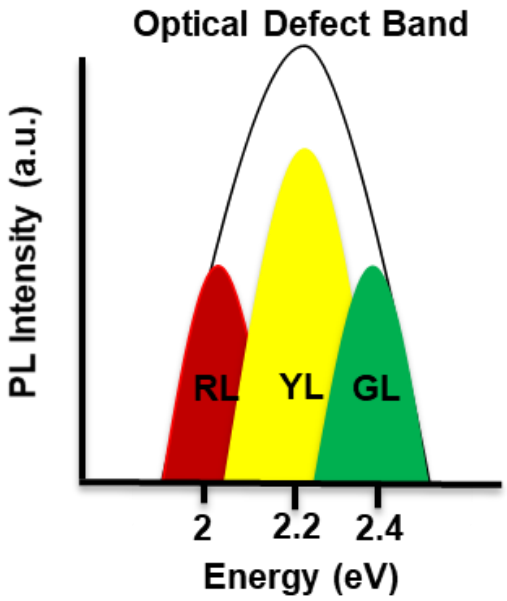

Fig. 145. Optical defect band composed of RL, YL and GL sub bands.

The color change LED was found to produce similar overlap to the defect peak, though additional PL is utilized to determine the origin of the signal. Instead of illumination at 325 nm, 405 nm light was utilized with both the u-GaN and color change LED, Fig. 146(a-b). In Fig. 146(a) the u-GaN sample shows only the 405 nm laser peak, where defects are not able to be pumped by sub-bandgap light [173]. In contrast QWs can be pumped by wavelengths with energy below the barrier, but above the bandgap of the QWs. These results show for the color change LED in Fig. 146(b) where the peak is still observed, indicating emission from the MQWs instead of GaN point defects. The alignment of the color change LED with the defect peaks appears to be coincidental.

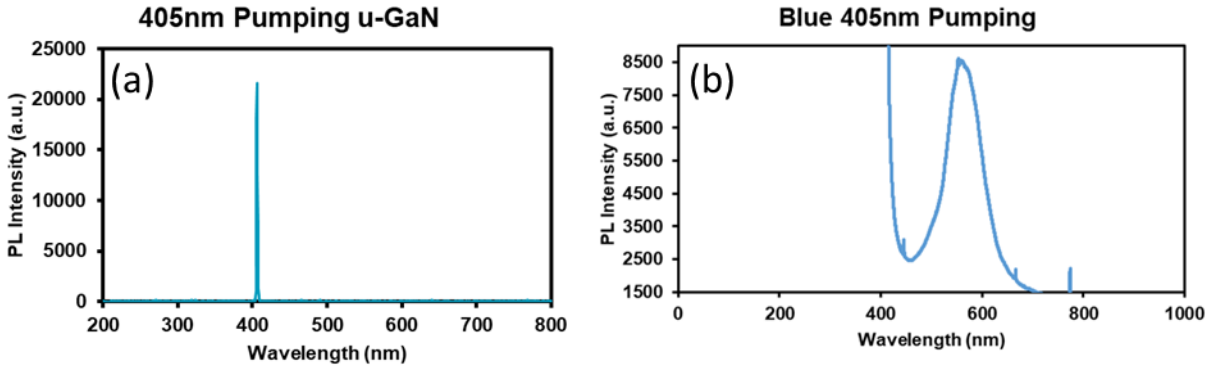

Fig. 146. (a)405 nm pumping of u-GaN layer, (b)405nm pumping of color change LED showing emission from QWs.

Additional confirmation is found through the variation of optical power in PL pumping of the u-GaN and color change LED samples. The idea that there are a limited number of defects can be exploited in order to separate the bandgap induced signal from the defect signal. Increasing the laser pumping power will lead to diminishing emission gain of the defect band, as these states fill up with carriers [173]. Beyond a point, further increases of pumping power lead to increased emission from the band edge of the material [173]. Fig. 147 showcases this where measurements were taken at different powers. The defect peak centered at 550 nm is seen to increase and presumably saturate, while the GaN band edge peak at 365 nm shoots up from microscopic levels.

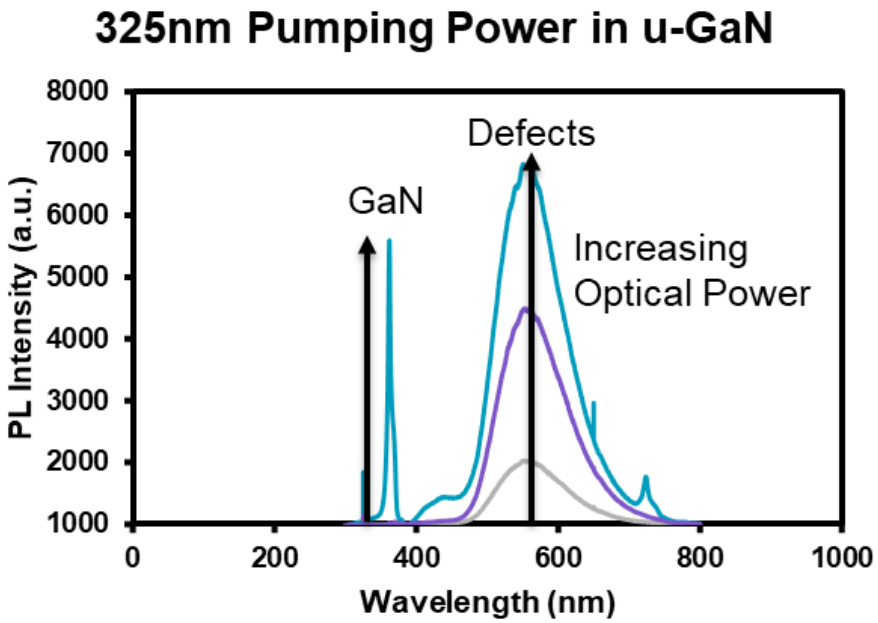

Fig. 147. Increasing optical power showing saturation of defect peak with increase in GaN peak.

Due to the limited number of defects, saturating behavior in the optical emission vs. power is expected. In contrast, the emission from the GaN band edge or MQWs will instead lead to a linear dependence. A 405 nm light was utilized as the photon source, where the light was positioned at different distanced from the sample in order to modulate optical power. The 405 nm light will only excite the MQW region and not the defects. Fig. 148 records the results of this, showing a linear dependence with distance, which is inversely proportional to power in this case. A linear trend is observed indicating the mechanism of light generation is due to the band edge in the MQWs.

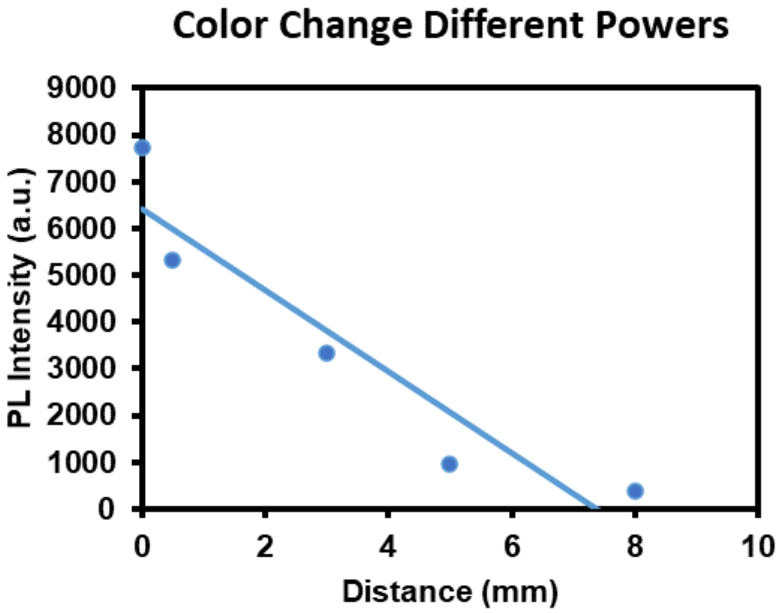

Fig. 148. Color change LED sample optically pumped at 405 nm at different distances leading to different effective optical power levels.

In order to investigate the cause of the broad emission, additional material analysis is performed. A focused ion beam (FIB) was utilized to prepare a lamella for transmission electron microscopy (TEM), as shown in Fig. 149. The lamella is a vertical slice from the LED, pictured above the extraction spot is the p-contact in Fig. 149. In conjunction with high resolution TEM imaging, secondary ion mass spectrometry (SIMS), energy-dispersive x-ray spectroscopy (EDS), and cathode luminescence (CL) techniques are performed.

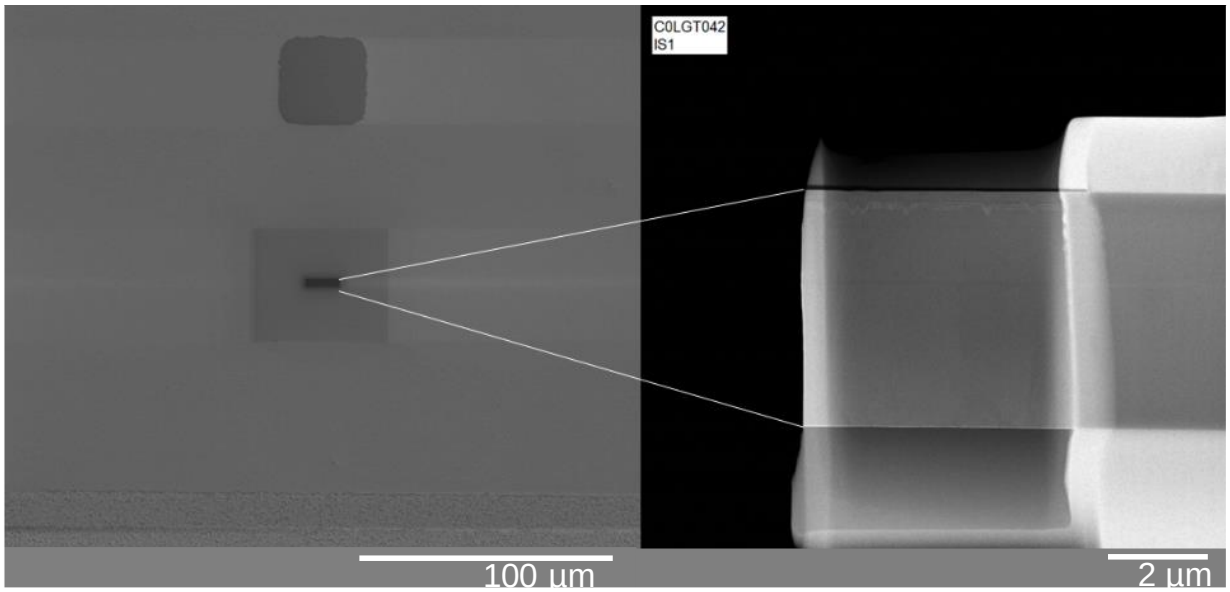

Fig. 149. PL intensity of u-GaN, backside green LED, color change LED, and referenced YL peak.

The SIMS results are first delved into in order to provide an initial check on the structure. SIMS is performed on both a conventional green LED for reference and the color change LED, Fig. 150(a-b) respectively. Note that the SIMS results provide relative though not absolute values around concentrations. Fig. 150(a) shows the conventional green LED with InGaN MQWs and a lower indium content InGaN-GaN super lattice for strain relief. The results seem to match up with what is provided as the growth structure in Fig. 136. While both should be the same structure, the color change LED in Fig. 150(b) is shown to be completely distinct. Of note, the color change LED has aluminum that has been incorporated into the structure, though also in unexpected ways. A thin p-AlGaN layer is often incorporated after the MQW to minimize electron overflow, though the additional instances are unexpected. There exists a p-AlGaN layer separately inserted into the p-GaN, which can induce added resistance. There is also an AlGaN layer inserted 350 nm below the MQW region which could be for potential strain relief. Then it appears at a depth of ~1.75 µm, an AlGaN-GaN super lattice is utilized to minimize defects between the buffer and active layers.

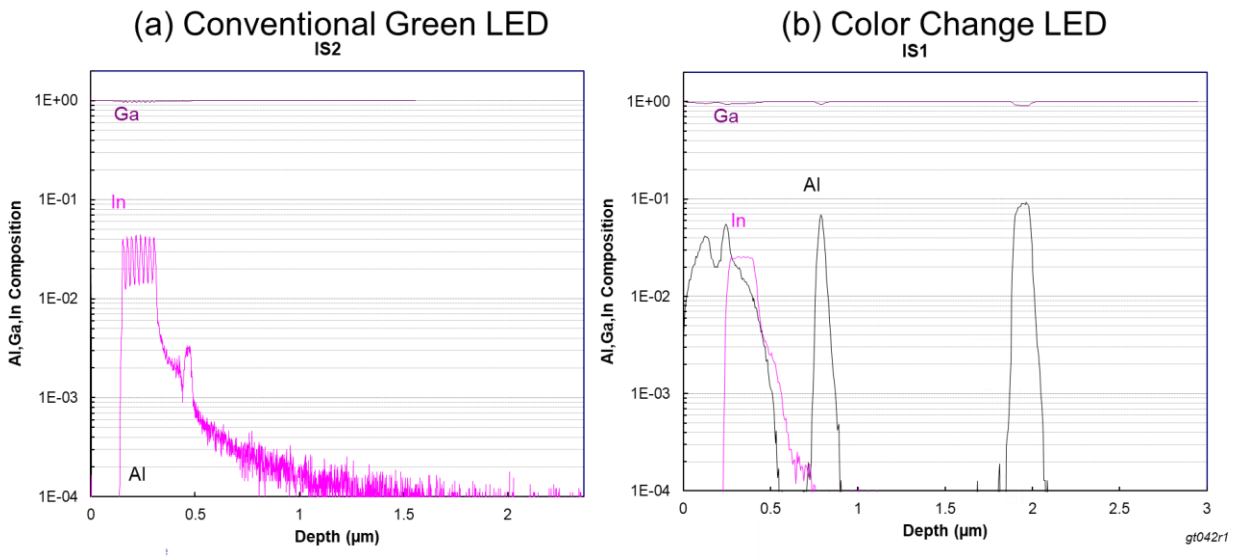

Fig. 150. (a)SIMS of conventional green LED, (b)SIMS of color change LED.

The SIMS results of the color change LED also show InGaN-GaN MQWs, like the reference green LED. The resolution of the detector is a bit worse for the color change LED, due to the additional detection of the aluminum signal, where the individual wells are not resolved. To investigate the sample a bit more TEM imaging is done. Fig. 151 ties the SIMS results to what can be observed through the TEM. Different atomic concentrations and makeups show up at different contrast levels due to the number of electrons and how the beam interacts. Therefore, the differing layer concentrations are visible, where the AlGaN appears darker and the InGaN appears brighter than GaN, Fig. 151. The depth and different contrasts can then be utilized to directly tie the images together. Distinct AlGaN regions are visible as well as distinct InGaN MQWs, verifying that the resolution of the SIMS was limited, and not that there existed a continuous InGaN layer.

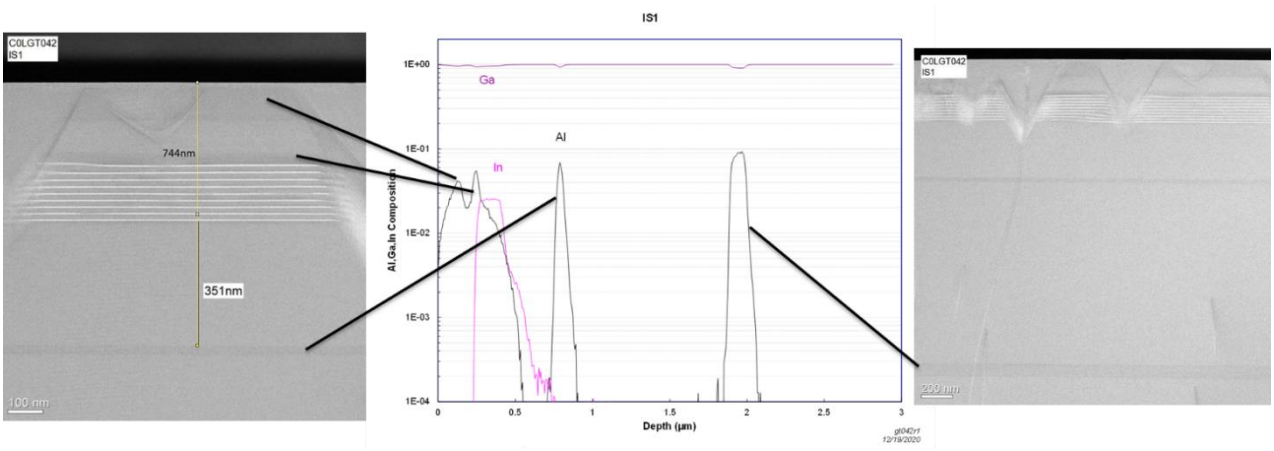

Fig. 151. SIMS of color change LED matched up with corresponding TEM images.

The TEM images of Fig. 151 also show V-groove defects that are present. V-grooves are V-shaped defects that terminate screw dislocation as can be seen by Fig. 151. The V-grooves are composed of $\{10\bar{1}1\}$ crystal facets that form a V-shape, where the angle is 62º from the c-plane direction. These are common defects which appear in GaN based LEDs. The V-grooves are one of the reasons GaN LEDs are so efficient despite high levels of defects. The V-grooves bend the QWs forming semi-polar wells; these wells are reported to contain less indium and be filled in with AlGaN [174-175]. The compositional differences form an energy barrier preventing electrons and holes from non-radiatively recombining in the screw dislocation [174-175]. The lower indium content has a wider bandgap compared to the higher indium content in the conventional wells, minimizing recombination in or around the screw dislocation. These reported results are reinforced here, where Fig. 152 shows negligible indium incorporation in the V-grooves, while the aluminum still forms a p-AlGaN layer in the region. This is also consistent with the difficulty in indium incorporation with non-polar or semi-polar substrates, due to differences in the indium sticking coefficient [176].

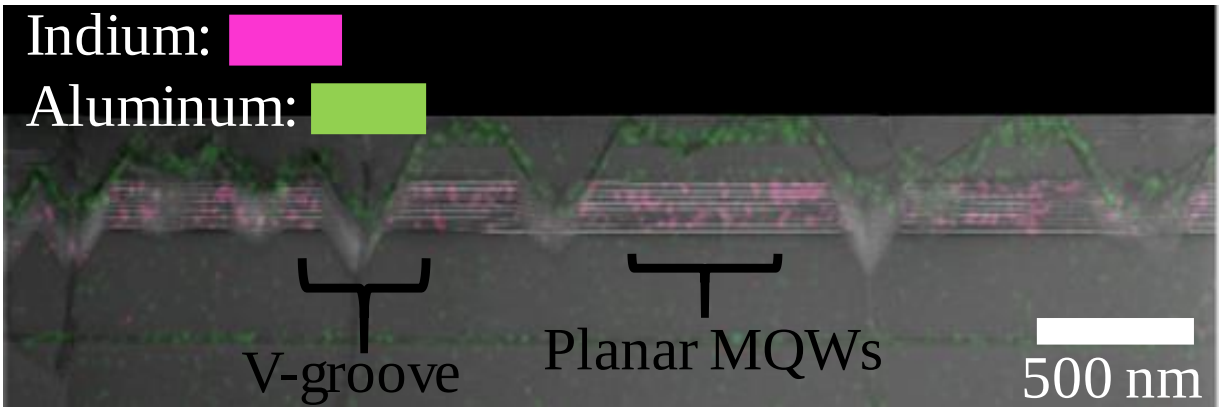

Fig. 152. Color change LED V-grooves with In and Al incorporation shown.

From Fig. 150(b) it appears that the color change LED has a large aluminum tail from the EBL into the MQW region. EDS and TEM images are taken around the MQW region, Fig. 153. Mappings of indium in pink and aluminum in green are overlaid with the TEM image in Fig. 153. The indium forms continuous QWs and the aluminum is located only in the EBL. These findings indicate that indium clusters are not the cause of the recorded red emission, and that the aluminum is not diffusing in the MQWs to impact emission. SIMS is sampled from a larger area, averaging the results. The aluminum tail is most likely caused by the V-grooves and not a continuous distribution in the MQWs. The indium and aluminum composition of the EDS scan are also plotted in Fig.153 normalized to the Ga composition. The aluminum in the EBL is found to be 5% which is typical for use to minimize electron overflow. It is found that the indium in the QWs is ~18%, which is the same for the reference LED. The exception is the middle QW which has an indium concentration of ~10%. The middle QW could be the cause of the 425 nm emission peak at high current injection levels, which comes into play after the above wells are filled.

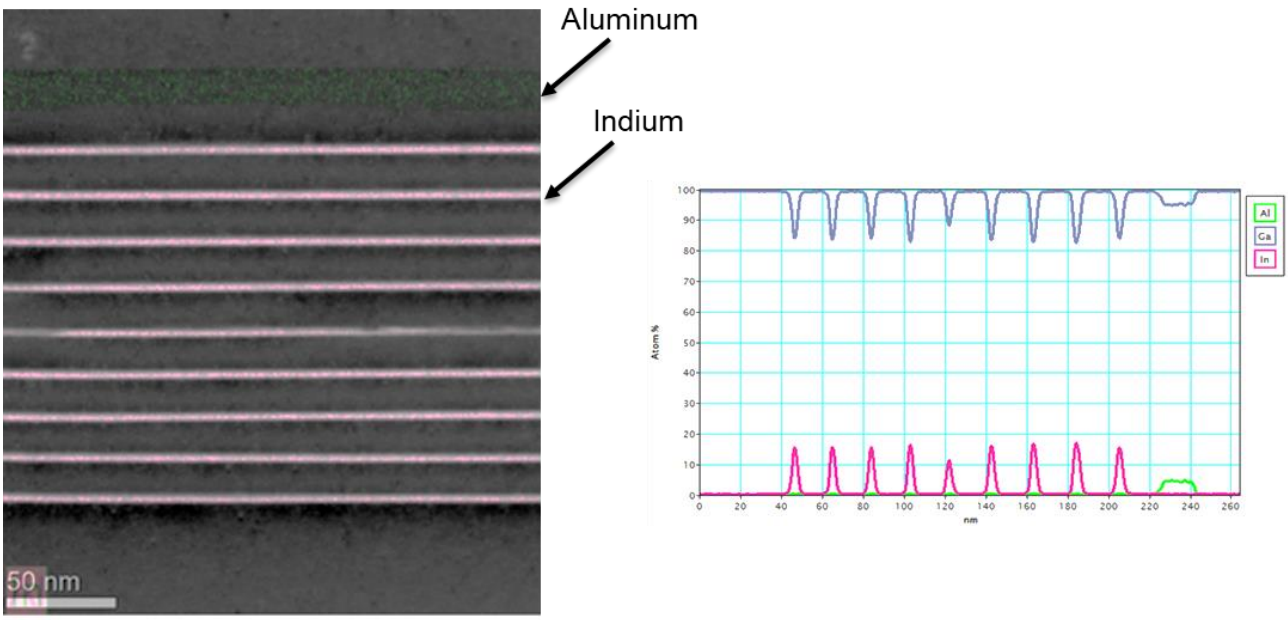

Fig. 153. TEM of MQWs for color change LED with map and composition.

Lattice strain is known to facilitate band bending through the QCSE, red shifting the emission wavelength. To investigate strain as a possible cause, high resolution TEM images are taken of the AlGaN layer located beneath the MQW region, Fig. 154. A fast Fourier transform (FFT) is applied to the image in order to convert from direct space to view the reciprocal lattice, Fig. 154. A high degree of crystallinity is observed from the reciprocal lattice, where each point represents a crystal plane. The c-plane is selected, which is the dot below the center, and converted back to direct space in order to extract the plane spacing "d". The value of d is found to be the same at 2.63 Å, leading to a lattice parameter "a" of 3.04 Å. There is a slight discrepancy with the reported value of 3.16 Å, which is attributed to measurement errors. The AlGaN layer is thin enough that at the current composition it should be strained to that of GaN, which is why both regions produce similar plane spacings. Inclusion of AlGaN would also reduce the lattice constant further, leading to a reduction in the QCSE when combined with InGaN QWs. Therefore, it is unexpected that QCSE is severe enough to lead to such a significant red shift for these LEDs.

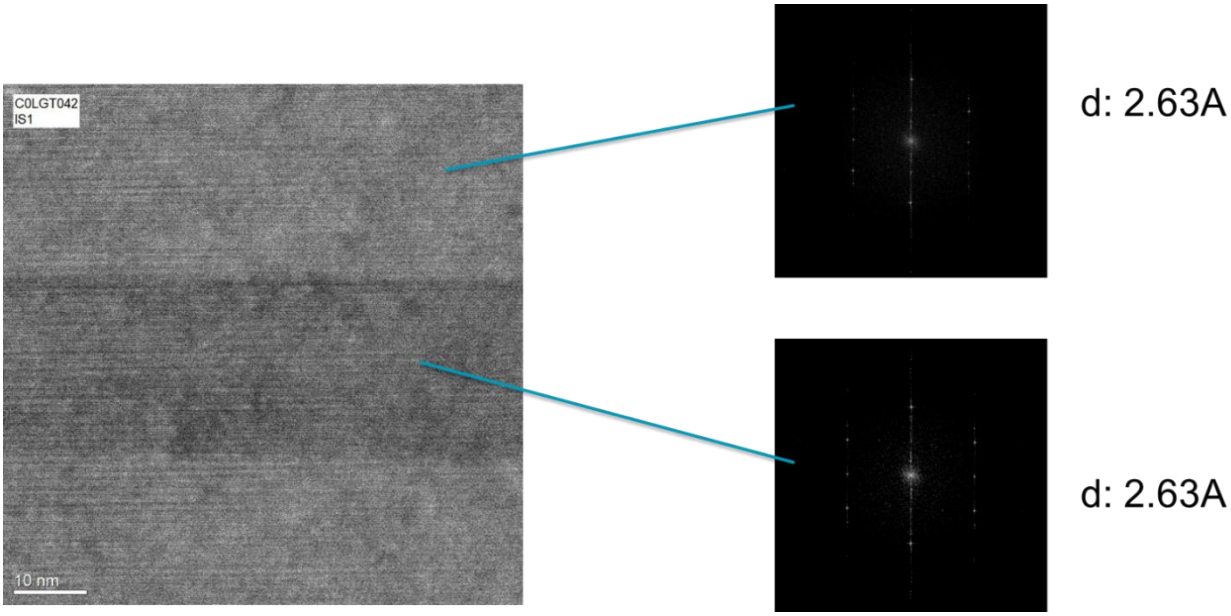

Fig. 154. Direct view and reciprocal space of AlGaN and GaN layer 350 nm under the MQW region.

CL measurements are performed on the TEM lamella at 10K. Due to the reduced thickness provided by the ~25 nm thick lamella, less internal electron scattering occurs, increasing resolution of the signal. Though limitations still exist, as visible light is on the order of 500 nm, while the quantum wells are 3 nm. An overview of the results are shown in Fig. 155 with the identified peaks. The peak positions are blue shifted due to the sample temperature of 10K. Multiple peaks are detected, leading to complex signal. These peaks though are located through the visible spectrum, from blue to green to red. The V-grooves also showcase bright emission, which will be investigated in more detail.

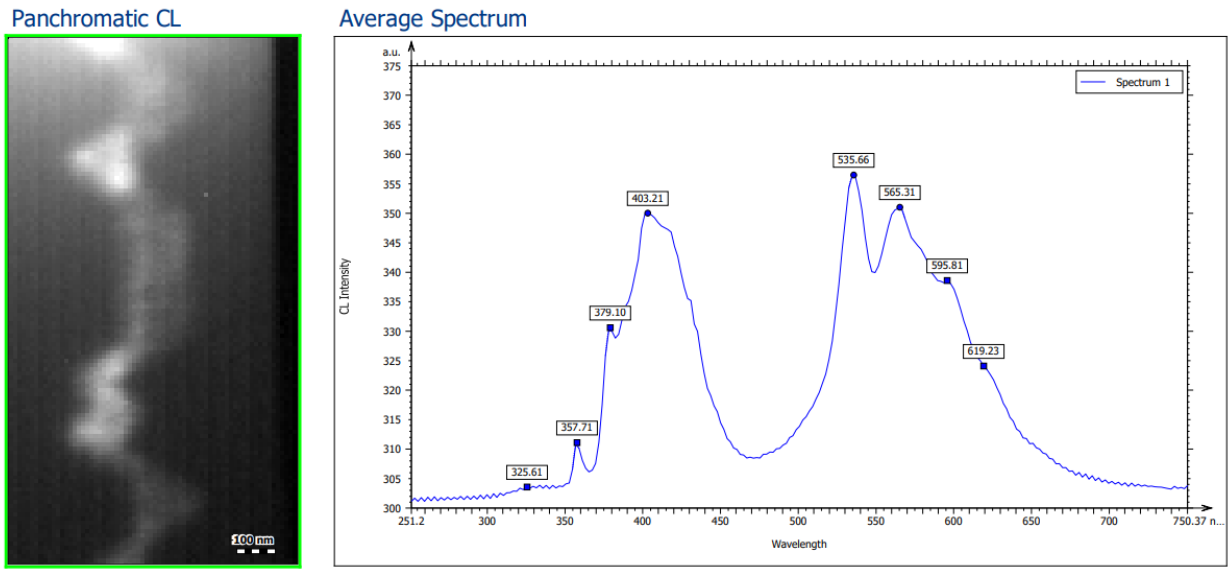

Fig. 155. Panchromatic CL and spectrum with peaks identified.

High resolution images are taken and overlaid with the CL signal in Fig. 156. Interesting that in this sample, the center of the V-grooves shows a high level of emission instead of a dark spot associated with non-radiative recombination in the screw dislocation. This could be due to the AlGaN filling and potentially being incorporated in the vertex. Recent findings by Yapparov et. al, suggest the importance of V-grooves and positives inclusion [175]. The width of these V-grooves is also large at 225 nm to 250 nm, leading to further efficiency enhancement compared to smaller V-grooves [174]. Blue emission appears to be emanating from V-grooves, potentially leading to the 425 nm peak at higher injection levels recorded in Fig. 137. This is consistent with the wells being thinner and incorporating less indium due to the semipolar plane. The relative position of the QW also makes a difference, where the lower wells show shorter emission than those higher up. Comparing MQWs, it appears the upper QWs are slightly red shifted, with the main peak going from 530 nm to 540 nm. This shift could be due to reduced polarization from reduced strain or hydrogen diffusion into the top QWs, neutralizing the polarization charges.

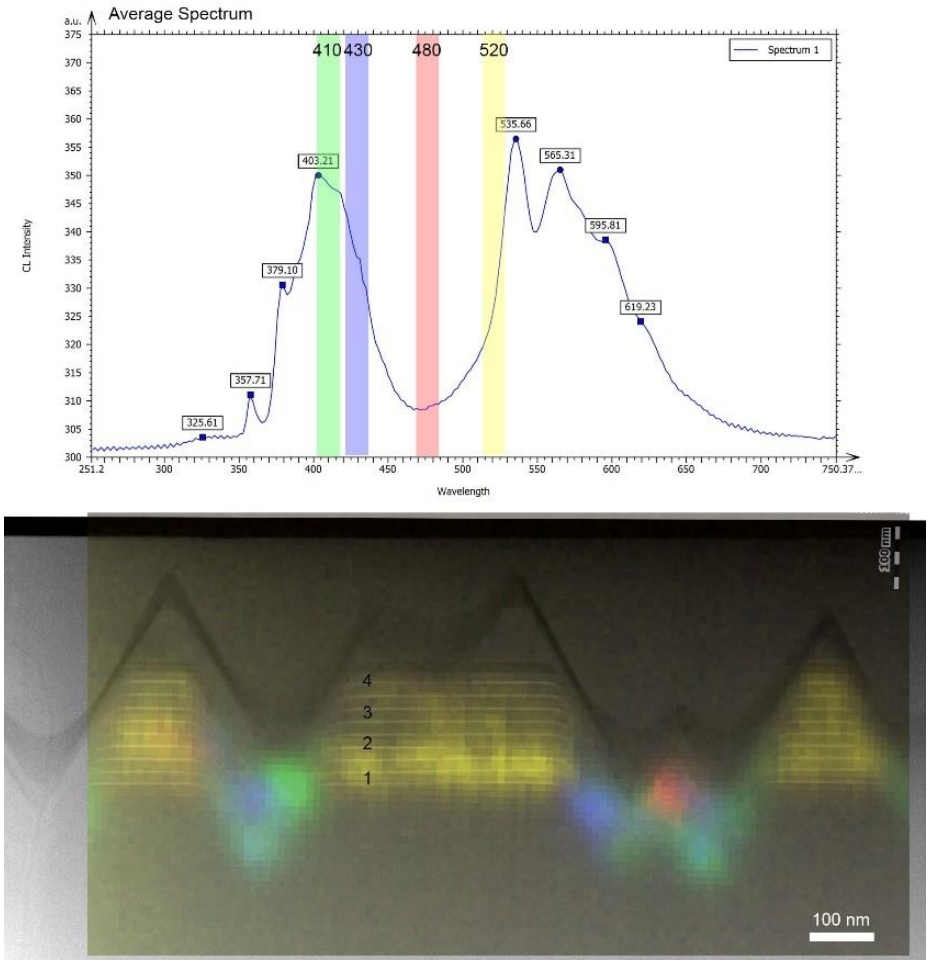

Fig. 156. Plotted spectra of TEM with CL signal

In order to further look at the variation in the MQWs, distinct regions are sampled. Fig. 157 shows the mapped CL emission from points of interest, including near a V-groove and the MQW region away from any V-groove, with the whole CL signal on top. The region near the V-groove is seen to be the source for the multi-color emission particularly in longer wavelengths. With peaks located at ~425 nm, 535 nm, 565 nm, 595 nm, and 619 nm. The emission is not expected to come from the non-polar planes, but from the regions nearby. The lack of indium in the QWs is compensated by with indium rich regions nearby [175]. As the V-grooves are formed due to surface depressions caused by threading dislocations, they act as strain relief, allowing

higher indium composition nearby for efficient red emission [175]. In contrast the MQWs CL signal away from the V-groove shows conventional green emission at 535 nm, with a possible first excited state emission, or emission from the middle quantum well.

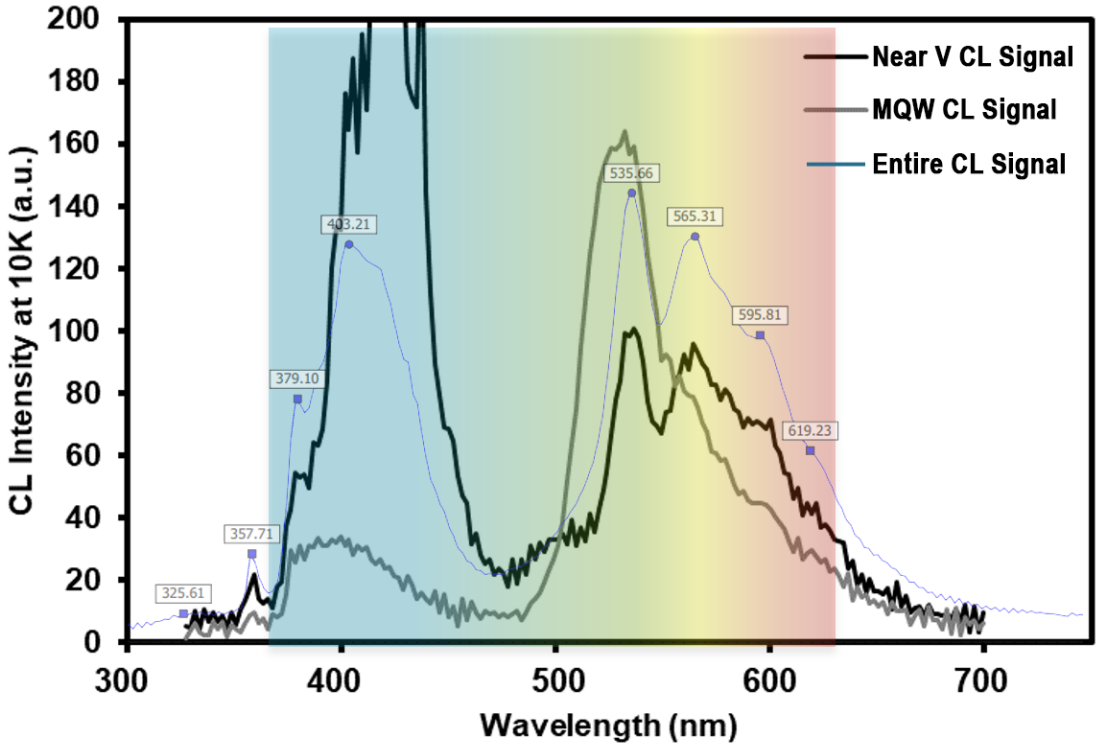

Fig. 157. Mapped CL of points of interest.

From the lamella the color change LED appears to have a very high density of V-grooves, facilitating the longer and shorter wavelength emission. The formation of the V-grooves could be further facilitated here due to the lack of underlying strain relief layers [174]. These V-grooves are exploited for efficient multi-color operation with localized strain relief. On a separate sample, hydroxyl-based etching is done, in order to highlight the V-grooves, where these regions etch while the conventional c-plane remains untouched [51]. An LED mesa with the hydroxyl etch is shown in Fig. 158. The V-grooves are estimated to be in excess of 4 x 10^8 cm^{-2}, though it is difficult to estimate the exact number due to extended defect density observed in Fig. 158. Ideally a high

number of a V-grooves is desired for scaling application and increased uniformity. Though too many V-grooves lead to a loss of active area, relative to the current injection benefits.

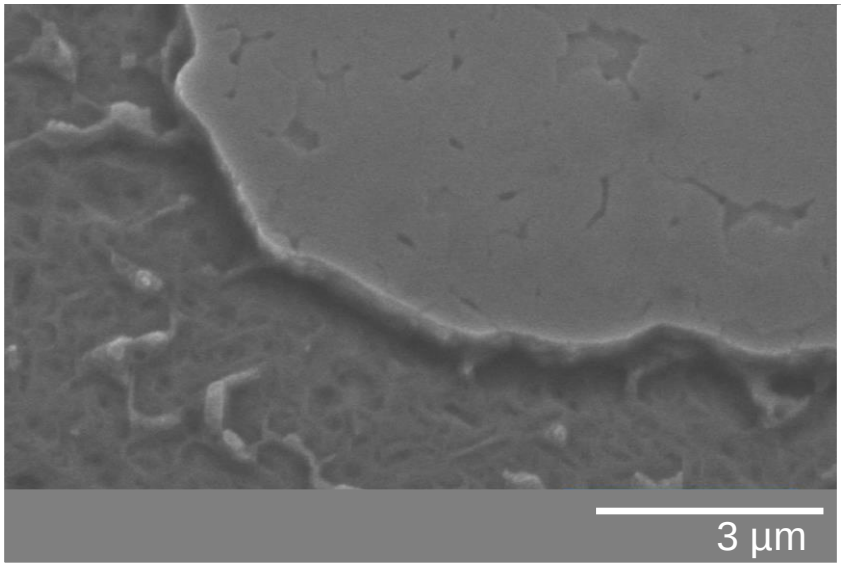

Fig. 158. Hydroxyl based etch of color change LED.

The multi-color emission is due to the incorporation of the V-grooves as the source of the longer wavelength and blue emission in the structure. The V-grooves provide lateral injection, which allows for further hole injection, increasing efficiency. These injected holes first populate indium rich areas, then indium poorer areas, combined with the vertical injection providing green and blue emission, Fig. 159. Less of a barrier exists for V-groove hole injection due to the semi-polar vs. c-polar plane [177]. At low injection current the increased indium quantum wells near the V-grooves populate first from laterally injected holes. As current and voltage increase further, carrier screening blue shifts the emission towards orange and yellow. At medium injection levels the top green QWs populate from lateral and vertical hole injection, giving off green emission like a conventional LED. With higher biases, carriers can overcome barriers to recombine around the V-grooves and in the middle QW potentially, leading to blue emission. Simultaneously, the QWs experience further carrier screening, leading to a further blue shift [169].

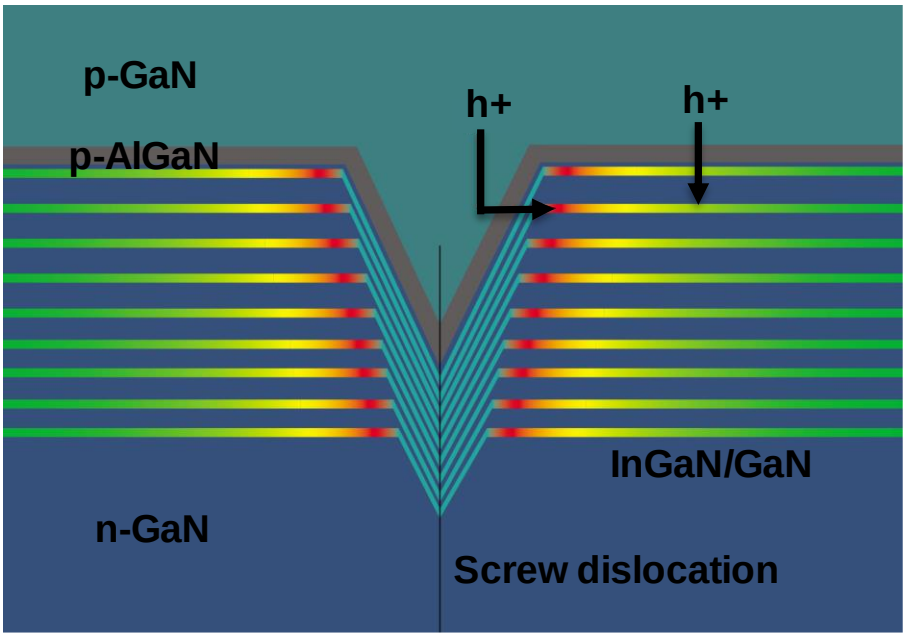

Fig. 159. Injection from non-polar V-groove and vertical injection.

The EL emission at blue, green, and red are plotted together on a CIE chromaticity diagram, Fig 160. For display purposes, three separate LEDs would be utilized in this monolithic format to create each pixel. Clear are pure red emission is obtained through emission at 640 nm with a relatively narrow FWHM of ~50 nm. Where the FWHM impacts the perception of the eye along with the peak location, particularly for red emission [178]. Distinct green emission is observed, though there is some variability on position which can be selected due to the dependence of wavelength on current. These three points can be utilized to reproduce any color within the triangle, spanning the color gamut. The plotted triangle represents about 25% of the visible spectra the human eye can see. Having these three points leads to the full rainbow of emission, though lacking the full depth of the blues and purples. Additional optimization of the blue emission would greatly expand the coverage. Importantly though, the white light center is contained within triangle, where a combination of these three colors can be utilized.

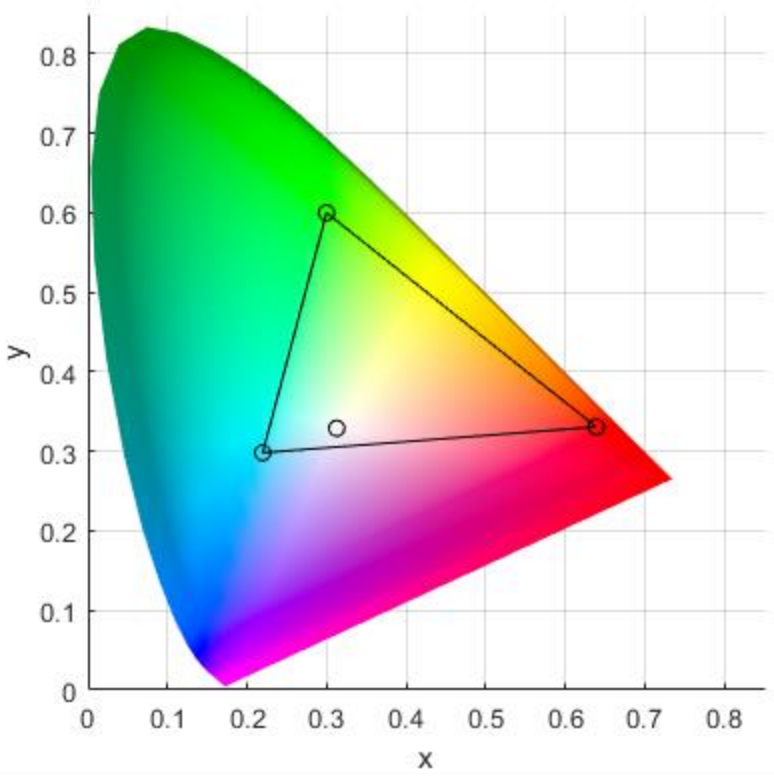

Fig. 160. CIE chromaticity diagram with plotted primary colors from color change LED.

There can be enhancement engineered to boost the green point higher on the CIE chart though further current manipulation, where the blue is mixed in with the green. The blue emission at high current is intermixed with a shifted green emission peak, leading to a light blue color. Engineering of additional V-grooves, band bending though a non-ohmic p-type contact, editing the MQW region, shrinking the LED size, or blocking the green emission are all approaches which can shift the blue emission point to lower values. Of which, shrinking of the LED size is the easiest to accomplish, where band banding further reduces QCSE, the V-grooves are less likely to be incorporated, and the increased current density populates higher energy states.

To demonstrate the effect of LED size dependence on green to blue emission, green nanowire LEDs with diameters of about ~1 μm, which were previously fabricated, were utilized. These nanowires are designed to emit green light, with MQWs containing 18% Indium. Fig. 161(a)

shows the results at µAs of current flow, though comparatively high current density due to the small diameter. Initial green emission changes to a clear blue when the current is increased, due to energy band bending and excited state filling. Fig. 161(b) shows one of the nanowires after formation and before metallization or spacer dielectric deposition. These nanowires are approximately 6 µm tall, though the nanowire format is not necessary for the color shift. Lower aspect ratio LEDs can be similarly utilized, as the diameter not the height is important.

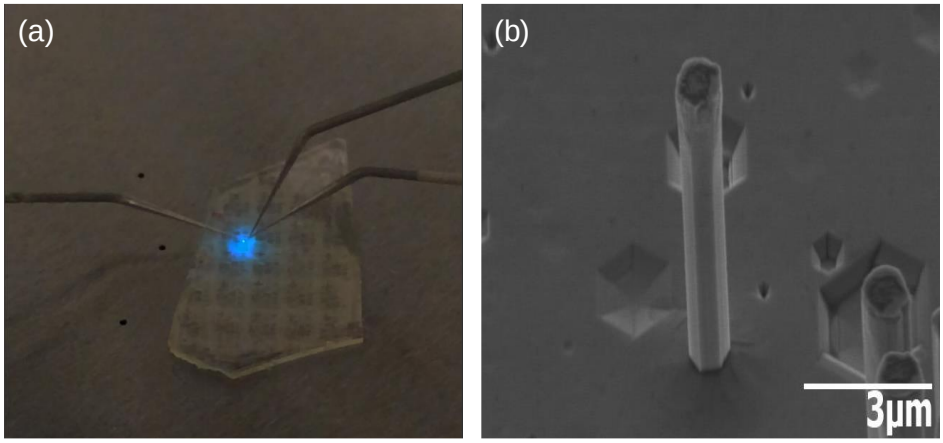

Fig. 161. (a) Multiple green nanowire emitting blue under high current density, (b) nanowire before fabrication.

The result of shrinking the diameter of the LEDs is found to be able to shift the emission possible to shorter wavelengths. Though similarly at low current the emission peak will not reach longer wavelengths due to the lack of V-grooves. Diameter reductions allow blue light is also able to be achieved at lower current values, which allow better matching to the green and red emission. The effect of smaller sizes in shifting the blue emission peak can be seen by the added points to the CIE color chart in Fig. 162(a). The outer most color triangle making use of small diameter LEDs for blue emission almost perfectly matches with the sRGB color space which is the color space utilized for online sites and content, Fig. 162(b). Therefore, when making use of the V-

groove structure, smaller diameter LEDs can be fabricated in addition to larger diameter LEDs for the realization of full color displays and beyond.

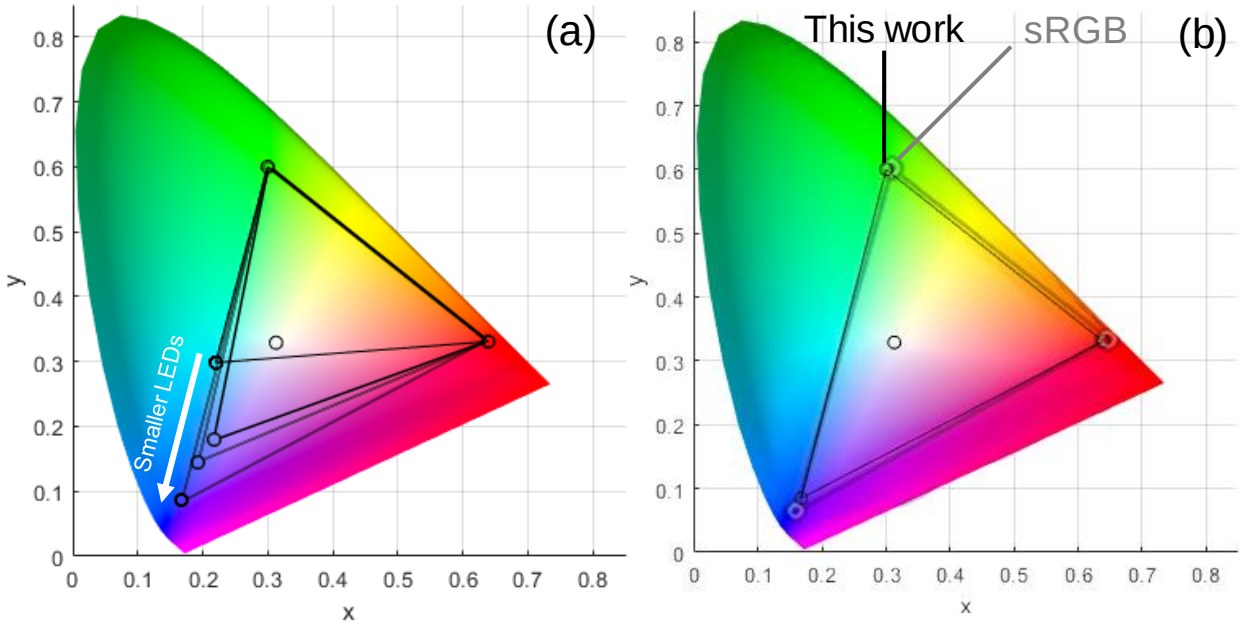

Fig. 162. (a) CIE chart of color change LEDs, with small diameter LEDs utilized to shift the blue emission point, (b) comparing the color change LEDs to sRGB space.

Utilization of V-grooves represents a novel breakthrough, which can lead to efficient monolithic color changing LEDs. The potential downside with this technique is the dependence on bias and corresponding current in order to create the various colors. Where the red will be far dimmer compared with the blue colors. A proposed solution is that multiple nanoscale red LEDs can be utilized to compensate for a single green or blue LED. In this way equal proportions of red, green, and blue can be created for µ-LED displays or commercial lighting. Further device optimization in both the MQWs and V-grooves can open the door to further enhancement and commercial applications.

4.5 AC Tunneling LEDs

LEDs provide efficient solid-state lighting for homes, businesses, and display technology [30, 109, 138-139]. LEDs are also poised to be utilized in ever expanding applications such as visible light communication and LiFi [116, 179]. Conventional LEDs utilized for these applications are based on GaN, which is a wide bandgap semiconductor. The persistent issues for those LEDs, however, have been the requirement of AC to DC converters, and the inefficient p-type doping compared to n-type doping. Conventional LEDs conduct current in one direction, with corresponding light emission. Thus, AC to DC converters are often employed to prevent loss of half the signal from the LEDs. Though even with AC to DC conversion the high turn-on voltage of LEDs, ~2 V for blue, can lead to a stroboscopic effect. On the aspect of p-type doping, Mg is most commonly utilized for III-Nitrides, though it has a high activation energy - from 170 meV in GaN blue LEDs to >500 meV for AlGaN UV LEDs [118, 180]. At room temperature, this high activation energy equates to less than 1% acceptor ionization for p-GaN, in contrast to the silicon (Si) n-type dopant where vertically 100% of the donors are ionized. Furthermore, instead of p-GaN vertical growth, selective area p-type doping is also difficult due to the thermal degradation of the surface during the high temperature anneal necessary to incorporate Mg into the lattice [181-183]. The challenges of selective area doping for p-type GaN limit LED device integration. These limits often separate GaN transistors from LEDs, due to differences in growth structure. Therefore, it is important to pursue and explore alternative devices which can lead to integration between LEDs and transistors for emerging applications such as LiFi.

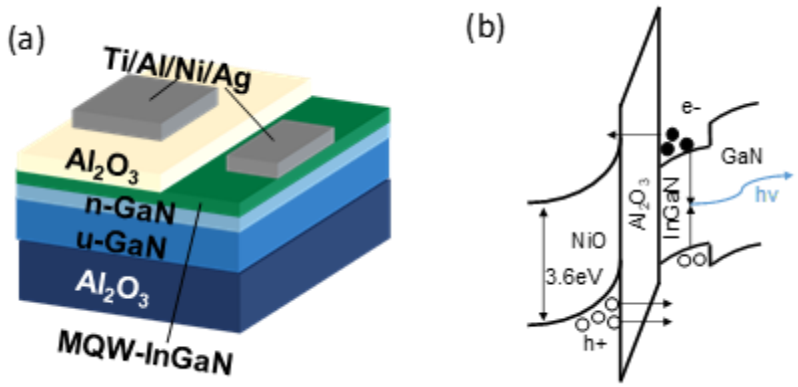

Fig. 163. (a) Schematic of hybrid AC LED, (b) corresponding forward biased band diagram showing hole and electron tunneling.

In order to address the lack of AC functionality and fundamental p-type issues, a novel approach is proposed and presented which removes the need for a p-GaN layer in the LED. Through this approach, AC functionality is demonstrated as a potential solution to eliminate the use of AC to DC converters [184]. However, to generate steady photon emission, both electrons and holes must be continuously supplied and radiatively recombine. Electrons can already be provided through impurity doping of Si, which has a low activation energy of 15 meV, allowing for complete ionization of donors at room temperature [185]. The intrinsic wide bandgap of 3.4 eV from GaN leads to a hole concentration of 10^{-10} cm^{-3}, which is worsened by vacancies which make the material slightly n-type [186]. Therefore, virtually no holes can be provided through thermal ionization or vacancies. To provide a steady source for holes, a material with excess holes must be utilized.

Here for our proposed tunneling GaN AC LED, holes are provided by a metal film stack and the formation of NiO, which together act as a source of both excess holes and electrons. The carriers tunnel through a dielectric film to be injected into the device. Use of NiO provides a better source of high density holes over other works with attempt to employ heavily doped GaN p-n

junctions [187] In this work, a Ti/Al/Ni/Ag metal film stack and a 50 nm Al_2O_3 dielectric film were used. Both the dielectric and metal stack were chosen due to the prevalence in GaN power devices to allow for potential integration. The epitaxial structure utilized is that of a conventional blue LED without the p-type layer, leaving the InGaN/GaN MQW region on top. A schematic view of the hybrid device is shown in Fig. 163(a). The metal film stack is annealed which is thought to form NiO from the Al_2O_3 film. NiO is a p-type semiconductor with a bandgap of ~3.6 eV and lowers the position of the valence band to promote hole tunneling. Uniform hole injection in the device provided by the NiO and metal can help overcome the current spreading and injection challenges without resorting to more complex designs [188-191]. The corresponding NiO band diagram under a forward bias is shown in Fig. 163(b). Application of a positive bias to the NiO reduces the effective barrier height and promotes Fowler-Nordheim (FN) tunneling [192-193]. The band-offset on the conduction band is increased due to the positive bias, where electrons accumulate near the MQW surface and minimize tunneling.

Previous works have made use of metal-insulator-semiconductor (MIS) structures with NiO and MgO as the p-type and insulating layers respectively [192-193]. Work by Wang, et. al, has previously showed use of 50 nm of MgO to be optimal for electron suppression, hole injection, and surface passivation [193]. These works are expanded upon here, making use of Al_2O_3 which shows lower interface states with GaN and more advantageous band alignment for hole injection [188-195]. For the first time, this work is also applied to InGaN/GaN MQWs to further optimize device performance, along with the use of an optimized metal stack. The holes provided through tunneling open up the possibility of device integration with existing GaN technologies such as HEMTs. Furthermore, a novel introduction of AC functionality is demonstrated from the tunneling GaN LED in this work.

An InGaN/GaN blue LED at 450 nm without the p-type GaN layer was utilized in this work. The growth was performed on a sapphire substrate with 2.5 µm of unintentionally doped GaN (~10^{16} cm^{-3} background doping), 2 µm of n-GaN (~$7x10^{18}$ cm-3), and 6 pairs of InGaN/GaN MQWs on top. The MQWs were composed of 3 nm of $In_{0.13}Ga_{0.87}N$ with 12.5 nm GaN barriers. To fabricate the devices, 50 nm of Al_2O_3 was first deposited using an Ultratech S200 thermal ALD system. Openings were patterned in the Al_2O_3 layer through a photoresist mask using a BOE. Next, lift-off resist and photoresist were coated and patterned. A 14/140/30/100 nm of Ti/Al/Ni/Ag were deposited through thermal evaporation and lifted-off, forming the capacitor and substrate contact. The capacitor and substrate contact sizes were each 100 μm^2. A thermal annealing process was performed in a nitrogen ambient environment at 850°C for 30 seconds to diffuse the metal to form a NiO layer, as well as forming an ohmic contact to the InGaN/GaN [196]. Use of the four metal layers was found to produce both increased photon emission and uniformity. Separate experiments were run with Ti/Al and Ni/Ag, finding no emission in the case of Ti/Al and weaker emission in the case of Ni/Ag, Fig. 164. Annealing introduced roughness to the metal layer due to the diffusion of aluminum, with the common formation of Ni-Al clusters [196-197].

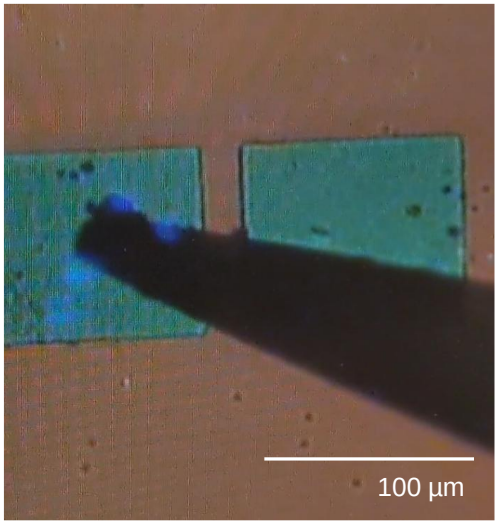

Fig. 164. Ni/Ag Al_2O_3 annealed stack showing non-uniform light emission.

Electrical and optical characterizations were performed on the fabricated hybrid AC LEDs. The I-V data collected for a single device are shown in Fig. 165(a). The measured I-V curve is comparable to reported measurements of previous NiO/MgO tunnel diodes, though with a lower turn-on voltage due to the reduced band offsets compared with MgO [192-193]. Under forward bias, the valance band offset is lowered and holes are injected into the MQW to recombine with electrons. While under reverse bias, the offset for the conduction band is lowered, and electrons supplied by the metal can tunnel through the insulator. In order to better clarify the tunneling mechanism, both room temperature measurements and cryogenic measurements with liquid nitrogen were performed for the p-type-less LED. At room temperature, significant noise was observed and can be attributed to interface states and traps states within the oxide film. Low temperature measurements with liquid nitrogen are used to study the impact of these interface states on the device. It can be seen that the I-V curve at low temperature is much smoother due to freeze-out of interface and trap states. EL was still observed even when the sample was at cryogenic temperatures. Looking at both tested temperatures, rectifying behavior was still recorded. Due to the rectification and observed light emission at low temperature, the hole injection is attributed to FN tunneling instead of a trap-assisted tunneling mechanism which is more temperature dependent [198].

Hole injection through band bending and tunneling instead of impurity doping allows the device to turn-on when a low forward bias is applied of ~0.5 V, as seen in Fig. 165(b) from a log-scale of the I-V. A low forward bias bends the energy bands of the dielectric enough to promote FN tunneling. This contrasts with conventional LEDs that have a higher turn on voltage around the value of the bandgap of 2.75 eV. The tunneling mechanism can also allow for a faster response

time in an LED when compared to conventional diffusion mechanisms. Excess forward voltages above 18 V are seen to induce breakdown of the capacitor dielectric. Once the capacitor has broken down, current flows in excess, however there was no longer observed light emission due the inability of the oxide to confine the opposite charge type at the surface.

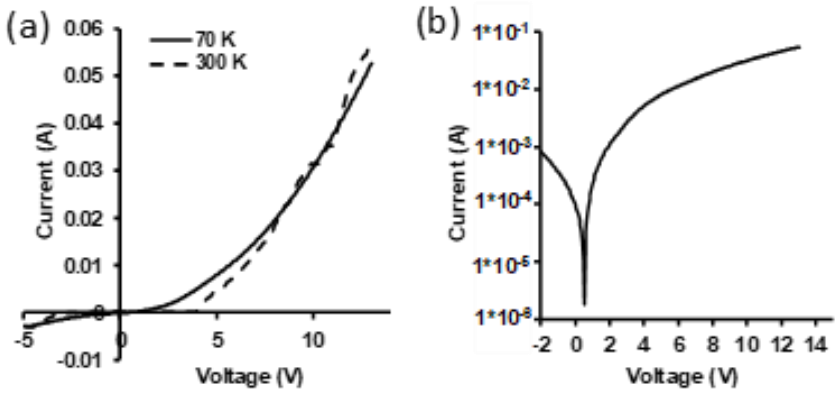

Fig. 165. (a) I-V curves of the hybrid AC LED at 300K and 70K, (b) Log I-V of hybrid AC LED at 70K.

Room temperature EL measurements were next performed, with results shown in Fig. 166. Significant photon emission begins at a forward bias of 6 V. Increasing the applied voltage from 6 V to 8 V leads to increased light emission by 4.25x, as more holes are injected through the oxide into the MQWs. The light emission is at 450 nm which corresponds to the bandgap of the InGaN QW. The linewidth was also narrower at ~20 nm compared to previously reported tunneling devices which had an extended tail, as the MQWs better confine carriers [193]. The $In_{0.13}Ga_{0.87}N$ has a bandgap of ~2.75 eV, where the intrinsic carrier concentration is at a level of 10^{-9} cm^{-3}, meaning tunneling must be the sole source of holes. Light was seen to be emitted primarily around the edges of the capacitor, as the thick metal blocks the light. Light emission at lower voltages may be observed if collected from the backside of the device. In future iterations, a flip-chip design would be effective for enhancing light extraction efficiency.

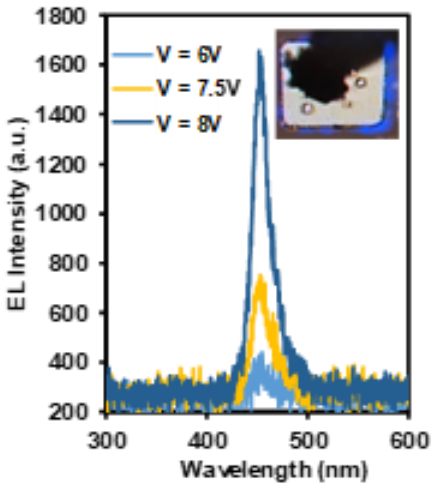

Fig. 166. EL spectra of the hybrid AC LED under different forward biases.

EL measurements were also performed at different AC driving frequencies on a single device at room temperature, as shown by Fig. 167, driven with a voltage of 11 V. The frequencies tested were 10 Hz, 33 Hz, and 50 Hz. The peak emission wavelengths from the EL spectra at each frequency remained constant at 450 nm with almost constant bandwidth. Future works on testing at higher frequencies will be done, where it is suspected that the tunneling mechanism can react faster compared to the higher capacitance associated with p-n junctions.

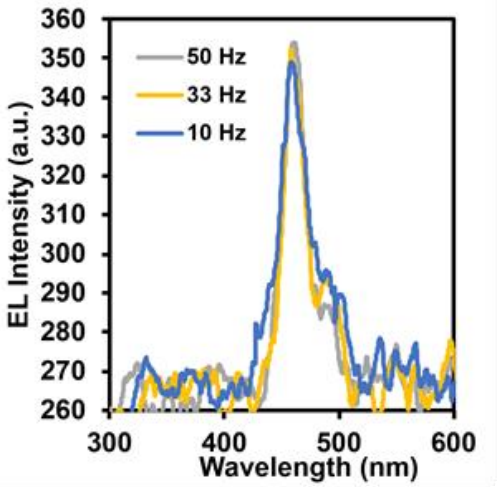

Fig. 167. EL spectra of the hybrid AC LED under different frequencies.

The AC aspect of the hybrid LED comes from utilization of the tunneling mechanism between two capacitors. Since the tunneling GaN LED can inject holes in forward bias, and electrons in reverse, the device acts symmetrically. The symmetry allows for more uniform performance, regardless of applied polarity of the voltage. Therefore, by probing two capacitors, EL can be produced in both forward and reverse bias. The capacitor that is in forward bias will supply holes and emit light, while the other capacitor is the source of injected electrons. An I-V curve showing the AC behavior is provided in Fig. 168, with insets showing the light emission on either ends and the equivalent circuit diagram. The equivalent circuit diagram is two diodes in parallel, but with opposite directions, where one LED is always on given an applied bias of either polarity. Both sides of the I-V curve are shown to be roughly symmetric, due to the symmetric electron/hole tunneling nature of the capacitors. An advantage of this two terminal LED device is that an AC waveform can be fed directly in, without need for an external AC to DC converter or loss of half the input power. Due to the continuum created by the tunneling current, the resulting AC signal will have minimal loss, as is the case with conventional GaN diodes with a high positive turn-on voltage of ~2 V. This novel hybrid AC LED can lead to a number of exciting applications such as on-chip communication, monolithic integration with transistors, and LiFi.

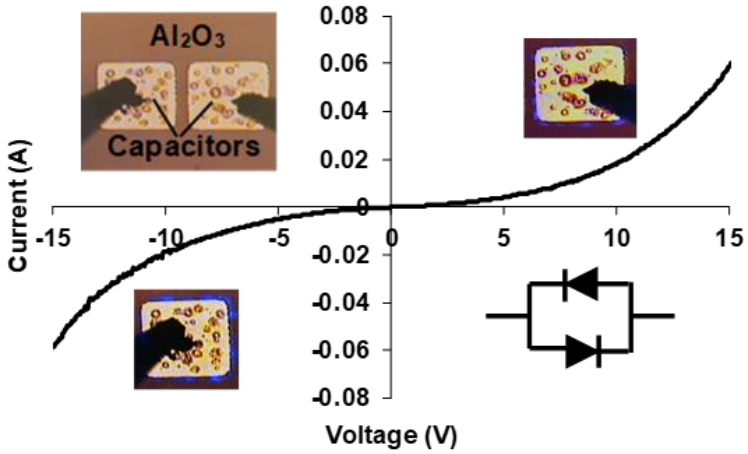

Fig. 168. I-V curve of hybrid AC behavior, probing two capacitors.

In summary, a novel tunneling GaN LED was presented. This device makes use of band bending and carrier tunneling in order to inject holes directly into the MQW region. Tunneling allows earlier device turn-on of ~0.5 V compared with conventional LEDs at ~2 V, a reduction of 75%. Cryogenic testing was performed on the device which points towards FN tunneling, as opposed to trap-assisted tunneling. EL measurements showed emission wavelengths corresponding to the bandgap of the MQW, with no variation in wavelength or intensity at different driving frequencies. The symmetric tunneling of electrons and holes leads to AC performance, with a continuous I-V curve and minimal signal loss. These results could open the door to emerging applications such as on-chip communications, monolithic LED integration with transistors, and signal processing with LiFi.

- **Future Device Optimizations**

Future works are aimed at the exploration of alternative materials to provide possible integration. Materials such as Ga_2O_3 and high Al % content $Al_xGa_{1-x}N$ have been initially explored, though initial results show no conduction or light emission, Fig. 169. This can be attributed to improper band alignment with NiO. Instead, alternative metal stacks can be engineered for hole or electron tunneling with better band alignment due to edited work functions.

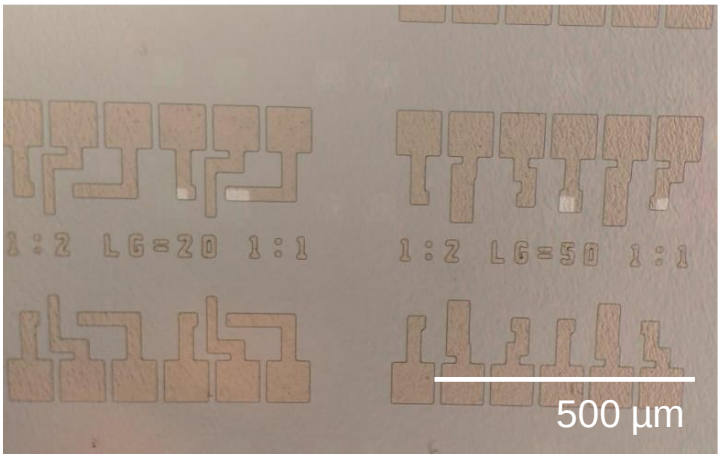

Fig. 169 Ti/Al/Ni/Ag Al_2O_3 on Ga_2O_3.

Chapter 5

NOVEL POWER DEVICE EXPORATION

5.1 Overview of Novel Power Device Exploration Chapter

This chapter focuses on novel concepts related to power devices which can be utilized to potentially drive high power LEDs. Integrated GaN-Si nanowires are explored in order to delve into the advantages of high power GaN nanowires tied in with the mature silicon platform. Gallium Oxide devices are additionally explored in order to further expand upon the vertical nanowire devices presented. Where Gallium Oxide offers a relatively low cost alternative to high power switches. These devices are explored through fabrication work along with device level simulations to explore the viability.

5.2 Integrated Si-GaN Nanowire Devices

The commercial development of integrating Si and GaN has opened a number of new possible device integration schemes. One such integration scheme now made possible, is vertical Si-GaN nanowire devices. Silicon is conventionally utilized to fabricate devices and is the most mature semiconductor material system. As such, there is a desire to integrate Si with GaN, as GaN can support high voltages, offer high electron mobility, and be used to generate light. Light generation through GaN LEDs is under investigation for displays and integration with Si technology can provide the needed control circuitry. Advanced Si transistors have moved from planar to fin technology and are now moving to Si nanowires [199]. Si nanowires provide better electrostatic gate control over the channel region, stemming leakage, due to the gate-all-around design. Vertical nanowires, as opposed to planar nanowires, offer increased density and possibility for 3-D device integration. Due to the benefits of the mature Si system, Si nanowires are investigated for use with GaN nanowire LEDs.

Work has previous been demonstrated in section 2.4 with regards to the formation of vertical Si nanowires at the base of GaN nanowires. The limitation in the way of then achieving integrated Si-GaN nanowire FETs, is the use of AlN for the buffer region. AlN provides the template for growth on the lattice mismatched <111> silicon wafer. For the work here, AlN acts as a dielectric which prevents current flow between the two nanowires. The AlN layer is 300 nm thick which prevents simple electron tunneling or electrical breakdown of the dielectric. Presented here is a novel solution to integrate Si nanowires with GaN nanowires for display applications.

The use of aluminum is purposed as a means to short the AlN, while balancing the contact resistivity between the two materials. A sidewall coating of Aluminum around the regions of the

AlN can provide the pathway for current flow between the two nanowires. The nanowires are initially formed through a dry etching process. Ion-implantation can be utilized with the vertical structure in order to form n+ source regions at the base of the nanowire. Alternatively, a schottky source can be used for electron injection, though with the cost of added leakage [200]. The bottom layers can be deposited forming the source contact at the base of the Si, followed by the gate wrapping around the Si nanowire. Placing the gate around the Si nanowire instead of the GaN wire provides better device pinch-off due to the higher relative permittivity (ε_r) of Si (11.7) over GaN (8.9). PDMS can be coated and etched back to exposure the top portion of the Si nanowire and everything above. Sputtering of Al can be performed in order to bridge the AlN by coating the entire wire. Photoresist can be next coated and etched back to reveal the upper portion of the GaN wire. Selective wet etching of the Al can remove the Al along the GaN wire, leaving the Al to only bridge the AlN layer. A final PDMS coating and etch back can be utilized to from the upper drain contact of the device. A schematic of the complete purposed structure is shown in Fig. 170.

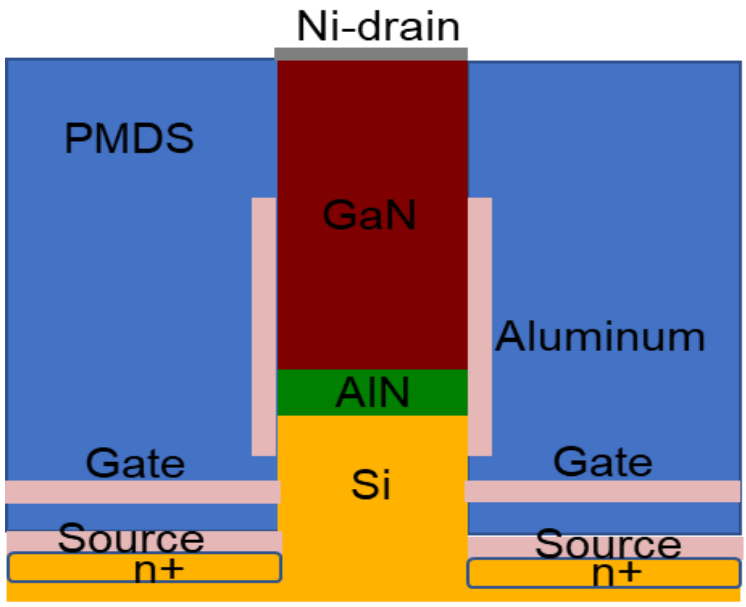

Fig. 170. Schematic of fabricated Si-GaN nanowire FET.

Initial fabrication tests have been performed in order to from the GaN nanowires on top of Si nanowires. A chlorine based dry etch has been performed in order to etch both types of nanowires. Prolonged etching to create taller Si nanowires at the base of the GaN has been found to lead to a more anisotropic etch Si etch over previous findings in section 2.4. Vertically etched nanowires remove or minimize the wet etching needed through KOH. Results for the dry etched GaN-Si nanowires are shown in Fig. 171. The diameter of the silicon nanowire matches that of the GaN nanowire which is needed for later fabrication. In order to flow current past the AlN barrier, use of Aluminum to short the dielectric is purposed. Having an undercut Si nanowire would inhibit sidewall coatings. The use of photoresist masking an Al wet etch of the tops of the nanowires has been previously demonstrated and can be applied here [201]. Further experimental results are expected to continue on the presented work.

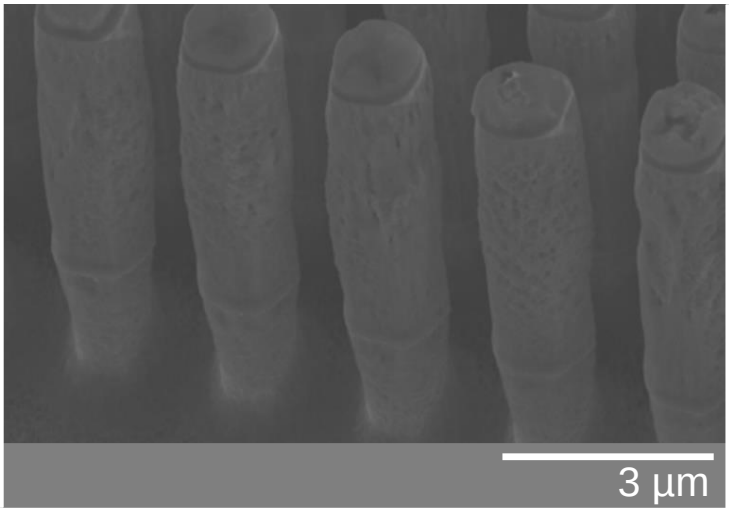

Fig. 171. Etched GaN-Si nanowires with Ni hard mask.

Silvaco Atlas simulations were performed on GaN-Si nanowires in order to model the device performance. Conventionally lightly p-type Si (10^{16} cm^{-3}) is utilized for the starting substrate. The diameter of the integrated nanowire is chosen to be 500 nm. To start, the band alignment with Si-AlN-GaN is studied and tested for current flow. The simulated transistor is

shown in Fig. 172(a). A 300 nm AlN layer is placed between 5 µm of GaN and 1.5 µm of Si, which approximates the etched structure. A cutline is taken from the top of the nanowire to the bottom, shown by Fig. 172(b). The AlN layer is found to natively prevent current flow between the two nanowires. The electron affinity for Si is 4.01 eV and GaN is 4.1 eV, which allows the conduction bands to be at approximate heights. The bandgap differences, however, lead to a large valence band offset for hole conduction. The barrier to hole conduction is a benefit to the integrated GaN-Si nanowire, as the hole current is leakage in the device. Also, of note is that electrons accumulate at the Si surface, while the electrons are repelled at the GaN surface. The energy bands of the materials are pinned to the surface based on the respective electron affinities, where the bands adjust to achieve a constant fermi-level. This effect leads to the hetero-structure behavior in the band-alignment. I-V characterization was simulated and showed no current flow through the AlN barrier.

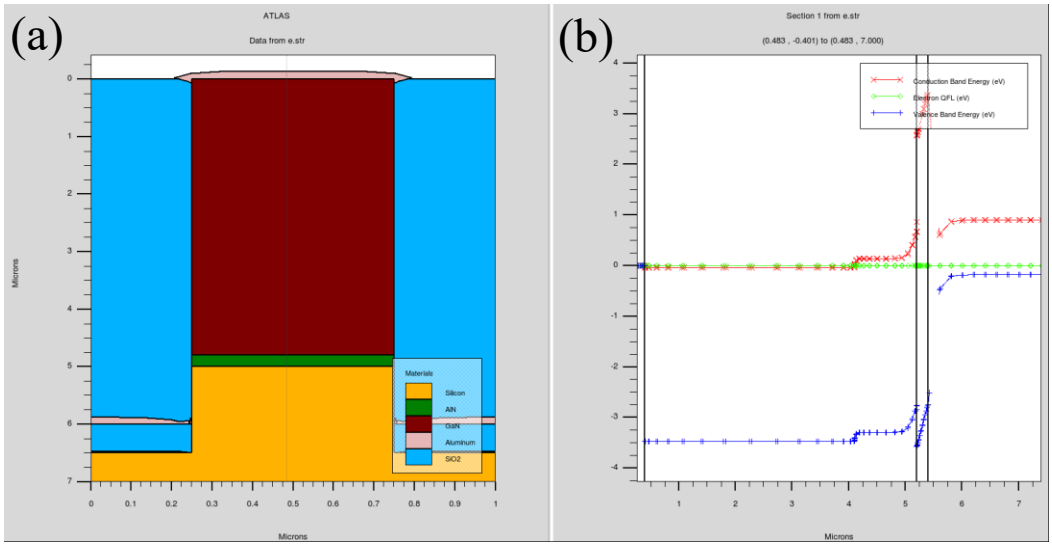

Fig. 172. (a) Simulated GaN-AlN-Si nanowire, (b) corresponding band alignment.

To simulate the effect of the shorting the AlN barrier layer, the AlN layer was removed from the structure. I-V characteristics where obtained and are shown in Fig. 173 with the I_D-V_D

performance with various gate biases. The gate is varied from 5 V to – 10 V for the recorded measurements. Use of Si for the channel material over GaN allows for the electric fields from the gate region to further penetrate to allow for better current pinch off. Compared to the results from the GaN SIT or GaN LED-FET, the 500 nm Si wire is able to achieve enhancement mode operation. Similar to the effects obtained through the smaller GaN nanowires, the Si wire is also able to operate with a forward bias to the schottky gate without full gate turn-on. The turn-on voltage for the nanowire is pushed out to more positive values as the reverse bias on the gate region increases. The DIBL effect is observed with the integrated Si wire similar to the GaN wire, through the effects are less severe, due to the differences in relative permittivity. The integrated GaN-Si nanowire is also expected to be able to operate at high voltage due to the material properties of GaN. At higher current injection, the device is seen to experience resistance for the thickness of the lightly doped GaN wire. Resistance in the wire would lead to a higher breakdown voltage at the cost of on-resistance. In order to lower on-resistance the Al layer can be also utilized to short the resistor of the GaN by taking the current up closer to the nanowire tip. The doping profile in the GaN nanowire can also be further optimized to reduce on-resistance.

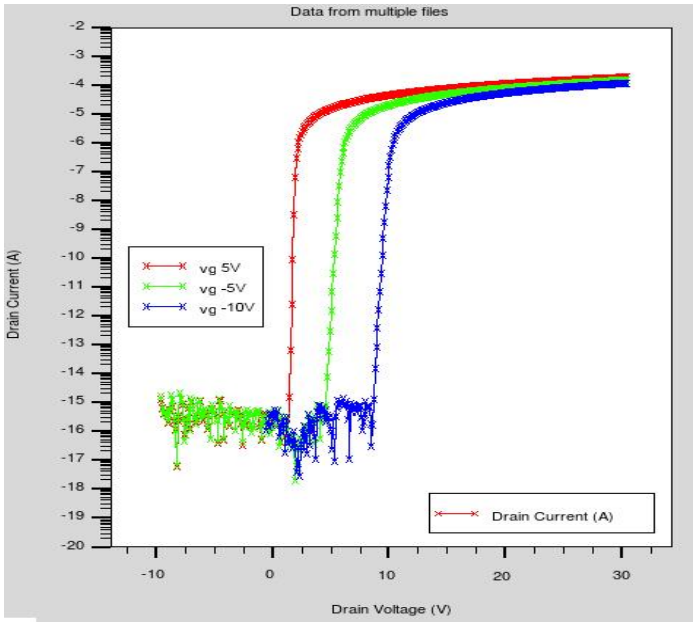

Fig. 173. I_D-V_D performance with various gate biases.

- **Future Device Directions**

Future work for the integrated Si-GaN nanowire device involves the continued fabrication of the prototype devices. The building blocks for the device are in place in order to fabricate the structure presented in Fig. 170. A similar process flow to the presented GaN SIT or GaN LED-FET can be followed with insertion of an additional sputtering and wet etching step. Simulation results provide an early indication of device behavior with additional simulations run as needed. The fabrication of the Si-GaN is another novel device which has wide reaching applications for display and power devices.

5.3 Ga_2O_3 Nanowire Devices

Wider bandgap material systems can support higher voltage operation for power electronic devices and provide a better trade-off between on-resistance and breakdown voltage [202-203]. GaN provides increased performance for power electronics compared with Si and SiC materials. A relatively recent addition to the power electronics area has been the introduction of β-Ga_2O_3. Gallium Oxide is a wide bandgap semiconductor with a bandgap of 4.8 eV, compared to that of 3.4 eV of GaN. There are five common polymorphs of Gallium Oxide, though the beta phase is most stable and is commonly utilized for both power electronics and solar blind applications. The other key advantage Ga_2O_3 has over GaN, is the ability to relatively cheaply grown native substrates. GaN substrates remain costly due to the high temperature and pressures needed, instead GaN is conventionally grown on cheaper substrates such as sapphire. Gallium Oxide possess a higher relative permittivity of 10 vs. the 8.9 of GaN. The higher permittivity allows to better gate schottky gate control for nanowire SIT devices.

The SIT or similar device make a good choice of transistor for Gallium Oxide. Gallium Oxide can easily be n-type doped, however there is not currently a viable p-type dopant [203]. The lack of p-type doping necessitates an n-i-n structure for a power transistor. Compared to a planar structure, the nanowire design offers increased electrostatic control from the gate. The increased electrostatic control through vertical nanowire with a gate-all-around can provide enhancement mode operation due to the lack of p-type dopant. Works on Gallium Oxide nanowire devices are sparse and present a new opportunity to develop initial device results. In this work, the initial work to develop a novel Gallium Oxide nanowire SIT is performed.

The first step in the formation of a nanowire Gallium Oxide SIT is also the hardest, the ability to form a nanowire structure. Gallium Oxide is difficult to etch with a stronger binding energy compared to GaN [203]. A chlorine based dry etch is utilized to etch Gallium Oxide, with use of high power to provide a physical component to the etch. For these initial tests, silica nanospheres with 3 µm in diameter are utilized. The current Gallium Oxide samples provided are small in size, making conventional photolithography difficult. The conventional RIE chlorine dry etch recipe used to etch nanowires [58] was utilized for a period of 56 minutes. The results from the dry etch are shown in Fig. 174. The dry etching led to a depth of ~2.2 µm, for an etch rate of 39 nm/min. This etch rate is in contrast to that of GaN which has an etch rate of 245 nm/min. The slower etch rate is due to the differences in atomic binding energies. The of the Gallium Oxide allow appear as roughened from the dry etch. The masking silica sphere is significantly flattened and almost fully removed from the dry etch. The etched height is barely enough to incorporate the three metal layers due to the added surface roughness. The diameter of the nanowire is also too large for enhancement mode operation, making only depletion mode possible. Further etching optimizations are planned on an ICP system to engineer an improved etched profile.

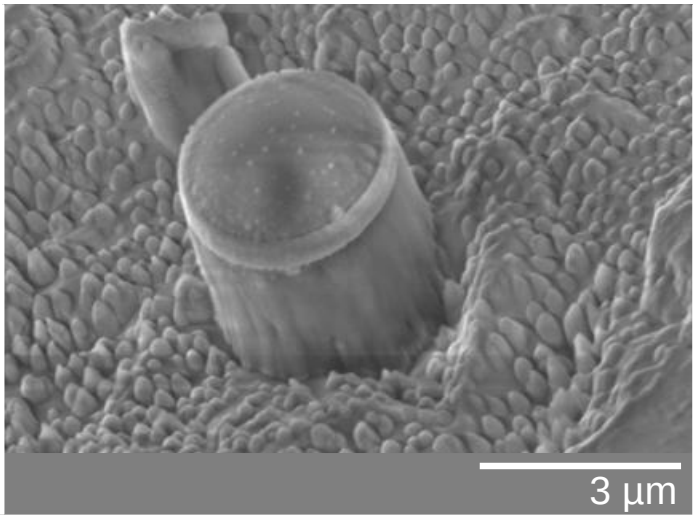

Fig. 174. Initial Gallium Oxide nanowire

Simulations were additionally performed in order to model the device performance for a Gallium Oxide SIT. Silvaco Atlas was utilized for the nanowire SIT simulations. As Gallium Oxide is a newer material system, Silicon was used form the device, with the properties of Silicon overridden to that of Gallium Oxide. The structure of the Gallium Oxide SIT is shown in Fig. 175. A 400 nm wire was tested with the similar three level structure previously used in sections 3.2 and 3.3. A 40 nm thick gate is utilized with a work function set at 5 eV.

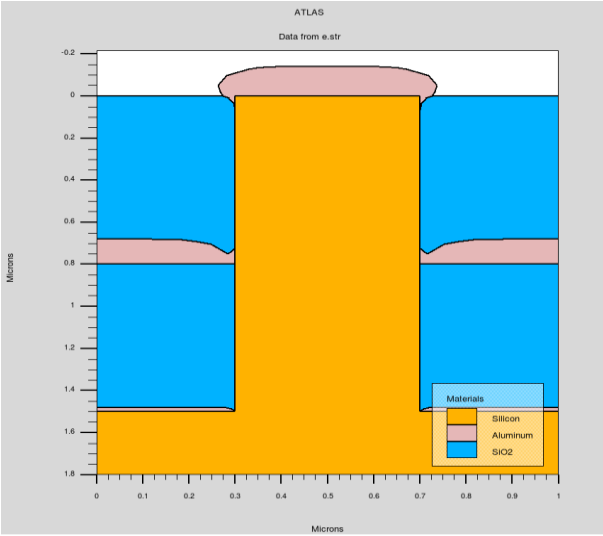

Fig. 175. Gallium Oxide nanowire simulated structure.

High voltage I-V characteristics were collected, with the family of curves for the device shown in Fig. 176. The drain voltage is varied from 0 V to 150 V to test higher voltages, though Gallium Oxide can support several hundred to several thousand volts. The gate voltage was correspondingly varied form -5 V to 5 V. The gate has excellent control over the nanowire, as only -2 V is needed to hold back over 150 V. A positive threshold voltage is recorded at 0 V the device is off until ~ 50 V. Increased blocking capabilities are possible, making use of smaller nanowire diameter or thicker gates. Compared to the nanowire SIT, the Gallium Oxide operates as enhancement mode, due to the increased relative permittivity over GaN. With positive gate biases,

the gate is seen to turn on, as the distinct curves for the 3 V and 5 V cases. Overall the Gallium Oxide SIT is expected to perform very well and support high voltages in a nanowire form factor.

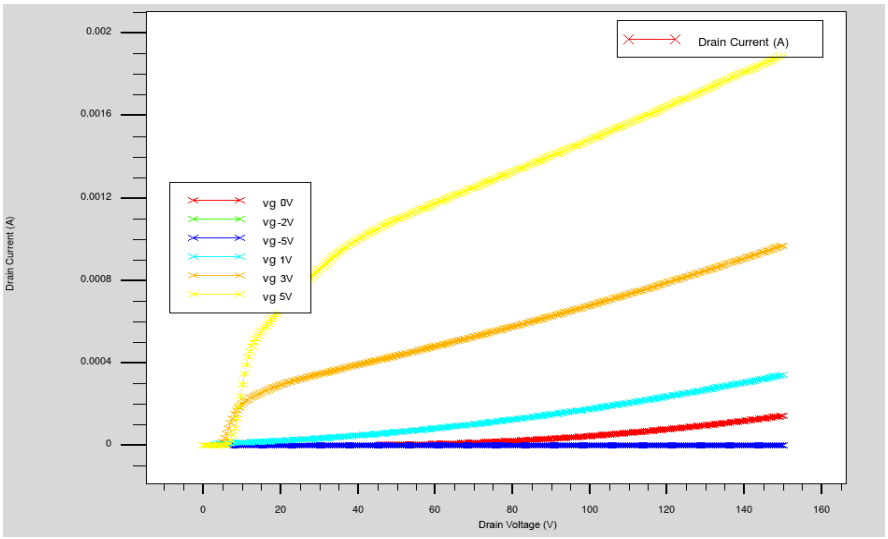

Fig. 176. Simulated Gallium Oxide SIT I_D vs. V_D curves for differing gate

- **Future Device Directions**

The next steps for the fabrication of the Gallium Oxide device involve first an optimization of the dry etch. A Plasma-Therm ICP system recently brought online will be utilized order to achieve a better etch profile for Gallium Oxide. Once an adequate etch recipe is established, device manufacturing will follow a similar process flow to that of the GaN nanowire SIT or GaN nanowire LED-FET. Once fabricated, additional high voltage device testing is planned in order to capitalize on the advantaged Gallium Oxide offers.

PUBLICATIONS

[1] M. Hartensveld, R. Maurer, M. Rodwell, “Characterizing TiN Resistivity using Plasma Enhanced Atomic Layer Deposition with TMAT” *NNIN Research Accomplishments,* 2014, doi: 10.6084/m9.figshare.14214452.

[2] M. Hartensveld and J. Zhang, "Monolithic Integration of GaN Nanowire Light-Emitting Diode With Field Effect Transistor", *IEEE Electron Dev. Lett.*, vol. 40, no. 3, pp. 427-430, 2019, doi: 10.1109/LED.2019.2895846.

[3] M. Hartensveld, C. Liu, and J. Zhang, “Proposal and Realization of Vertical GaN Nanowire Static Induction Transistor”, *IEEE Electron Dev. Lett.*, vol 40, no. 2, pp. 259-262, 2019, doi: 10.1109/LED.2018.2886246.

[4] M. Hartensveld, G. Ouin, C. Liu, and J. Zhang, “Effect of KOH passivation for top-down fabricated InGaN nanowire light emitting diodes,” *J. of Appl. Phys*., vol. 126, 2019, doi: 10.1063/1.5123171.

[5] M. Hartensveld, B. Melanson and J. Zhang, "Electrostatic Field Effect Light-Emitting Diode", *IEEE Photonics J.*, vol. 12, no. 3, pp. 1-8, 2020, doi: 10.1109/jphot.2020.2992278.

[6] C. Liu, B. Melanson, Y. Ooi, M. Hartensveld and J. Zhang, "Analysis on light extraction property of AlGaN-based flip-chip ultraviolet light-emitting diodes by the use of self-assembled SiO2 microsphere array", *Gallium Nitride Mater. and Dev. XIV*, 2019, doi: 10.1117/12.2510488.

[7] M. Hartensveld, B. Melanson and J. Zhang, "Ultraviolet Electrostatic Field Effect Light-Emitting Diode", *IEEE Photonics J.*, vol. 12, no. 5, pp. 1-8, 2020, doi: 10.1109/jphot.2020.3020384.

[8] M. Hartensveld, B. Melanson, V. T. Vangipuram, and J. Zhang, “450 nm Gallium Nitride alternating current light-emitting diode”, *IEEE Photonics J.*, 2020, doi: 10.1109/JPHOT.2020.3032382.

[9] B. Melanson, D. Starling, M. Hartensveld, G. Howland, S. Preble and J. Zhang, "Narrow Linewidth Photoluminescence from Top-Down Fabricated 20 nm InGaN/GaN Quantum Dots at Room Temperature", *Conf. Lasers Electro-Optics*, 2020, doi: 10.1364/cleo_si.2020.sth4h.2.

[10] M. Hartensveld and J. Zhang, "Field Effect Light-Emitting Diode Integration for Enhanced Hole Utilization", *IEEE Device Research Conf.*, 2020, doi: 10.1109/DRC50226.2020.9135145.

[11] M. Hartensveld, "Towards Monolithic Active Matrix Nanowire Light-Emitting Diodes", *International Display Week Conf.*, 2020.

[12] B. Melanson, C. Liu, M. Hartensveld, and J. Zhang, "Light extraction analysis of AlGaN nanowires with inverse taper for DUV LEDs", *Light-Emit. Dev.*, Mater. Appl. XXV, 2021.

[13] M. Hartensveld, "Fully Monolithic GaN µLED Display System", *SID Display Week 2021*, 2021.

[14] M.Hartensveld, B. Melanson, C. Liu, and J. Zhang, "AlGaN Nanowires with Inverse Taper for Flexible DUV Emitters", *J. Phys. Photonics*, 2021, doi.org/10.1088/2515-7647/abf6be.

PATENTS

[1] M. Hartensveld and J. Zhang “Nanowire Light Emitting Switch Devices and Methods Thereof,” 2019, Patent pending. (Granted)

[2] M. Hartensveld and J. Zhang “Capacitive Current Spreading LED,” 2019, Patent pending.

[3] M. Hartensveld “Monolithic Semiconductor LED Display Systems and Methods Thereof”, 2020, Patent pending.

[4]. M. Hartensveld “Volume Engineering for LEDs and Methods Thereof”, 2021, Patent pending.

[5] M. Hartensveld “Monolithic Multi-Color Light Emitting Diodes and Methods Thereof”, 2021, Patent pending.

REFERENCES

[1] S. Nakamura and M. Krames, "History of Gallium–Nitride-Based Light-Emitting Diodes for Illumination", *Proc. of the IEEE*, vol. 101, no. 10, pp. 2211-2220, 2013. Doi: 10.1109/JPROC.2013.2274929

[2] C. Liu, and J. Zhang, "Influence of quantum well design on light polarization switching in AlGaN ultraviolet emitters," *AIP Advances*, 8 (8), 085125, 2018.

[3] C. Liu, Y. K. Ooi, S.M. Islam, H.G. Xing, D. Jena, and J. Zhang, "234 nm and 246nm AlN Delta- GaN Quantum Well Deep Ultraviolet Light-Emitting Diodes," *Appl. Phys. Lett*., 112, 011101, 2018.

[4] M. Kneissl, F. Mehnke, C. Kuhn, C. Reich, M. Guttmann, J. Enslin, T. Wernicke, A. Knauer, V. Kueller, U. Zeimer, M. Lapeyrade, J. Ras, N. Lobo-Ploch, T. Kolbe, J. Glaab, S. Einfeldt and M. Weyers, "Deep ultraviolet LEDs: From materials research to real-world applications", 2015 *IEEE Summer Topicals Meeting Series (SUM)*, 2015.

[5] S. Stockman, A. Kim, M. Misra, P. Grillot, L. Cook, S. Watanabe, R. Mann, L. Hudson, W. Gotz, M. Krames, D. Steigerwald, P. Martin, F. Wall and F. Steranka, "High-power GaN-based LEDs for lighting and display applications", *Intern. Semi. Dev. Research Sym.*, 2003.

[6] H. Jiang and J. Lin, "Nitride micro-LEDs and beyond - a decade progress review", *Optics Expr.*, vol. 21, no. 3, p. A475, 2013.

[7] J. Park, H. Chae, H. Chung and S. Lee, "Thin film encapsulation for flexible AM-OLED: a review", *Semi. Sci. and Tech.*, vol. 26, no. 3, p. 034001, 2011.

[8] H. Kim, J. Lee, C. Huh, S. Kim, D. Kim, S. Park and H. Hwang, "Modeling of a GaN-based light-emitting diode for uniform current spreading", *Appl. Phys. Lett.*, vol. 77, no. 12, p. 1903, 2000.

[9] T. Fujii, Y. Gao, R. Sharma, E. Hu, S. DenBaars and S. Nakamura, "Increase in the extraction efficiency of GaN-based light-emitting diodes via surface roughening", *Appl. Phys. Lett.*, vol. 84, no. 6, pp. 855-857, 2004.

[10] Kyulux, “Is Hyperfluorescence™ ready for AMOLED adoption?,” Kyulux, 31-Jul-2017. [Online]. Available: https://www.kyulux.com/is-hyperfluorescence-ready-for-amoled-adoption/.

[11] J. Chen, W. Cranton and M. Fihn, Handbook of Visual Display Technology, 1st ed. Berlin, Heidelberg: Springer Berlin Heidelberg, 2020, pp. 1223-1237.

[12] K. Zhang, Y. Liu, H. Kwok and Z. Liu, "Investigation of Electrical Properties and Reliability of GaN-Based Micro-LEDs", *Nanomaterials*, vol. 10, no. 4, p. 689, 2020. doi: 10.3390/nano10040689.

[13] M. Kim, M. Schubert, Q. Dai, J. Kim, E. Schubert, J. Piprek, and Y. Park, “Origin of efficiency droop in GaN-based light-emitting diodes,” *Appl. Phys. Lett*, vol. 91, no. 183507, 2007, doi: 10.1063/1.2800290.

[14] Z. Liu and K. Zhang, "Decoding Micro-LED’s Current Driving Methods", Ledinside.com, 2020. [Online]. Available: https://www.ledinside.com/knowledge/2016/10/decoding_micro_leds_current_driving_methods.

[15] J. Day, J. Li, D. Lie, C. Bradford, J. Lin and H. Jiang, "III-Nitride full-scale high-resolution microdisplays", *Appl. Phys. Lett.*, vol. 99, no. 3, p. 031116, 2011, doi: 10.1063/1.3615679.

[16] H. Chung, "Novel 5T1C pixel circuit for high-ppi AMOLED displays with n-channel LTPS TFTs", *J. Info. Display*, vol. 20, no. 1, pp. 39-43, 2019, doi: 10.1080/15980316.2019.1569565.

[17] Y. Ji, F. Ran, H. Xu, W. Shen and D. Lilja, "A digitally driven pixel circuit with current compensation for AMOLED microdisplays", *J. Soc. Info. Display*, vol. 22, no. 9, pp. 465-472, 2014, doi: 10.1002/jsid.259.

[18] Y. Cai, X. Zou, C. Liu, and K. M. Lau, "Voltage-controlled GaN HEMT-LED devices as fast-switching and dimmable light emitters," *IEEE Electron Device Lett.*, vol. 39, no. 2, pp. 224–227, Feb. 2018. doi: 10.1109/LED.2017.2781247

[19] Z. Guo, C. Hitchcock, G. Piao, Y. Yano, S. Koseki, T. Tabuchi, K. Matsumoto, M. Bulsara and T. Chow, "Integrable Quasi-Vertical GaN UMOSFETs for Power and Optoelectronic ICs", *physica status solidi (a)*, 2019.

[20] B. Tull, N. Twu, Y. Hsu, S. Leblebici, I. Kymissis and V. Lee, "19-1:Invited Paper: Micro-LED Microdisplays by Integration of III-V LEDs with Silicon Thin Film Transistors", *SID Symp. Digest Tech. Papers*, vol. 48, no. 1, pp. 246-248, 2017, doi: 10.1002/sdtp.11680.

[21] R. Cok et al., "Inorganic light-emitting diode displays using micro-transfer printing", *J. Soc. Info. Display*, vol. 25, no. 10, pp. 589-609, 2017, doi: 10.1002/jsid.610.

[22] Y. Liu, K. Liao and Y. Li, "30-1: Invited Paper: Development of MicroLED Display by PixeLED Display Technology", *SID Symp. Digest Tech. Papers*, vol. 51, no. 1, pp. 429-431, 2020, doi: 10.1002/sdtp.13896.

[23] C. Bower, "Micro-Transfer-Printing (μTP): Technology Overview", 2014.

[24] "eLux", Eluxdisplay.com, 2019. [Online]. Available: https://www.eluxdisplay.com.

[25] L. Dobos, B. Pécz, L. Tóth, Z. Horváth, Z. Horváth, A. Tóth, and M.-A. Poisson, “Annealed Ti/Cr/Al contacts on n-GaN,” *Vac.*, vol. 100, pp. 46-49, 2014, doi: 0.1016/j.vacuum.2013.07.038.

[26] Z.-H. Feng, X.-B. Wang, L. Wang, Y.-J. Lv, Y.-L. Fang, S.-B. Dun, and Z.-P. Zhao, “Ti/Al Based Ohmic Contact to As-Grown N-Polar GaN,” *Chinese Phys. Lett*., vol. 32, no. 8, pp. 087102, 2015, doi: 10.1088/0256-307X/32/8/087102.

[27] D. Look and R. Molnar, "Degenerate layer at GaN/sapphire interface: Influence on Hall-effect measurements", *Appl. Phys. Lett.*, vol. 70, no. 25, pp. 3377-3379, 1997, doi: 10.1063/1.119176.

[28] M. Cheong, K. Kim, C. Oh, N. Namgung, G. Yang, C. Hong, K. Lim, E. Suh, K. Nahm, H. Lee, D. Lim and A. Yoshikawa, "Conductive layer near the GaN/sapphire interface and its effect on electron transport in unintentionally doped n-type GaN epilayers", *Appl. Phys. Lett.*, vol. 77, no. 16, pp. 2557-2559, 2000, doi: 10.1063/1.1318728.

[29] H. Yu, M. Kemal Ozturk, S. Ozcelik and E. Ozbay, "A study of semi-insulating GaN grown on AlN buffer/sapphire substrate by metalorganic chemical vapor deposition", *J. Crystal Growth*, vol. 293, no. 2, pp. 273-277, 2006, doi: 10.1016/j.jcrysgro.2006.05.056.

[30] M. Hartensveld and J. Zhang, "Monolithic Integration of GaN Nanowire Light-Emitting Diode With Field Effect Transistor", IEEE Electron Device Letters, vol. 40, no. 3, pp. 427-430, 2019.

[31] M. Hartensveld, C. Liu, and J. Zhang, “Proposal and Realization of Vertical GaN Nanowire Static Induction Transistor,” *IEEE Electron Dev. Lett.*, accepted, doi: 10.1109/LED.2018.2886246.

[32] S. Sze, and K. Ng, “Thyristors and Power Devices,” in Physics of Semiconductor Devices, 3rd ed., Hoboken, NJ, US: Wiley, 2007, ch. 11, sec. 4.2, pp. 586-591.

[33] J. Nishizawa, T. Terasaki, and J. Shibata, “Field-effect transistor vs. analog transistor (static induction transistor),” *IEEE Trans. Electron Dev.*, vol. 22, no. 4, pp. 185-197 , 1975, doi: 10.1109/T-ED.1975.18103.

[34] W. Li, D. Ji, R. Tanaka, S. Mandal, M. Laurent and S. Chowdhury, "Demonstration of GaN Static Induction Transistor (SIT) Using Self-Aligned Process", *IEEE Electron Dev. Soc.*, vol. 5, no. 6, pp. 485-490, 2017, doi: 10.1109/JEDS.2017.2751065.

[35] K. Chung, J. Sui, B. Demory, C. Teng and P. Ku, "Monolithic integration of individually addressable light-emitting diode color pixels", *Appl. Phys. Lett.*, vol. 110, no. 11, p. 111103, 2017.

[36] S. Zhao, M. Kibria, Q. Wang, H. Nguyen and Z. Mi, "Growth of large-scale vertically aligned GaN nanowires and their heterostructures with high uniformity on SiOx by catalyst-free molecular beam epitaxy", *Nanoscale*, vol. 5, no. 12, p. 5283, 2013.

[37] W. Götz, M. Johnson, J. Walker, D. P. Bour, and R. A. Street, "Activation of acceptors in Mg-doped GaN grown by metalorganic chemical vaor deposition", *Appl. Phys. Lett.*, vol. 65, no. 5, pp. 667, 1996, doi: 10.1063/1.116503.

[38] P. Upadhyay and D. Saha, "Improved Mg Dopant Activation in p-GaN and Enhanced Electroluminescence in InGaN/GaN LEDs by Plasma Immersion Ion Implantation of Phosphorus", *physica status solidi (a),* 2018.

[39] E. Schubert, Light-emitting diodes. Cambridge: Cambridge Univ. Press, 2014.

[40] S. Zhou, M. Liu, H. Xu, Y. Liu, Y. Gao, X. Ding, S. Lan, Y. Fan, C. Cui, and S. Liu, "High-efficiency GaN-Based LED with patterned SiO2 current blocking layer deposited on patterened ITO", *Optics and Laser Tech.,* vol. 109, pp. 627-632, 2019, doi: 10.1016/j.optlastec.2018.09.049.

[41] T. M. Chen, S. J. Wang, K. M. Uang, H. Y. Kuo, C. C. Tsai, W. C. Lee, and H. Kuan, "Current Spreading and Blocking Designs for Improving Light Output Power from the Vertical-Strcutured GaN-Based Light-Emitting Diodes", *IEEE Photon. Tech.. Lett*., vol. 20, no. 9, pp. 703-705, 2008, doi:20.1109/LPT.2008.920031.

[42] V. Sheremet, M. Genç, M. Elçi, N. Sheremet, A. Aydinli, I. Altuntaşe, K. Ding, V. Avrutin, Ü. Özgürf, and H. Morkoç, "The role of ITO resistivity on current spreading and leakage in InGaN/GaN light emitting diodes", *Superlattices and Microstrucutres,* vol. 111, pp. 1177-1194, 2017, doi: 10.1016/j.smi.2017.08.026.

[43] Q. Li, Y. Li, M. Zhang, W. Ding, and F. Yun, "Current spreading in GaN-based light-emitting diodes", *Chinese Phys. B,* vol. 25, no. 11, pp. 117102, 2016, doi: 10.1088/1674-1056/25/11/117102.

[44] Y. C. Lin, S. J. Chang, Y. K. Su, T. Y. Tsai, C. S. Chang, S. C. Shei, C. W. Kou, and S. C. Chen, "InGaN/GaN light emitting diodes with Ni/Au, Ni/ITO and ITO p-type contacts," *Solid State Electron.,* vol. 47, pp. 849-853, 2003, doi: 10.1016/S0038-1101(02)00440-9.

[45] S. Bharadwaj, SM. Islam, K. Lee, A. Devine, V. Protasenko, S. Rouvimov, H. Xing, and D. Jena, “High-Temperature p-Type Polarization Doped AlGaN Classing for sub-250 nm deep-UV Quantum Well LEDs by MBE,” *Dev. Research Conf.*, 2017, doi: 10.1109/DRC.2017/7999517.

[46] Y. Lin and C. Hsu, "Study of schottky barrier heights of indium-tin-oxide on p-GaN using x-ray photoelectron spectroscopy and current-voltage measurements", *J. of Electronic Mater*., vol. 33, no. 9, pp. 1036-1040, 2004, doi: 10.1007/s11664-004-0032-y.

[47] F. Lacy, "Developing a theoretical relationship between electrical resistivity, temperature, and film thickness for conductors", *Nanoscale Research Lett.*, vol. 6, no. 1, 2011.

[48] M. Hartensveld, B. Melanson, and J. Zhang “Capacitive Current Spreading LED,” *IEEE Electron Dev. Lett.*, submitted, 2019.

[49] K. Kim, S. Jung, D. Kim, H. Kang, K. Im, J. Oh, J. Ha, J. Shin and J. Lee, "Effects of TMAH Treatment on Device Performance of Normally Off Al2O3/GaN MOSFET", *IEEE Electron Dev. Lett.*, vol. 32, no. 10, pp. 1376-1378, 2011.

[50] Q. Li, K. Westlake, M. Crawford, S. Lee, D. Koleske, J. Figiel, K. Cross, S. Fathololoumi, Z. Mi and G. Wang, "Optical performance of top-down fabricated InGaN/GaN nanorod light emitting diode arrays", *Optics Express*, vol. 19, no. 25, p. 25528, 2011.

[51] M. Hartensveld, G. Ouin, C. Liu, and J. Zhang, “Effect of KOH passivation for top-down fabricated InGaN nanowire light emitting diodes,” *J. of Appl. Phys*., vol. 126, 2019, doi: 10.1063/1.5123171.

[52] H. Kim, E. Brueckner, J. Song, Y. Li, S. Kim, C. Lu, J. Sulkin, K. Choquette, Y. Huang, R. Nuzzo and J. Rogers, "Unusual strategies for using indium gallium nitride grown on silicon (111)

for solid-state lighting", *Proc. of the National Academy of Sci*., vol. 108, no. 25, pp. 10072-10077, 2011.

[53] N. Guan, X. Dai, A. Babichev, F. Julien and M. Tchernycheva, "Flexible inorganic light emitting diodes based on semiconductor nanowires", *Chem. Sci.*, vol. 8, no. 12, pp. 7904-7911, 2017.

[54] D. Son, Y. Jo, J. Seo, C. Won, K. Im, Y. Lee, H. Jang, D. Kim, I. Kang and J. Lee, "Low voltage operation of GaN vertical nanowire MOSFET", *Solid-State Electron.,* vol. 145, pp. 1-7, 2018, doi: 10.1016/j.sse.2018.03.001.

[55] K. Keil, M. Hauptmann, J. Kretz, C. Constancias, L. Pain and J. Bartha, "Resolution and total blur: Correlation and focus dependencies in e-beam lithography", *J. Vac. Sci. Tech. B,* vol. 27, no. 6, p. 2722, 2009, doi: 10.1116/1.3246365.

[56] Z. Qin, Z. Chen, Y. Tong, X. Ding, X. Hu, T. Yu and G. Zhang, "Study of Ti/Au, Ti/Al/Au, and Ti/Al/Ni/Au ohmic contacts to n -GaN", *Appl. Phys. A,* vol. 78, no. 5, pp. 729-731, 2004.

[57] J. Plummer, M. Deal and P. Griffin, Silicon VLSI technology.

[58] M. Hartensveld, "Optimization of Dry and Wet GaN Etching to Form High Aspect Ratio Nanowires", Thesis, Rochester Institute of Technology, 2018.

[59] M. Yokoyama, J. Li, S. Su and Y. Su, "Characteristics of Indium-Tin Oxide Thin Film Etched by Reactive Ion Etching", *Japan. Jo. of Appl. Phys*., vol. 33, no. 1, 12, pp. 7057-7060, 1994.

[60] J. Zhou, "Indium tin oxide (ITO) deposition, patterning and Schottky contact fabrication", Masters, Rochester Institute of Technology, 2006.

[61] B. Ren et al., "Interface trap characterization of Al2O3/GaN vertical-type MOS capacitors on GaN substrate with surface treatments", *J. Alloys and Comp.*, vol. 767, pp. 600-605, 2018, doi: 10.1016/j.jallcom.2018.07.150.

[62] H. Cramer, J. Oliver and G. Dix, "MMIC capacitor dielectric reliability", *1998 GaAs Reliability Workshop. Proc.* (Cat. No.98EX219), doi: 10.1109/gaasrw.1998.768035.

[63] W. Li et al., "Activation of buried p-GaN in MOCVD-regrown vertical structures", *Appl. Phys. Letters*, vol. 113, no. 6, p. 062105, 2018, doi: 10.1063/1.5041879.

[64] M. Fatahilah et al., "Top-down GaN nanowire transistors with nearly zero gate hysteresis for parallel vertical electronics", *Scientific Reports*, vol. 9, no. 1, 2019, doi: 10.1038/s41598-019-46186-9.

[65] C. Kuo et al., "Low Temperature Activation of Mg-Doped GaN in O2 Ambient", *Japanese J. of Appl. Phys.*, vol. 41, no. 2, 2, pp. L112-L114, 2002. Available: 10.1143/jjap.41.l112.

[66] R. Haitz, and J. Y. Tsao, "Solid-state lighting: 'The case' 10 years after and future prospects", *Phys. Status Solidi A*, vol. 208, no. 1, pp. 17–29, 2011, doi: 10.1002/pssa.201026349.

[67] J. J. D. McKendry, R. P. Green, A. E. Kelly, Z. Gong, B. Guilhabert, D. Massoubre, E. Gu, and M. D. Dawson, "High-Speed Visible Light Communications Using Individual Pixels in a Micro Light-Emitting Diode Array", *IEEE Photonics Technol. Lett.*, vol. 22, no. 18, pp. 1346 - 1348, 2010, doi: 10.1109/LPT.2010.2056360.

[68] R. X. G. Ferreira, E. Xie, J. J. D. McKendry, S. Rajbhandari, H. Chun, G. Faulkner, S. Watson, A. E. Kelly, E. Gu, R. V. Penty, I. H. White, D. C. O'Brien, and M. D. Dawson, "High Bandwidth

GaN-Based Micro-LEDs for Multi-Gb/s Visible Light Communications", *IEEE Photonics Technol. Lett.*, vol. 28, no. 19, pp. 2023 - 2026, 2016, doi: 10.1109/LPT.2016.2581318.

[69] D.W.F. van Krevelen, and R. Poelman, "A Survey of Augmented Reality Technologies, Applications and Limitations", *The International Journal of Virtual Reality*, vol. 9, no. 2, pp. 1-20, 2010, doi: 10.1.1.454.8190.

[70] E. Moon, M. Kim, J. Roh, H. Kim, and J. Hahn, " Holographic head-mounted display with RGB light emitting diode light source", *Opt. Express*, vol. 22, no. 6, pp. 6526-6534, 2014, doi: 10.1364/OE.22.006526.

[71] Z. Liu, T. Huang, J. Ma, C. Liu and K. Lau, "Monolithic Integration of AlGaN/GaN HEMT on LED by MOCVD", *IEEE Electron Device Letter*, vol. 35, no. 3, pp. 330-332, 2014, doi: 10.1109/LED.2014.2300897.

[72] M. Atalla, A. Noor Elahi, C. Mo, Z. Jiang, J. Liu, S. Ashok and J. Xu, "On the design of GaN vertical MESFETs on commercial LED sapphire wafers", *Solid-State Electron*., vol. 126, pp. 23-31, 2016, doi: 10.1016/j.sse.2016.09.019

[73] J. Herrnsdorf, J. McKendry, Shuailong Zhang, Enyuan Xie, R. Ferreira, D. Massoubre, A. Zuhdi, R. Henderson, I. Underwood, S. Watson, A. Kelly, E. Gu and M. Dawson, "Active-Matrix GaN Micro Light-Emitting Diode Display With Unprecedented Brightness" *IEEE Trans. Electron Devices*, vol. 62, no. 6, pp. 1918-1925, 2015, doi: 10.1109/TED.2015.2416915.

[74] T. Ogi, L.B. Modesto-Lopez, F. Iskandar, and K. Okuyama, "Fabrication of a large area monolayer of silica particles on a sapphire substrate by a spin coating method," *Colloids Surf. A*, vol. 297, no. 1-3, pp. 71-78, 2007, doi: 10.1016/j.colsurfa.2006.10.027.

[75] G. Bjørnsen and J. Roots, “Plasma etching of polydimethylsiloxane: Effects from process gas composition and dc self-bias voltage,” *J. Vac. Sci. Technol. B,* vol. 29, pp. 011001, 2011, doi: 10.1116/1.3521489.

[76] J. Garra, T. Long, J. Currie, T. Schneider, R. White, and M. Paranjape, “Dry etching of polydimethylsiloxane for microfluidic systems,” *J. Vac. Sci. Technol*. A, vol. 20, pp. 975-982, 2002, doi: 10.1116/1.1460896.

[77] F. Yu, S. Yao, F. Römer, B. Witzigmann, T. Schimpke, M. Strassburg, A. Bakin, H. Schumacher, E. Peiner, H. Wasisto and A. Waag, " GaN nanowire arrays with nonpolar sidewalls for vertically integrated field-effect transistors", *Nanotechnology,* vol. 28, no. 9, p. 095206, 2017, doi: 10.1088/1361-6528/aa57b6.

[78] Y. Zhang, M. Sun, J. Perozek, Z. Liu, A. Zubair, D. Piedra, N. Chowdhury, X. Gao, K. Shepard and T. Palacios, "Large Area 1.2 kV GaN Vertical Power FinFETs with a Record Switching Figure-of-Merit", *IEEE Electron Dev. Lett*., pp. 1-1, 2018.

[79] A. Strollo and E. Napoli, "Optimal ON-resistance versus breakdown voltage tradeoff in superjunction power devices: a novel analytical model", *IEEE Trans. on Electron Dev*., vol. 48, no. 9, pp. 2161-2167, 2001.

[80] P. Pattison, M. Hansen, and J. Tsao, " LED lighting efficacy: Status and directions Efficacité de l'éclairage LED : état de l'art et directions", *Comptes Rendus Physique*, pp. 134-145, 2018, doi: 10.1016/j.crhy.2017.10.013.

[81] A. Cerdeira, M. Estrada, L. Marsal, J. Pallares and B. Iñiguez, "On the series resistance in staggered amorphous thin film transistors", *Microelectronics Reliability,* vol. 63, pp. 325-335, 2016, doi: 10.1016/j.microrel.2016.05.005.

[82] W. Ma, H. Hsu, C. Fang, C. Jao and T. Liao, "Impacts of channel film thickness on poly-Si tunnel thin-film transistors", Thin Solid Films, vol. 660, pp. 926-930, 2018, doi: 10.1016/j.tsf.2018.02.026.

[83] J. Park, K. Jang, D. Shin, M. Shin and J. Yi, "Gate-induced drain leakage current characteristics of p-type polycrystalline silicon thin film transistors aged by off-state stress", *Solid-State Electron*., vol. 148, pp. 20-26, 2018, doi: 10.1016/j.sse.2018.07.009.

[84] H. Amano, "Development of GaN-based blue LEDs and metalorganic vapor phase epitaxy of GaN and related materials", *Progress in Crystal Growth and Characterization of Materials*, vol. 62, no. 2, pp. 126-135, 2016, doi: 0.1016/j.pcrysgrow.2016.04.006.

[85] U. Mishra, S. Likun, T. Kazior and Y. Wu, "GaN-Based RF Power Devices and Amplifiers", *Proceedings of the IEEE*, vol. 96, no. 2, pp. 287-305, 2008, doi: 10.1109/JPROC.2007.911060.

[86] L. Kuritzky, C. Weisbuch and J. Speck, "Prospects for 100% wall-plug efficient III-nitride LEDs", *Optics Express*, vol. 26, no. 13, pp. 16600, 2018, doi: 10.1364/OE.26.016600.

[87] Y. Deshayes, R. Baillot, S. Joly, Y. Ousten and L. Bechou, "Overview on Sustainability, Robustness, and Reliability of GaN Single-Chip LED Devices", *IEEE Trans. on Dev. and Materials Reliability*, vol. 15, no. 4, pp. 621-625, 2015, doi: 10.1109/TDMR.2015.2488978.

[88] C. Zhao, N. Alfaraj, R. Chandra Subedi, J. Liang, A. Alatawi, A. Alhamoud, M. Ebaid, M. Alias, T. Ng and B. Ooi, "III-nitride nanowires on unconventional substrates: From materials to optoelectronic device applications", *Progress in Quantum Electronics*, vol. 61, pp. 1-31, 2018, doi: 10.1016/j.pquantelec.2018.07.001.

[89] Z. Liu, W. Chong, K. Wong and K. Lau, "GaN-based LED micro-displays for wearable applications", *Microelectronic Engineering*, vol. 148, pp. 98-103, 2015, doi: 10.1016/j.mee.2015.09.007.

[90] Z. Fan, J. Lin and H. Jiang, "III-nitride micro-emitter arrays: development and applications", *J. of Phys. D: Appl. Phys*., vol. 41, no. 9, p. 094001, 2008, doi: 10.1088/0022-3727/41/9/094001.

[91] Y. Cai, X. Zou, C. Liu and K. Lau, "Voltage-Controlled GaN HEMT-LED Devices as Fast-Switching and Dimmable Light Emitters", *IEEE Electron Dev. Lett*., vol. 39, no. 2, pp. 224-227, 2018, doi: 0.1109/LED.2017.2781247.

[92] B. Tull, Z. Basaran, D. Gidony, A. Limanov, J. Im, I. Kymissis and V. Lee, "26.2:Invited Paper: High Brightness, Emissive Microdisplay by Integration of III-V LEDs with Thin Film Silicon Transistors", *SID Symposium Digest of Technical Papers*, vol. 46, no. 1, pp. 375-377, 2015, doi: 10.1002/sdtp.10256.

[93] D. Look and R. Molnar, "Degenerate layer at GaN/sapphire interface: Influence on Hall-effect measurements", *Appl. Phys. Lett*., vol. 70, no. 25, pp. 3377-3379, 1997, doi: 10.1063/1.119176.

[94] M. Cheong, K. Kim, C. Oh, N. Namgung, G. Yang, C. Hong, K. Lim, E. Suh, K. Nahm, H. Lee, D. Lim and A. Yoshikawa, "Conductive layer near the GaN/sapphire interface and its effect on electron transport in unintentionally doped n-type GaN epilayers", *Appl. Phys. Lett*., vol. 77, no. 16, pp. 2557-2559, 2000, doi: 10.1063/1.1318728.

[95] H. Yu, M. Kemal Ozturk, S. Ozcelik and E. Ozbay, "A study of semi-insulating GaN grown on AlN buffer/sapphire substrate by metalorganic chemical vapor deposition", *J. Crystal Growth*, vol. 293, no. 2, pp. 273-277, 2006, doi: 10.1016/j.jcrysgro.2006.05.056.

[96] D. Cai, A. Neyer, R. Kuckuk and H. Heise, "Optical absorption in transparent PDMS materials applied for multimode waveguides fabrication", *Optical Materials*, vol. 30, no. 7, pp. 1157-1161, 2008, doi: 0.1016/j.optmat.2007.05.041.

[97] C. Brennan, C. Neumann and S. Vitale, "Comparison of gate dielectric plasma damage from plasma-enhanced atomic layer deposited and magnetron sputtered TiN metal gates", *J. of Appl. Phys.*, vol. 118, no. 4, p. 045307, 2015.

[98] B. Dong, J. Lin, N. Wang, L. Jiang, Z. Liu, X. Hu, K. Cheng, and H. Yu, "Trap behaviours characterization of AlGaN/GaN high electron mobility transistors by room-temperature transient capacitance measurement", *AIP Advances*, vol. 6, p. 095021, 2016, doi: 10.1063/1.4963740.

[99] Z. Liu, W. Chong, K. Wong and K. Lau, "GaN-based LED micro-displays for wearable applications", *Microelectronic Eng.*, vol. 148, pp. 98-103, 2015, doi: 10.1016/j.mee.2015.09.007.

[100] Z. Fan, J. Lin and H. Jiang, "III-nitride micro-emitter arrays: development and applications", *J. Phys. D*, vol. 41, no. 9, p. 094001, 2008, doi: 10.1088/0022-3727/41/9/094001.

[101] Y. Cai, X. Zou, C. Liu and K. Lau, "Voltage-Controlled GaN HEMT-LED Devices as Fast-Switching and Dimmable Light Emitters", *IEEE Electron Dev. Lett.*, vol. 39, no. 2, pp. 224-227, 2018, doi: 10.1109/led.2017.2781247.

[102] I. Pappas, S. Siskos and C. Dimitriadis, New Developments in Liquid Crystals,, 1st ed. *InTech*, 2021, pp. 147-170.

[103] J. McKendry et al., "Individually Addressable AlInGaN Micro-LED Arrays With CMOS Control and Subnanosecond Output Pulses", *IEEE Photon. Tech. Lett.*, vol. 21, no. 12, pp. 811-813, 2009, doi: 10.1109/lpt.2009.2019114.

[104] S. Nakamura and M. Krames, "History of Gallium–Nitride-Based Light-Emitting Diodes for Illumination", *Proc. IEEE*, vol. 101, no. 10, pp. 2211-2220, 2013, doi: 10.1109/jproc.2013.2274929.

[105] C. Liu, Y. Cai, X. Zou and K. Lau, "Low-Leakage High-Breakdown Laterally Integrated HEMT-LED via n-GaN Electrode", *IEEE Photon. Techn. Lett.*, vol. 28, no. 10, pp. 1130-1133, 2016, doi: 10.1109/lpt.2016.2532338.

[106] Y. Huang, E. Hsiang, M. Deng and S. Wu, "Mini-LED, Micro-LED and OLED displays: present status and future perspectives", *Light: Sci. & App.*, vol. 9, no. 1, 2020, doi: 10.1038/s41377-020-0341-9.

[107] K. Yeo, W. Ng, M. Soh and T. Teo, "Micro-LED arrays for display and communication: Device structure and driver architecture", *2017 IEEE 12th Intern. Conf. on ASIC (ASICON)*, 2017, doi: 10.1109/asicon.2017.8252645.

[108] X. Ding, Y. Zhou and J. Cheng, "A review of gallium nitride power device and its applications in motor drive", *CES Trans. Electr. Mach. Syst.*, vol. 3, no. 1, pp. 54-64, 2019, doi: 10.30941/cestems.2019.00008.

[109] H. Chiu and S. Cheng, "LED Backlight Driving System for Large-Scale LCD Panels", *IEEE Trans. on Industrial Electronics*, vol. 54, no. 5, pp. 2751-2760, 2007, doi: 10.1109/tie.2007.899938.

[110] M. Hartensveld and J. Zhang, "Monolithic Integration of GaN Nanowire Light-Emitting Diode With Field Effect Transistor", *IEEE Electron Dev. Lett.*, vol. 40, no. 3, pp. 427-430, 2019, doi: 10.1109/LED.2019.2895846.

[111] S. Lee, H. Kim, M. Choi, and K. Byun, “New design and application of high efficiency LED driving system for RGB-LED backlight in LCD display,” *IEEE Power Electron. Specialists Conf.*, 2006, doi: 10.1109/pesc.2006.1711925.

[112] T. Wu, C.-W. Sher, Y. Lin, C.-F. Lee, S. Liang, Y. Lu, S.-W. H. Chen, W. Guo, H.-C. Kuo, and Z. Chen, “Mini-LED and Micro-LED: Promising Candidates for the Next Generation Display Technology,” *Appl. Sci.*, vol. 8, no. 9, pp. 1557, 2018, doi: 10.3390/app8091557.

[113] T. Tsunemasa, "Present Status of Energy Saving Technologies and Future Prospect in White LED Lighing", *IEEJ Trans*., vol. 3, pp. 21-26, 2008, doi: 10.1002/tee.20228.

[114] S. Nakamura and M. Krames, "History of Gallium–Nitride-Based Light-Emitting Diodes for Illumination", *Proceedings of the IEEE*, vol. 101, no. 10, pp. 2211-2220, 2013, doi: 0.1109/JPROC.2013.2274929.

[115] F. Li, D. Chen, X. Song and Y. Chen, "LEDs: A Promising Energy-Saving Light Source for Road Lighting", *IEEE PES Asia-Pacific*, 2009, doi: 10.1109/APPEEC.2009.4918460.

[116] S. Kulkarni, A. Darekar and P. Joshi, "A Survey on Li-Fi technology", Proc. Int. Conf. Wireless Commun., *Signal Process. Netw.*, 2016, doi: 10.1109/WiSPNET.2016.7566413.

[117] P. Krishnan, "Design of Collision Detection System for Smart Car Using Li-Fi and Ultrasonic Sensor", *IEEE Trans. on Vehicular Tech*., vol. 67, no. 12, pp. 11420-11426, 2018, doi: 10.1109/TVT.2018.2870995.

[118] W. Götz, M. Johnson, J. Walker, D. P. Bour, and R. A. Street, "Activation of acceptors in Mg-doped GaN grown by metalorganic chemical vapor deposition", *Appl. Phys. Lett*., vol. 65, no. 5, pp. 667, 1996, doi: 10.1063/1.116503.

[119] B. Cao et al., "Effects of current crowding on light extraction efficiency of conventional GaN-based light-emitting diodes", *Optics Express*, vol. 21, no. 21, p. 25381, 2013, doi: 10.1364/oe.21.025381.

[120] J. Simon, V. Protasenko, C. Lian, H. Xing and D. Jena, "Polarization-Induced Hole Doping in Wide-Band-Gap Uniaxial Semiconductor Heterostructures", *Science*, vol. 327, no. 5961, pp. 60-64, 2009, doi: 10.1126/science.1183226.

[121] R. Chuang, Y. Chiu and C. Yu, "Iridium-based semi-transparent current spreading layer on short-period-superlattice (SPS) tunneling contact of InGaN/GaN LEDs", *Solid-State Electronics*, vol. 50, no. 7-8, pp. 1212-1215, 2006, doi: 10.1016/j.sse.2006.06.003.

[122] A. Ebong, S. Arthur, E. Downey, X. Cao, S. LeBoeuf and D. Merfeld, "Device and circuit modeling of GaN/InGaN light emitting diodes (LEDs) for optimum current spreading", *Solid-State Electronics*, vol. 47, no. 10, pp. 1817-1823, 2003, doi: 10.1016/s0038-1101(03)00139-4.

[123] B. Saini, S. Adhikari, S. Pal and A. Kapoor, "Polarization compensation at low p-GaN doping density in InGaN/GaN p-i-n solar cells: Effect of InGaN interlayers", *Superlattices and Microstructures*, vol. 107, pp. 127-135, 2017. doi: 10.1016/j.spmi.2017.04.014.

[124] C. Hu, Modern semiconductor devices for integrated circuits. Boston: Pearson, 2010.

[125] E. Schubert, Light-emitting diodes, 2nd ed. Cambridge: Cambridge Univ. Press, 2014.

[126] G. Gupta, B. Rajasekharan and R. Hueting, "Electrostatic Doping in Semiconductor Devices", *IEEE Trans. on Electron Dev.*, vol. 64, no. 8, pp. 3044-3055, 2017, doi: 10.1109/ted.2017.2712761.

[127] H. Sood, V. Srivastava and G. Singh, "Advanced MOSFET Technologies for Next Generation Communication Systems - Perspective and Challenges: A Review", *J. of Eng. Sci. and Techn. Review*, vol. 11, no. 3, pp. 180-195, 2018, doi: 10.25103/jestr.113.25.

[128] Y. Lin and C. Hsu, "Study of schottky barrier heights of indium-tin-oxide on p-GaN using x-ray photoelectron spectroscopy and current-voltage measurements", *J. of Electronic Mater.*, vol. 33, no. 9, pp. 1036-1040, 2004, doi: 10.1007/s11664-004-0032-y.

[129] J. Simmons, "Poole-Frenkel Effect and Schottky Effect in Metal-Insulator-Metal Systems", *Physical Review*, vol. 155, no. 3, pp. 657-660, 1967, doi: 10.1103/physrev.155.657.

[130] P. Kozodoy, M. Hansen, S. DenBaars and U. Mishra, "Enhanced Mg doping efficiency in Al0.2Ga0.8N/GaN superlattices", *Appl. Phys. Lett.*, vol. 74, no. 24, pp. 3681-3683, 1999, doi: 10.1063/1.123220.

[131] E. Schubert, W. Grieshaber and I. Goepfert, "Enhancement of deep acceptor activation in semiconductors by superlattice doping", *Appl. Phys. Lett.*, vol. 69, no. 24, pp. 3737-3739, 1996, doi: 10.1063/1.117206.

[132] J. Jamaux, "Polarization-induced doping and its application to light-emitting diodes", Thesis, McGill University, 2014.

[133] G. Verzellesi et al., "Efficiency droop in InGaN/GaN blue light-emitting diodes: Physical mechanisms and remedies", *J. Appl. Phys.*, vol. 114, no. 7, p. 071101, 2013, doi: 10.1063/1.4816434.

[134] M. Kneissl and J. Rass, III-Nitride Ultraviolet Emitters: Technology and Applications (Springer International Publishing, 2016).

[135] H. Hirayama, N. Maeda, S. Fujikawa, S. Toyoda and N. Kamata, "Recent progress and future prospects of AlGaN-based high-efficiency deep-ultraviolet light-emitting diodes", *Japanese J. of Appl. Phys.*, vol. 53, no. 10, p. 100209, 2014. doi: 10.7567/jjap.53.100209.

[136] S. Lee, H. Kim, M. Choi, and K. Byun, "New design and application of high efficiency LED driving system for RGB-LED backlight in LCD display," *IEEE Power Electron. Specialists Conf.*, 2006, doi: 10.1109/pesc.2006.1711925.

[137] P. Jarvis, O. Autin, E. Goslan and F. Hassard, "Application of Ultraviolet Light-Emitting Diodes (UV-LED) to Full-Scale Drinking-Water Disinfection", *Water*, vol. 11, no. 9, p. 1894, 2019, doi: 10.3390/w11091894.

[138] S. Nakamura and M. Krames, "History of Gallium–Nitride-Based Light-Emitting Diodes for Illumination", *Proc. of the IEEE*, vol. 101, no. 10, pp. 2211-2220, 2013, doi: 0.1109/JPROC.2013.2274929.

[139] T. Tsunemasa, "Present Status of Energy Saving Technologies and Future Prospect in White LED Lighing", *IEEJ Trans.*, vol. 3, pp. 21-26, 2008, doi: 10.1002/tee.20228.

[140] Y. Taniyasu, M. Kasu and T. Makimoto, "An aluminium nitride light-emitting diode with a wavelength of 210 nanometres", *Nature*, vol. 441, no. 7091, pp. 325-328, 2006, doi: 10.1038/nature04760.

[141] F. Lacy, "Developing a theoretical relationship between electrical resistivity, temperature, and film thickness for conductors", *Nanoscale Res. Lett.*, vol. 6, no. 1, 2011, doi: 10.1186/1556-276x-6-636.

[142] M. Hartensveld, B. Melanson, and J. Zhang, "Electrostatic Field Effect Light-Emitting Diode", *IEEE Photon. J.*, vol 12, no 3, 2020, doi: 10.1109/JPHOT.2020.2992278.

[143] G. Gupta, B. Rajasekharan and R. Hueting, "Electrostatic Doping in Semiconductor Devices", *IEEE Trans. on Electron Dev.*, vol. 64, no. 8, pp. 3044-3055, 2017, doi: 10.1109/ted.2017.2712761.

[144] H. Sood, V. Srivastava and G. Singh, "Advanced MOSFET Technologies for Next Generation Communication Systems - Perspective and Challenges: A Review", *J. of Eng. Sci. Techn. Rev.*, vol. 11, no. 3, pp. 180-195, 2018. doi: 10.25103/jestr.113.25.

[145] C. Hu, Modern semiconductor devices for integrated circuits. Boston: Pearson, 2010.

[146] M. Pawlik et al., "Electrical and Chemical Studies on Al2O3 Passivation Activation Process", Energy Procedia, vol. 60, pp. 85-89, 2014. doi: 10.1016/j.egypro.2014.12.347.

[147] P. Kozodoy, M. Hansen, S. DenBaars and U. Mishra, "Enhanced Mg doping efficiency in Al0.2Ga0.8N/GaN superlattices", *Appl. Phys. Lett.*, vol. 74, no. 24, pp. 3681-3683, 1999, doi: 10.1063/1.123220.

[148] S. Zhao, J. Lu, X. Hai and X. Yin, "AlGaN Nanowires for Ultraviolet Light-Emitting: Recent Progress, Challenges, and Prospects", *Micromachines*, vol. 11, no. 2, p. 125, 2020, doi: 10.3390/mi11020125.

[149] H. Kim, E. Brueckner, J. Song, Y. Li, S. Kim, C. Lu, J. Sulkin, K. Choquette, Y. Huang, R. Nuzzo and J. Rogers, "Unusual strategies for using indium gallium nitride grown on silicon (111) for solid-state lighting", *Proc. of the National Academy of Sci.*, vol. 108, no. 25, pp. 10072-10077, 2011, doi: 10.1073/pnas.1102650108.

[150] N. Guan, X. Dai, A. Babichev, F. Julien and M. Tchernycheva, "Flexible inorganic light emitting diodes based on semiconductor nanowires", *Chem. Sci.*, vol. 8, no. 12, pp. 7904-7911, 2017, doi: 10.1039/C7SC02573D.

[151] N. Guan et al., "Flexible White Light Emitting Diodes Based on Nitride Nanowires and Nanophosphors", *ACS Photon.*, vol. 3, no. 4, pp. 597-603, 2016, doi: 10.1021/acsphotonics.5b00696.

[152] M. Hartensveld, G. Ouin, C. Liu and J. Zhang, "Effect of KOH passivation for top-down fabricated InGaN nanowire light emitting diodes", *J. of Appl. Phys*., vol. 126, no. 18, p. 183102, 2019, doi: 10.1063/1.5123171.

[153] F. Yu et al., "GaN nanowire arrays with nonpolar sidewalls for vertically integrated field-effect transistors", *Nanotechn.*, vol. 28, no. 9, p. 095206, 2017, doi: 10.1088/1361-6528/aa57b6.

[154] W. Chen et al., "GaN nanowire fabricated by selective wet-etching of GaN micro truncated-pyramid", J. of Crystal Growth, vol. 426, pp. 168-172, 2015, doi: 10.1016/j.jcrysgro.2015.06.007.

[155] M. Elwenspoek, "On the Mechanism of Anisotropic Etching of Silicon", *J. Electrochem. Soc.*, vol. 140, no. 7, pp. 2075-2080, 1993, doi: 10.1149/1.2220767.

[156] M. Xie, S. Seutter, W. Zhu, L. Zheng, H. Wu and S. Tong, "Anisotropic Step-Flow Growth and Island Growth of GaN(0001) by Molecular Beam Epitaxy", *Phys. Rev. Lett.*, vol. 82, no. 13, pp. 2749-2752, 1999, doi: 10.1103/physrevlett.82.2749.

[157] T. Li et al., "Growth behavior of ammonothermal GaN crystals grown on non-polar and semi-polar HVPE GaN seeds", *Cryst. Eng. Comm.*, vol. 21, no. 33, pp. 4874-4879, 2019, doi: 10.1039/c9ce00806c.

[158] M. DeVre, R. Westerman, G. Muir and L. Bellon, "Advances in GaN Dry Etching Process Capabilities", Unaxis Wafer Processing, Available: http://plasma-therm.com/pdfs/papers/7.%20Advances%20in%20GaN%20Dry%20Etching%20Process%20Capabilities.pdf.

[159] B. Wang et al., "Development of antibacterial and high light transmittance bulk materials: Incorporation and sustained release of hydrophobic or hydrophilic antibiotics", *Colloids Surf. B*, vol. 141, pp. 483-490, 2016, doi: 10.1016/j.colsurfb.2016.02.021.

[160] Q. Li et al., "Optical performance of top-down fabricated InGaN/GaN nanorod light emitting diode arrays", *Optics Express*, vol. 19, no. 25, p. 25528, 2011, doi: 10.1364/oe.19.025528.

[161] Y. Liu, K. Zhang, B. Hyun, H. Kwok and Z. Liu, "High-Brightness InGaN/GaN Micro-LEDs With Secondary Peak Effect for Displays", *IEEE Electron Dev. Lett.*, vol. 41, no. 9, pp. 1380-1383, 2020, doi: 10.1109/led.2020.3014435.

[162] J. Zhong, A. Abileah, J. Hogan, N. Vergith and S. Thomsen, "Ultralow-reflectance organic black matrix for color TFT-LCDs", *Display Dev. Sys. II*, 1998, doi: 10.1117/12.319691.

[163] K. Liang, W. Kuo, H. Shen, P. Yu, Y. Fang and C. Lin, "Advances in color-converted micro-LED arrays", *Japanese J. Appl. Phys.*, vol. 60, no., p. SA0802, 2020, doi: 10.35848/1347-4065/abba0f.

[164] C. Chen, H. Chuang, G. Chi, C. Chuo and J. Chyi, "Stimulated-emission spectra of high-indium-content InGaN/GaN multiple-quantum-well structures", *Appl. Phys. Lett.*, vol. 77, no. 23, pp. 3758-3760, 2000, doi: 10.1063/1.1332403.

[165] Y. Ra et al., "Full-Color Single Nanowire Pixels for Projection Displays", *Nano Letters*, vol. 16, no. 7, pp. 4608-4615, 2016, doi 10.1021/acs.nanolett.6b01929.

[166] Ž. Gačević, D. Gómez Sánchez and E. Calleja, "Formation Mechanisms of GaN Nanowires Grown by Selective Area Growth Homoepitaxy", *Nano Letters*, vol. 15, no. 2, pp. 1117-1121, 2015, doi: 10.1021/nl504099s.

[167] B. Mitchell, V. Dierolf, T. Gregorkiewicz and Y. Fujiwara, "Perspective: Toward efficient GaN-based red light emitting diodes using europium doping", *J. Appl. Phys.*, vol. 123, no. 16, p. 160901, 2018, doi: 10.1063/1.5010762.

[168] J. Zhan et al., "Investigation on strain relaxation distribution in GaN-based μLEDs by Kelvin probe force microscopy and micro-photoluminescence", *Optics Express*, vol. 26, no. 5, p. 5265, 2018, doi: 10.1364/oe.26.005265.

[169] A. Daami et al., "Green InGaN/GaN based LEDs: high luminance and blue shift", *Gallium Nitride Mater. Dev. XIV*, 2019, doi: 10.1117/12.2509396.

[170] M. Reshchikov, J. McNamara, H. Helava, A. Usikov and Y. Makarov, "Two yellow luminescence bands in undoped GaN", *Scientific Reports*, vol. 8, no. 1, 2018, doi: 10.1038/s41598-018-26354-z.

[171] T. Shibin Krishna et al., "Probing the correlation between structure, carrier dynamics and defect states of epitaxial GaN film on $(11\bar{2}0)$ sapphire grown by rf-molecular beam epitaxy", *RSC Advances*, vol. 5, no. 89, pp. 73261-73267, 2015, doi: 10.1039/c5ra10099b.

[172] M. Lee, S. Wang, Y. Yeh, P. Liao and J. Sheu, "Light-emitting diodes with surface gallium nitride p–n homojunction structure formed by selective area regrowth", *Scientific Reports*, vol. 9, no. 1, 2019, doi: 10.1038/s41598-019-40095-7.

[173] E. Evropeitsev et al., "State-of-the-art and prospects for intense red radiation from core–shell InGaN/GaN nanorods", *Scientific Reports*, vol. 10, no. 1, 2020, doi: 10.1038/s41598-020-76042-0.

[174] S. Zhou et al., "The effect of nanometre-scale V-pits on electronic and optical properties and efficiency droop of GaN-based green light-emitting diodes", *Scientific Reports*, vol. 8, no. 1, 2018, doi: 10.1038/s41598-018-29440-4.

[175] R. Yapparov et al., "Variations of light emission and carrier dynamics around V-defects in InGaN quantum wells", *J. Appl. Phys.*, vol. 128, no. 22, p. 225703, 2020, doi: 10.1063/5.0031863.

[176] K. Song et al., "Characteristics of indium incorporation in InGaN/GaN multiple quantum wells grown on a-plane and c-plane GaN", *Appl. Phys. Lett.*, vol. 100, no. 21, p. 212103, 2012, doi: 10.1063/1.4720507.

[177] Z. Quan, L. Wang, C. Zheng, J. Liu, and F. Jiang, "Roles of V-shaped pits on the improvement of quantum efficiency in InGaN/GaN multiple quantum well light-emitting diodes", *J. Appl. Phys.*, vol. 116, no. 18, p. 183107, 2014, doi: 10.1063/1.4901828.

[178] Z. Liu et al., "Micro-light-emitting diodes with quantum dots in display technology", *Light: Sci. & App.*, vol. 9, no. 1, 2020, doi: 10.1038/s41377-020-0268-1.

[179] H. Haas et al., "Introduction to indoor networking concepts and challenges in LiFi", *J. of Optical Comm. and Networking*, vol. 12, no. 2, p. A190, 2019, doi: 10.1364/jocn.12.00a190.

[180] Y. Taniyasu, M. Kasu and T. Makimoto, "An aluminium nitride light-emitting diode with a wavelength of 210 nanometres", *Nature*, vol. 441, no. 7091, pp. 325-328, 2006, doi: 10.1038/nature04760.

[181] T. Niwa, T. Fujii and T. Oka, "High carrier activation of Mg ion-implanted GaN by conventional rapid thermal annealing", *Appl. Phys. Express*, vol. 10, no. 9, p. 091002, 2017, doi: 10.7567/apex.10.091002.

[182] C. Ronning, "Ion implantation into gallium nitride", *Phys. Reports*, vol. 351, no. 5, pp. 349-385, 2001, doi: 10.1016/s0370-1573(00)00142-3.

[183] G. Aluri et al., "Microwave annealing of Mg-implanted andin situBe-doped GaN", *J. of Appl. Phys.*, vol. 108, no. 8, p. 083103, 2010, doi: 10.1063/1.3493266.

[184] Y. Li and C. Chen, "A Novel Single-Stage High-Power-Factor AC-to-DC LED Driving Circuit With Leakage Inductance Energy Recycling", *IEEE Tran. on Industrial Electronics*, vol. 59, no. 2, pp. 793-802, 2012, doi: 10.1109/TIE.2011.2151817.

[185] W. Götz, N. Johnson, C. Chen, H. Liu, C. Kuo and W. Imler, "Activation energies of Si donors in GaN", *Appl. Phys. Lett.*, vol. 68, no. 22, pp. 3144-3146, 1996, doi: 10.1063/1.115805.

[186] K. Ueno, A. Kobayashi and H. Fujioka, "Characteristics of unintentionally doped and lightly Si-doped GaN prepared via pulsed sputtering", *AIP Advances*, vol. 9, no. 7, p. 075123, 2019, doi: 10.1063/1.5103185.

[187] S. Krishnamoorthy, F. Akyol and S. Rajan, "InGaN/GaN tunnel junctions for hole injection in GaN light emitting diodes", *Appl. Phys. Lett.*, vol. 105, no. 14, p. 141104, 2014, doi: 10.1063/1.4897342.

[188] J. Che et al, “Doping-Induced Energy Barriers to Improve the Current Spreading Effect for AlGaN-Based Ultaviolet-B Light-Emitting Diodes”, *IEEE Electron Dev. Lett.*, vol. 41, no. 7, p. 1001-1004, 2020, doi: 10.1109/LED.2020.2997476.

[189] Z. Zhang et al., “Hole Transport Manipulation To Improve the Hole Injection for Deep Ultaviolet Light-Emitting Diodes”, *ACS Photonics*, vol. 4, no. 7, p. 1846-1850, 2017, doi: 10.1021/acsphotonics.7b00443.

[190] Z. Zhang et al, “UVA light-emitting diode grown on Si substrate with enhanced electron and hole injections”, *Optics Lett*., vol. 42, no. 21, p. 4533-4536, 2017, doi: 10.1364/OL.42.004533.

[191] Z. Zhang et. al, “A charge inverter for III-nitride light-emittiing diodes”, *Appl. Phys. Lett*., vol. 108, no. 133502, p. 1-5, 2016, doi: 10.1063/1.4945257.

[192] H. Zhu et al., "Ultralow-Threshold Laser Realized in Zinc Oxide", *Adv. Mater.*, vol. 21, no. 16, pp. 1613-1617, 2009, doi: 10.1002/adma.200802907.

[193] H. Wang et al., "Ultraviolet electroluminescence properties of the p-NiO/n-GaN-based heterojunction diodes", *Semiconductor Sci. and Tech.*, vol. 26, no. 12, p. 125015, 2011, doi: 10.1088/0268-1242/26/12/125015.

[194] H. Wang et al., "AlGaN/GaN MIS-HEMTs With High Quality ALD-Al2O3 Gate Dielectric Using Water and Remote Oxygen Plasma As Oxidants", *IEEE J. of the Electron Dev. Soc.*, vol. 6, pp. 110-115, 2018, doi: 10.1109/jeds.2017.2779172.

[195] Z. Zhang, Y. Guo and J. Robertson, "Atomic structure and band alignment at Al2O3/GaN, Sc2O3/GaN and La2O3/GaN interfaces: A first-principles study", *Microelectronic Eng.*, vol. 216, p. 111039, 2019, doi: 10.1016/j.mee.2019.111039.

[196] S. Mahajan, A. Dhaul, R. Laishram, S. Kapoor, S. Vinayak and B. Sehgal, "Micro-structural evaluation of Ti/Al/Ni/Au ohmic contacts with different Ti/Al thicknesses in AlGaN/GaN HEMTs", *Mater. Science and Eng.: B*, vol. 183, pp. 47-53, 2014, doi: 10.1016/j.mseb.2013.12.005.

[197] X. Li, J. Zhang, M. Sun, B. Ye, J. Huang, Z. Xu, W. Dong, J. Wang and K. Xu, "Effect of annealing temperature on Ti/Al/Ni/Au ohmic contacts on undoped AlN films", *J. of Semiconductors*, vol. 38, no. 11, p. 116002, 2017, doi: 10.1088/1674-4926/38/11/116002.

[198] J. Wu, L. Register and E. Rosenbaum, "Trap-assisted tunneling current through ultra-thin oxide", *1999 IEEE International Reliability Phys. Symp. Proc. 37th Annual*, doi: 10.1109/RELPHY.1999.761644.

[199] M. Mirza, F. Schupp, J. Mol, D. MacLaren, G. Briggs and D. Paul, "One dimensional transport in silicon nanowire junction-less field effect transistors", *Scientific Reports*, vol. 7, no. 1, 2017.

[200] S. Rishton, K. Ismail, J. Chu and K. Chan, "An MOS transistor with Schottky source/drain contacts and a self-aligned low-resistance T-gate", *Microelectronic Engineering*, vol. 35, no. 1-4, pp. 361-363, 1997.

[201] G. Ouin, "Etching Processes for GaN Nanowire Fabrication and Single Photon Emitter Device Application", Thesis, Rochester Institute of Technology, 2019.

[202] M. Higashiwaki, K. Sasaki, A. Kuramata, T. Masui and S. Yamakoshi, "Development of gallium oxide power devices", *physica status solidi (a)*, vol. 211, no. 1, pp. 21-26, 2013.

[203] J. Hogan, S. Kaun, E. Ahmadi, Y. Oshima and J. Speck, "Chlorine-based dry etching ofβ-Ga_2O_3", *Semi. Sci. and Tech.,* vol. 31, no. 6, p. 065006, 2016.