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# **Process Investigations on Sputter Deposited Indium Tungsten Oxide TFT**

RISHMITHAA SIVAKANTHAN  
May 2021

A Thesis Submitted  
In Partial Fulfillment  
of the Requirements for the Degree of  
Master of Science  
in  
Electrical Engineering



*Department of Electrical and Microelectronic Engineering*

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# **Process investigations on Sputter Deposited Indium Tungsten Oxide TFT**

Rishmithaa Sivakanthan

A thesis submitted in partial fulfillment of the requirements for the degree of  
Master of Science in Electrical Engineering

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# Acknowledgment

I would like to convey my gratitude to all the people who have generously helped and inspired me in every possible way to complete my thesis. First, I would also like to thank my committee members, Dr. Robert Pearson and Dr. Ivan Puchades for their valuable input and productive feedback as they guided me throughout the project. Next, I would like to thank the members of the team: Eli Powell, Muhammed Salahuddin Kabir and Glenn Packard, not only for their professional support but also for our building of comradery as we worked towards accomplishing our goals. I would also like to acknowledge the SMFL staff: Sean O'Brien, John Nash, Bruce Tollesen, Rich Battaglia and Thomas Grimsley for their tireless work, behind the scenes, in ensuring smooth operation in the cleanroom.

Finally, I would like to specially thank my advisor, Dr. Karl Hirschman. His constant sense of optimism made our work enjoyable and worthwhile even when faced against our greatest challenges and hurdles. I am grateful to have witnessed his immense dedication to his students, firsthand, and I will earnestly strive to reciprocate that dedication on to others. I consider him my mentor and hope to continue learning from him.

# Abstract

Indium-Tungsten Oxide (IWO) has been investigated as a potential semiconductor material for next-generation display devices. Several publications have reported on IWO thin-film transistors (TFTs) with a channel mobility  $\mu_{ch} \sim 20 \text{ cm}^2/\text{Vs}$ , approximately 2X higher than typically reported for Indium-Gallium-Zinc Oxide (IGZO). However, other attributes of the device characteristics have not performed as well as IGZO such as the subthreshold behavior. This work presents a study on the electronic properties of sputtered IWO, with the sputter ambient (i.e. percent  $\text{O}_2$ ) and  $\text{O}_2$  annealing conditions as the primary factors investigated. In the early stages of the study, a problem with the IWO target surface condition was found to be responsible for non-reproducible TFT properties. This initiated an extensive investigation on the details of target reconditioning, pre-sputter conditions and reactive sputter ambient with oxygen. IWO sputter recipes and procedures were implemented which ensured consistent plasma characteristics and target surface condition.

Reactive sputter conditions with low  $\text{O}_2$  content resulted in electrical behavior that was very different from argon-only sputtering (zero percent oxygen). IWO TFTs processed with 1.2%  $\text{O}_2$  sputter ambient, followed by  $\text{O}_2$  annealing at  $300^\circ\text{C}$  for 8-10 hours demonstrated promising current-voltage characteristics, with a low-field channel mobility  $\mu_{ch} \sim 18 \text{ cm}^2/\text{Vs}$  @  $V_{DS} = 0.1\text{V}$ . While higher oxygen content sputter conditions (10%  $\text{O}_2$ ) demonstrated a higher post-anneal resistivity, the device operation was inferior to the low oxygen treatment TFT. This was apparent in both on-state and off-state conditions, with the low oxygen treatment exhibiting higher current drive and steeper subthreshold. Increasing the  $\text{O}_2$  anneal temperature to  $350^\circ\text{C}$  on TFTs with the low oxygen treatment showed encouraging gate-controlled channel modulation for a 2 hour anneal. Raising this temperature to  $400^\circ\text{C}$  resulted in reduced gate control and current modulation, suggesting the onset of an additional defect mechanism. Degradation in device operation demonstrated by the high oxygen treatment as-sputtered material, or by aggressive  $\text{O}_2$  annealing at  $T > 350^\circ\text{C}$ , may have a similar origin.

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# *Chapter 1*

## **1.1 Introduction**

With the increase in dependency and use of complex devices day-to-day, there is a need for displays with high resolution, low weight, good image quality and quick response rate. Catering to these expectations led to a growth in the active-matrix liquid crystal display (AMLCD) market. The active-matrix Flat Panel Displays use a backplane consisting of thin-film transistors (TFTs) in order to address pixels that create an image on the front surface of display. Organic light emitting diodes (OLED) is another technology that is emerging in the display industry that also uses active matrix addressing (AMOLED). They offer high performance and low potential cost when compared to AMLCD. [1][2]

## **1.2 Liquid Crystal Display (LCD)**

LCD screens are present in almost every display device in current times. Their popularity is contributed to its sleek and slim structure when compared to the old-style cathode ray tube monitors that are bulkier in appearance. The cathode ray tube works by the vibration of electron guns that move back and forth painting a moving image on the back of the screen.

LCDs are made of pixels that are either red, green or blue in color. These pixels are switched on or off rapidly to create a moving picture and the pixels are normally dark. A liquid crystal is placed between two polarizers, where the second polarizer is oriented  $90^\circ$  to the first polarizer. The function of the first polarizer is to polarize the unpolarized incident light from the source. If the nematic liquid crystal is on, it does not rotate the polarized light from the first polarizer, hence the

light will not pass through the second polarizer, this can be seen in Figure 1.1a. If the nematic liquid crystal is switched off, it rotates the incident polarized light by  $90^\circ$  giving it the orientation to pass through the second polarizer and onto the screen turning the screen bright as seen in Figure 1.1b. Switching the nematic liquid crystal between on and off states is done by thin film transistors [3]. These TFTs ideally should have fast switching speeds and low delay time for a more efficient display. The speed of the TFTs depend on many factors, such as the length of the transistors, the mobility of the semiconductor material used, the amount of junction capacitance present, etc. A crucial requirement for processing of TFTs for display technology is also that the semiconductor material being used must be compatible to be processed in low temperatures. This could enable the production of large area flexible electronics as well as give it the capability to be fabricated on glass substrates.

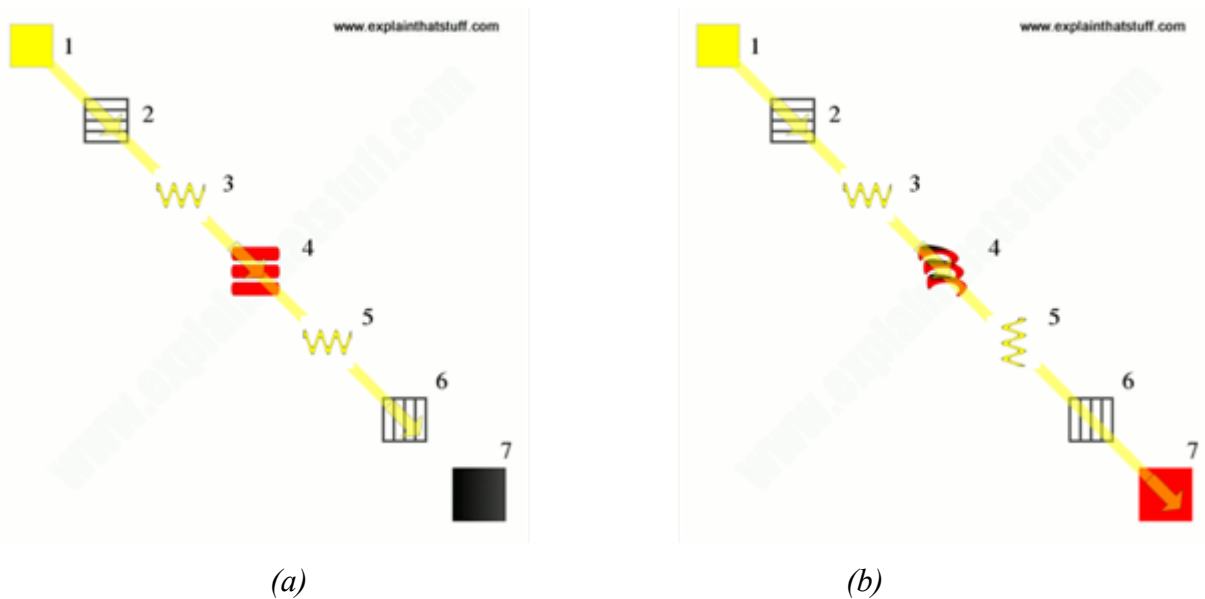
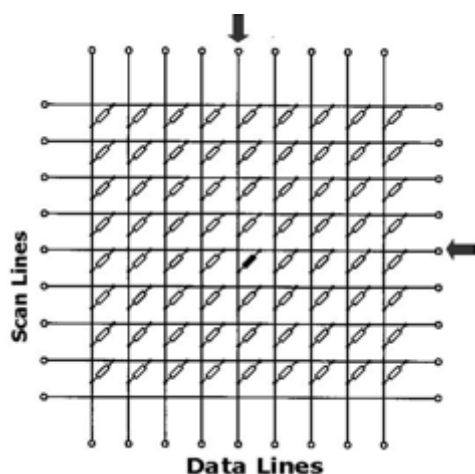


Figure 1.1 How to turn pixel a) off, b) on. Adapted from [3]

### 1.3 Pixel addressing

Before the growth of active matrix displays, passive matrix displays were the standard for LCDs. Passive matrix displays consist of rows and columns of electrodes that are directly connected to the pixel. A favorable material of electrode fabrication is indium tin oxide (ITO), a semi-transparent metal oxide. The intersection of a row and column forms the pixel element (Figure 1.2). Each pixel must maintain its state passively without the use of the circuitry.

To achieve higher pixel density, the number of rows and columns need to be increased. This results in an increase in the voltage needed to drive the display. When a row and column is selected to drive a pixel the liquid crystal material near the selected row and column can be influenced by this high voltage. This means that sometimes the neighboring pixels can be partially activated as well resulting in the degradation of image quality. This phenomenon is referred to as cross talk [4].



*Figure 1.2 Passive Matrix Addressing. Adapted from [4]*

An active matrix consists of a switch connected across each pixel as seen in (Figure 1.3). This switch controls the charging of the capacitor to the desired level, until the next frame refresh, while the other pixels are being addressed. This helps prevent crosstalk, which is a major issue of passive

matrix. Also, unlike passive matrix where all rows must be charged to address a single pixel, in active matrix, each pixel can be controlled directly, resulting in a faster response time.

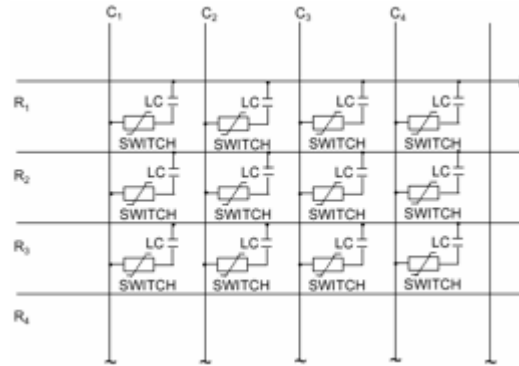


Figure 1.3 Active matrix addressing. Adapted from [4]

AMLCD (Active Matrix Liquid Crystal Display) technology is more expensive but addresses the limitation of passive matrix displays, poor contrast ratio, grey scale, as well as flicker induced by holding signals in pixels in a multiplexed system. The diagram below (Figure 1.4) shows how thin film transistors are incorporated into a matrix. [4]

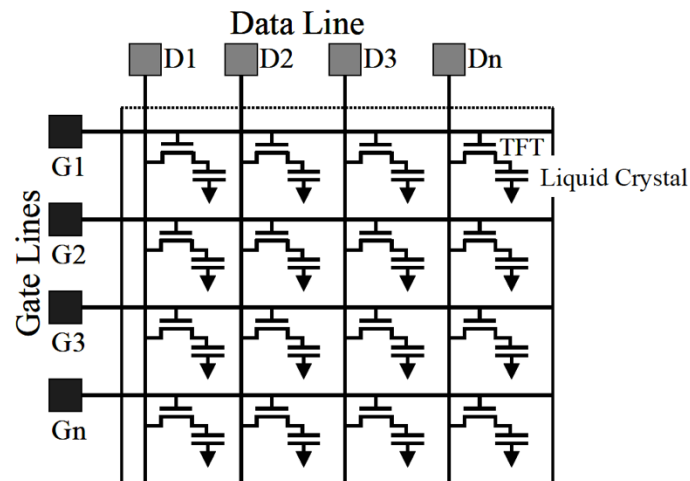
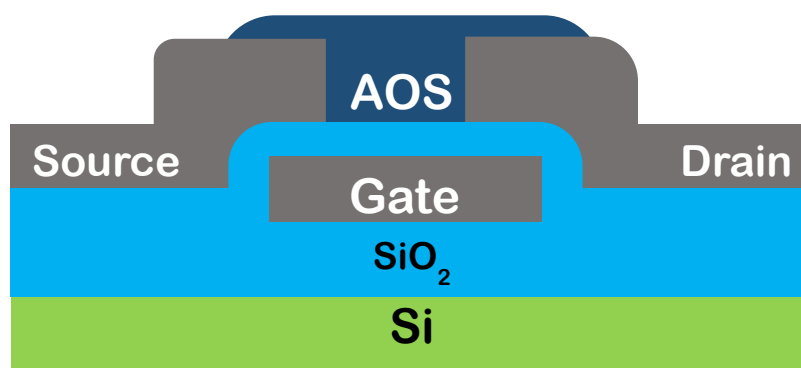


Figure 1.4 Active Matrix Thin Film transistor. Adapted from [4]

## 1.4 History of Amorphous Oxide Semiconductor Devices

The first oxide-semiconductors came into use after the publication of a CdS TFT in 1962 [5]. Following this, several binary material TFTs were demonstrated including  $\text{In}_2\text{O}_3$  in 1964,  $\text{ZnO}$  in 1968 and  $\text{SnO}_2$  in 1970. Their advantage over crystalline semiconductors is the ability to deposit thin films onto substrates at low temperatures. In 1996 transparent amorphous oxide semiconductors (AOS) were proposed as a novel class of amorphous semiconductors having large electron mobility comparable to that of the corresponding crystals. Since then, extensive research on the application of AOS TFTs, especially  $\text{In}_2\text{O}_3\text{--Ga}_2\text{O}_3\text{--ZnO}$  (IGZO), which is a key semiconductor being used in backplanes of current display technology [6]. Figure 1.5 shows the cross-section schematic of a bottom gate TFT, where AOS represents one of several demonstrated metal oxide semiconductor materials.



*Figure 1.5 cross-section schematic of a Bottom Gate AOS TFT*



## 1.5 Current TFT technology and limitations

Many characteristics are required to address the demands of future of display technology; higher mobility for better current drives and faster switching speeds, low temperature processing for flexible displays, large area uniformity and of course cost effectiveness [7]. As TFTs are typically fabricated on glass substrates with a thermal tolerance of around 600 °C, the ability to fabricate at low temperatures is also required.

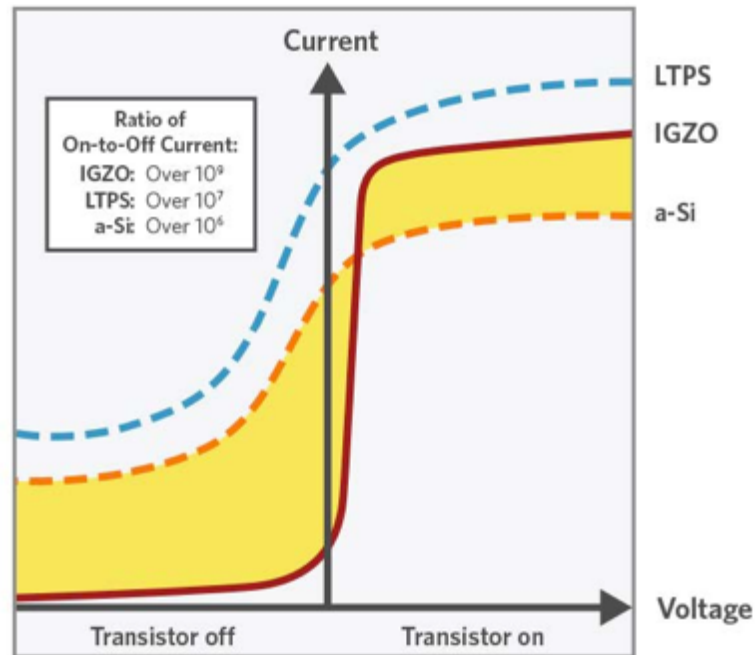
Amorphous hydrogenated silicon (a-Si:H) has been used as a candidate for TFTs due to its high produce large area uniformity which is achieved by its amorphous structure. Amorphous silicon also addresses the need to fabricate at low temperatures as it can be deposited at temperatures under 350 °C using plasma-enhanced chemical-vapor deposition (PECVD). It is relatively low cost and has been studied and understood for a long period of time.

However, a-Si:H has low mobility ( $\mu_{FE} < 1 \text{ cm}^2/(\text{Vs})$ ). Advancements in technology require semiconductors with higher mobility; that results in better current drives, lower time delays and faster switching speeds with ultimately better circuit performance. Two materials that are beginning to replace a-Si for LCD and OLED displays are low-temperature polysilicon (LTPS) and metal oxide (MOx). [8] LTPS has the highest mobility characteristics when compared to amorphous silicon and metal oxides. Table 1-1 shows a comparison of properties between different TFT channel materials.

TFT ACTIVE MATERIALS	a-Si	METAL OXIDE	LTPS
Carrier Mobility ( $\text{cm}^2/\text{Vs}$ )			
Reported	< 1	1 - 50	50 - 300
Typical	0.6 - 0.8	5 - 10	60 - 100
Off Current ( $\mu\text{A}$ )	< E-6	< E-7	< E-6
TFT Stability (NBTS @60C/-20V/10k sec)	Poor (> 30 V)	Good (< 2 V)	Excellent (< 0.5 V)
TFT Uniformity (Gen 8)	Good	Good	Poor
Manufacturing Yield	High (> 95%)	Unknown	Low (~85%)
Mask #	4 - 5	4 - 7	5 - 12
Cost	Low	Low	High
Scalable to Large Panels	Yes	Yes	?
Process (Semiconductor)	PECVD	PVD	PECVD
Process Temperature (C)	> 300	RT	> 400

*Table 1-1 Comparison of properties between different channel TFT materials [8]*

The technology for LTPS utilizes polycrystalline silicon which results in improved electrical properties. While LTPS has the highest mobility and TFT stability when compared to the other two candidates, it also requires a more complex fabrication techniques which results in more steps as well as increased costs. Figure 1.6 shows that while LTPS backplanes have the highest electron mobility, which results in faster switching speeds, LTPS backplanes also have a higher off-state currents compared to a-Si and Metal Oxide technology. A higher off state results in higher current leakage and high power consumption. Metal oxides boast a lower off state which enables faster refresh rates and lower power consumption in mobile devices.[8]

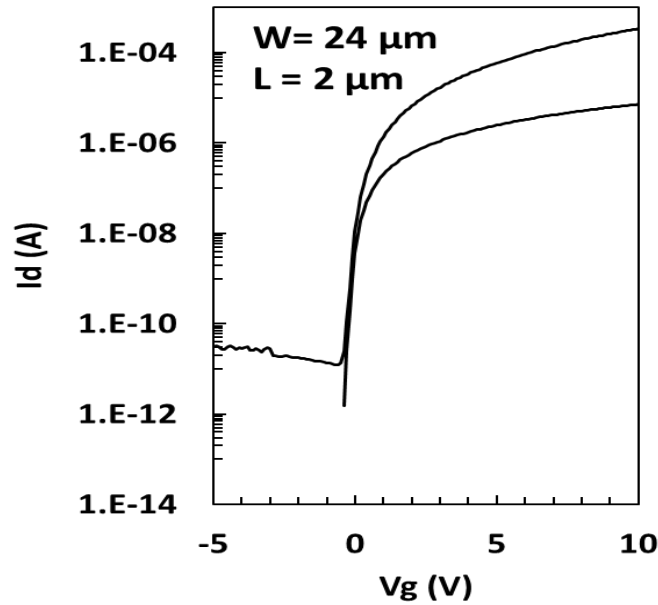


*Figure 1.6 Schematic comparison of TFT I-V transfer curves for a-Si, indium gallium zinc oxide and LTPS, the three main materials used to make TFTs for flat-screen displays. Adapted from [8].*

### 1.5.1 IGZO TFT Development at RIT

A promising AOS currently used in displays is indium gallium zinc oxide (IGZO) due to its high mobility and large-scale uniformity. It also offers low-temperature compatibility, low voltage operation, low off-state leakage, low fabrication cost and transparency to visible light.

Over the last decade there have been several investigations on the development of IGZO TFTs by the Thin-Film Electronics Research Group, led by Prof. K.D. Hirschman at the Rochester Institute of Technology. The research work involved processing self-aligned bottom gate devices as well as high-performing scaled IGZO devices [9]. Figure 1.7 shows an  $L = 2\mu\text{m}$  IGZO device manufactured by the group with 50nm gate dielectric. The device demonstrates electrical performance among the best reported in the literature.



*Figure 1.7 Transfer characteristics from IGZO BG device fabricated with oxide thickness of 50nm with length 2um [9]*

The team has also worked on fabricating passivated devices; passivation was done as the last stage of the TFT fabrication where a 50 nm PECVD  $\text{SiO}_2$  layer was deposited as the passivation material. The device was then annealed for 3 hours in  $\text{O}_2$  at  $400^\circ\text{C}$  and was immediately followed by an HMDS vapor treatment at  $140^\circ\text{C}$  to avoid water adsorption. The devices were then capped with alumina film using atomic layer deposition (ALD) at  $200^\circ\text{C}$ . The gate and S/D contact windows were patterned and etched using 10:1 buffered HF solution. Passivation is done to protect the devices from degradation over time.

The IGZO devices were also subjected to thermal and bias stress to test the stability and durability of the device. Bias stress test included the bottom gate being subjected to bias-stress conditions performed at room temperature to evaluate the resistance to the degradation of electrical characteristics. Positive bias-stress (PBS) and negative bias-stress (NBS) tests involved setting the gate voltage to  $\pm 10$  V with source and drain grounded. The transfer characteristics were tested after 1 hour of stress application [9]. Figure 1.8 shows the effect of the PBS is effectively negligible, however the NBS resulted in a slight shift in curve, however both effects were reversible [9].

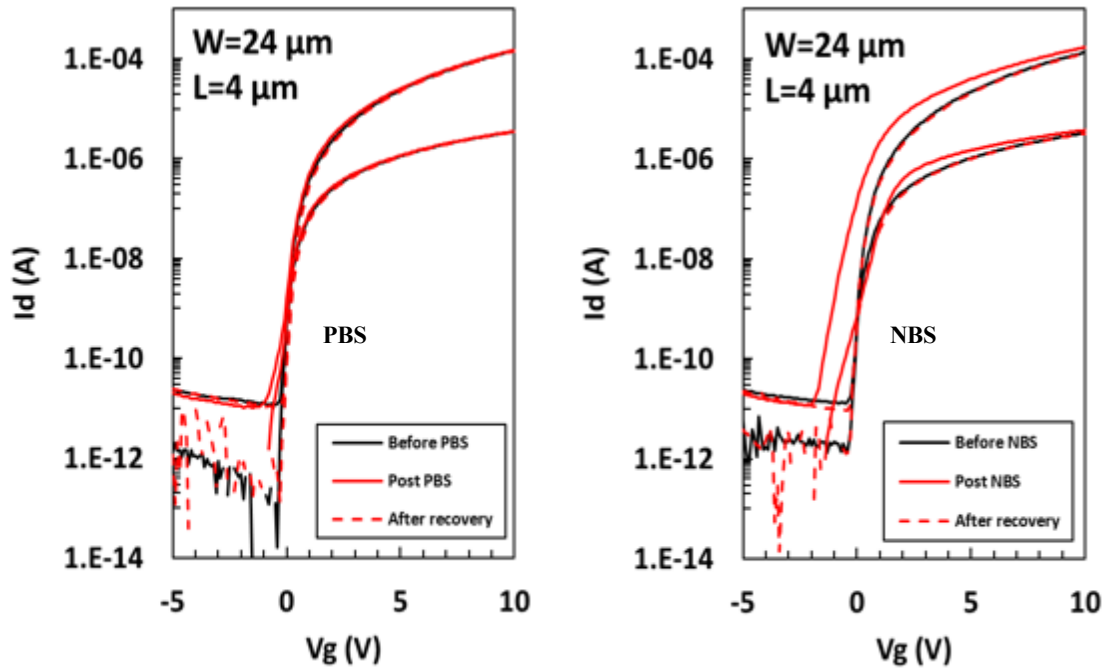


Figure 1.8 Bottom Gate devices showing effects of PBS and NBS applied at  $V_G = \pm 10$  V with source and drain grounded [9]

## 1.6 IWO as a candidate for Metal Oxide TFTs

IWO possesses a high mobility of  $20 \text{ cm}^2/\text{Vs}$  when compared to  $10 \text{ cm}^2/\text{Vs}$  of IGZO. IGZO contains acid-soluble  $\text{Ga}_2\text{O}_3$  and  $\text{ZnO}$  [10] which is very sensitive to wet etching processes. To address the above issues, amorphous oxides semiconductors, that aren't composed of Ga or Zn, such as indium tungsten oxide (IWO) can be examined for making high performance and stable flexible TFTs. In IWO,  $\text{In}_2\text{O}_3$  exhibits a high electron mobility due to band conduction originating from an edge-sharing polyhedral structure [11], [12]. Properties of IWO are discussed extensively in chapter 2.

## 1.7 Goal and objectives

The goal of this investigation was to develop an understanding of the dependence of IWO semiconductor properties and TFT operation on sputter and annealing process parameters. This goal was accomplished through the following objectives.

1. A sputter process and procedures that support reproducible material and electronic properties was established.
2. Sputter and annealing experiments with varying the volume percentage of oxygen in the sputter gas ambient (hereafter referred to as  $\#\% \text{O}_2$ ) were performed.
3. Material resistivity was characterized to determine appropriate factor settings for TFTs.
4. TFTs were fabricated with variations in  $\%\text{O}_2$ , anneal time and temperature.
5. TFT characteristics were analyzed to distinguish differences in device performance related to process settings.

## 1.8 Document outline

Chapter 1 has summarized the recent developments in the display industry and the role of TFT in the structure of an active-matrix display device. Different candidates for TFTs have been discussed and compared. Previous generation technology is briefly talked about while leading in to the need for next-generation investigations. The goal and objectives of the study have been presented.

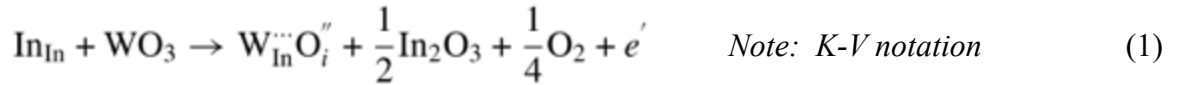
Chapter 2 reports on literature and past investigations on IWO process techniques is reviewed. Chapter 3 describes issues with consistency in the sputtered IWO material, and an investigation focused on the sputter process. Sputter conditions and procedures that were established to address consistency in the target surface condition will be discussed. Chapter 4 provides details on the IWO TFT fabrication process, with the realization of working transistors. Electrical characteristics of TFTs with variations in process conditions are presented, with a focus on the role of oxygen in the sputter ambient and post-sputter anneal. Finally, chapter 5 provides a summary of findings and conclusions on the investigation.

## Chapter 2

### 2.1 Literature review on IWO

InOx-based metal oxide semiconductors have been widely investigated as a channel material in TFT since they show high electron mobility owing to their edge-sharing polyhedral structure [13]. Higher mobility improves electrical conductivity without the cost of optical transparency in the visible light range, providing high operation speed in transparent electronic devices [14].

The oxygen vacancies or the activated  $W^{6+}$  ions on substitutional sites of  $In^{3+}$  ions are responsible for n-type behavior in IWO semiconductor film [15]. According to the complex theory, in IWO,  $W^{6+}$  should provide one carrier when it associates with one interstitial  $O^{2-}$ , as shown in Equation 1. The substitution of  $W^{6+}$  for  $In^{3+}$  associated with interstitial oxygen should result in decreased ionized impurity scattering due to a lower average ionic charge [16].



With increasing oxygen, oxygen vacancies ( $V_o$ ) can be filled and the substituted  $W^{6+}$  ions can be deactivated by forming W-O complexes [17]. Therefore, the optimization of the  $O_2/Ar$  ratio is the key to obtain a suitable film for TFT channel. In IWO,  $WO_3$  has higher oxygen bond-dissociation energy (720 kJ/mol) than  $In_2O_3$  (346 kJ/mol) [18]. The high W-O bond-dissociation energy supports the reduction of excess oxygen vacancies, acting as a carrier suppressor and decreasing associated trap states.



The optical transmittance also enhances with increasing O<sub>2</sub>/Ar ratio within the visible and NIR region. Z. Lu et al. showed that the average transmittance of the IWO film increased from 81.88% to 84.89% in the visible region and from 90.87% to 93.33% in the NIR region with increasing O<sub>2</sub>/Ar ratio from 11% to 17% [19] as shown in Figure 2.1.

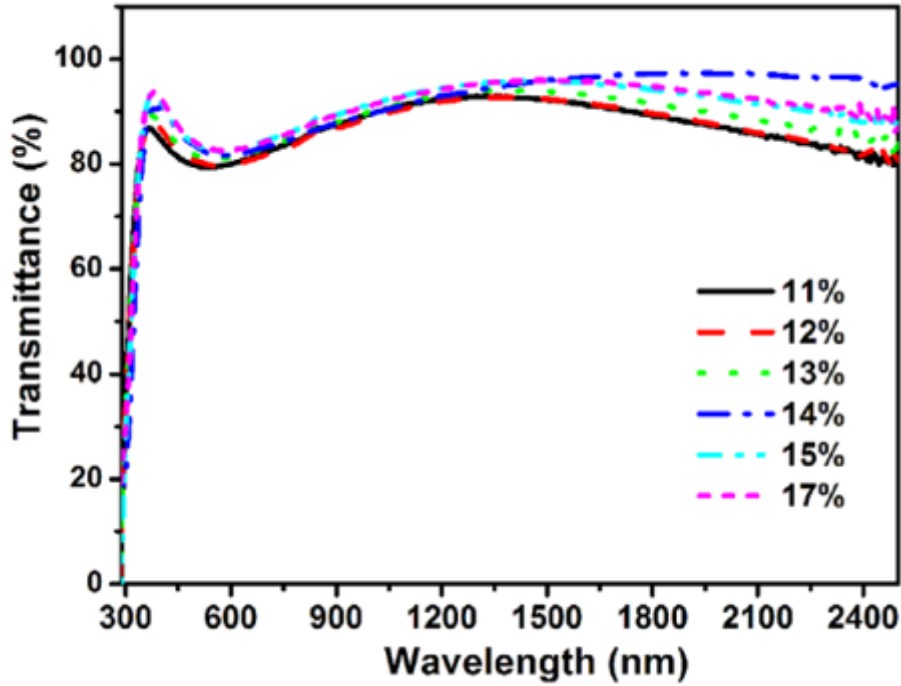


Figure 2.1 Optical transmittance of IWO films with various O<sub>2</sub>/Ar ratios.[19]

The presence of a very small amount of WO<sub>3</sub> prevents crystallization of In<sub>2</sub>O<sub>3</sub> film and provides a very smooth surface [20]. This will lead to reduction in carrier mobility degradation since surface roughness impedes charge transport. The a-IWO film thickness can be scaled down without increasing surface roughness; since the channel thickness affects the absolute number of free carriers, switching behavior can be enhanced by using thinner channel [21]. This cannot be achieved in ZnO-based TFTs due to the polycrystalline back-channel morphology.

The first ever a-IWO TFTs were reported by Aikawa et al. also demonstrated IWO TFTs using DC magnetron sputtering with a high field-effect mobility, with representative characteristics shown in Figure 2.2 [20].

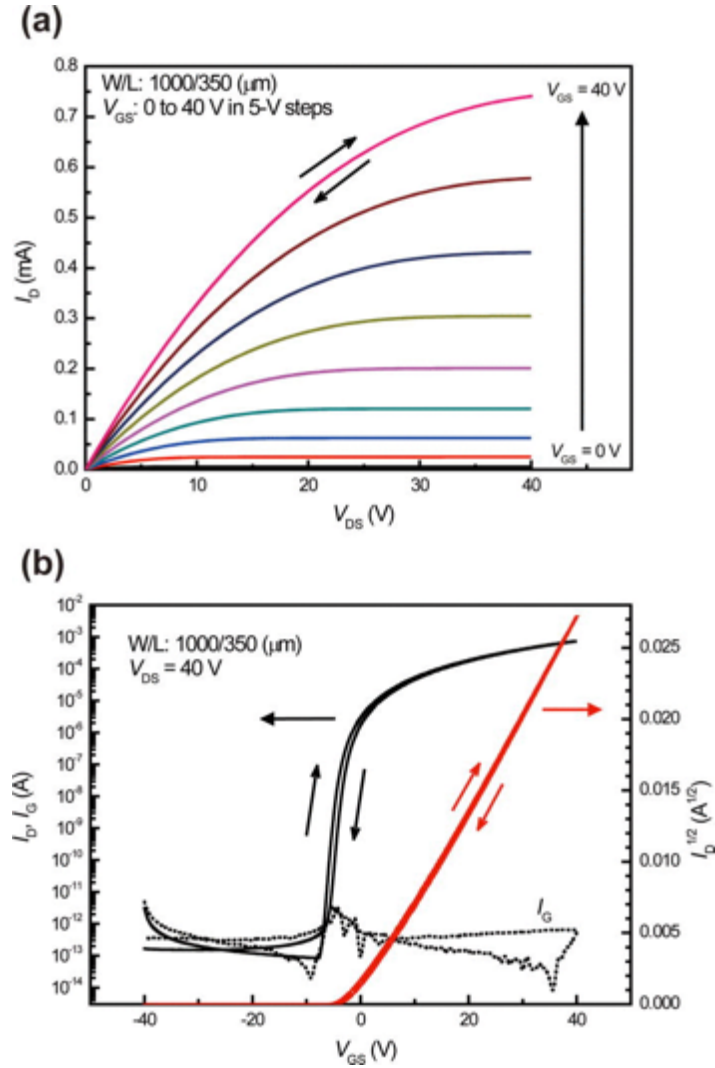


Figure 2.2 IWO TFT transfer curves, with  $\mu_{FE} = 19.3 \text{ cm}^2/\text{V}\cdot\text{s}$ ,  $I_{on}/I_{off} = 8.9 \times 10^9$ , and  $SS = 0.47 \text{ V/decade}$  [20]

While the electrical characteristics shown in Figure 2.2 have a steep subthreshold and minimal hysteresis, the device exhibits an on-state threshold voltage  $V_T \sim 0V$ . The threshold voltage of IWO TFTs has been shown to depend on the sputter ambient oxygen content, as seen in Figure 2.3. This adjustment appears to require %O<sub>2</sub> optimization in order to achieve an acceptable  $V_T$  without significant compromise to the subthreshold operation and hysteresis, as shown in Table II [22] These results suggest that excess oxygen may result in charge trapping defects in the IWO channel and/or channel/dielectric interface.

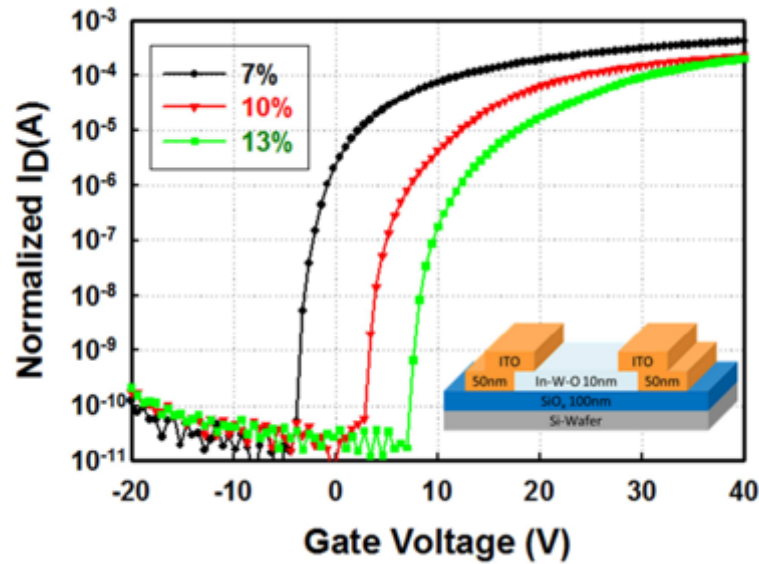


Figure 2.3 Transfer curves of IWO TFTs as a function of oxygen partial pressures. Adapted from[22]

**TABLE II.** Comparison of various device parameters of a-IWO TFTs

$P_{O_2}$	$V_{th}$ (V)	$S.S$ (V/ decade)	Mobility ( $cm^2/V S$ )	Hysteresis (V)
7%	-3.4	0.39	36.7	0.06
10%	4.2	0.42	26.2	0.11
13%	8.4	0.55	22.4	0.29

Table 2-1 Comparison of device parameters of IWO TFTs with varying  $PO_2$  [22]

## 2.2 Reactive Sputtering of IWO

The CVC601 sputtering system is a DC sputter tool being used for physical vapor deposition of the Indium Tungsten Oxide target. Physical vapor deposition, as its name implies, involves physically depositing atoms, ions, or molecules of a coating species on to a substrate, in this case it will be Indium Tungsten Oxide. Sputtering involves the electrical generation of a plasma between the coating species and the substrate. [23]



*Figure 2.4: CVC 601 Sputter tool in SMFL laboratory at RIT*

The composition of the 4-inch IWO ceramic target consists of indium oxide to tungsten oxide at a 98:2 ratio respectively. The target has been consistently sputtered at a pressure of 7mT, power of 50W, and with sputter time and gas ambient ratio of Ar:O<sub>2</sub> being varied.

The ratio of oxygen and argon in the ambient is calculated in the following way. With respect to the CVC601 sputter tool being used, the MFC installed for argon is a 200sccm MFC calibrated for N<sub>2</sub>. The Gas Calibration Factor for Argon (relative to N<sub>2</sub>) is 1.4, so the actual full range for

the MFC becomes  $200 \times 1.4 = 280\text{sccm}$ . The MFC installed for Oxygen is a  $20\text{sccm}$  MFC calibrated for  $\text{O}_2$ , so there is no multiplier for the gas calibration factor. The display on the sputter tool for each gas gives the percentage of the full range for the MFC. For example, if the display shows 10% Ar, the gas flow is 10% of  $280\text{ sccm}$ , or  $28\text{ sccm}$ . Since the  $\text{O}_2$  gas flow is calibrated to  $\text{O}_2$  itself, if the display on the tool for  $\text{O}_2$  is 10%, that means the gas flow is 10% of  $20\text{sccm}$ , which is 2.

$$\text{Argon gas flow} = \frac{x}{100} \times 280\text{sccm}$$

$$\text{Oxygen gas flow} = \frac{y}{100} \times 20\text{sccm}$$

$$\% \text{O}_2 \text{ in total gas flow} = \frac{\text{Oxygen gas flow}}{\text{Oxygen gas flow} + \text{Argon gas flow}} \times 100$$

Varying the percentage of  $\text{O}_2$  in the ambient plays a significant role in our investigations. To calculate the ratio of  $\text{O}_2$  in the total gas ambient the gas flow for each gas must be calculated separately and then the ratio of the gas flow of  $\text{O}_2$  to the total gas flow should be taken. For example, to obtain 10% of  $\text{O}_2$  in the total gas ambient during the sputter run we need, 13% of the total Argon gas flow in the MFC controller and 20% of the total Oxygen gas flow in the MFC controller, this results in 10% of  $\text{O}_2$  in the total gas ambient.

By using this logic, % of O<sub>2</sub> is calculated:

*Table 2-2 % Gas flow*

% of Ar on MFC	Argon gas flow	% of O <sub>2</sub> on MFC	Oxygen gas flow	% of O <sub>2</sub>
30	84	0	0	<b>0</b>
34	95	6	1.2	<b>1.25</b>
24	67	6	1.2	<b>1.75</b>
15	42	15	3	<b>6.67</b>
13	36	20	4	<b>10</b>
8	22	20	41.	<b>15</b>

## 2.3 Annealing on IWO films

Since oxygen vacancies in oxide semiconductors are the main source of free electrons, the conductivity of the film can be controlled by controlling the oxygen vacancy content in the film during annealing [24]. Therefore, proper annealing ambient impacts the mesa of the metal-oxide TFT and leads to an enhancement in the oxidation state of the metal. Oxygen annealing is thus effective for controlling the carrier concentration of the active layer, decreasing electron traps, and enhancing TFT performance.[25]

In the literature on experimental work done on IWO TFTS, annealing performed at temperature as low as 100°C has produced enhancement-mode devices [22][20]. Most anneal experiments have been performed at or below 300°C to avoid crystallization that may occur at

higher temperatures. Since low temperature processing was not a primary focus of this work, most experiments were done using furnace annealing in  $O_2$  at  $300^\circ C$ .

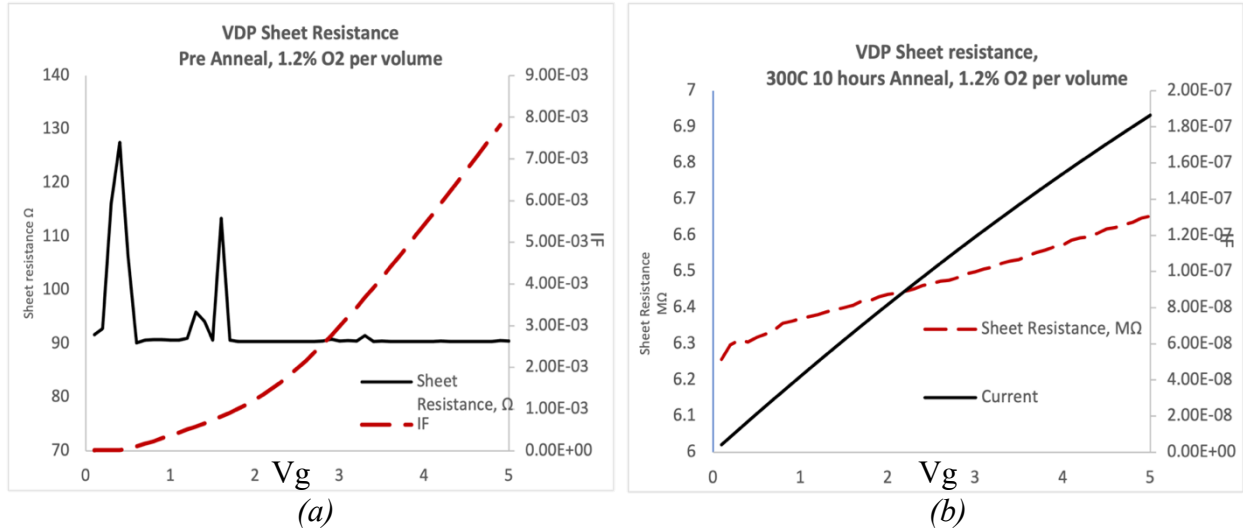


Figure 2.5 Van der Pauw sheet resistance for sputter ambient of 1.2% $O_2$ : a) before anneal, b) after 10 hour,  $300^\circ C$   $O_2$  anneal

An increase in sheet resistance with annealing can be clearly depicted by Figure 2.5 where before annealing the sheet resistance was approximately 90 Ohms/sq but with a  $300^\circ C$  anneal for 10 hours, the sheet resistance increased to approximately 6 Megaohms/sq.

## 2.4 Preliminary results

The first set of TFTs fabricated were sputtered at a 6.7% $O_2$  ambient at 50W, 7mT for 15 minutes. The target was pre-sputtered for 15 minutes in an argon and oxygen ambient and the TFTs were finally annealed for 2 hours at  $300^\circ C$  in dry  $O_2$ . The transfer characteristics obtained can be seen in Figure 2.6.

The preliminary experiments conducted on IWO TFTs produced encouraging results as we observe semiconductor behavior represented on the transfer curves.

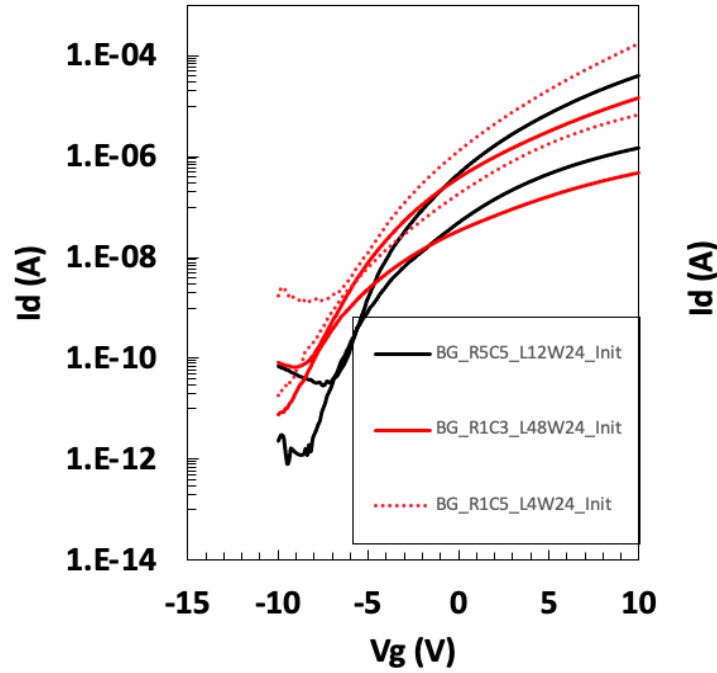


Figure 2.6 Preliminary transfer characteristics of IWO TFTs, 6.7%O<sub>2</sub>, annealed in O<sub>2</sub> for 2 hours at 300°C

As an attempt to recreate these results a new run was commenced recreating the same conditions as that from before, but by reducing the sputter time by half, the logic behind this being that a thinner mesa would result in less channel conductivity and better gate modulation.

However, on doing so the devices tested produced two inconsistencies; firstly, many of the devices were not able to handle large negative voltages applied to the gate and secondly, the few



devices that were tolerant, resulted in highly conductive channels with poor current modulation as can be seen in Figure 2.7.

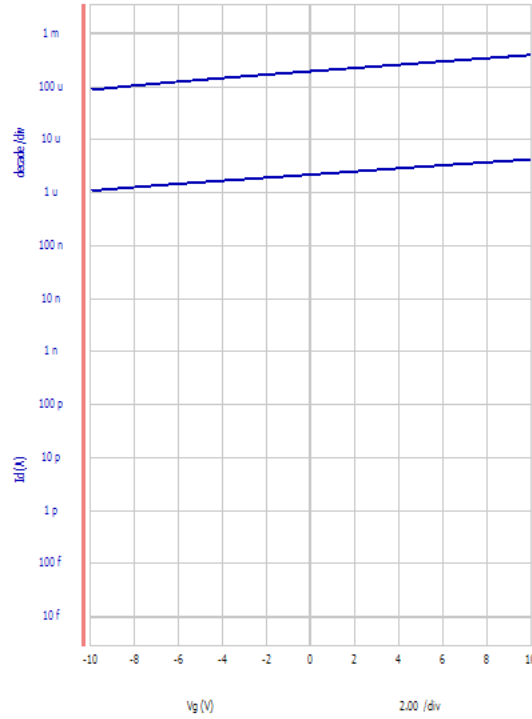


Figure 2.7 Reproduced transfer characteristics,  $L=48\mu\text{m}$ , 6.7% $\text{O}_2$ , annealed in  $\text{O}_2$  for 2 hours at  $300^\circ\text{C}$

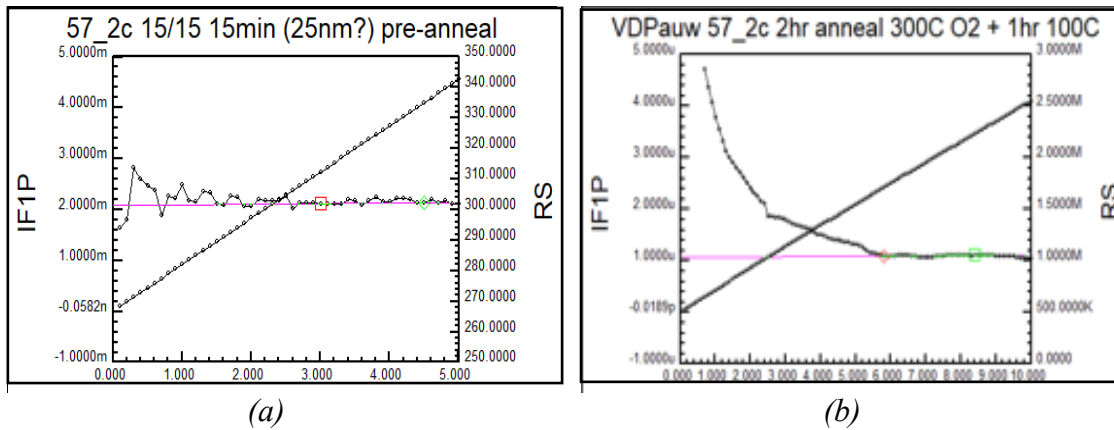


Figure 2.8 Sheet resistance of preliminary TFTs, 6.7% $\text{O}_2$ , 50nm, annealed in  $\text{O}_2$  for 2 hours at  $300^\circ\text{C}$  a) before anneal b) after anneal

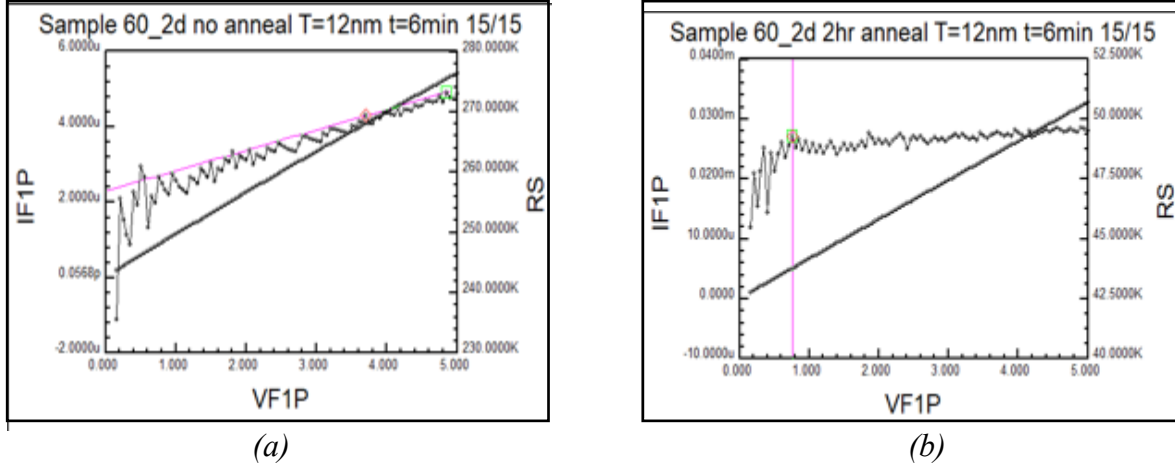


Figure 2.9 Sheet resistance of reproduced TFTs, 6.7%O<sub>2</sub>, 12nm, annealed in O<sub>2</sub> for 2 hours at 300°C a) before anneal b) after anneal

On testing the Van der Pauw structures the sheet resistance produced no significant difference in value before and after the 300°C O<sub>2</sub> anneal, seen on Figure 2.8. For a better understanding of the film, we compared these results to the preliminary test results, seen on Figure 2.9. The VDP structures from the preliminary data shown a great increase in sheet resistance after anneal, an effect not seen in the re-produced TFTs.

As discussed before, annealing causes an increase in sheet resistance, however the measured sheet resistance of the TFTs does not support this theory. The inconsistencies in the change in sheet resistance with anneal suggested that the sputtered IWO material properties were not the same as that which yielded the encouraging transfer characteristics shown in Figure 2.6. This suggests a possible change in the IWO target surface, prompting a focused investigation on the target surface condition and sputter gas ambient which will be discussed in chapter 3.

## *Chapter 3*

### **3.1 Initial evaluation of the IWO target appearance**

On observing the IWO target after multiple runs, a green-like racetrack was noticed on the target surface as seen on Figure 3.2. The target seemed to have changed much in appearance since before its first use, which is depicted by Figure 3.1. This may have been contributed by some side-effects caused due to magnetron sputtering.

Magnetron discharge technology is adopted to perform sputtering of desired material from target to substrate. By applying a magnetic field onto the target, secondary electrons change trajectories and move long distances before reaching the chamber wall coating films onto the substrate while doing so. This results in more ions to be discharged and maintain the low pressures of the gas chamber. However, since the discharge plasma is not uniform over the target, a racetrack erosion profile forms over the target, possibly causing erosion on the IWO target. [26]

The target was then reconditioned, this involved restoring the target surface back to the original state by mechanical abrasion and an isopropyl alcohol clean. After reconditioning, the target was sputtered for 30 minutes at 6.7%O<sub>2</sub> ambient, which is the same sputter conditions as the first successful run. The voltage and current of the sputter run were noted to be at 39V and 1.5A, the target was once again observed, and it was noted that greenish racetracks had re-appeared (Figure 3.3)

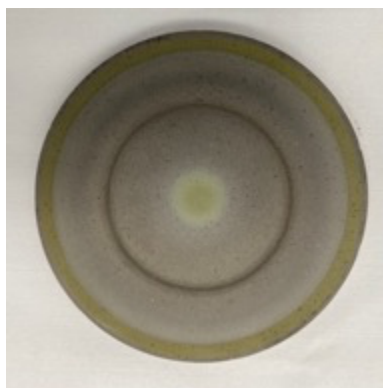


Figure 3.2 Target before re-conditioning, after several runs.

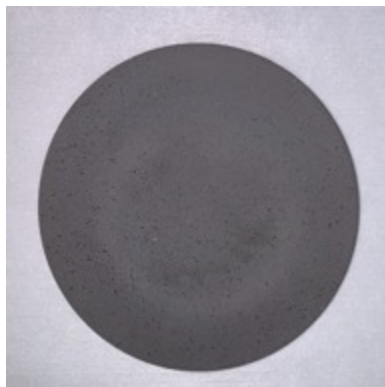


Figure 3.1 Target before after reconditioning.



Figure 3.3 Target after one run in 6.7%  $O_2$  for 30 minutes.

Sheet resistance was measured from a Van der Pauw structure for a wafer sputtered at 6.7% $O_2$  for 15 minutes before and after the 2 hour 300°C  $O_2$  anneal (Figure 3.4) to understand if the anneal has caused any change in the electrical characteristics of the material.

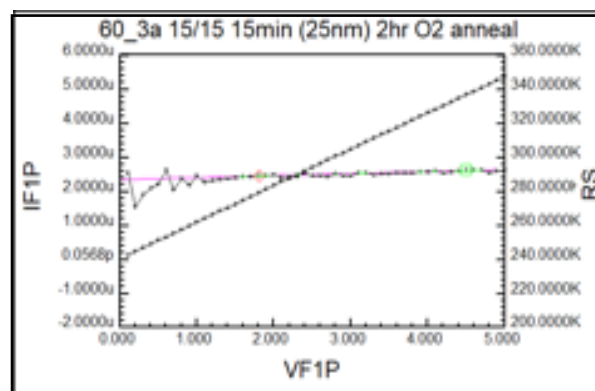
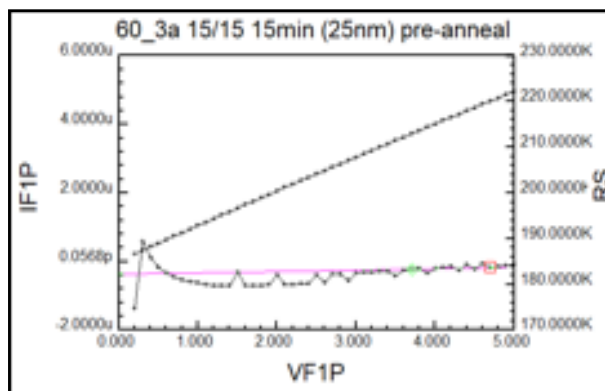


Figure 3.4 VDP Sheet resistance for recreated devices sputtered at 6.7% $O_2$ : a) before b) after anneal at 300°C  $O_2$  for 2 hrs.

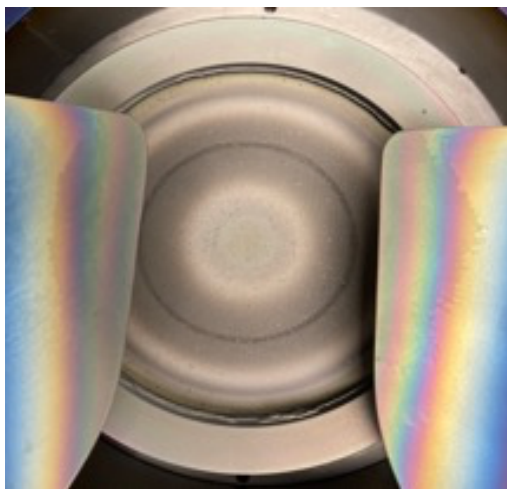
It can be noted that there was no significant change in sheet resistance before and after the anneal. However, this does not agree with the known fact that annealing eliminates  $O_2$  vacancy defects,

which in-turn increases sheet resistance. As such, the integrity of the sputtered material is questionable.

The appearance of the target and inconsistencies in the test results indicate that - including  $O_2$  in the ambient may cause a variation in the sputter run. In order to understand the impact of  $O_2$  on the target surface sputter runs were performed with a low  $O_2$  flow in the ambient. Afterwards, the target was once again reconditioned to its original state (Figure 3.1) and the sputter ambient was evaluated.

### 3.2 Oxygen content in reactive sputter ambient

To understand how the surface of the target behaves with no  $O_2$  flow, the target was sputtered for one hour with zero % $O_2$  per volume, after being reconditioned to its original state; no wafers were included in the chamber during this run. After approximately 10 minutes, the target was sputtering at a voltage of 39V and a current of 1.5A, consistent to the parameters at which it ran previously. However, for the remainder of the sputter run, the target began to sputter at a voltage of 320V and

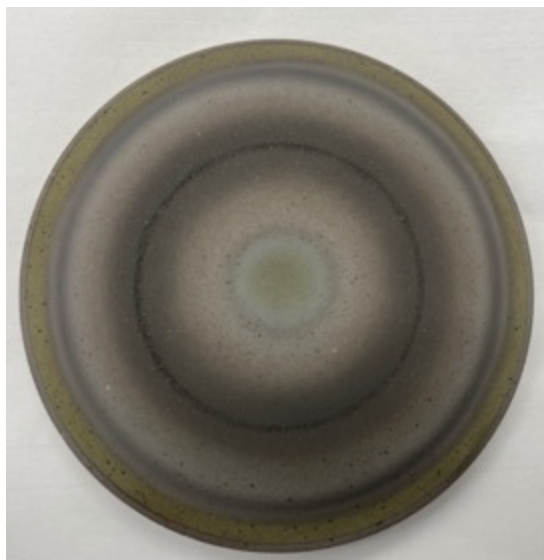


*Figure 3.5 Target after recondition 2, and sputtered at 0%  $O_2$  per volume for 1 hour.*

current of 0.15A. At the end of the 1 hour of sputtering the target was once again inspected and can be seen on Figure 3.5.

A key take-away from this experiment is that the target has a much slighter greenish surface appearance along the perimeter and center of the “racetrack”, in comparison to sputtering with the addition of  $O_2$ . This greenish residue is likely due to reaction of oxygen with the target surface, which must be avoided to support a consistent target surface condition. Pre-sputtering in an argon-only gas ambient removes any such sub-oxide films from the plasma erosion racetrack region.

Two films with different levels of  $\%O_2$  were studied to understand the impact of including  $O_2$  in the ambient during deposition. The first wafer underwent a 30 minute sputter at a sputter ambient of zero  $\%O_2$  per volume and the second wafer underwent a 30 minute sputter at an ambient of 1.75 $\%O_2$ . Before depositing IWO on the device wafers the target underwent a 30 minute pre-sputter with argon only, the current and voltage remained at 320V and 0.15A. The state of the target was once again noted after the consecutive sputter runs and can be seen on Figure 3.6.



*Figure 3.6 Target after sputter for 2.5 hours 0 $\%O_2$  ambient and 30 minutes 1.75 $\%O_2$  ambient.*

Figure 3.6 shows that including  $O_2$  in the ambient does indeed result in a green racetrack on the target. This observation supports that  $O_2$  in some way impacts the metal oxide composition different to the original state of the target. Going forward we measured the electrical response by measuring the Van der Pauw sheet resistance measured before and after a 2-hour  $O_2$  anneal in  $300^\circ\text{C}$  for devices sputtered in both ambient as seen in Figure 3.7 and Figure 3.8.

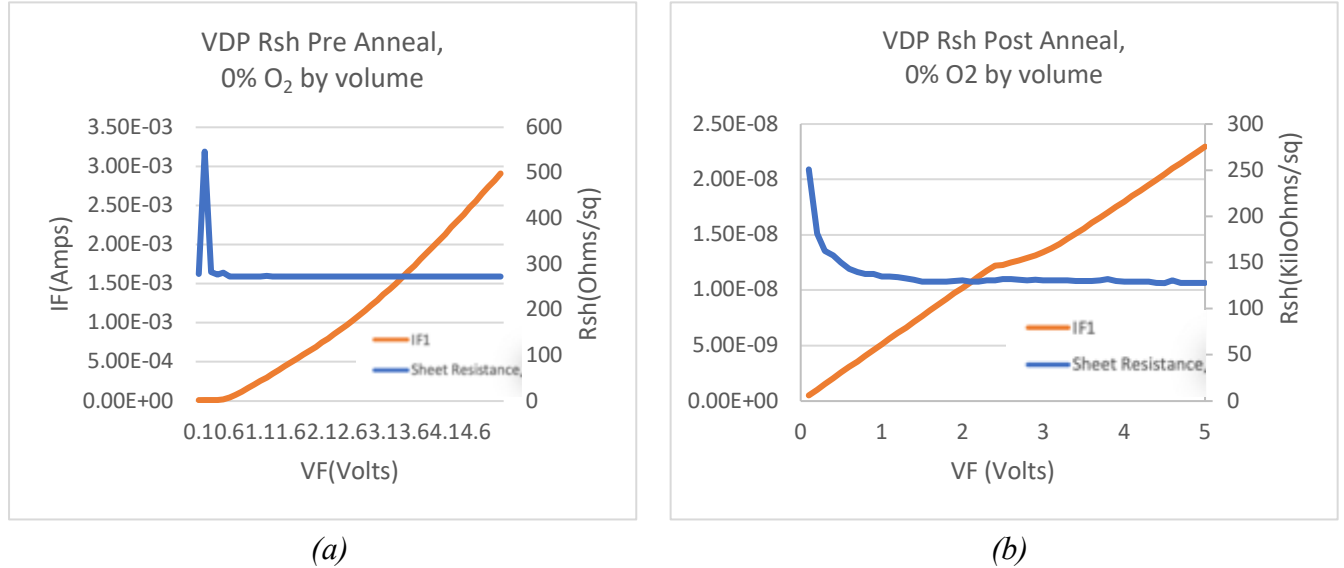


Figure 3.7 VDP Sheet resistance for TFTs sputter at 0% $O_2$  ambient. a) before anneal b) after anneal, in dry  $O_2$  at  $300^\circ\text{C}$  for 2hr.

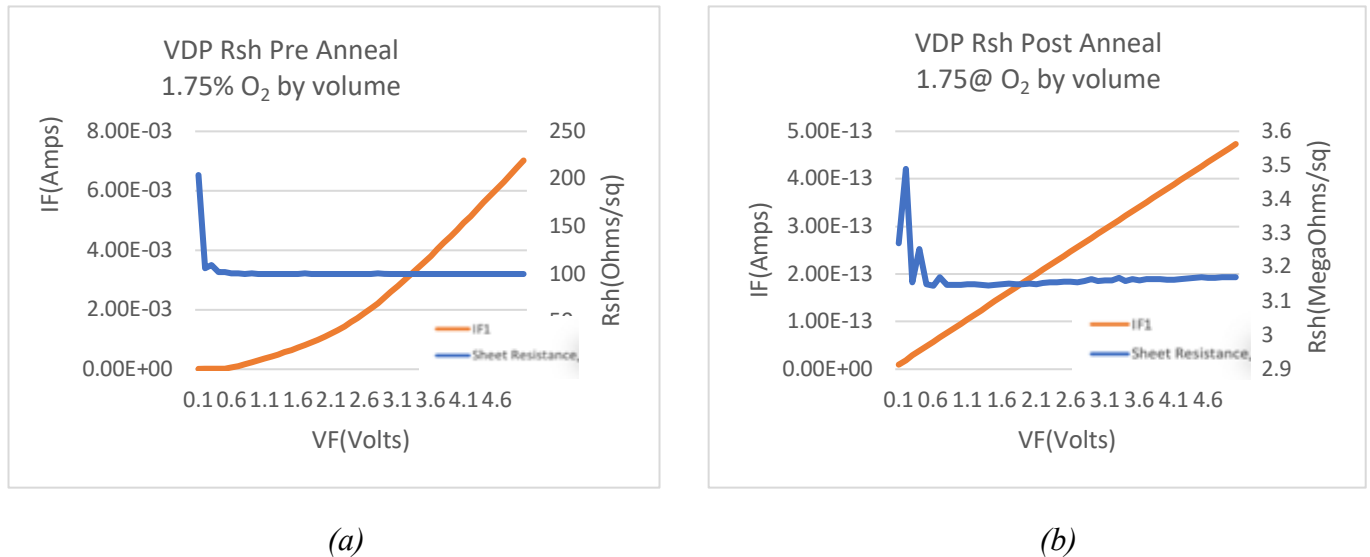


Figure 3.8 VDP Sheet resistance for TFTs sputter at 1.75% $O_2$  ambient. a) before anneal b) after anneal, in dry  $O_2$  at  $300^\circ\text{C}$  for 2hr.

Prior to anneal the sheet resistance, of films with zero %O<sub>2</sub> and 1.75%O<sub>2</sub> was around 300Ω/sq and 100Ω/sq, respectively, after annealing the sheet resistance increased to roughly 6kΩ/sq and 1MΩ/sq. This significant difference in change of sheet resistance when comparing both wafers is a key indicator that including O<sub>2</sub> content in the ambient does hold an important role in characterizing the IWO mesa.

While it is important to note that annealing has increased the sheet resistance by eliminating O<sub>2</sub> vacancies, the anneal is not nearly as effective for the wafer with zero %O<sub>2</sub> as it is for the wafer with a mere 1.75%O<sub>2</sub>. This concludes that, including O<sub>2</sub> in the sputter ambient will have a greater effect on sheet resistance after annealing when compared to having no O<sub>2</sub> in the sputter ambient.

### **3.2.1 Sheet resistance as a function of oxygen content in sputter ambient**

The impact of annealing for films sputtered at different oxygen content (0%, 1.2% & 1.75%) was studied. Figure 3.9 shows a graph of sheet resistance versus oxygen content in the sputter ambient, before and after annealing in O<sub>2</sub> for 2 hours at 300°C. The graph shows that for pre-anneal treatments, an increase in O<sub>2</sub> content in the sputter ambient causes a decrease in sheet resistance however, after the anneal, an increase in O<sub>2</sub> content in the sputter ambient causes an increase in



sheet resistance. The anneal may have a larger impact on the oxygen defects on the film when the sputter ambient already includes oxygen.

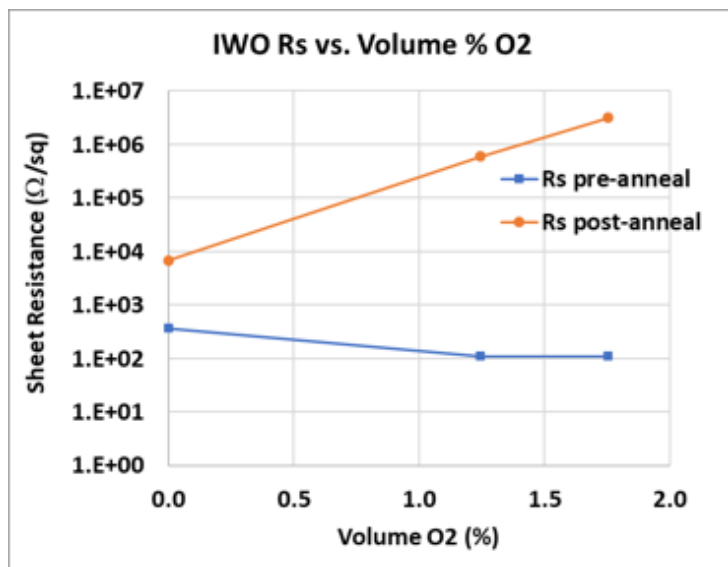
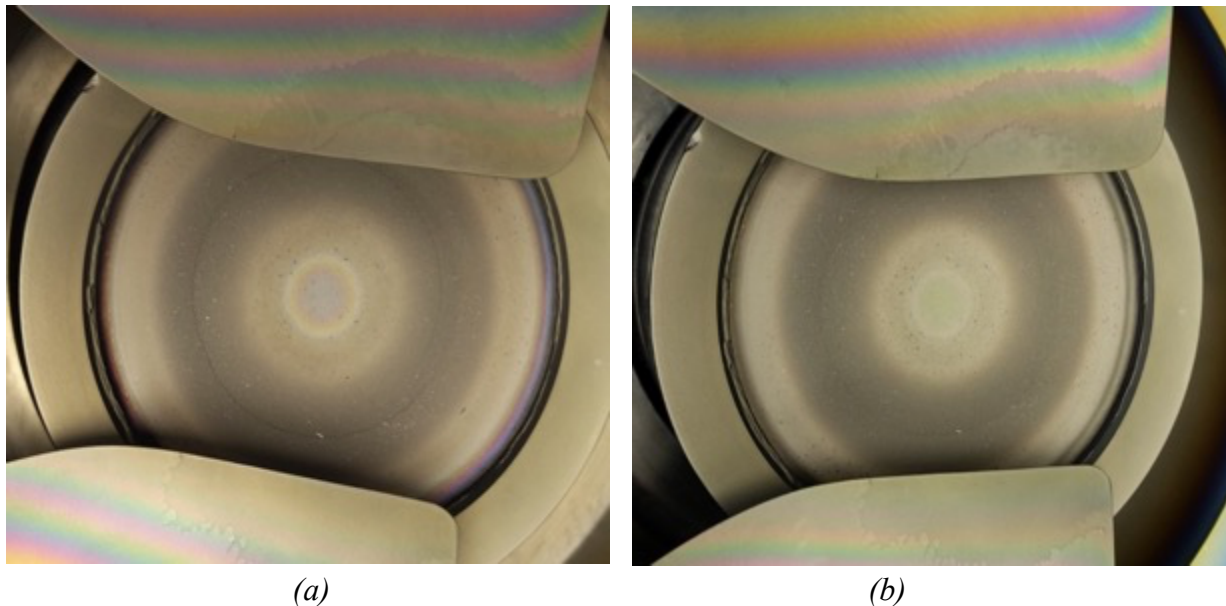


Figure 3.9 Sheet resistance vs. %O<sub>2</sub> in sputter ambient, before annealing and after anneal in O<sub>2</sub> for 2 hours at 300°C

While the Van der Pauw structures confirm differences in the electrical properties of the IWO material, the semiconductor behavior (i.e. ability to modulate charge) must be investigated within a TFT device structure. This will be the focus of chapter 4.

### 3.3 Pre-sputter treatment defined

Once more the target was reconditioned to its original state and sputtered, in an Argon only ambient in two 30-minute intervals. The sputter was done after a weekend tool pump-down. The current and voltage stayed consistent at 320V and 0.15A as noted previously. After the initial 30 minutes of sputter the target was observed Figure 3.10 (a) . As seen in the figure the target seemed to develop a blue racetrack. A second 30-minute sputter was done, resulting in the removal of the apparent surface residue shown in Figure 3.10 (b). Note the target surface appeared as it did in Figure 3.5, which also had only 1 hour of argon sputter.



*Figure 3.10 Target after a) 30 minutes b) 1 hour of argon only sputter*

This result confirms that a long sputter, with argon only in the plasma ambient, is pertinent to ensure that any residual effects due to target recondition are removed and a further 30-minute argon only pre-sputter should be performed prior to any device deposition. Target reconditioning may be considered if significant discoloration of the target is observed, or the appropriate current/voltage plasma condition (i.e. 0.15A/330V) is not attained.

## *Chapter 4*

### **4.1 TFT Fabrication**

Experiments on the process development of IWO devices are performed by varying the oxygen percentage in the sputter ambient, the anneal time and the anneal duration. Devices were fabricated on silicon wafers with bottom gate staggered configuration on a thick thermally grown isolation  $\text{SiO}_2$ , of a thickness of approximately 650nm. A 150 nm Molybdenum gate electrode was sputtered and patterned, followed by a 50 nm  $\text{SiO}_2$  gate dielectric deposited by PECVD (TEOS precursor, 390 °C). The  $\text{SiO}_2$  was densified for 2 hours in  $\text{N}_2$  ambient at 600 °C in a furnace. The IWO mesa was patterned using negative lift-off lithography. The mesa was patterned and defined by the lift-off technique which uses Futurrex NR9g-1500PY as the negative photoresist. IWO was sputtered for 30 minutes at 7mT pressure with an oxygen ambient between zero and 10% , delivering a mesa of approximately 50nm. The sputter voltage and current was observed to remain at 320V and 0.15A. The S/D contact metal composed of a Mo-Al bilayer, with thickness of 50nm Mo and 75nm Al, was then sputtered and defined by lift-off technique using Futurrex NR9g-1500PY negative photoresist. The wafer was then broken into four quarters and each quarter was subjected to different annealing conditions. After annealing, the gate and S/D contact windows on each quarter were patterned lithographically and finally etched, to open contact to the gate, using 10:1 buffered HF solution.

A device wafer was processed with 30-minute Argon only pre-sputter and then a 30 minute deposition at an ambient of 1.2% $\text{O}_2$ . The devices were then processed as usual and annealed for 2 hours at 300°C  $\text{O}_2$ . The devices were then tested, using an Agilent B1500 parameter analyzer, and the Id-Vg transfer curves were obtained. The devices behaved in a conductive fashion however

a slight upward slope in the graph was noticed as seen in Figure 4.1. The sample was then once again annealed for 8 more hours in 300°C O<sub>2</sub> and tested. The devices clearly demonstrated gate-controlled current modulation as seen in Figure 4.2.

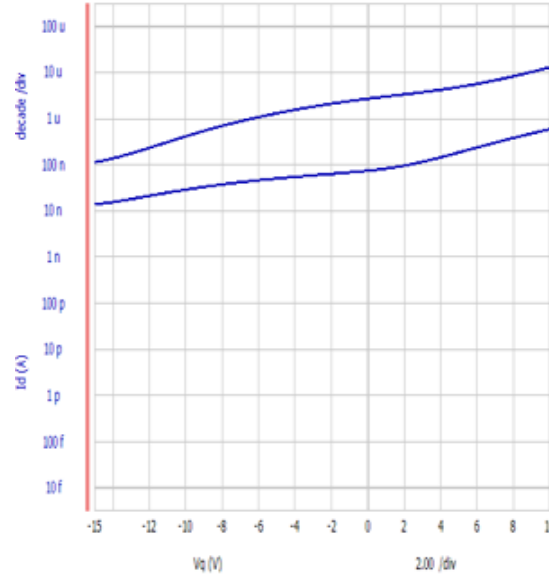


Figure 4.1 Transfer characteristics, 48um, 1.2% O<sub>2</sub> per volume, 300C dry O<sub>2</sub> 2-hour anneal.

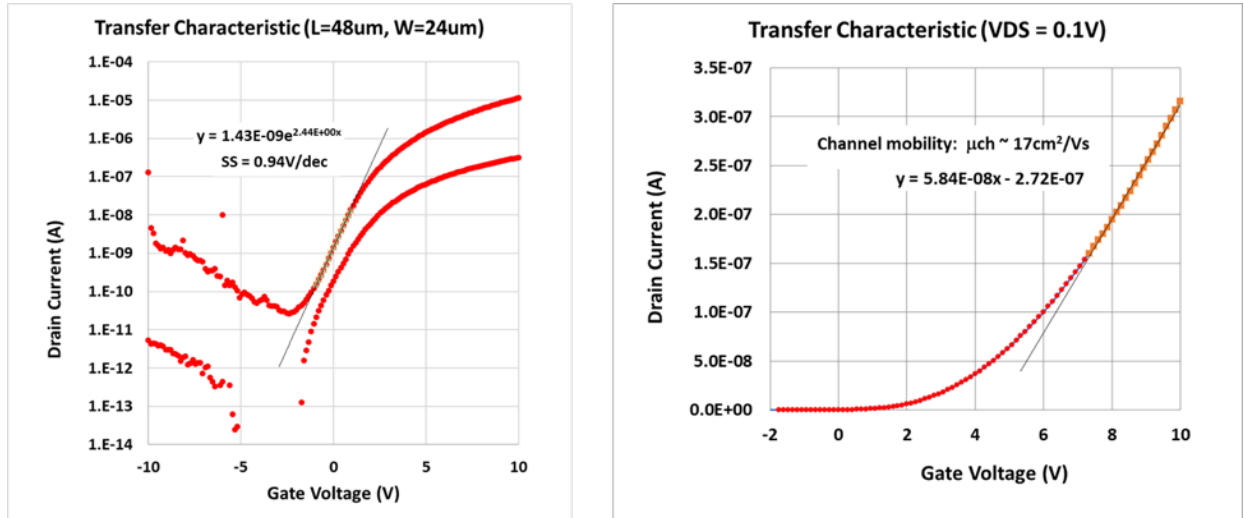
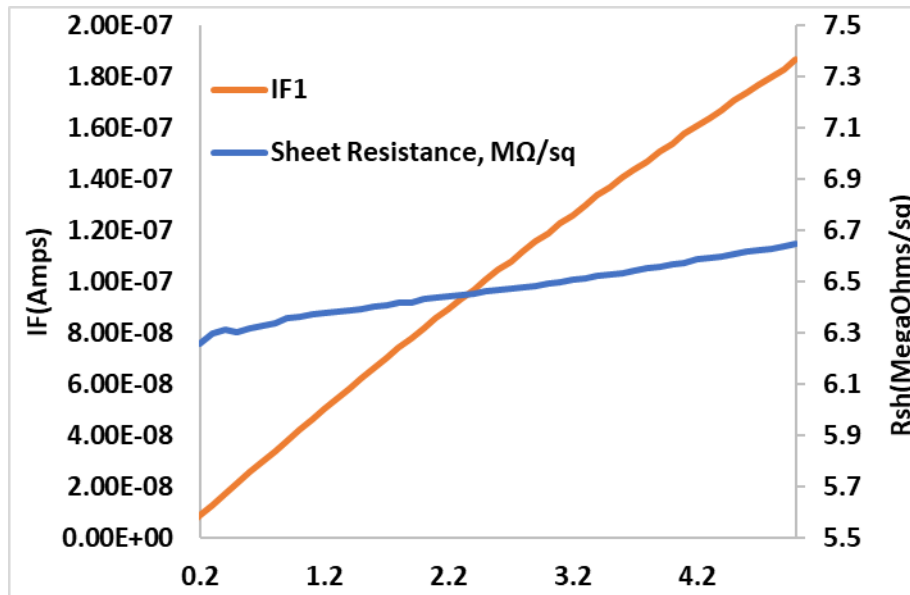


Figure 4.2 TFT transfer characteristics for  $L = 48\mu\text{m}$  device, sputtered at 1.2%O<sub>2</sub> and annealed for 10 hours at 300C in dry O<sub>2</sub>.

The electrical parameters of the 48 $\mu$ m device extracted from this curve was, subthreshold slope of 0.94V/dec,  $\mu = 17\text{cm}^2/\text{Vs}$  and threshold voltage ( $V_T$ ) = 0.8V taken to be  $I_D = 50\text{pA}/\mu\text{m}$  @  $V_{DS} = 0.1\text{ V}$ . Van der Pauw test structures were used to find the sheet resistance corresponding to the 1.2% $\text{O}_2$  devices, measured to be  $R_s \sim 6\text{ M}\Omega/\text{sq}$  (see Figure 4.3). Note that the semiconductor behavior of the transistors realized after surface reconditioning and 30min argon pre-sputter, was not previously achieved when the plasma current/voltage conditions were different than those specified in the details of TFT fabrication (i.e. 320V, 0.15A). This provided the confirmation necessary to further investigate alternative treatment combinations.



*Figure 4.3 VDP Sheet resistance for 1.2% $\text{O}_2$  after 10 hour anneal in dry  $\text{O}_2$  at 300°C*

## 4.2 Impact of Oxygen content in TFT behavior

Until this point all previous sputter conditions had a maximum 1.75%O<sub>2</sub>, with successful devices being sputtered at 1.2%O<sub>2</sub>. The 1.75%O<sub>2</sub> sample may have demonstrated working devices; however, the devices were plagued by gate dielectric failure for reasons unrelated to this study.

Since a reliable target sputter process was established, the next stage of the process development investigation was to understand the impact of high oxygen content in the sputter ambient; 10%O<sub>2</sub>. As standard practice, the run had a half hour argon only pre-sputter, and half an hour deposition at 7mT and 50W. The voltage and current during sputter remained at ~320V and ~0.15A. Figure 4.4 shows that the material resistivity, in samples annealed at 300°C in O<sub>2</sub> for two hours, does increase as the volume percentage of oxygen increases, with  $\rho = 0.74\Omega\cdot\text{cm}$  at 10%O<sub>2</sub>.

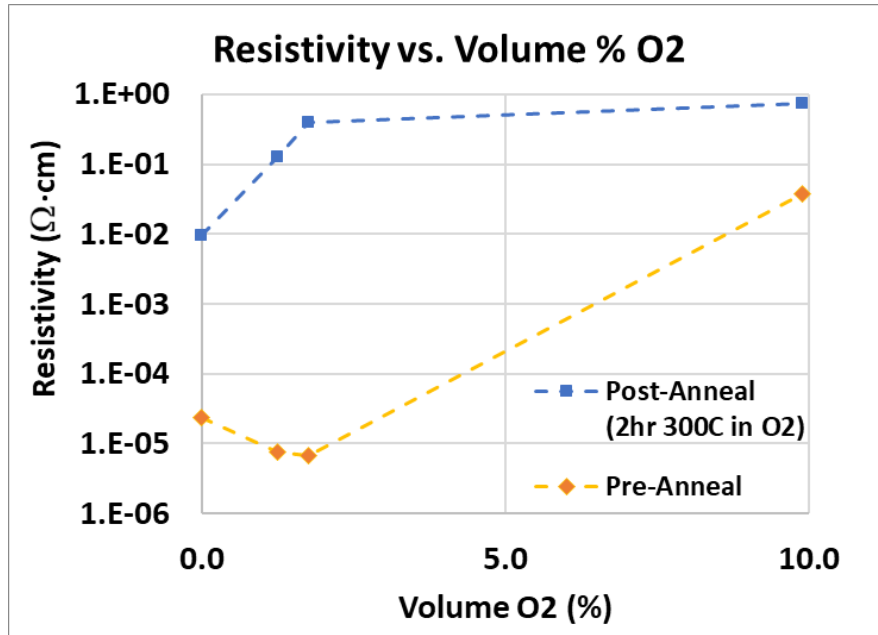


Figure 4.4 Resistivity vs. %O<sub>2</sub>, annealed in dry O<sub>2</sub> at 300°C for 2 hr. Note plot is an extension of Figure 3.11 with the addition of 10%O<sub>2</sub>, and  $R_s$  measurements converted to the material resistivity ( $\Omega\cdot\text{cm}$ ).

Note that the pre-anneal resistivity dependence on %O<sub>2</sub> was not as straightforward. For devices sputtered at oxygen ambient < 2%, an increase in %O<sub>2</sub> caused a decrease in resistivity.

However, high %O<sub>2</sub> in the sputter ambient resulted in significant increase in resistivity. While the resistivity of the IWO was higher for the 10%O<sub>2</sub> treatment in comparison to the 1.2%O<sub>2</sub> treatment, the TFT characteristics were not as encouraging. The 10%O<sub>2</sub> devices following an 8-10 hour O<sub>2</sub> anneal at 300°C exhibited semiconductor behavior, however representative transfer curves demonstrated inferior performance. An overlay of the 1.2% and 10%O<sub>2</sub> characteristics is shown in Figure 4.5. While a high resistivity material is required for proper TFT behavior, this result suggest there are other effects that compromise the device operating characteristics. Apart from the %O<sub>2</sub> sputter treatment, both devices underwent similar process conditions. Based on the transfer curves in Figure 4.5, the increasing O<sub>2</sub> content in the ambient does not necessarily result in better enhancement-mode TFTs. These results suggest that excess oxygen may result in charge trapping defects in the IWO channel and/or channel/dielectric interface [20]. Further investigations need to be performed to completely understand the impact of increasing the %O<sub>2</sub> in the sputter ambient.

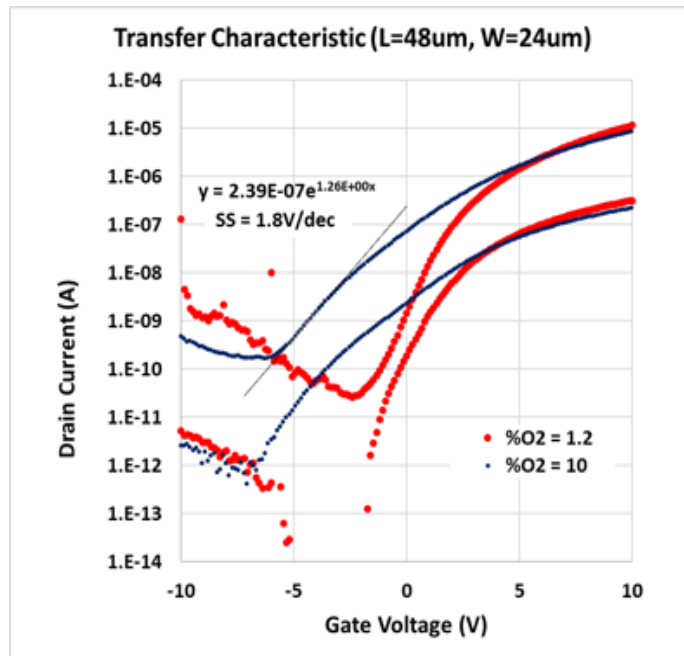


Figure 4.5 Transfer curves for 48um device sputtered in ambient of 1.2% and 10% O<sub>2</sub> per volume and annealed dry O<sub>2</sub> for 10-hour at 300°C

Table 4-1. Comparison of various device parameters of 1.2%O<sub>2</sub> vs. 10%O<sub>2</sub> TFTs

Parameter	1.2 %O <sub>2</sub>	10 %O <sub>2</sub>
S.S (V/decade)	0.94	1.8
Mobility (cm <sup>2</sup> /Vs)	17	9
V <sub>T</sub> @ 50pA/μm (@V <sub>DS</sub> =0.1V)	0.8	-1
ΔV (sat-linear) @ 50pA/μm	0.9	3.4

### 4.3 Impact of Annealing on TFT behavior

The most successful anneal treatment so far has been the 10-hour 300°C dry O<sub>2</sub> anneal treatment. To avoid polycrystalline material formation, the temperature was initially kept at a consistent 300°C. Eventually higher anneal temperatures were studied for possible improvements in device operation and/or reduction in required anneal time. The temperatures investigated were 350°C and

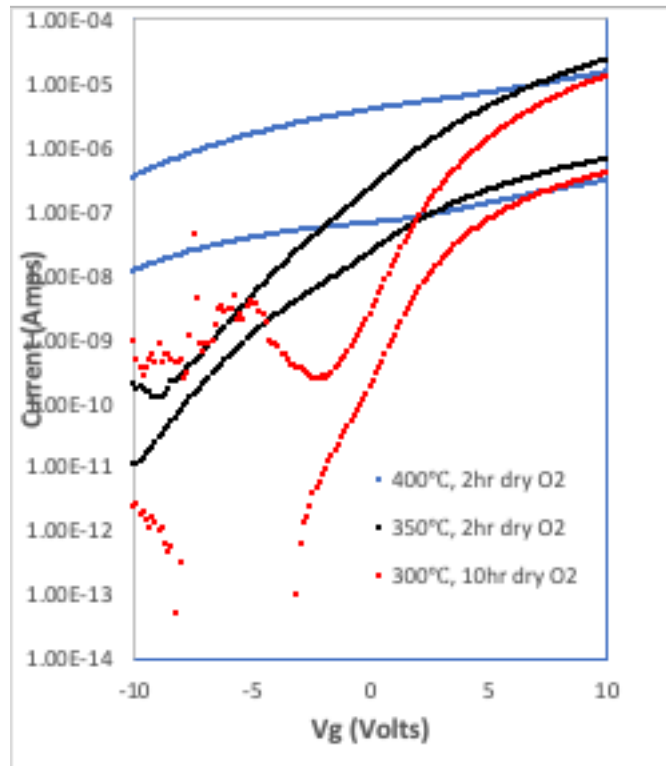


Figure 4.6 Transfer curve of 24μm device sputtered in ambient of 1.2%O<sub>2</sub> and annealed at different temperatures



400°C, with 2 hour anneal time. Figure 4.6 shows transfer curves of 48um devices with 1.2%O<sub>2</sub>, with 350°C and 400°C O<sub>2</sub> anneal for 2 hours, and 300°C O<sub>2</sub> anneal for 10 hours.

While the device operation of the sample annealed at 300°C appears superior to the higher temperature samples, the comparison is relative due to the difference in anneal times. However, the 350°C treatment has better semiconductor behavior in comparison to the 400°C treatment, suggesting that the material may have experienced an additional defect mechanism, with compromised device operation as a result when the temperature reaches 400°C.

## *Chapter 5*

### **5.1 Conclusions**

In the early stages of the study, a problem with the IWO target surface condition was found to be responsible for non-reproducible TFT properties. This initiated an extensive investigation on the details of target reconditioning, pre-sputter conditions and reactive sputter ambient with oxygen. Following target surface reconditioning, it was determined that long pre-sputter times with argon-only ensured that the plasma operating conditions, i.e. voltage and current, were at levels for appropriate DC sputter. Pre-sputter runs with argon-only ambient, for at least 30 minutes, provided a consistent operating condition of 0.15A & 320V at 50W power. This voltage-current combination remained stable over all experimental treatment combinations. While the target showed erosion consistent with magnetron configuration, the pre-sputter process was verified to be effective at removing discoloration associated with surface reactions during reactive sputtering with O<sub>2</sub>.

Reactive sputter conditions with low O<sub>2</sub> content resulted in electrical behavior that was very different from argon-only sputtering (zero %O<sub>2</sub>). Pre-annealed behavior revealed that a low O<sub>2</sub> treatment (i.e. < 2%O<sub>2</sub>) has a lower sheet resistance than zero-oxygen treatments. The same low O<sub>2</sub> treatments resulted in a post-anneal resistivity  $\rho \sim 1 \Omega\cdot\text{cm}$ ; over an order of magnitude higher than zero-oxygen treatments. These results suggested that annealing at 300°C with O<sub>2</sub> should produce films with high enough resistivity for TFTs.

This was indeed the case as demonstrated for IWO TFTs processed with low (1.2%) and high (10%) oxygen content in the sputter ambient, with O<sub>2</sub> annealing at 300°C for 8-10 hr. While the high oxygen treatment material demonstrated a higher post-anneal resistivity, the device operation

was inferior to the low oxygen treatment TFT. This was apparent in both on-state and off-state conditions, with the low oxygen treatment exhibiting higher current drive and steeper subthreshold. While the 10 hr O<sub>2</sub> anneal at 300°C demonstrated marked improvement over the 2 hr anneal, it likely represents an upper limit for benefits to the electrical behavior under these conditions and suggests an increase in annealing temperature may be required for additional performance improvement.

Increasing the O<sub>2</sub> anneal temperature to 350°C on TFTs with the low %O<sub>2</sub> showed promising results for a 2 hr anneal; a longer anneal time may demonstrate improvement over the 300°C treatment. Raising this temperature to 400°C resulted in reduced gate control and current modulation, suggesting the onset of an additional defect mechanism. Degradation in device operation demonstrated by the high %O<sub>2</sub> material, or by aggressive O<sub>2</sub> annealing at T > 350°C, may have a similar origin.

Materials analysis is needed to determine relationships between %O<sub>2</sub> ambient, O<sub>2</sub> annealing, and the role of oxygen within the IWO film. The physical content of oxygen may be quantified using secondary ion mass spectroscopy (SIMS). The chemical distinctions of oxygen (e.g. lattice, interstitial) may be characterized by x-ray photoelectron spectroscopy (XPS). Note that the ability to detect such differences in a metal-oxide material presents a significant challenge. Refined experimental designs that considers these findings, followed by materials analysis to quantify treatment combination differences, will provide further understanding and progress towards parameter optimization needed to realize the potential of IWO as a next-generation TFT candidate for display and other applications.

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