

Effects of Variations in RCA Clean on Breakdown Characteristics of Thin Gate Oxides

Bryan Kasprowicz
Senior Microelectronic Engineering Student
Rochester Institute of Technology

Abstract - Several variations on the order of the RCA clean have been investigated for their effects on oxide charges and interface trap density of thin gate oxides (200-250Å). Surface Charge Analysis (SCA) will be employed to evaluate charges and traps immediately after oxide growth. Capacitors with aluminum gate were then fabricated to determine the dielectric strength of the devices via destructive electric field breakdown testing on an HP4145 parametric analyzer, the total oxide charge and interface trap density have been obtained from C-V testing using a Keithley simultaneous high frequency / low frequency system.

I. Introduction

Aqueous cleaning processes are the most commonly used technique for removal of contamination. Such removal is of paramount importance to the semiconductor industry since it is generally accepted that over 50% of yield losses in integrated circuit fabrication are due to microcontamination¹. Furthermore, metals that are left on the surface will spread and diffuse into the silicon and cause yield loss and/or reliability issues. Whether the contaminants are specific or general, or whether the source of the contaminants is known or unknown, the successful removal of contamination is the essence of cleaning^{2,3}.

Electronic properties of silicon dioxide, and of the oxide-silicon interface, have a profound effect on operation and long-term reliability of devices. In most cases, these effects are accounted for in the device design and processing.

Of the many cleaning solutions that have been used, the most prevalent have been the RCA solutions, which are aqueous mixtures of hydrogen peroxide with ammonium hydroxide (APM), and hydrochloric acid (HPM). The purpose of the APM is to oxidize surface organic films and remove some

metal ions, while the HPM is used to remove alkali cations. Recent studies have shown that the sequence of the RCA Clean has a considerable effect on contamination^[2].

The integrity and reliability (*the probability that it will not suffer breakdown under the stated operating conditions for the defined lifetime of the system*) of the oxide are of great importance to metal-oxide-semiconductor (MOS) ultra-large-scale-integration (ULSI) technology. MOS capacitance-voltage (C-V) measurement is the most commonly used technique for monitoring contamination in thermally grown oxides. Various characteristics of the C-V curve are used to extract several qualities of the oxide, including total oxide charge (Q_{ox}) and interface trap density (D_{it}). Unfortunately, C-V measurement techniques require additional post-oxidation processing (which could introduce contamination) to fabricate capacitors and therefore delay their detection.

The introduction of Surface Charge Analysis, which is a non-destructive method to monitor the electronic properties of a bare oxide covered wafer surface. This method uses the ac surface photovoltage (SPV) from the ac photocurrent that is induced when a beam of chopped light of a photon energy greater than the semiconductor bandgap is incident upon the surface. Figure 1 represents a schematic diagram of the SCA².

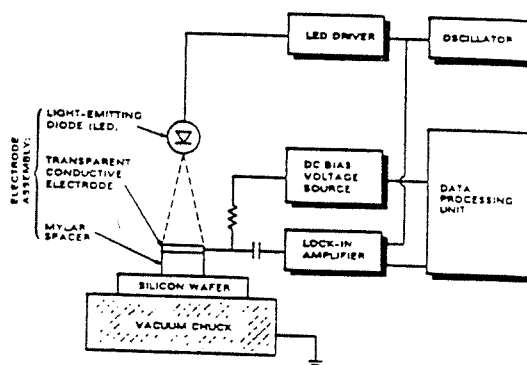


Figure 1. Schematic of Surface Charge Analyzer.

The location of typical oxide charges at the silicon surface is illustrated in Figure 2.

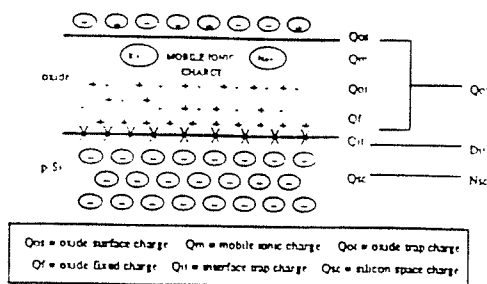


Figure 2. Location of charges in the Si-SiO₂ structure.

II. Experiment

A 2³ full factorial experimental design (utilized 4", <100>, p-type silicon wafers with resistivities of approximately 10Ω-cm), shown in Figure 3, was used to monitor the responses of dielectric breakdown strength and, total and effective oxide charge. The order of the clean (HPM last vs. APM last), anneal (whether or not the wafers were passivated) and whether or not the wafers had a final HF Dip or just concluded with a rinse with no subsequent HF Dip, were the factors that were varied.

Prior to processing the wafers through the RCA Clean, great care was taken to thoroughly clean both

chemical tanks with DI water and HCl for several hours to minimize excess contamination.

After the cleaning sequences were performed, a 225Å oxide was thermally grown according to the process outlined in Appendix A. Immediately after oxidation, charges in the oxide on Group A wafers were measured using a voltage sweep from inversion to accumulation on the SCA and Q_{OX} was recorded. Group B wafers were passivated in H₂N₂ forming gas for 20 minutes at 425°C.

Further processing included evaporating Aluminum on the front side of the wafers and patterning the aluminum to produce capacitor gates. After patterning, a thick layer of resist was coated on the front side and the native oxide was removed from the backsides of the wafers using a BOE dip. Aluminum was then evaporated on the backside to a good ohmic contact for subsequent testing. The aluminum was then sintered on all wafers in H₂N₂ forming gas for 25 minutes at 425°C.

The dielectric breakdown strength was determined using a catastrophic ramped voltage test. I will elaborate on the design of this testing in the next section. Also, C-V measurements were taken using a Keithley System 82 to obtain the Q_{eff}.

III. Breakdown Voltage Testing

The setup for the ramped breakdown voltage test consisted of an isolation box - to minimize unwanted photogenerated carriers and background noise, an HP4145A parametric analyzer and a resistor in series with the capacitor.

The test itself consisted of ramping the voltage at 20 V/sec until the rupture point was seen³ (V_{total}). Once breakdown occurred, the voltage was then appended producing the linear resistor characteristic curve. At the common current where the rupture occurred, the voltage drop across the resistor was determined. Equations 1 and 2 below were used in determining the field strength:

$$V_{\text{Breakdown}} = V_{\text{Total}} - V_R \quad (1)$$

$$E_{\text{Breakdown}} = \frac{V_{\text{Breakdown}}}{t_{\text{OX}}} \quad (2)$$

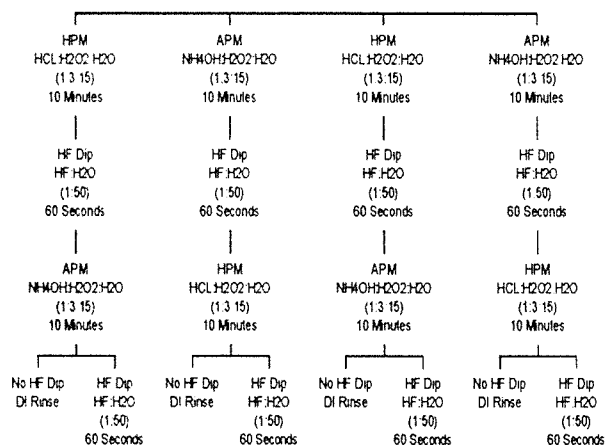


Figure 3. Experimental Design.

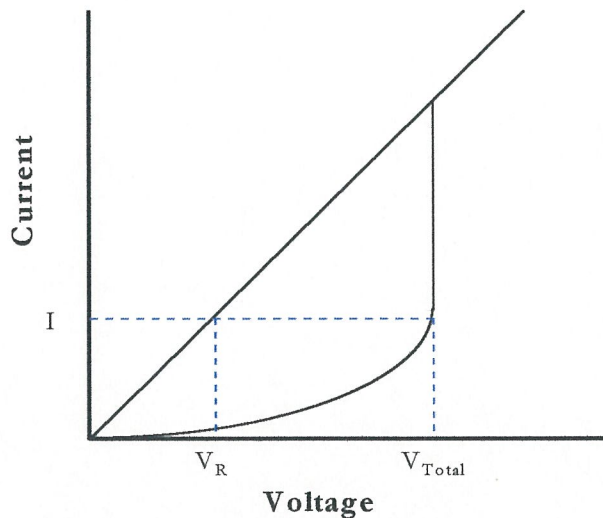


Figure 4. Theoretical Breakdown Voltage Test

IV. Results and Discussion

The cumulative distribution plots shown in Figures 5 and 6, illustrate the field strength of the oxide. In either case, with or without passivation it is clearly seen that the largest field breakdown is observed when the HPM solution was used last.

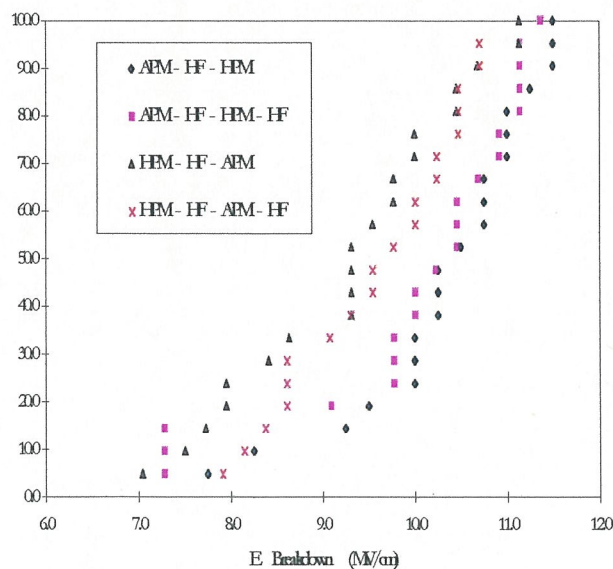


Figure 5. Effects of RCA Clean on Electric Field Breakdown (Non-passivated).

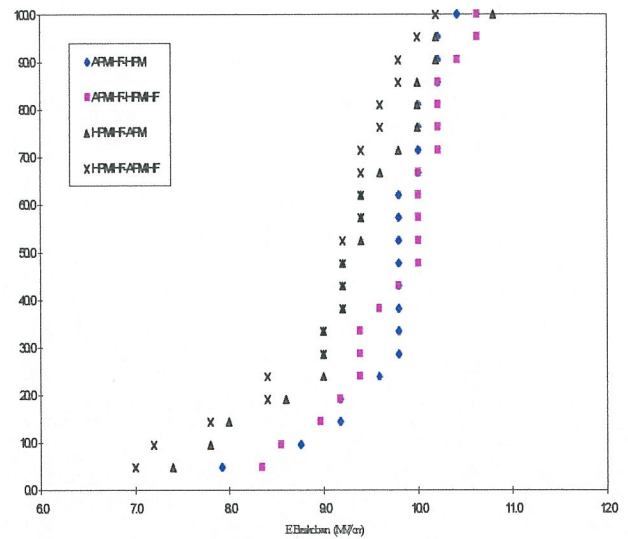


Figure 6. Effects of RCA Clean on Electric Field Breakdown (Passivated).

A correlation was made between the SCA and C-V results. As seen in the graphical representation in Figure 7, the final rinse only (No HF) increased the oxide charge while the HF Dip tended to make the charges found in the oxide more positive.

The passivated wafers had a more negative oxide charge due to H_2 passivation of the density of interface traps (D_{it}) which therefore reduced the positively charged interface traps (Q_{it}).

The reduction observed between the Keithley C-V system and the SCA measurements was due to subsequent processing, namely the aluminum sinter which helped to additionally passivate D_{it} .

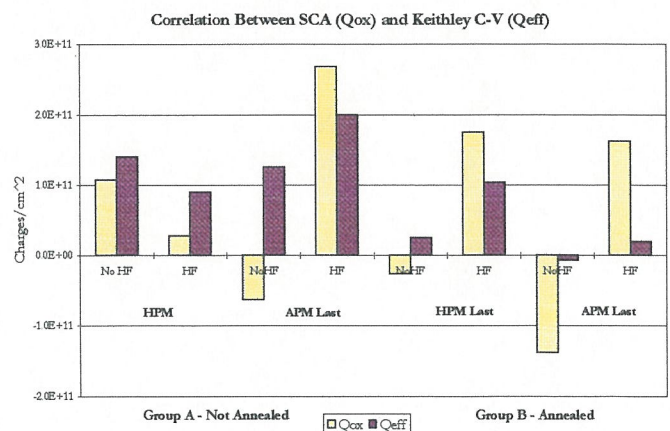


Figure 7. Correlation between SCA & Keithley C-V.

V. Conclusions

A designed experiment has been used in determining that the sequence of the RCA Clean that had the HPM (hydrochloric acid) solution last produced the largest field strength in the oxide. One possible reason may be due to the reduction of metallics on the surface which would reduce the charges in the oxide.

The oxide charges were increased with the APM solution last and no final HF dip while the HF Dip made the charges more positive. This may be due the tin that was used to stabilize the hydrogen peroxide used during the cleans.

Good agreement was seen between the Keithley C-V Model 82 system and the SemiTest 2000 Surface Charge analyzer. The enhanced results of the Keithley system are probably due to hydrogen passivation of the interface traps during the aluminum sinter. There is one establishment that remains to be made. That is the determination of the total charge, and whether the total charge actually is reduced as previously thought, or is there a net charge that is added to the total charge.

VI. Acknowledgments

I would like to express my gratitude to Dr. Santosh Kurinec for her enlightening guidance and especially Dr. Michael Jackson for his particular efforts, enthusiasm and encouragement in support of this work.

VII. References

- [1] T. Ohmi, et al. *IEEE Transactions on Electron Devices*, 39 (3), 537-544, March 1992.
- [2] E. Kamieniecki, et al. *Proceedings of the First International Symposium on Cleaning Technology in Semiconductor Manufacturing*, 90(9), 335-340, 1989.
- [3] J. Kato & Y. Mauro, *Journal of Electrochemical Society*, 139(6), 1756-1789, June 1992.
- [4] E. Kamieniecki & G. Foggaito, *Handbook of Semiconductor Wafer Cleaning Technology*, W. Kern, Ed., Noyes Publications. 1993, pp. 497-516.
- [5] G. Groenseneken, *IEEE - IEDM Short Course on Advance Device Characterization and Test Methodologies* - 1994.

APPENDIX A

225 Angstrom Oxidation Process

- 1) TCA Clean Furnace (1050°C for 60 minutes)
- 2) Push (12"/min) at 800°C in 6 slpm N₂
- 3) Ramp to 1000°C in 6 slpm N₂
- 4) Oxidation at 1000°C for 2 minutes in 5.5 slpm of O₂
- 5) Oxidation at 1000°C for 5 minutes in 5.5 slpm O₂ and 160 sccm of TCA
- 6) Oxidation at 1000°C for 2 minutes in 5.5 slpm of O₂
- 7) Ramp to 800°C in 6 slpm N₂
- 8) Pull (12"/min) at 800°C in 6 slpm N₂